ISL80138

40V, High Accuracy, Low Quiescent Current, 150mA Linear Regulator

FN7969
Rev 2.00
Feb 20, 2019

The ISL80138 is a high voltage, adjustable V_{OUT} low quiescent current linear regulator ideally suited for “always-on” and “keep alive” applications. The ISL80138 operates from an input voltage of +6V to +40V under normal operating conditions and consumes only 18µA of quiescent current at no load.

The ISL80138 features an EN pin that can be used to put the device into a low-quiescent current shutdown mode where it draws only 2µA of supply current. The device features over-temperature shutdown and current limit protection.

The ISL80138 is rated to operate across the -40°C to +125°C temperature range and is available in a 14 lead HTSSOP with an exposed pad package.

Related Literature

For a full list of related documents, visit our website:

- ISL80138 device page

Features

- Wide V_{IN} range of 6V to 40V
- Adjustable output voltage from 2.5V to 12V
- Ensured 150mA output current
- Ultra low 18µA typical quiescent current
- Low 2µA of typical shutdown current
- ±1% accurate voltage reference (over temperature, load)
- Low dropout voltage of 295mV at 150mA
- Low 26µV_{RMS} noise
- 40V tolerant logic level (TTL/CMOS) enable input
- Stable operation with 10µF output capacitor
- 5kV ESD HBM rated
- Thermal shutdown and current limit protection
- Thermally enhanced 14 Ld exposed pad HTSSOP package

Applications

- Industrial
- Telecommunications

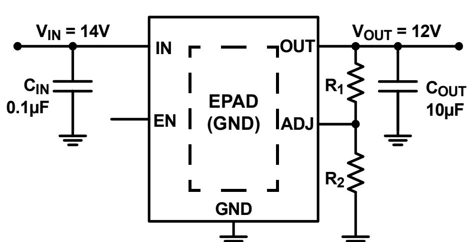


FIGURE 1. TYPICAL APPLICATION

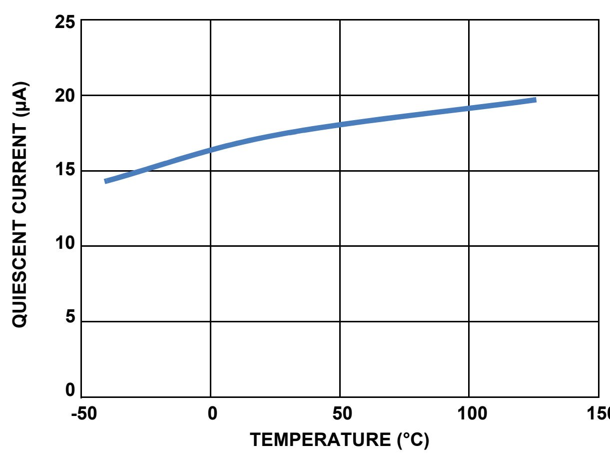
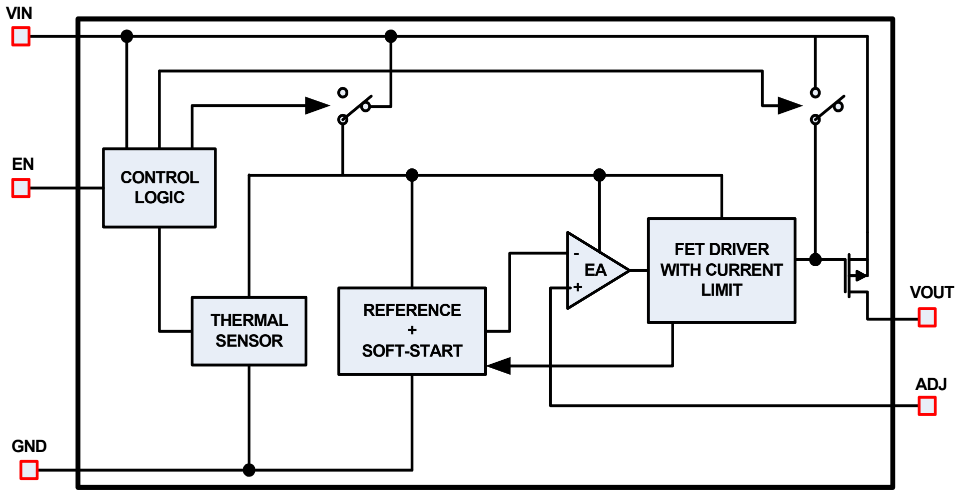


FIGURE 2. QUIESCENT CURRENT vs TEMPERATURE (AT UNITY GAIN). V_{IN} = 14V

Block Diagram



Ordering Information

PART NUMBER (Notes 2, 3)	PART MARKING	TEMP. RANGE (°C)	ENABLE PIN	OUTPUT VOLTAGE (V)	TAPE AND REEL (Units) (Note 1)	PACKAGE (RoHS Compliant)	PKG. DWG. #
ISL80138IVEAJZ	80138 IAJZ	-40 to +125	Yes	ADJ	-	14 Ld HTSSOP	M14.173B
ISL80138IVEAJZ-T	80138 IAJZ	-40 to +125	Yes	ADJ	2.5k	14 Ld HTSSOP	M14.173B
ISL80138IVEAJZ-T7A	80138 IAJZ	-40 to +125	Yes	ADJ	250	14 Ld HTSSOP	M14.173B
ISL80138EVAL1Z	Evaluation Platform						

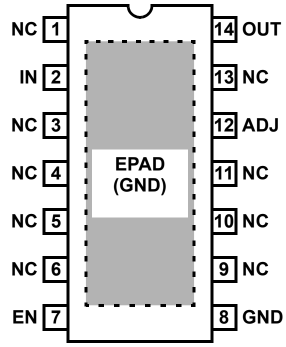
NOTES:

1. See TB347 for details about reel specifications.
2. These Pb-free plastic packaged products employ special Pb-free material sets, molding compounds/die attach materials, and 100% matte tin plate plus anneal (e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations). Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.
3. For Moisture Sensitivity Level (MSL), see the ISL80138 device page. For more information about MSL, see TB363.

TABLE 1. KEY DIFFERENCES IN FAMILY OF 40V LDO PARTS

PART NUMBER	MINIMUM I_{OUT}	IC PACKAGE
ISL80410	150mA	8 Ld EPSOIC
ISL80136	50mA	8 Ld EPSOIC
ISL80138	150mA	14 LD HTSSOP

Pin Configuration



Pin Descriptions

PIN NUMBER	PIN NAME	DESCRIPTION
1, 3, 4, 5, 6, 9, 10, 11, 13	NC	Pins have internal termination and can be left unconnected. Connection to ground is optional.
2	IN	Input voltage pin. A minimum 0.1µF ceramic capacitor is required for proper operation. Range 6V to 40V.
7	EN	Enable pin. High on this pin enables the device. Range 0V to V_{IN}.
8	GND	Ground pin.
12	ADJ	This pin is connected to the external feedback resistor divider which sets the LDO output voltage.
14	OUT	Regulated output voltage. A 10µF ceramic capacitor is required for stability. Range 0V to 12V.
-	EPAD	It is recommended to solder the EPAD to the ground plane.

Absolute Maximum Ratings

IN Pin to GND Voltage . . . . GND - 0.3V to 45V
OUT Pin to GND Voltage . . . . GND - 0.3V to 16V
ADJ Pin to GND Voltage . . . . GND - 0.3V to 3V
EN Pin to GND Voltage . . . . GND - 0.3V to VIN
Output Short-Circuit Duration . . . . Indefinite
ESD Rating
Human Body Model (Tested per JESD22-A114E). 5kV
Machine Model (Tested per JESD-A115-A) 200V
Charge Device Model (Tested per JESD22-C101C). 2.2kV
Latch-Up (Tested per JESD78B; Class II, Level A) 100mA

Thermal Information

Thermal Resistance (Typical)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
14 Ld HTSSOP Package (Notes 4, 5)	37	5

Maximum Junction Temperature . . . . +150°C
Maximum Storage Temperature Range . . . . -65°C to +175°C
Pb-Free Reflow Profile . . . . see TB493

Recommended Operating Conditions

Ambient Temperature Range . . . . -40°C to +125°C
IN pin to GND Voltage. . . . . +6V to +40V
OUT pin to GND Voltage . . . . +2.5V to +12V
EN pin to GND Voltage . . . . 0V to +40V

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions can adversely impact product reliability and result in failures not covered by warranty.

NOTES:

4. θ_{JA} is measured in free air with the component mounted on a high-effective thermal conductivity test board with "direct attach" features. See TB379.
5. For θ_{JC}, the "case temp" location is the center of the exposed metal pad on the package underside.

Electrical Specifications

Recommended Operating Conditions, unless otherwise noted. V_{IN} = 14V, I_{OUT} = 1mA, T_A = T_J = -40°C to +125°C, unless otherwise noted. Typical specifications are at T_A = +25°C. **Boldface limits apply across the operating temperature range, -40°C to +125°C.**

PARAMETER	SYMBOL	TEST CONDITIONS	MIN (Note 8)	TYP	MAX (Note 8)	UNIT
Input Voltage Range	V_{IN}		**6**		**40**	V
Guaranteed Output Current	I_{OUT}	V_{IN} = V_{OUT} + VDO	**150**			mA
ADJ Reference Voltage	V_{OUT}	EN = High, V_{IN} = 14V, I_{OUT} = 0.1mA to 150mA	**1.211**	1.223	**1.235**	V
Line Regulation	(V_{OUT} low line - V_{OUT} high line)/V_{OUT} low line	6V < V_{IN} < 40V, I_{OUT} = 1mA		0.04	**0.15**	%
Load Regulation	(V_{OUT} no load - V_{OUT} high load)/V_{OUT} no load	V_{IN} = 14V, I_{OUT} = 100µA to 150mA		0.3	**0.6**	%
Dropout Voltage (Note 6)	ΔV_{DO}	I_{OUT} = 1mA, V_{OUT} = 2.5V		7	**33**	mV
		I_{OUT} = 150mA, V_{OUT} = 2.5V		380	**571**	mV
		I_{OUT} = 1mA, V_{OUT} = 5V		7	**33**	mV
		I_{OUT} = 150mA, V_{OUT} = 5V		295	**507**	mV
Shutdown Current	I_{SHDN}	EN = LOW		2	**3.64**	µA
Quiescent Current	IQ	EN = HIGH, I_{OUT} = 0mA		18	**24**	µA
		EN = HIGH, I_{OUT} = 1mA		22	**42**	µA
		EN = HIGH, I_{OUT} = 10mA		34	**60**	µA
		EN = HIGH, I_{OUT} = 150mA		90	**125**	µA
Power Supply Rejection Ratio	PSRR	f = 100Hz; V_{IN_RIPPLE} = 500mV_{P-P}; Load = 150mA		66		dB
Output Voltage Noise		V_{IN} = 14V, V_{OUT} = 3.3V, C_{OUT} = 10µF, I_{OUT} = 10mA, BW = 100Hz to 100kHz		26		µV_{RMS}

Electrical Specifications Recommended Operating Conditions, unless otherwise noted. V_{IN} = 14V, I_{OUT} = 1mA, T_A = T_J = -40°C to +125°C, unless otherwise noted. Typical specifications are at T_A = +25°C. **Boldface limits apply across the operating temperature range, -40°C to +125°C.** **(Continued)**

PARAMETER	SYMBOL	TEST CONDITIONS	MIN (Note 8)	TYP	MAX (Note 8)	UNIT
EN FUNCTION						
EN Threshold Voltage	V_{EN_H}	V_{OUT} = Off to On			**1.485**	V
	V_{EN_L}	V_{OUT} = On to Off	**0.975**			V
EN Pin Current	I_{EN}	V_{OUT} = 0V		0.026		µA
EN to Regulation Time (Note 7)	t_{EN}			1.65	**1.93**	ms
PROTECTION FEATURES						
Output Current Limit	I_{LIMIT}	V_{OUT} = 0V	**175**	410		mA
Thermal Shutdown	T_{SHDN}	Junction Temperature Rising		+165		°C
Thermal Shutdown Hysteresis	T_{HYST}			+20		°C

NOTES:

6. Dropout voltage is defined as (V_{IN} - V_{OUT}) when V_{OUT} is 2% below the value of V_{OUT}.
7. Enable to Regulation Time is the time the output takes to reach 95% of its final value with V_{IN} = 14V and EN is taken from V_{IL} to V_{IH} in 5ns. For the adjustable versions, the output voltage is set at 5V.
8. Parameters with MIN and/or MAX limits are 100% tested at +25°C, unless otherwise specified. Temperature limits established by characterization and are not production tested.

Typical Performance Curves

V_{IN} = 14V, I_{OUT} = 1mA, V_{OUT} = 5V, T_J = +25°C, unless otherwise specified.

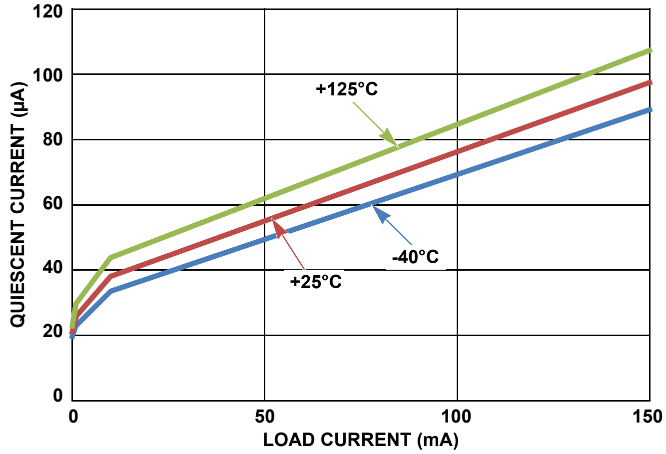


FIGURE 3. QUIESCENT CURRENT vs LOAD CURRENT

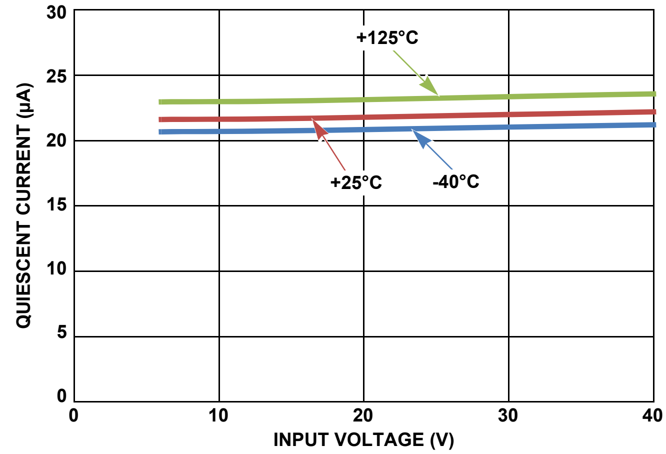


FIGURE 4. QUIESCENT CURRENT vs INPUT VOLTAGE (NO LOAD)

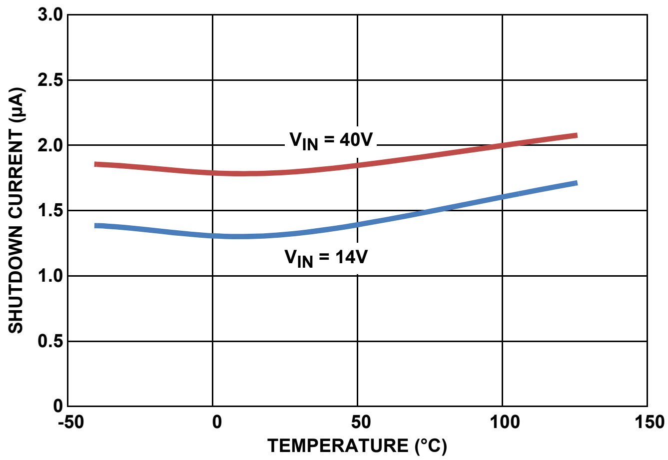


FIGURE 5. SHUTDOWN CURRENT vs TEMPERATURE (EN = 0)

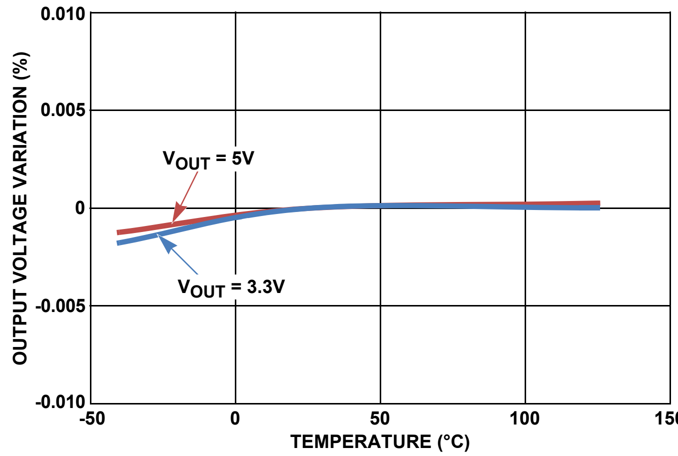


FIGURE 6. OUTPUT VOLTAGE vs TEMPERATURE (LOAD = 50mA)

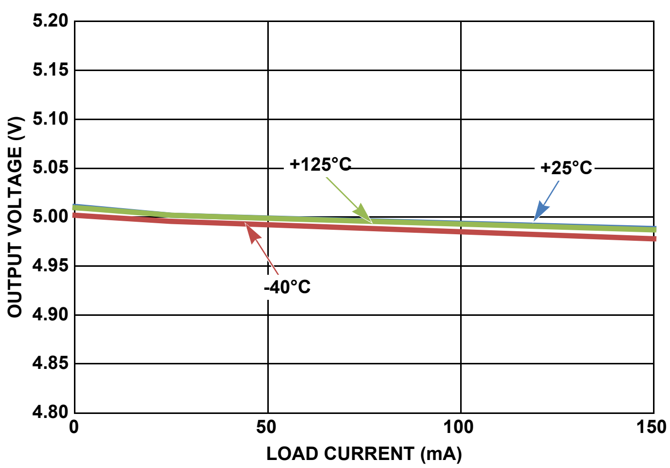


FIGURE 7. OUTPUT VOLTAGE vs LOAD CURRENT

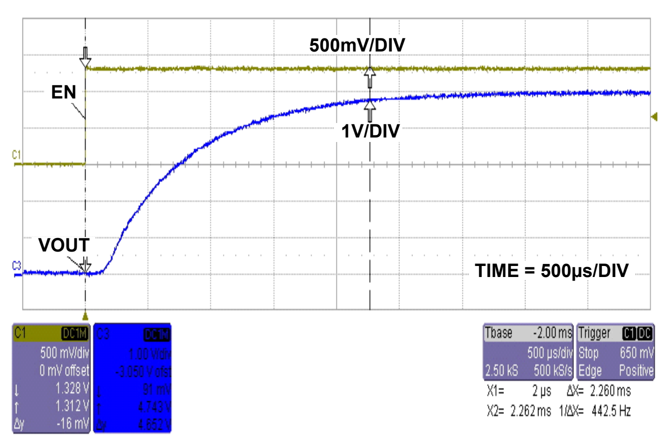


FIGURE 8. START-UP WAVEFORM

Typical Performance Curves V_{IN} = 14V, I_{OUT} = 1mA, V_{OUT} = 5V, T_J = +25°C, unless otherwise specified. **(Continued)**

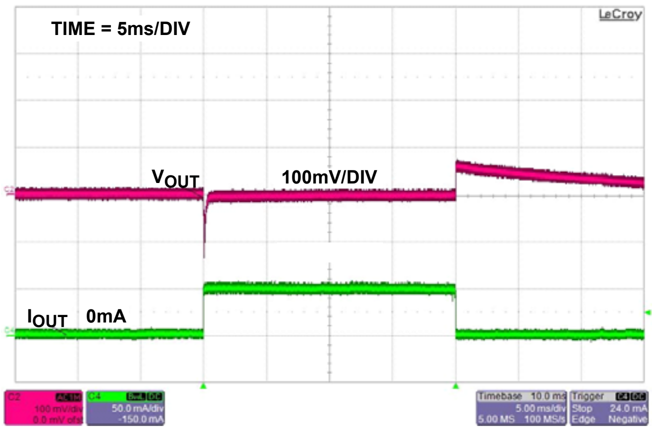


FIGURE 9. LOAD TRANSIENT RESPONSE

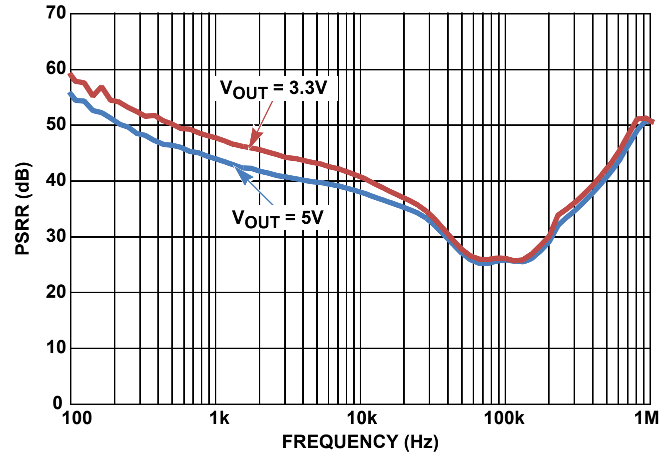


FIGURE 10. PSRR vs FREQUENCY FOR VARIOUS OUTPUT VOLTAGES, (LOAD = 150mA)

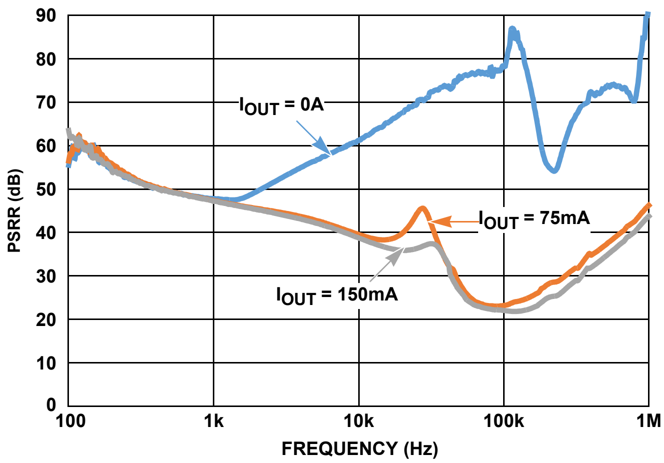
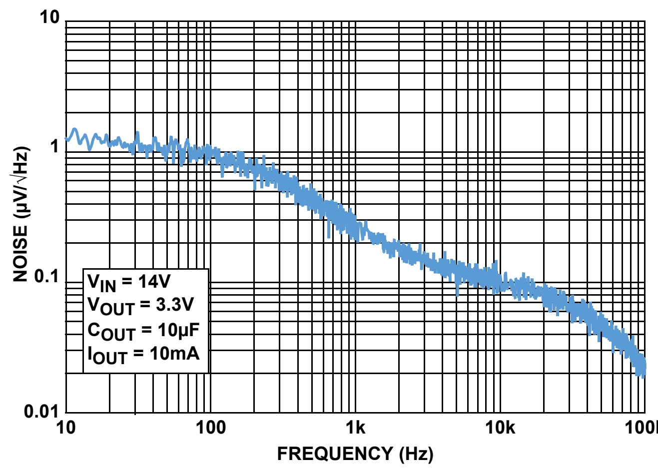
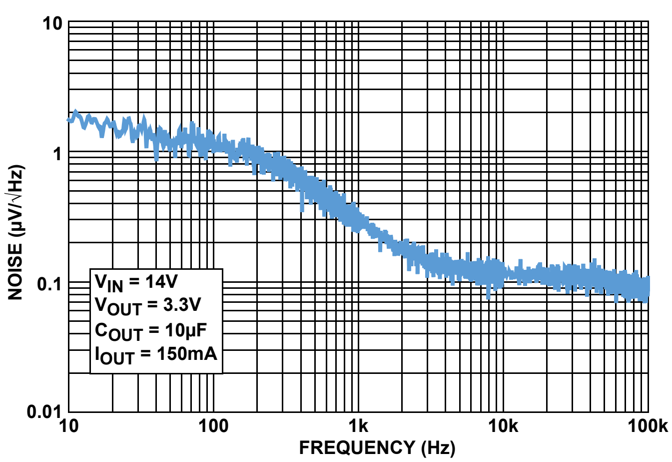


FIGURE 11. PSRR vs FREQUENCY FOR VARIOUS LOAD CURRENTS, V_{OUT} = 3.3V



BW = 100 < f < 100kHz output noise voltage ~ 26 µVrms

FIGURE 12. OUTPUT NOISE SPECTRAL DENSITY, I_{OUT} = 10mA



BW = 100 < f < 100kHz output noise voltage ~ 38 µVrms

FIGURE 13. OUTPUT NOISE SPECTRAL DENSITY, I_{OUT} = 150mA

Functional Description

Functional Overview

The ISL80138 is a high performance, high voltage, low-dropout regulator (LDO) with 150mA sourcing capability. The part is rated to operate across the -40°C to +125°C temperature range. Featuring ultra-low quiescent current, it is an ideal choice for "always-on" applications. It works well under a "load dump condition" where the input voltage could rise up to 40V. This LDO device also features current limit and thermal shutdown protection.

Enable Control

The ISL80138 has an enable pin that turns the device on when pulled high. When EN is low, the IC goes into shutdown mode and draws less than 2µA of current. Tie the EN pin to IN for "always-on" operation.

Current Limit Protection

The ISL80138 has internal current limiting functionality to protect the regulator during fault conditions. During current limit, the output sources a fixed amount of current largely independent of the output voltage. If the short or overload is removed from V_{OUT}, the output returns to normal voltage regulation mode.

Thermal Fault Protection

If the die temperature exceeds a typical value of +165°C, the output of the LDO shuts down until the die temperature cools down to a typical +145°C. The level of power dissipated, combined with the ambient temperature and the thermal impedance of the package, determines if the junction temperature exceeds the thermal shutdown temperature. See "Power Dissipation" for more details.

Application Information

Input and Output Capacitors

A minimum 0.1µF ceramic capacitor is recommended at the input for proper operation. For the output, a ceramic capacitor with a capacitance of 10µF is recommended for the ISL80138 to maintain stability. Route the ground connection of the output capacitor directly to the GND pin of the device and place it close to the IC.

Output Voltage Setting

The ISL80138 output voltage is programmed using an external resistor divider as shown in Figure 14.

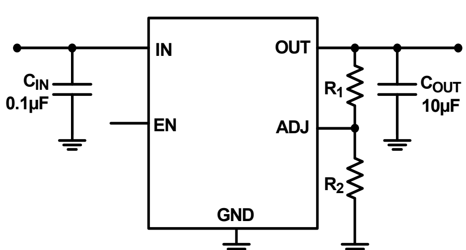


FIGURE 14. OUTPUT VOLTAGE SETTING

The output voltage is calculated using Equation 1:

$$V_{OUT} = 1.223V \times \left(\frac{R_1}{R_2} + 1\right) \quad \text{(EQ. 1)}$$

Power Dissipation

The junction temperature must not exceed the range specified in "Recommended Operating Conditions" on page 4. The power dissipation can be calculated using Equation 2:

$$P_D = (V_{IN} - V_{OUT}) \times I_{OUT} + V_{IN} \times I_{GND} \quad \text{(EQ. 2)}$$

The maximum allowable junction temperature, $T_{J(MAX)}$ and the maximum expected ambient temperature, $T_{A(MAX)}$ determine the maximum allowable junction temperature rise (ΔT_J), as shown in Equation 3:

$$\Delta T_J = T_{J(MAX)} - T_{A(MAX)} \quad \text{(EQ. 3)}$$

To calculate the maximum ambient operating temperature, use the junction-to-ambient thermal resistance (θ_{JA}) as shown in Equation 4:

$$T_{J(MAX)} = P_{D(MAX)} \times \theta_{JA} + T_A \quad \text{(EQ. 4)}$$

Board Layout Recommendations

A good PCB layout is important to achieve expected performance. When placing the components and routing the trace, minimize the ground impedance and keep the parasitic inductance low. The input and output capacitors should have a good ground connection and be placed as close to the IC as possible. The feedback trace in the adjustable version should be away from other noisy traces. The 14 Ld HTSSOP package uses the copper area on the PCB as a heat sink. The EPAD of this package must be soldered to the copper plane (GND plane) for effective heat dissipation. Figure 15 shows a curve for θ_{JA} of the package for different copper area sizes.

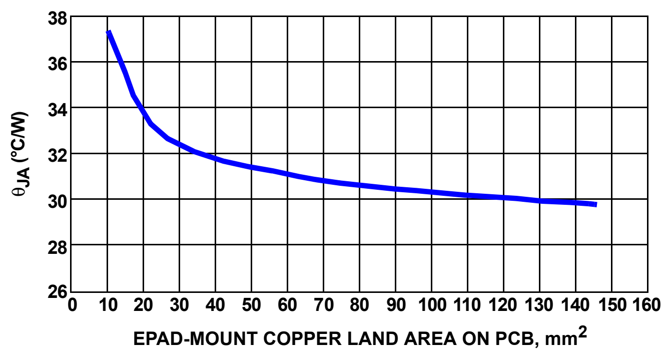


FIGURE 15. θ_{JA} vs EPAD-MOUNT COPPER LAND AREA ON PCB

Revision History

The revision history provided is for informational purposes only and is believed to be accurate, but not warranted. Please go to web to make sure you have the latest Rev.

DATE	REVISION	CHANGE
Feb 20, 2019	FN7969.2	Updated title Updated the 6th bullet and added the 8th bullet in the features list. Updated Related Literature section. Updated ordering information table with tape and reel information and updated notes. Updated Table 1 and moved to page 2. Added Output Voltage Noise specification. Removed About Intersil section. Updated disclaimer
Jan 15, 2016	FN7969.1	Updated entire datasheet applying Intersil's new standards. On page 1, updated Key Differences Table, Replaced "ADJ OR FIXED VOUT" Column with "IC PACKAGE" column. On page 2, updated Block Diagram, removed two resistors and switched polarity of EA. Onpage 3, removed "Range 0V to 3V." from the ADJ Pin Description On page 4, updated Note 4 from "θ_{JA} is measured with the component mounted on a high effective thermal conductivity test board in free air. See Tech Brief TB379 for details." to "θ_{JA} is measured in free air with the component mounted on a high effective thermal conductivity test board with "direct attach" features. See Tech Brief TB379." On page 4, removed "C_{IN} = 0.1µF, C_{OUT} = 10µF" from the Electrical Specification heading. On page 4, updated the Line Regulation -Symbol, from "$\Delta V_{OUT}/\Delta V_{IN}$" to "($V_{OUT}$ low line - V_{OUT} high line)/V_{OUT} low line". -Test Conditions, from "3V ≤ V_{IN} ≤ 40V, I_{OUT} = 1mA" to "6V < V_{IN} < 40V, I_{OUT} = 1mA" On page 4, updated the Load Regulation -Symbol, from "$\Delta V_{OUT}/\Delta I_{OUT}$" to "($V_{OUT}$ no load - V_{OUT} high load)/V_{OUT} no load". -Test Conditions from "V_{IN} = V_{OUT} +V_{DO}" to "V_{IN} = 14V" On page 3, updated the Dropout Voltage (Two rows only): -Test Conditions from "VOUT = 3.3V" to "VOUT = 2.5V" -Changed maximum value for condition, IOUT = 150mA, VOUT = 2.5V, from "525" to "571" -Changed maximum value for condition, IOUT = 150mA, VOUT = 5V, from "460" to "507" Updated Note 6 from "Dropout voltage is defined as (V_{IN} - V_{OUT}) when V_{OUT} is 2% below the value of V_{OUT} when V_{IN} = V_{OUT} + 3V." to "Dropout voltage is defined as (V_{IN} - V_{OUT}) when V_{OUT} is 2% below the value of V_{OUT}." On page 7, switched Figures 9 and 10 location, then updated title for Figure 10 from "POWER SUPPLY REJECTION RATIO (LOAD = 150mA)" to "PSRR vs FREQUENCY FOR VARIOUS OUTPUT VOLTAGES (LOAD = 150mA)" Added Figures 11, 12 and 13 on page 7. Updated Products verbiage to About Intersil verbiage.
Jan 11, 2012	FN7969.0	Initial Release.

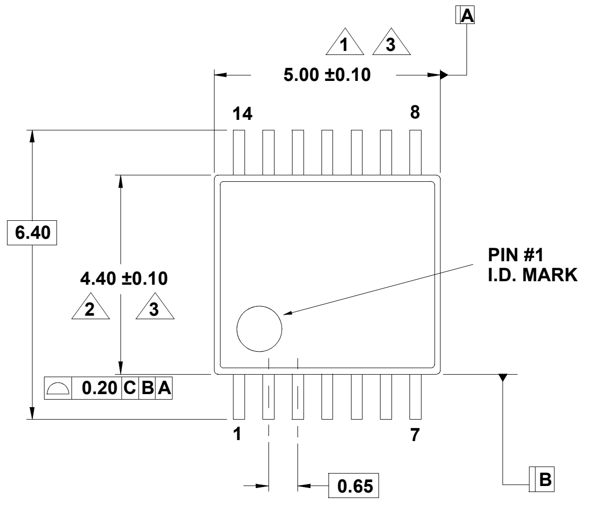
Package Outline Drawing

For the most recent package outline drawing, see M14.173B.

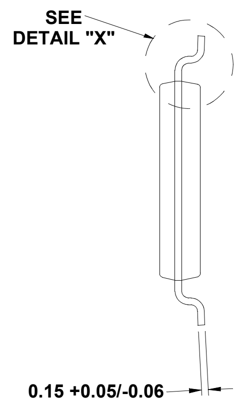
M14.173B

14 LEAD HEAT-SINK THIN SHRINK SMALL OUTLINE PACKAGE (HTSSOP)

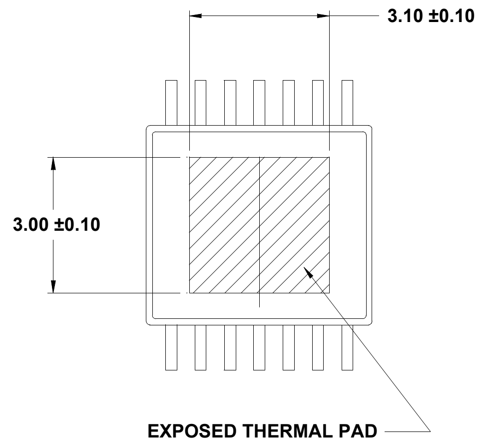
Rev 1, 1/10



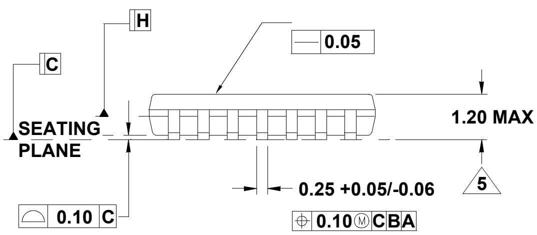
TOP VIEW



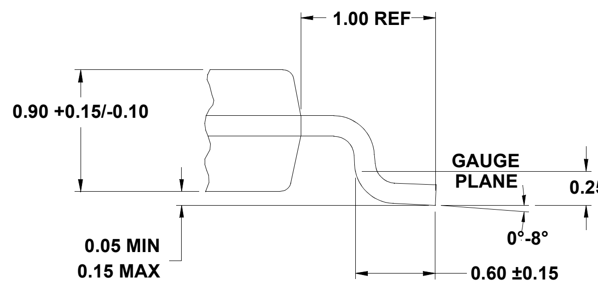
END VIEW



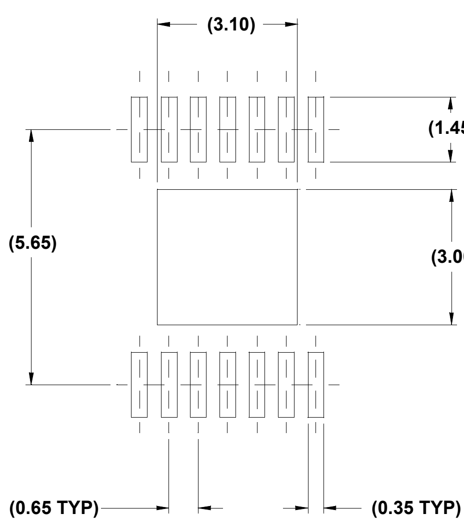
BOTTOM VIEW



SIDE VIEW



DETAIL "X"



TYPICAL RECOMMENDED LAND PATTERN

NOTES:

1. Dimension does not include mold flash, protrusions or gate burrs. Mold flash, protrusions or gate burrs shall not exceed 0.15 per side.
2. Dimension does not include interlead flash or protrusion. Interlead flash or protrusion shall not exceed 0.25 per side.
3. Dimensions are measured at datum plane H.
4. Dimensioning and tolerancing per ASME Y14.5M-1994.
5. Dimension does not include dambar protrusion. Allowable protrusion shall be 0.80mm total in excess of dimension at maximum material condition. Minimum space between protrusion and adjacent lead is 0.07mm.
6. Dimension in ( ) are for reference only.
7. Conforms to JEDEC MO-153, variation ABT-1.

Notice

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(Rev.4.0-1 November 2017)

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