FemtoClock® Crystal/LVCMOS-to-LVDS/LVCMOS Frequency Synthesizer

ICS844S0258-07

DATASHEET

General Description

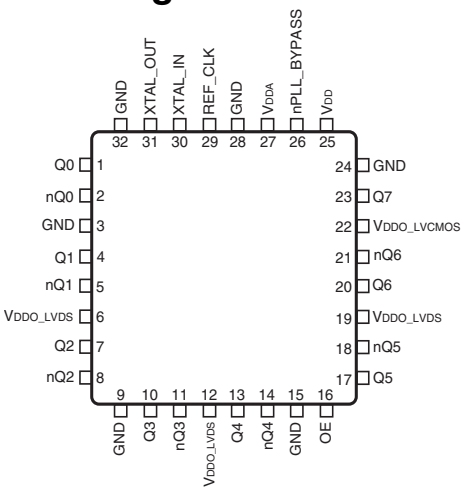
The ICS844S0258-07 is an eight output synthesizer optimized to generate Gigabit and 10 Gigabit Ethernet clocks. Using a 25MHz, 18pF parallel resonant crystal, the device will generate 125MHz clocks with mixed LVDS and LVCMOS/ LVTTL output levels.

ICS844S0258-07 uses IDT's 3rd generation low phase noise VCO technology and can achieve <1ps typical RMS phase jitter, easily meeting Ethernet jitter requirements. ICS844S0258-07 is packaged in a small, 32-pin VFQFN package that is optimum for applications with space limitations.

Features

- Seven LVDS differential output at 125MHz
  One LVCMOS/LVTTL single-ended outputs at 125MHz
- Selectable crystal oscillator interface or LVCMOS/LVTTL single-ended input and PLL bypass from a single select pin
- Output enable signal for three LVDS outputs
- RMS phase jitter @ 125MHz, using a 25MHz crystal (1.857MHz - 20MHz): 0.278ps (typical)
- PCI Express (2.5Gb/s) and Gen 2 (5 Gb/s) jitter compliant
- Full 3.3V supply mode
- 0°C to 70°C ambient operating temperature
- Lead-free (RoHS 6) packaging

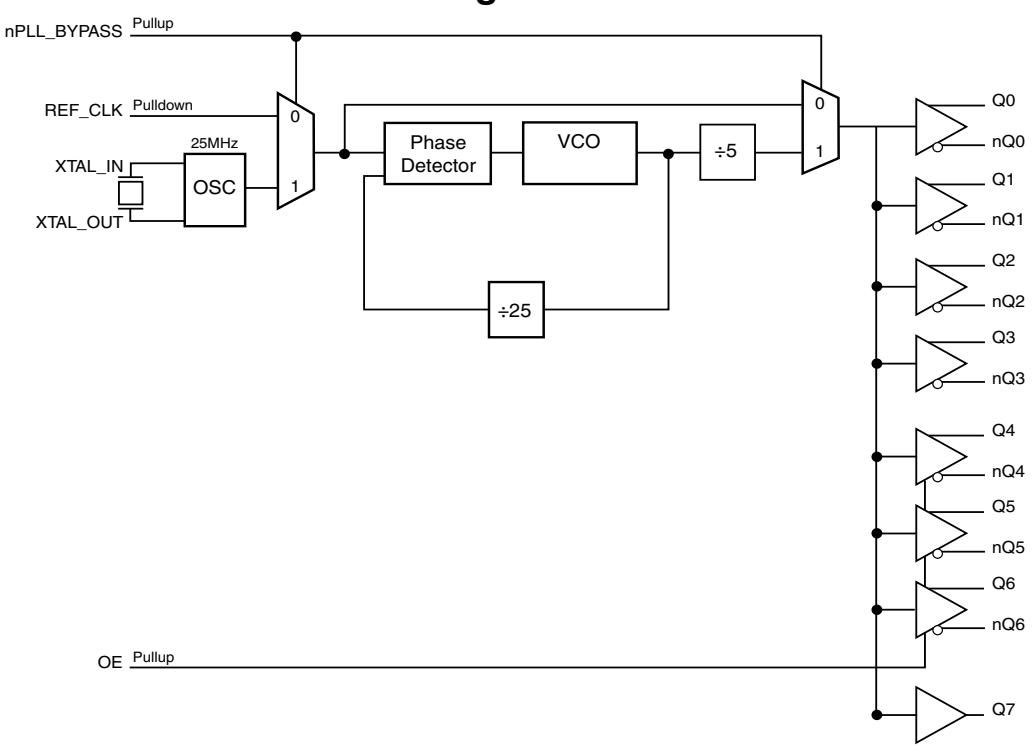
Pin Assignment



ICS844S0258-07

32-Lead VFQFN
5mm x 5mm x 0.925mm
package body
K Package
Top View

Block Diagram



Pin Descriptions and Characteristics

Table 1. Pin Descriptions

Number	Name	Type		Description
1, 2	Q0, nQ0	Output		Differential clock outputs. LVDS interface levels.
3, 9, 15, 24, 28, 32	GND	Power		Power supply ground.
4, 5	Q1, nQ1	Output		Differential clock outputs. LVDS interface levels.
6, 12, 19	V_{DDO_LVDS}	Power		Output supply pins for differential LVDS outputs.
7, 8	Q2, nQ2	Output		Differential clock outputs. LVDS interface levels.
10, 11	Q3, nQ3	Output		Differential clock outputs. LVDS interface levels.
13, 14	Q4, nQ4	Output		Differential clock outputs. LVDS interface levels.
16	OE	Input	Pullup	Output enable pin for Q[4:6]/nQ[4:6] outputs. If connected to HIGH or left open, enables the outputs. When connected to LOW or GND, disables the outputs to high-impedance state. LVCMOS/LVTTL interface levels.
17, 18	Q5, nQ5	Output		Differential clock outputs. LVDS interface levels.
20, 21	Q6, nQ6	Output		Differential clock outputs. LVDS interface levels.
22	V_{DDO_LVCMOS}	Power		Output supply pin for single-ended output.
23	Q7	Output		Single-ended clock output. LVCMOS/LVTTL levels.
25	V_{DD}	Power		Core supply pin.
26	nPLL_BYPASS	Input	Pullup	Input select and PLL bypass control pin. See Table 3. LVCMOS/LVTTL interface levels.
27	V_{DDA}	Power		Analog supply pin.
29	REF_CLK	Input	Pulldown	Single-ended reference clock input. Only selected in nPLL_BYPASS mode. LVCMOS/LVTTL interface levels.
30,31	XTAL_IN, XTAL_OUT	Input		Crystal oscillator interface. XTAL_OUT is the output, XTAL_IN is the input.

NOTE: *Pullup* and *Pulldown* refer to internal input resistors. See Table 2, *Pin Characteristics,* for typical values.

Table 2. Pin Characteristics

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
C_{IN}	Input Capacitance				2		pF
C_{PD}	Power Dissipation Capacitance	Q7	V_{DD}, V_{DDO_LVCMOS} = 3.465V		12		pF
R_{PULLUP}	Input Pullup Resistor				51		kΩ
$R_{PULLDOWN}$	Input Pulldown Resistor				51		kΩ
R_{OUT}	Output Impedance	Q7			20		Ω

Function Table

Table 3. PLL Bypass and Input Select Function Table

Inputs		
nPLL_BYPASS	**PLL Bypass**	**Input Selected**
0	PLL Bypassed	REF_CLK
1	PLL Enabled	XTAL_IN/XTAL_OUT

Absolute Maximum Ratings

NOTE: Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of the product at these conditions or any conditions beyond those listed in the *DC Characteristics or AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Item	Rating
Supply Voltage, V_{DD}	4.6V
Inputs, V_I XTAL_IN Other Inputs	 0V to V_{DD} -0.5V to V_{DD} + 0.5V
Outputs, I_O (LVCMOS)	-0.5V to V_{DDO_LVCMOS} + 0.5V
Outputs, I_O (LVDS) Continuos Current Surge Current	 10mA 15mA
Operating Temperature Range, T_A	0°C to +70°C
Package Thermal Impedance, θ_{JA}	39.5°C/W (0 mps)
Storage Temperature, T_{STG}	-65°C to 150°C

DC Electrical Characteristics

Table 4A. Power Supply DC Characteristics, $V_{DD} = V_{DDO\_LVCMOS} = V_{DDO\_LVDS} = 3.3V \pm 5\%$, $T_A = 0°C$ to 70°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{DD}	Core Supply Voltage		3.135	3.3	3.465	V
V_{DDA}	Analog Supply Voltage		V_{DD} – 0.20	3.3	V_{DD}	V
V_{DDO_LVCMOS} V_{DDO_LVDS}	Output Supply Voltage		3.135	3.3	3.465	V
I_{DD}	Power Supply Current				80	mA
I_{DDA}	Analog Supply Current				20	mA
I_{DDO_LVCMOS}, I_{DDO_LVDS}	Power Supply Current				120	mA

NOTE: The device has a power sequence requirement, refer to the Applications Section.

Table 4B. LVCMOS/LVTTL DC Characteristics, $V_{DD} = V_{DDO\_LVCMOS} = 3.3V \pm 5\%$, $T_A = 0°C$ to 70°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
V_{IH}	Input High Voltage			2.2		V_{DD} + 0.3	V
V_{IL}	Input Low Voltage			-0.3		0.8	V
I_{IH}	Input High Current	REF_CLK	$V_{DD} = V_{IN} = 3.465V$			150	µA
		OE, nPLL_BYPASS	$V_{DD} = V_{IN} = 3.465V$			10	µA
I_{IL}	Input Low Current	REF_CLK	$V_{DD} = 3.465V$, $V_{IN} = 0V$	-10			µA
		OE, nPLL_BYPASS	$V_{DD} = 3.465V$, $V_{IN} = 0V$	-150			µA
V_{OH}	Output High Voltage	Q7	V_{DDO_LVCMOS} = 3.3V±5%	2.6			V
V_{OL}	Output Low Voltage	Q7	V_{DDO_LVCMOS} = 3.3V±5%			0.5	V

Table 4C. LVDS DC Characteristics, $V_{DD} = V_{DDO\_LVDS} = 3.3V \pm 5\%$, $T_A = 0°C$ to $70°C$

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{OD}	Differential Output Voltage		300	400	525	mV
ΔV_{OD}	V_{OD} Magnitude Change				50	mV
V_{OS}	Offset Voltage		1.15	1.30	1.45	V
ΔV_{OS}	V_{OS} Magnitude Change				50	mV

Table 5. Crystal Characteristics

Parameter	Test Conditions	Minimum	Typical	Maximum	Units
Mode of Oscillation			Fundamental		
Frequency			25		MHz
Equivalent Series Resistance				50	Ω
Shunt Capacitance				7	pF

Table 6. AC Characteristics, $V_{DD} = V_{DDO\_LVCMOS} = V_{DDO\_LVDS} = 3.3V \pm 5\%$, $T_A = 0°C$ to $70°C$

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
f_{out}	Output Frequency				125		MHz
$t_{jit}(Ø)$	RMS Phase Noise Jitter; NOTE 1	LVDS	125MHz, Integration Range: 1.857MHz - 20MHz		0.278		ps
		LVCMOS	125MHz, Integration Range: 1.857MHz - 20MHz		0.284		ps
t_j	Phase Jitter Peak-to-Peak; NOTE 2		125MHz, (1.2MHz – 21.9MHz), Evaluation Band: 0Hz - Nyquist (clock frequency/2)		8.57		ps
$t_{REFCLK\_HF\_RMS}$	Phase Jitter RMS; NOTE 3		125MHz, 25MHz crystal input High Band: 1.5MHz - Nyquist (clock frequency/2)		0.86		ps
$t_{REFCLK\_LF\_RMS}$	Phase Jitter RMS; NOTE 3		125MHz, 25MHz crystal input Low Band: 10kHz - 1.5MHz		0.12		ps
t_R / t_F	Output Rise/Fall Time	Q[0:6]: nQ[0:6]	30% to 70%, 15pF Load	70		650	ps
		Q7	20% to 80%	400		900	ps
odc	Output Duty Cycle			48		52	%
odc	Output Duty Cycle, Bypass Mode			45		55	%

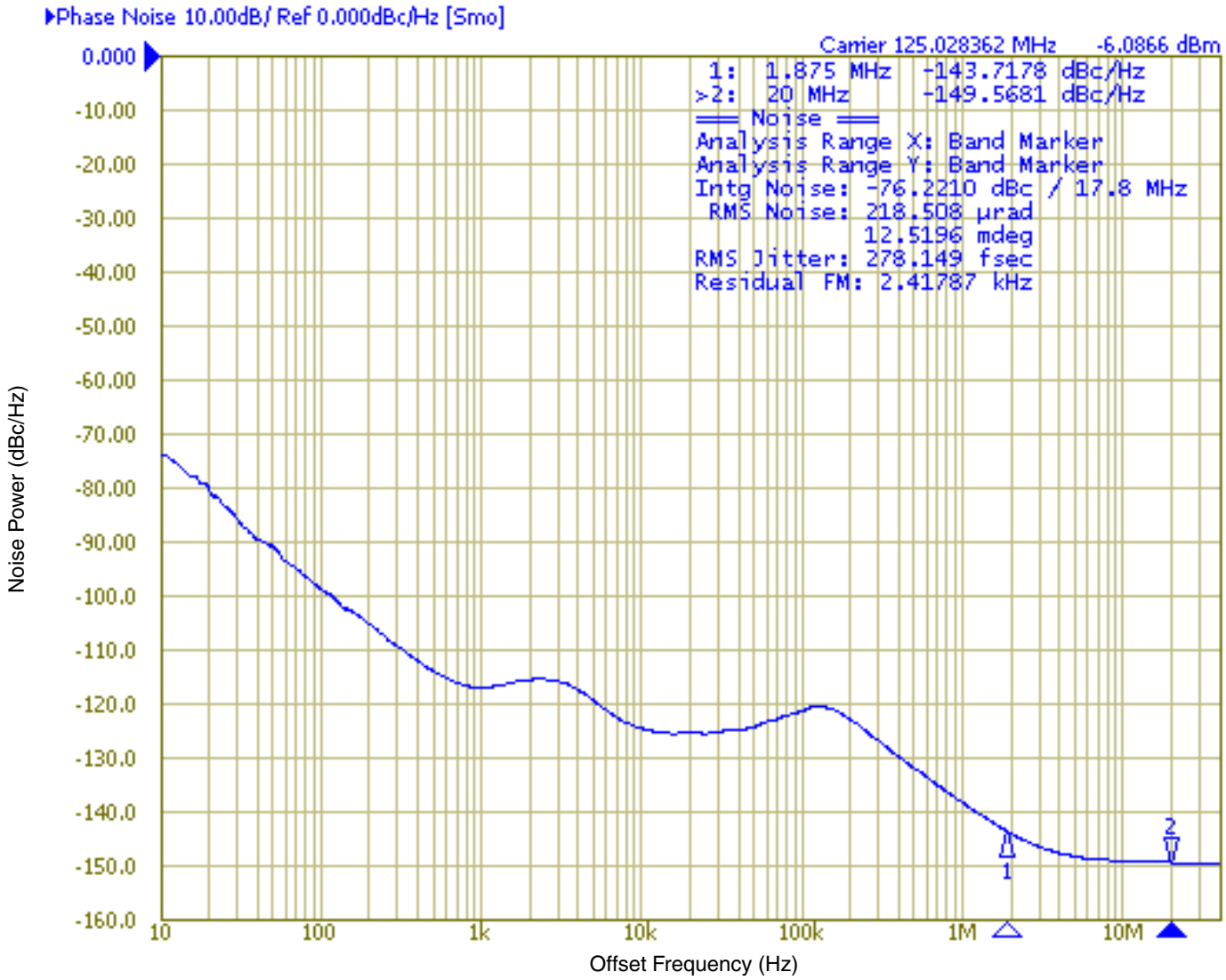
NOTE: Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lfpm. The device will meet specifications after thermal equilibrium has been reached under these conditions.

NOTE 1: Refer to Phase Noise Plots.

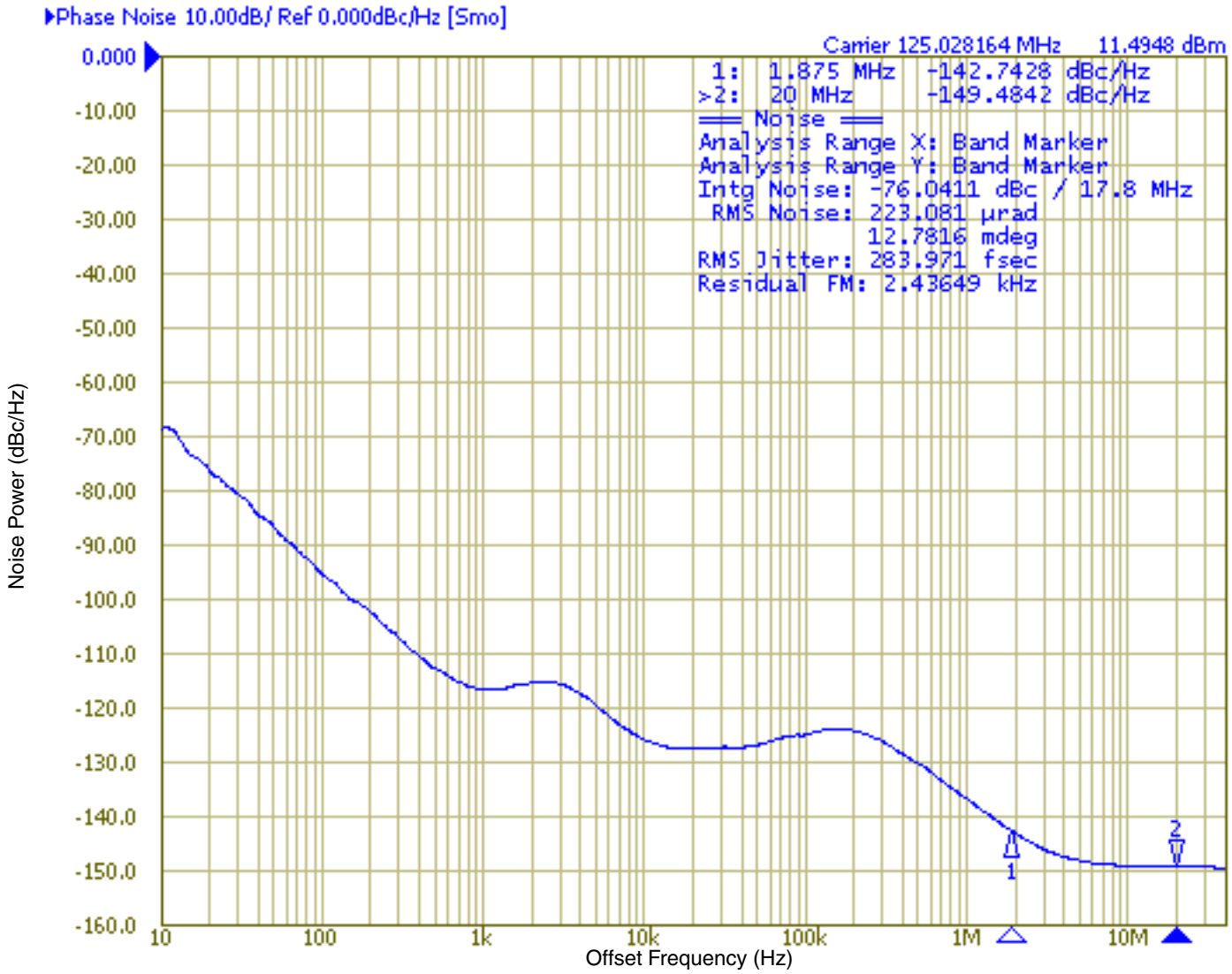
NOTE 2: Peak-to-Peak jitter after applying system transfer function for the Common Clock Architecture. Maximum limit for PCI Express Gen 1 is 86ps peak-to-peak for a sample size of 10^6 clock periods. See IDT Application Note *PCI Express Reference Clock Requirements* and also the PCI Express Application section of this datasheet which show each individual transfer function and the overall composite transfer function.

NOTE 3: RMS jitter after applying the two evaluation bands to the two transfer functions defined in the Common Clock Architecture and reporting the worst case results for each evaluation band. Maximum limit for PCI Express Generation 2 is 3.1ps rms for $t_{REFCLK\_HF\_RMS}$ (High Band) and 3.0ps RMS for $t_{REFCLK\_LF\_RMS}$ (Low Band). See IDT Application Note *PCI Express Reference Clock Requirements* and also the PCI Express Application section of this datasheet which show each individual transfer function and the overall composite transfer function.

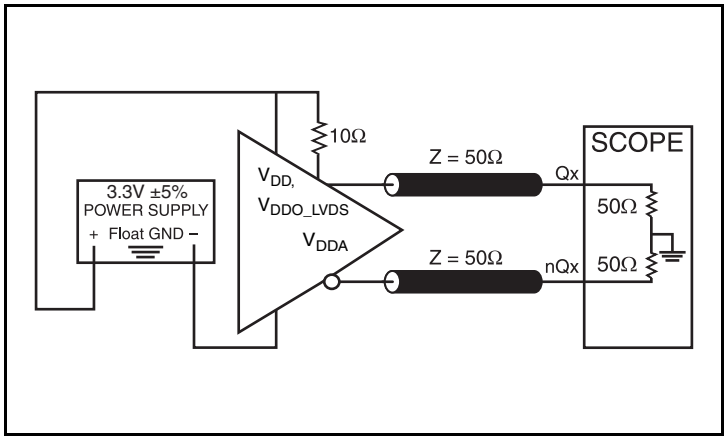
Typical Phase Noise at 125MHz (LVDS)



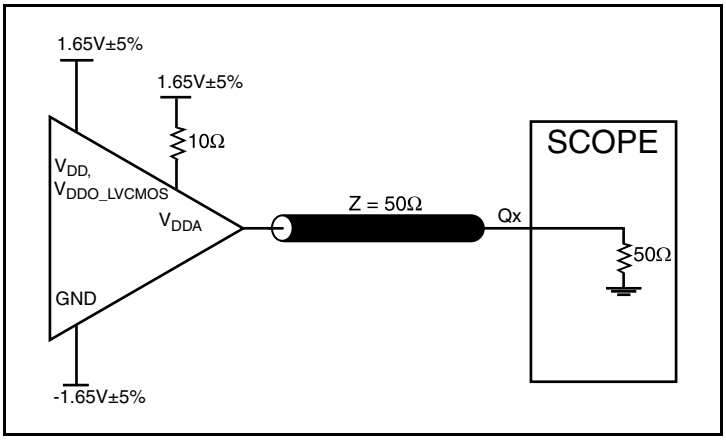
Typical Phase Noise at 125MHz (LVCMOS)



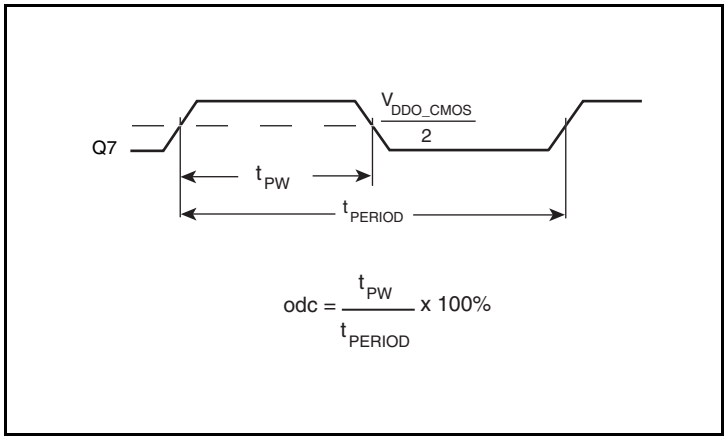
Parameter Measurement Information



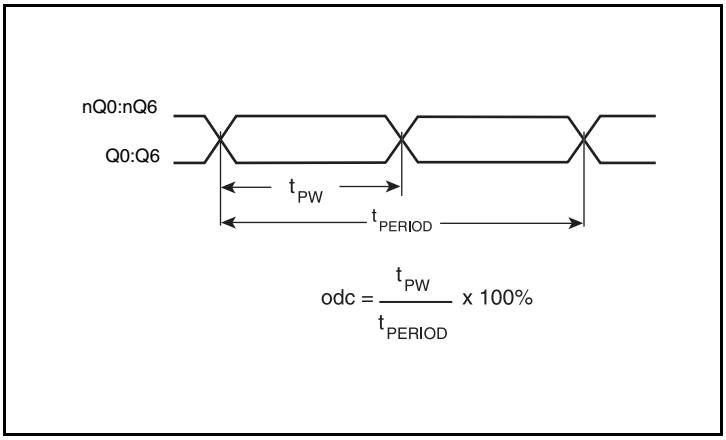
3.3V LVDS Output Load AC Test Circuit



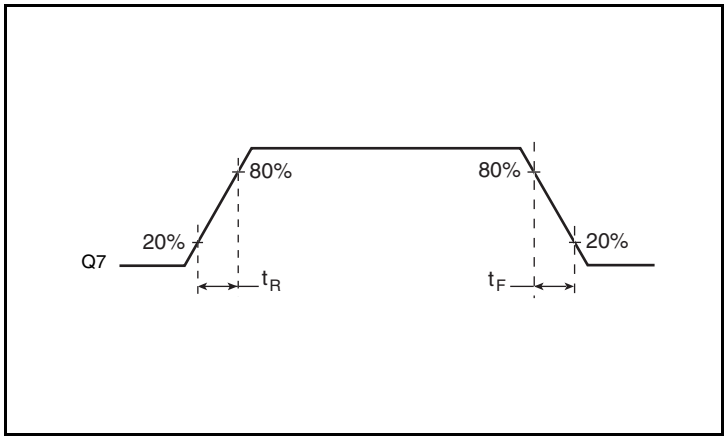
3.3V LVCMOS Output Load AC Test Circuit



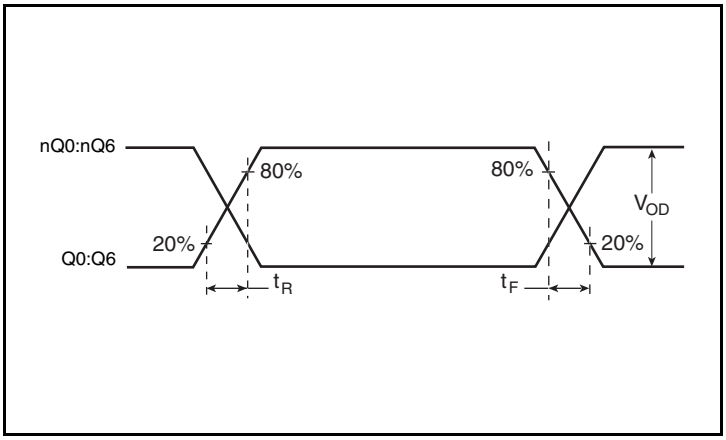
Single-Ended Output Duty Cycle/Pulse Width/Period



Differential Output Duty Cycle/Pulse Width/Period

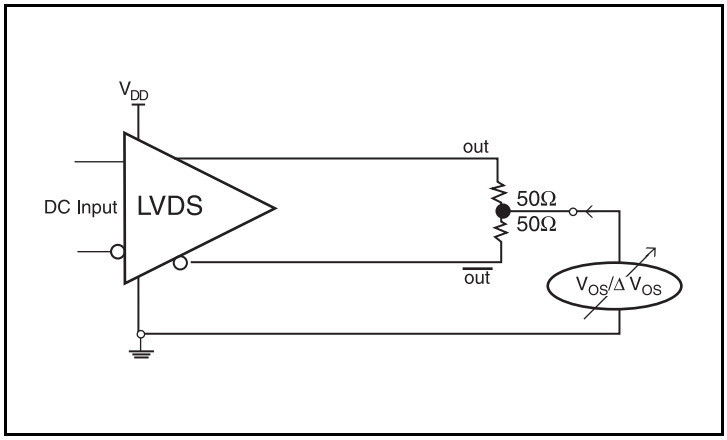


LVCMOS Output Rise/Fall Time

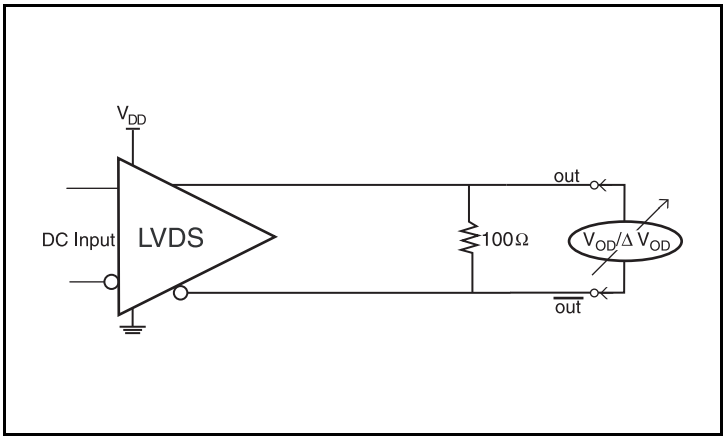


LVDS Output Rise/Fall Time

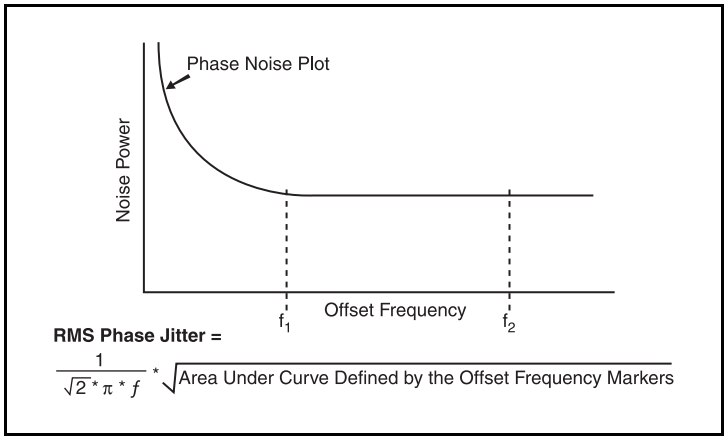
Parameter Measurement Information, continued



Offset Voltage Setup



Differential Output Duty Cycle/Pulse Width/Period



RMS Phase Jitter

Applications Information

Power Supply Filtering Technique

As in any high speed analog circuitry, the power supply pins are vulnerable to random noise. To achieve optimum jitter performance, power supply isolation is required. The ICS844S0258-07 provides separate power supplies to isolate any high switching noise from the outputs to the internal PLL. V_{DD}, V_{DDA}, V_{DDO_LVDS} and V_{DDO_LVCMOS} should be individually connected to the power supply plane through vias, and 0.01µF bypass capacitors should be used for each pin. *Figure 1* illustrates this for a generic V_{DD} pin and also shows that V_{DDA} requires that an additional 10Ω resistor along with a 10µF bypass capacitor be connected to the V_{DDA} pin.

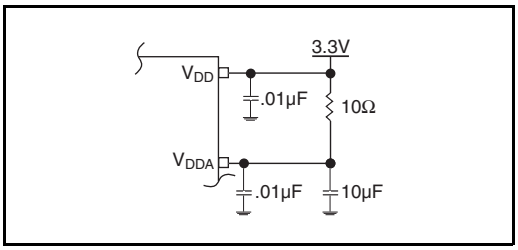


Figure 1. Power Supply Filtering

Power Supply Sequence Requirement

The ICS844S0258-07 has a power supply sequence requirement. This device requires that V_{DD} and V_{DDA} are powered simultaneously. This device has been characterized using the recommended power supply filtering techniques in Figure 1.

Power Sequence:

1. V_{DD} and V_{DDA}
2. V_{DDO_LVCMOS} and V_{DDO_LVDS}

Recommendations for Unused Input and Output Pins

Inputs:

Crystal Inputs

For applications not requiring the use of the crystal oscillator input, both XTAL_IN and XTAL_OUT can be left floating. Though not required, but for additional protection, a 1kΩ resistor can be tied from XTAL_IN to ground.

REF_CLK Input

For applications not requiring the use of a reference clock input, it can be left floating. Though not required, but for additional protection, a 1kΩ resistor can be tied from the REF_CLK input to ground.

LVCMOS Control Pins

All control pins have internal pullups or pulldowns; additional resistance is not required but can be added for additional protection. A 1kΩ resistor can be used.

Outputs:

LVDS Outputs

All unused LVDS output pairs can be either left floating or terminated with 100Ω across. If they are left floating, there should be no trace attached.

LVCMOS Output

All unused LVCMOS output can be left floating. There should be no trace attached.

Overdriving the XTAL Interface

The XTAL_IN input can be overdriven by an LVCMOS driver or by one side of a differential driver through an AC coupling capacitor. The XTAL_OUT pin can be left floating. The amplitude of the input signal should be between 500mV and 1.8V and the slew rate should not be less than 0.2V/nS. For 3.3V LVCMOS inputs, the amplitude must be reduced from full swing to at least half the swing in order to prevent signal interference with the power rail and to reduce internal noise. *Figure 2A* shows an example of the interface diagram for a high speed 3.3V LVCMOS driver. This configuration requires that the sum of the output impedance of the driver (Ro) and the series resistance (Rs) equals the transmission line impedance. In addition, matched termination at the crystal input will attenuate the signal in half. This can be done in one of two ways. First, R1 and R2 in parallel should equal the transmission line impedance. For most 50Ω applications, R1 and R2 can be 100Ω. This can also be accomplished by removing R1 and changing R2 to 50Ω. The values of the resistors can be increased to reduce the loading for a slower and weaker LVCMOS driver. *Figure 2B* shows an example of the interface diagram for an LVPECL driver. This is a standard LVPECL termination with one side of the driver feeding the XTAL_IN input. It is recommended that all components in the schematics be placed in the layout. Though some components might not be used, they can be utilized for debugging purposes. The datasheet specifications are characterized and guaranteed by using a quartz crystal as the input.

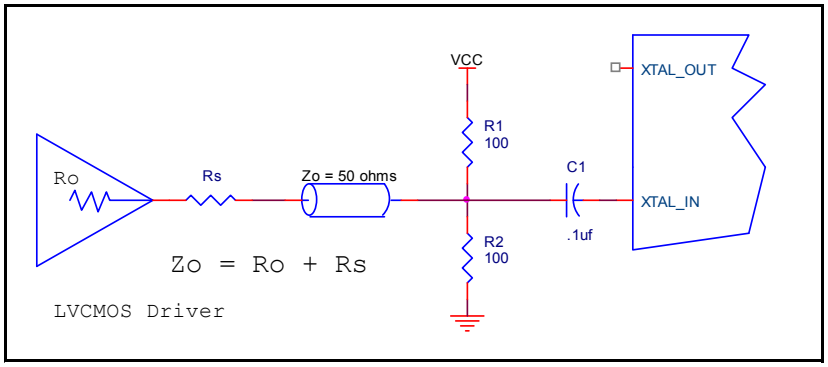


Figure 2A. General Diagram for LVCMOS Driver to XTAL Input Interface

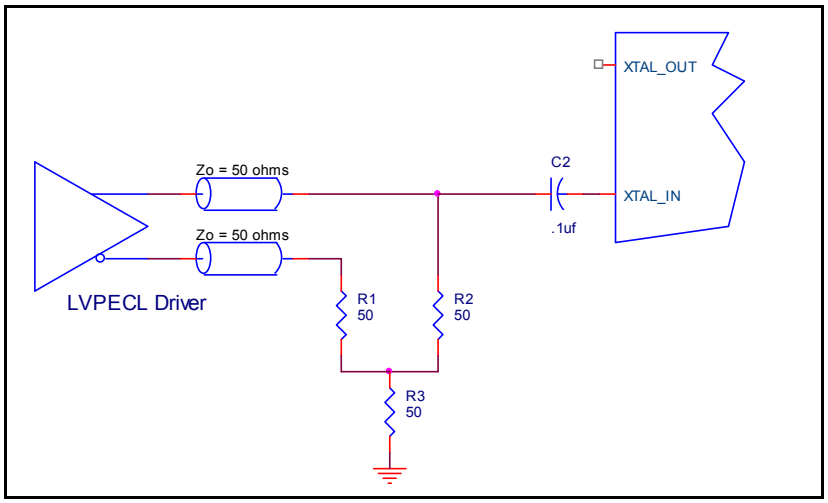


Figure 2B. General Diagram for LVPECL Driver to XTAL Input Interface

Crystal Input Interface

The ICS844S0258-07 has been characterized with 18pF parallel resonant crystals. The capacitor values shown in *Figure 2* below were determined using a 25MHz, 18pF parallel resonant crystal and were chosen to minimize the ppm error.

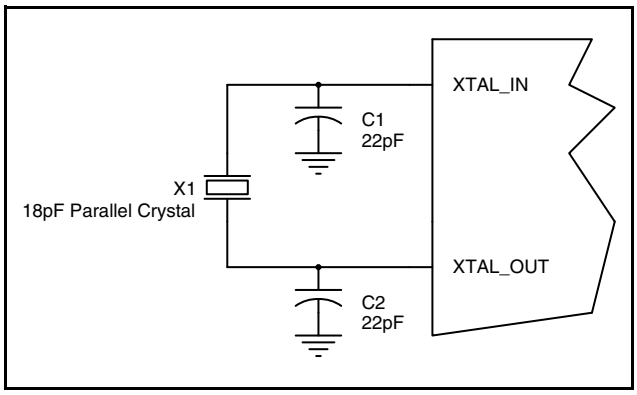


Figure 2. Crystal Input Interface

LVDS Driver Termination

A general LVDS interface is shown in *Figure 4.* Standard termination for LVDS type output structure requires both a 100Ω parallel resistor at the receiver and a 100Ω differential transmission line environment. In order to avoid any transmission line reflection issues, the 100Ω resistor must be placed as close to the receiver as possible. IDT offers a full line of LVDS compliant devices with two types of output structures: current source and voltage source. The standard termination schematic as shown in Figure 4 can be used with either type of output structure. If using a non-standard termination, it is recommended to contact IDT and confirm if the output is a current source or a voltage source type structure. In addition, since these outputs are LVDS compatible, the input receivers amplitude and common mode input range should be verified for compatibility with the output.

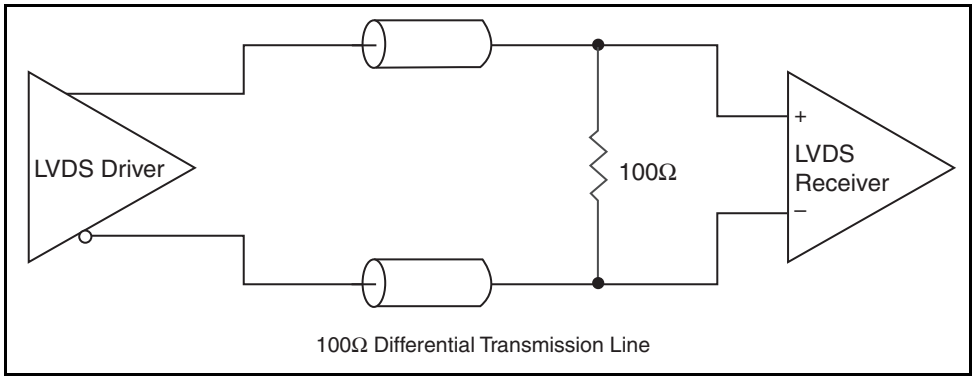


Figure 4. Typical LVDS Driver Termination

VFQFN EPAD Thermal Release Path

In order to maximize both the removal of heat from the package and the electrical performance, a land pattern must be incorporated on the Printed Circuit Board (PCB) within the footprint of the package corresponding to the exposed metal pad or exposed heat slug on the package, as shown in *Figure 5.* The solderable area on the PCB, as defined by the solder mask, should be at least the same size/shape as the exposed pad/slug area on the package to maximize the thermal/electrical performance. Sufficient clearance should be designed on the PCB between the outer edges of the land pattern and the inner edges of pad pattern for the leads to avoid any shorts.

While the land pattern on the PCB provides a means of heat transfer and electrical grounding from the package to the board through a solder joint, thermal vias are necessary to effectively conduct from the surface of the PCB to the ground plane(s). The land pattern must be connected to ground through these vias. The vias act as “heat pipes”. The number of vias (i.e. “heat pipes”) are application specific and dependent upon the package power dissipation as well as electrical conductivity requirements. Thus, thermal and electrical analysis and/or testing are recommended to determine the minimum number needed. Maximum thermal and electrical performance is achieved when an array of vias is incorporated in the land pattern. It is recommended to use as many vias connected to ground as possible. It is also recommended that the via diameter should be 12 to 13mils (0.30 to 0.33mm) with 1oz copper via barrel plating. This is desirable to avoid any solder wicking inside the via during the soldering process which may result in voids in solder between the exposed pad/slug and the thermal land. Precautions should be taken to eliminate any solder voids between the exposed heat slug and the land pattern. Note: These recommendations are to be used as a guideline only. For further information, please refer to the Application Note on the Surface Mount Assembly of Amkor’s Thermally/ Electrically Enhance Leadframe Base Package, Amkor Technology.

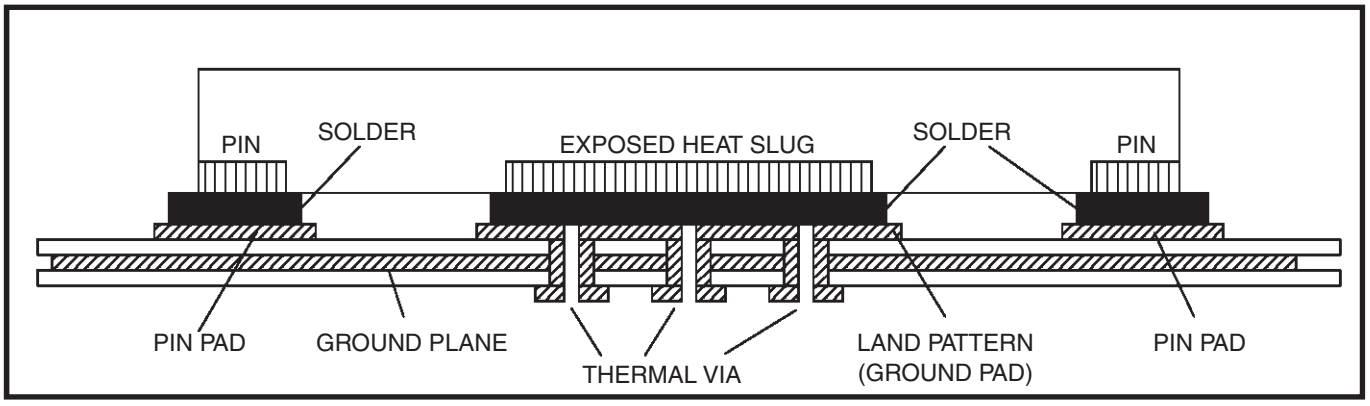


Figure 5. P.C. Assembly for Exposed Pad Thermal Release Path – Side View (drawing not to scale)

Schematic Example

Figure 6 shows an example of ICS844S0258-07 application schematic. In this example, the device is operated at $V_{DD} = V_{DDO\_LVDS} = V_{DDO\_LVCMOS} = 3.3V$. The 18pF parallel resonant 25MHz crystal is used. The C1 = 22pF and C2 = 22pF are recommended for frequency accuracy. For different board layouts, the C1 and C2 may be slightly adjusted for optimizing frequency accuracy. Two examples of LVDS for receiver without built-in termination and one example of LVCMOS are shown in this schematic.

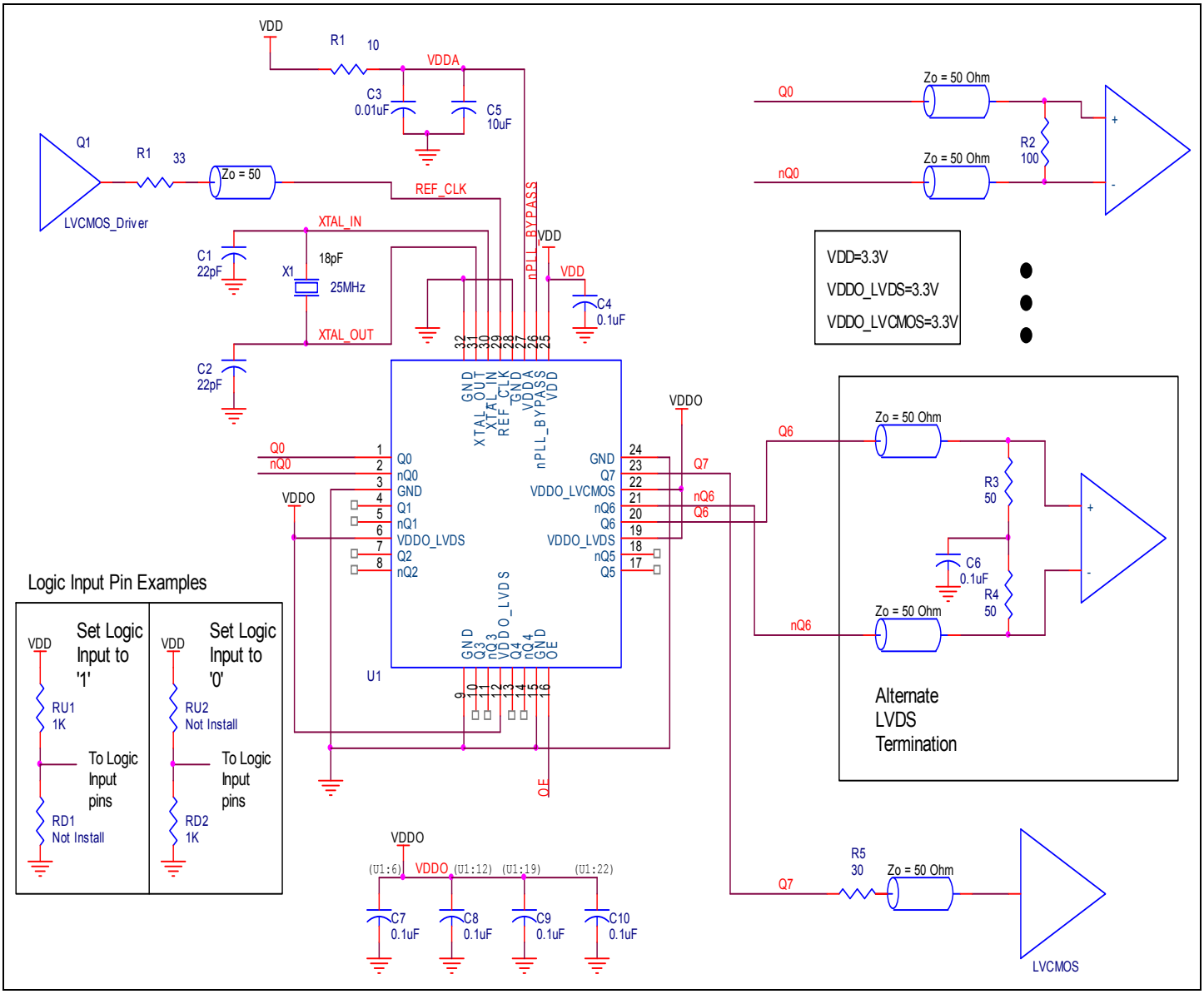
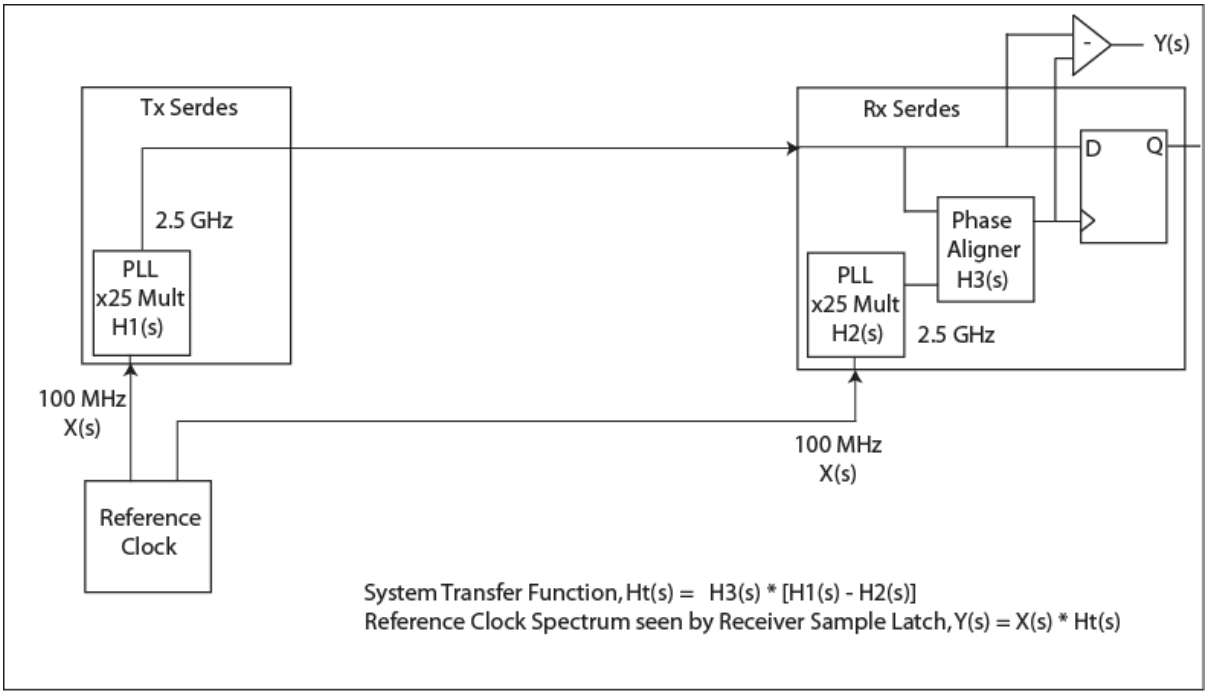


Figure 6. ICS844S0258-07 Schematic Example

PCI Express Application Note

PCI Express jitter analysis methodology models the system response to reference clock jitter. The below block diagram shows the most frequently used *Common Clock Architecture* in which a copy of the reference clock is provided to both ends of the PCI Express Link.



In the jitter analysis, the Tx and Rx serdes PLLs are modeled as well as the phase interpolator in the receiver. These transfer functions are called H1, H2, and H3 respectively. The overall system transfer function at the receiver is:

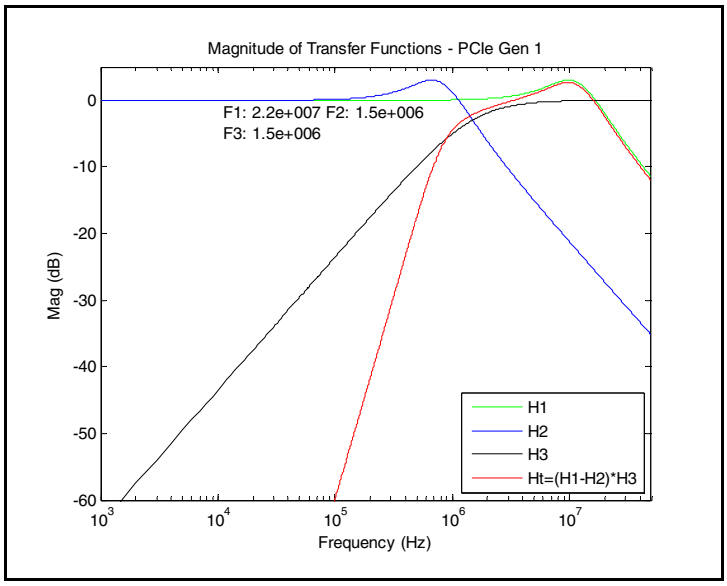
$$Ht(s) = H3(s) \times [H1(s) - H2(s)]$$

The jitter spectrum seen by the receiver is the result of applying this system transfer function to the clock spectrum X(s) and is:

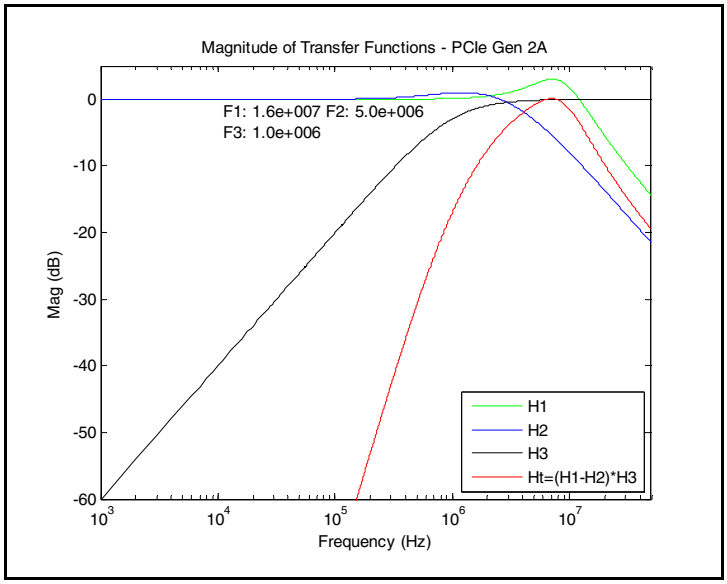
$$Y(s) = X(s) \times H3(s) \times [H1(s) - H2(s)]$$

In order to generate time domain jitter numbers, an inverse Fourier Transform is performed on X(s)*H3(s) * [H1(s) - H2(s)].

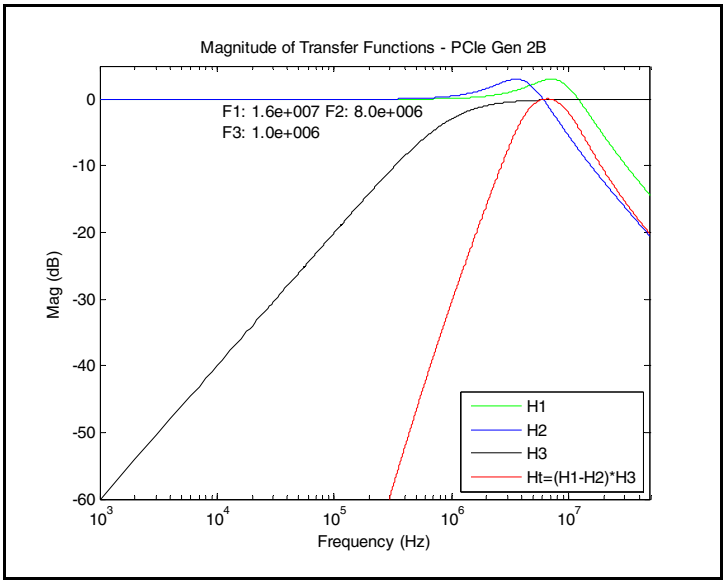
For PCI Express Gen 1, one transfer function is defined and the evaluation is performed over the entire spectrum: DC to Nyquist (e.g for a 100MHz reference clock: 0Hz to 50MHz) and the jitter result is reported in peak-peak. For PCI Express Gen 2, two transfer functions are defined with 2 evaluation ranges and the final jitter number is reported in rms. The two evaluation ranges for PCI Express Gen 2 are 10kHz - 1.5MHz (Low Band) and 1.5MHz - Nyquist (High Band). The below plots show the individual transfer functions as well as the overall transfer function Ht. The respective -3 dB pole frequencies for each transfer function are labeled as F1 for transfer function H1, F2 for H2, and F3 for H3. For a more thorough overview of PCI Express jitter analysis methodology, please refer to IDT Application Note *PCI Express Reference Clock Requirements.*



PCIe Gen 1 Magnitude of Transfer Function



PCIe Gen 2A Magnitude of Transfer Function



PCIe Gen 2B Magnitude of Transfer Function

Power Considerations

This section provides information on power dissipation and junction temperature for the ICS844S0258-07. Equations and example calculations are also provided.

1. Power Dissipation.

The total power dissipation for the ICS44S0258-07 is the sum of the core power plus the analog plus the power dissipated in the load(s). The following is the power dissipation for V_{DD} = 3.3V + 5% = 3.465V, which gives worst case results.

Core and LVDS Output Power Dissipation

- Power (core, LVDS) = V_{DD_MAX} * (I_{DD} + I_{DDO_LVDS} + I_{DDA}) = 3.465V * (80mA + 120mA + 20mA) = **762.3mW**

LVCMOS Output Power Dissipation

- Output Impedance R_{OUT} Power Dissipation due to Loading 50Ω to V_{DDO}/2
  Output Current I_{OUT} = V_{DDO_MAX} / [2 * (50Ω + R_{OUT})] = 3.465V / [2 * (50Ω + 20Ω)] = **24.75mA**
- Power Dissipation on the R_{OUT} per LVCMOS output
  Power (R_{OUT}) = R_{OUT} * (I_{OUT})^2 = 20Ω * (24.75mA)^2 = **12.25mW per output**
- Dynamic Power Dissipation at 125MHz
  Power (125MHz) = C_{PD} * Frequency * (V_{DDO})^2 = 12pF * 125MHz * (3.465V)^2 = **18.01mW per output**

Total Power Dissipation

- **Total Power**
  = Power (core, LVDS) + Power (R_{OUT}) + Power (125MHz)
  = 762.3mW + 12.25mW + 18.01mW
  = 792.56mW

2. Junction Temperature.

Junction temperature, Tj, is the temperature at the junction of the bond wire and bond pad directly affects the reliability of the device. The maximum recommended junction temperature is 125°C. Limiting the internal transistor junction temperature, Tj, to 125°C ensures that the bond wire and bond pad temperature remains below 125°C.

The equation for Tj is as follows: Tj = θ_{JA} * Pd_total + T_A

Tj = Junction Temperature

θ_{JA} = Junction-to-Ambient Thermal Resistance

Pd_total = Total Device Power Dissipation (example calculation is in section 1 above)

T_A = Ambient Temperature

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance θ_{JA} must be used. Assuming no air flow and a multi-layer board, the appropriate value is 39.5°C/W per Table 7 below.

Therefore, Tj for an ambient temperature of 70°C with all outputs switching is:

70°C + 0.793W * 39.5°C/W = 101.3°C. This is well below the limit of 125°C.

This calculation is only an example. Tj will obviously vary depending on the number of loaded outputs, supply voltage, air flow and the type of board (multi-layer).

Table 7. Thermal Resistance θ_{JA} for 32 Lead VFQFN, Forced Convection

θ_{JA} **Vs. Air Flow**			
Meters per Second	**0**	**1**	**2.5**
Multi-Layer PCB, JEDEC Standard Test Boards	39.5°C/W	34.5°C/W	31.0°C/W

Reliability Information

Table 8. θ_{JA} vs. Air Flow Table for a 32 Lead VFQFN

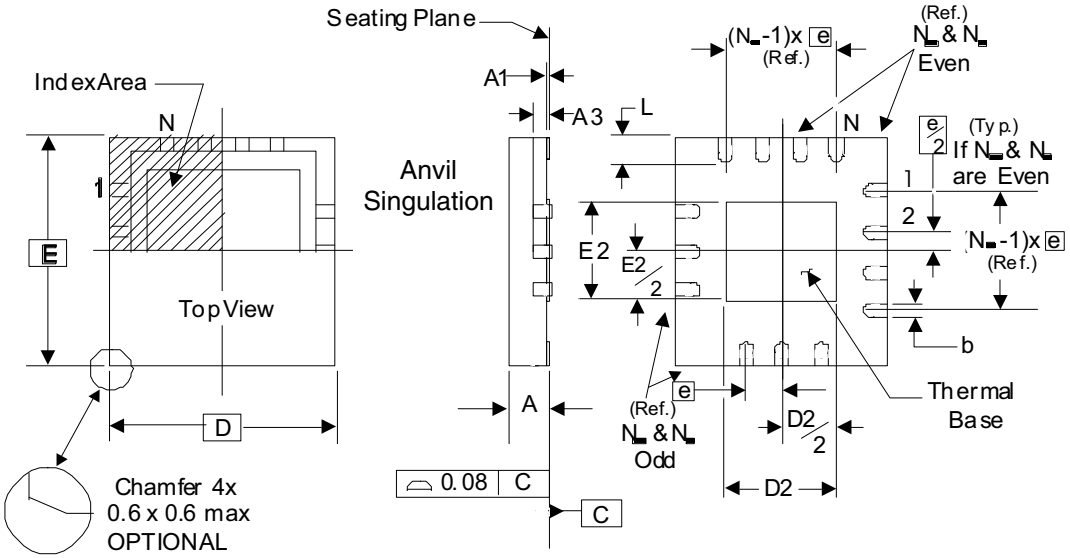
θ_{JA} vs. Air Flow			
Meters per Second	**0**	**1**	**2.5**
Multi-Layer PCB, JEDEC Standard Test Boards	39.5°C/W	34.5°C/W	31.0°C/W

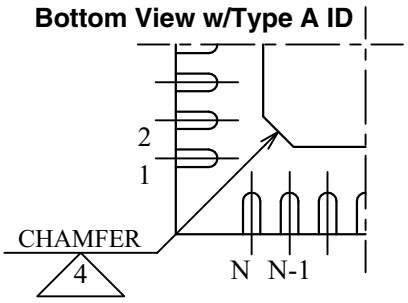
Transistor Count

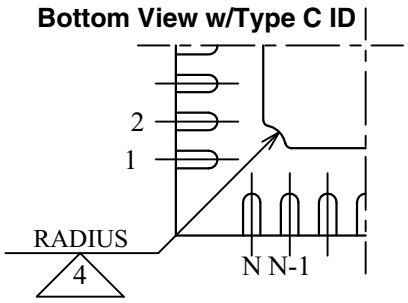
The transistor count for ICS844S0258-07 is: 8989

Package Outline and Package Dimensions

Package Outline - K Suffix for 32 Lead VFQFN







There are 2 methods of indicating pin 1 corner at the back of the VFQFN package:

1. Type A: Chamfer on the paddle (near pin 1)
2. Type C: Mouse bite on the paddle (near pin 1)

Table 9. Package Dimensions

JEDEC Variation: VHHD-2/-4 All Dimensions in Millimeters			
Symbol	**Minimum**	**Nominal**	**Maximum**
N		32	
A	0.80		1.00
A1	0		0.05
A3		0.25 Ref.	
b	0.18	0.25	0.30
N_D & N_E			8
D & E		5.00 Basic	
D2 & E2	3.0		3.3
e		0.50 Basic	
L	0.30	0.40	0.50

Reference Document: JEDEC Publication 95, MO-220

The following package mechanical drawing is a generic drawing that applies to any pin count VFQFN package. This drawing is not intended to convey the actual pin count or pin layout of this device. The pin count and pinout are shown on the front page. The package dimensions are in Table 9.

Ordering Information

Table 10. Ordering Information

Part/Order Number	Marking	Package	Shipping Packaging	Temperature
844S0258CK-07LF	ICS0258C07L	“Lead-Free” 32 Lead VFQFN	Tray	0°C to 70°C
844S0258CK-07LFT	ICS0258C07L	“Lead-Free” 32 Lead VFQFN	Tape & Reel	0°C to 70°C

Revision History Sheet

Rev	Table	Page	Description of Change	Date
A	 T10 T10	1 19 19	Deleted HyperClock logo. Deleted quantity from ordering information. Deleted leaded parts note.	12/2/2013

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