Application Note

Dialog's GreenFET Load Switch Basics

AN-1068

Abstract

This application note describes the general operation and protection circuits of GreenFET Load Switch products.

Contents

Abstract **1**

Contents **2**

Figures **2**

References **2**

1 Introduction **3**

2 GreenFET Load Switch Operation **4**

2.1 General Circuit Operation 4

2.2 Discharge Function 4

2.3 Active Current Limit 7

2.4 Thermal Protection 7

2.5 Short-Circuit Current Limit 8

3 Reverse Current Blocking **9**

3.1 Using Back-to-Back FETs 9

3.2 Using FET Bulk Switching 9

3.3 V_{OUT} Slew Rate Control 10

4 Slew Rate Control Sensitivity Analysis **11**

5 Conclusion **11**

Revision History **11**

Figures

Figure 1: SLG59610V Load Switch Block Diagram with Discharge 3
Figure 2: SLG59611V Load Switch Block Diagram No Discharge 4
Figure 3: General Circuit Operation Timing Diagram without Discharge Circuit 5
Figure 4: General Circuit Operation Timing Diagram with Discharge Circuit 5
Figure 5: Waveforms of Active Current Limit, Then to Thermal Shutdown 6
Figure 6: Waveforms Displaying Short Circuit Current Limit 6
Figure 7: Active Current Limit and Thermal Protection Operation 8
Figure 8: Active Current Limit and Thermal Protection Operation 8
Figure 9: Back-to-Back FET Reverse Blocking 9
Figure 10: Reverse Voltage Detection 10
Figure 11: Cross Section of the Bulk Switching FET 10
Figure 12: SLG59M1527V Block Diagram 10
Figure 13: Slew Rate Control Sensitivity Diagram 11

References

[1] SLG59M301V Datasheet, Dialog Semiconductor

[2] SLG59M1446V Datasheet, Dialog Semiconductor

[3] SLG59M610V Datasheet, Dialog Semiconductor

[4] SLG59M611V Datasheet, Dialog Semiconductor

[5] SLG59M1527V Datasheet, Dialog Semiconductor

1 Introduction

GreenFET load switch protection circuits include active current limit, thermal protection, short-circuit protection and reverse current blocking. From Figure 1 and Figure 2, the SLG59M610V and the SLG59M611V block diagrams illustrate several functions that will be discussed. Figure 1 is representative of a reverse blocking load switch with protection features and an additional component known as a discharge circuit. Figure 2 is that of Figure 1 but without the discharge circuit. Finally, the V_{OUT} slew-rate control including sensitivity analysis will be discussed with respect to the use of an external capacitor.

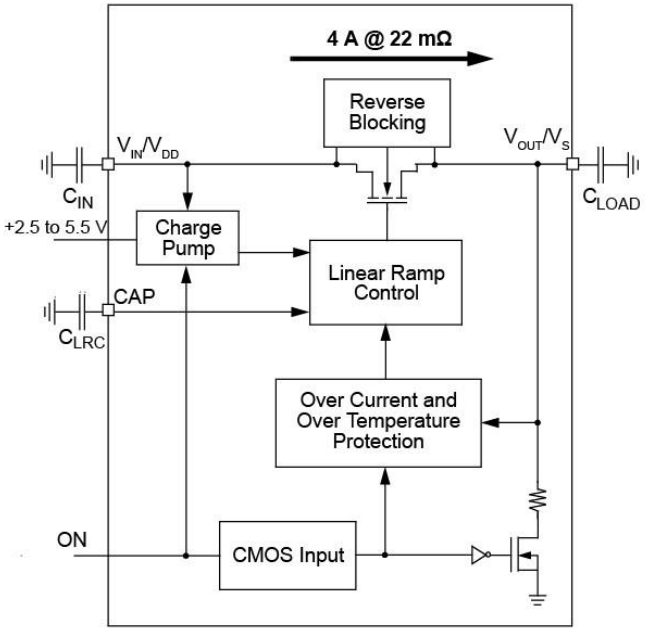

Figure 1: SLG59610V Load Switch Block Diagram with Discharge

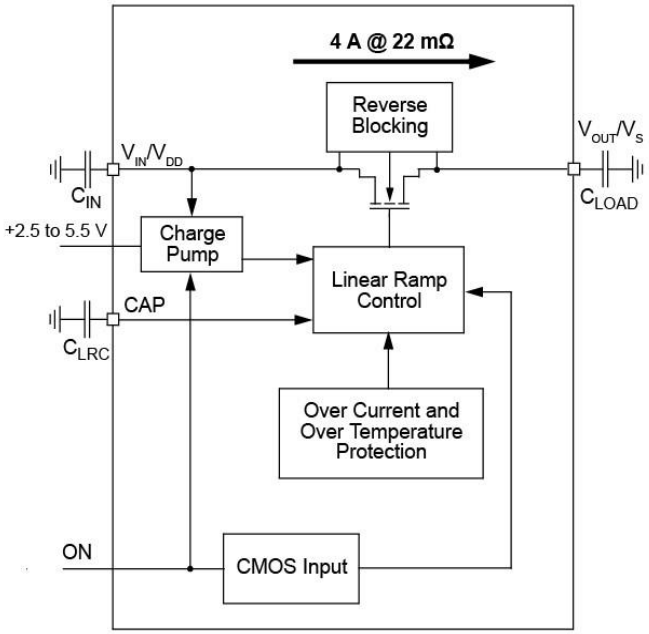

Figure 2: SLG59611V Load Switch Block Diagram No Discharge

2 GreenFET Load Switch Operation

2.1 General Circuit Operation

The operational start up procedure, displayed in Figure 3 and Figure 4, applies to all GreenFET devices. The V_{DD} voltage is first applied then V_D is applied. The GreenFET Load Switch internal state machine is actuated when V_{DD} is higher than 1 V, typically the minimum turn-on voltage. V_D will rise to the V_{DD} value after which V_{DD} is set greater than 1 V. Once V_{DD} and V_D reach their respective steady-state value, the ON pin is toggled low to high for active HIGH Load Switch options or high to low for active LOW Load Switch options. While the ON pin is HIGH, the voltage on the source terminal of the FET will rise to the V_{DD} value after a time delay, t_{ON} DLY. The rise time, t_{RISE}, of the output voltage at V_S is defined to be from the V_S signal at 10% to 90% of its steady-state value.

The slope or the slew-rate varies depending on the internal and external components of the GreenFET circuits. This will be discussed in further detail in the V_{OUT} slew-rate control section. The total amount of time for the V_S waveform to reach 90% of the steady state value from the rising edge of the ON cycle labeled as t_{ON}. The ON pin delay time, t_{ON} DLY, and the total turn on time, t_{ON}, are stated in the datasheet.

2.2 Discharge Function

Dialog's GreenFET Load Switches without discharge circuit would mean that the V_S, the output voltage on the C_{LOAD}, would be held at its voltage value, for there is no current flow to release charge when the ON pin is toggled low. This is portrayed through the timing diagrams shown in Figure 3.

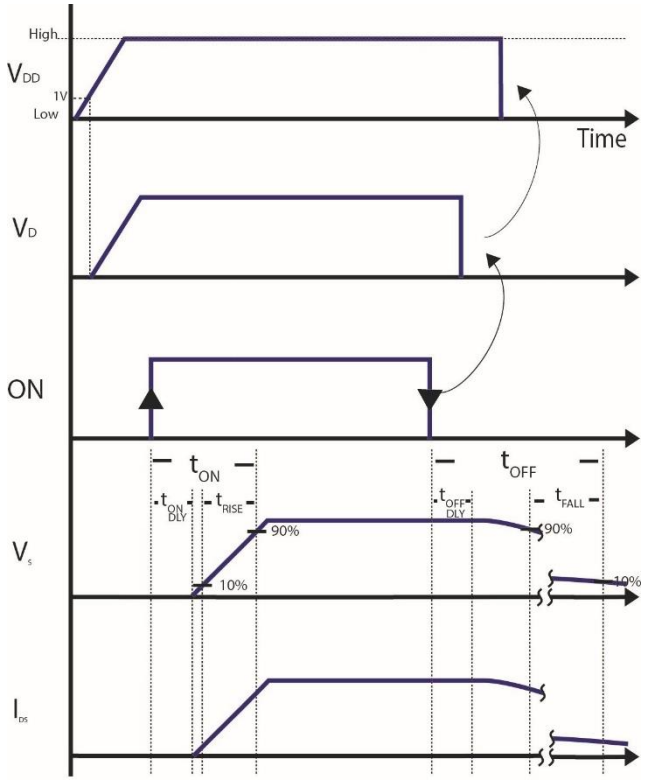

Figure 3: General Circuit Operation Timing Diagram without Discharge Circuit

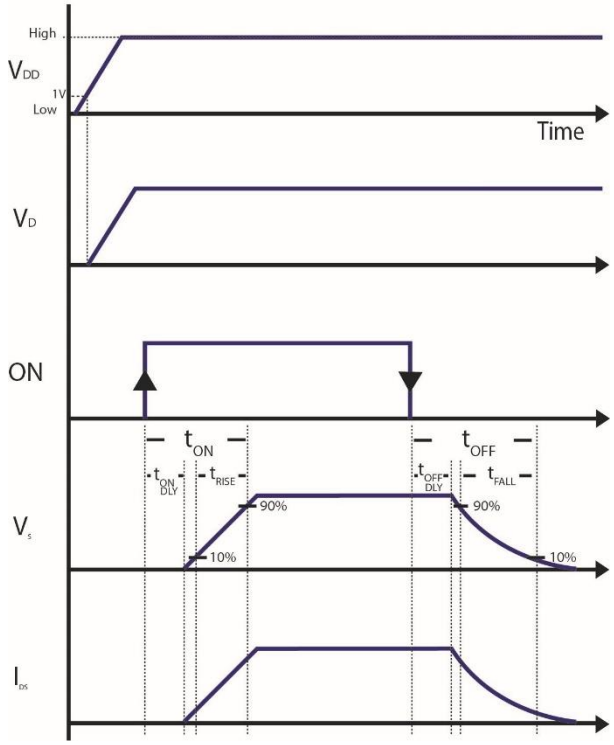

Figure 4: General Circuit Operation Timing Diagram with Discharge Circuit

Even with the V_D and the V_{DD} switched off, the V_S signal will be mainly unaffected because of the absence of a discharge circuit. Eventually, with the ON pin still low, V_S will decay to parasitic leakage current.

Select GreenFET Load Switches feature a discharge function. Figure 4 shows, with the addition of a discharge circuit, output voltage fall time is reduced. When the ON pin toggles low, there is a time delay before the V_S starts to decay denoted as t_{OFF} DLY. The total time for which the V_S dissipates from the ON pin toggled low to V_S decayed to 10% of its peak value, is indicated as t_{OFF}. The discharge circuit is analogous to the voltage response of a RC circuit, an exponential decay from its initial voltage level.

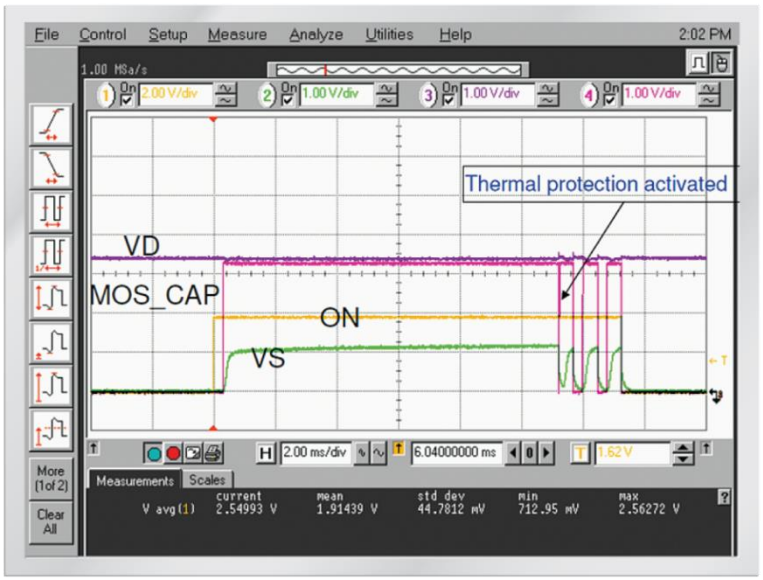

Figure 5: Waveforms of Active Current Limit, Then to Thermal Shutdown

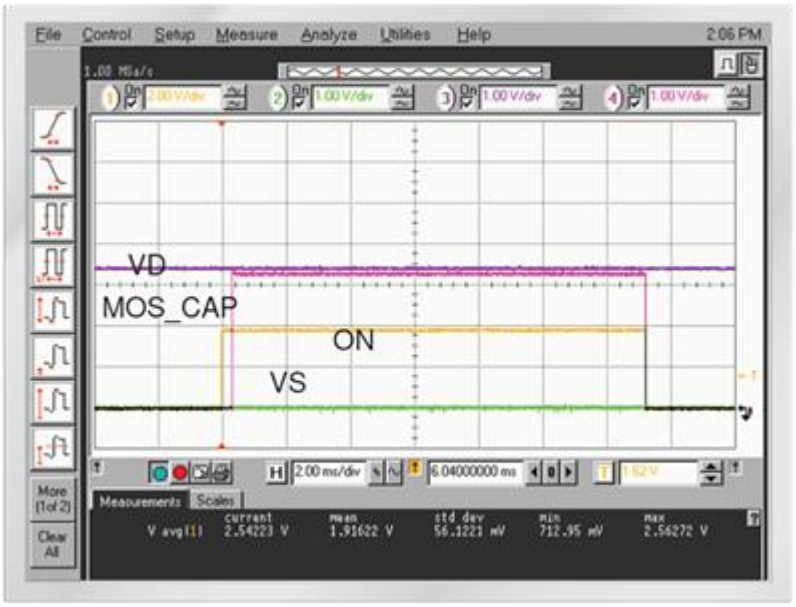

Figure 6: Waveforms Displaying Short Circuit Current Limit

2.3 Active Current Limit

While the GreenFET is in operation, the FET limits how much current it could handle. In those GreenFET Load Switches where this feature is available, the GreenFET Load Switches' active current limit is implemented internally on the I GreenFET Load Switches' main FET, by monitoring the status of the V_S pin voltage. If the voltage of V_S pin is higher than 1 V, the internal active current circuitry is not enabled. If an overcurrent event causes the V_S pin voltage to fall approximately 1 V, then the GreenFET Load Switches' internal active current limit (ACL) circuitry is enabled. The voltage is compared to the band gap voltage of which determines whether the current protection is enacted or not. If the input voltage falls below the gate drive voltage or less than one, this protection would be enacted. The active current limit protection scheme is illustrated through the timing diagram shown in Figure 7, highlighted in blue.

This protection scheme can be triggered by intentionally attaching a small load on the source terminal, to reduce the V_S voltage and cause a large amount of current to flow through the FET. As shown in the I_{DS} waveform, slight inrush current occurs and is held at the active current limit until the input voltage becomes greater than the gate drive voltage of the FET. Lowering the V_D voltage would lower the current flow, bringing it out of active current limitation mode and return back to its steady state current value.

2.4 Thermal Protection

This form of current limiting is to prevent the device from operating at high junction temperatures. From Figure 7, the orange shaded region displays the thermal protection operation after the active current limit circuit is automatically deactivated. The thermal protection circuit shuts off the FET when the die temperature reaches 125 °C, caused by heating.

V_S drops to 250 mV and I_{DS} drops to short current limit, then at thermal shutoff turn-off temperature the FET recovers to its normal operation.

The listed thermal shutoff turn-on temperature and the thermal shutoff turn-off temperature are based on the junction temperature, Tj. The equation for junction temperature is:

$$T_j = P_D * \theta_{jA} + T_A$$

TA is the ambient temperature during operation

θ_{jA} is the junction to air thermal impedance, roughly 70 °C/W for the GreenFETs

P_D is power dissipation produced by the I_{DS} current squared times the RDS(ON). This parameter is shown in the timing diagram below in Figure 7 and Figure 8.

From Figure 8, when the FET is in active current limitation mode, thermal protection operation may be induced by internal heating. As the gate voltage drops, the RDS(ON) of the FET increases, limiting the current, but also increases the power dissipation of the integrated circuit. The IC does not dissipate a lot of power due to its architecture so instead it will heat up to address the current limit condition. When the GreenFET Load Switch reaches to its thermal shutoff turn on temperature, the gate voltage will be driven low to turn off the FET. In this process, the I_{DS} switches between the ACL level and SCL(short circuit) level. From the scope capture of Figure 5 as shown, V_S is toggling when thermal protection is activated. The V_{DD} will increase the gate voltage in order to resume driving the GreenFET when the die cools down to 100 °C. If the current limiting condition still persists and the device heats up to 125 °C, the process of which the gate drive voltage shuts off the FET will repeat.

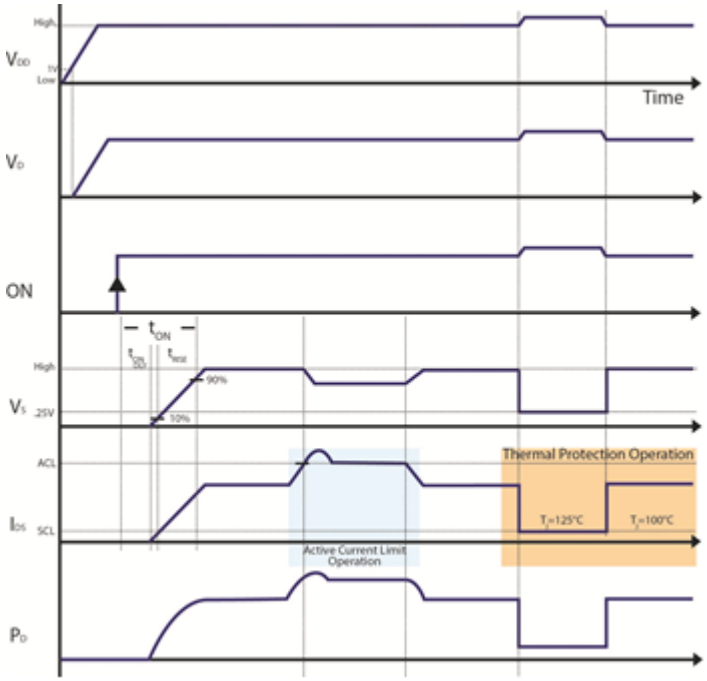

Figure 7: Active Current Limit and Thermal Protection Operation

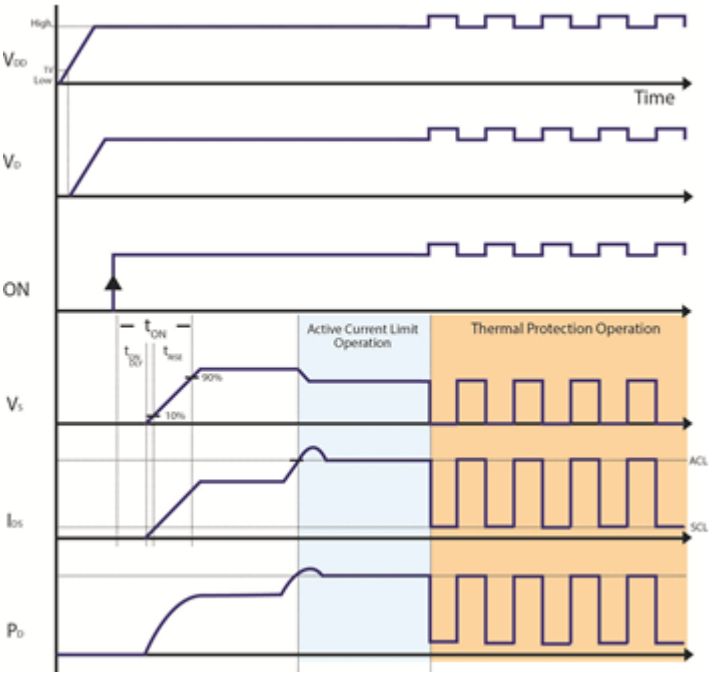

Figure 8: Active Current Limit and Thermal Protection Operation

2.5 Short-Circuit Current Limit

Short circuit current limit protects the device by limiting an excessive amount of current in the event of a short circuit. Short-circuit protection can only be disabled when the overcurrent event has elapsed, allowing V_S to increase above 0.25 V, or the GreenFET Load Switch is turned off by toggling its ON pin. If an output overcurrent event causes the V_S pin voltage below 250 mV, the short circuit protection is actuated. From the scope capture in Figure 6, where V_S is 0V and the ON pin is high,

short circuit current limit is enacted. Depending on the V_{DD} and the GreenFET Load Switch, the current limit will vary from 0.3 A - 1.0 A. The source voltage will need to rise above the 250 mV to disable the short circuit current limiting mode. Short circuit may induce thermal protection in the event that the junction temperature reaches the thermal shutoff turn-on temperature.

3 Reverse Current Blocking

3.1 Using Back-to-Back FETs

One form of reverse current blocking is known as back-to-back FET reverse blocking. A schematic that illustrates this reverse current blocking scheme is shown in Figure 9. Figure 9 shows a pulse wave acting as the gate driver for the two N-channel MOSFET in an opposing cascade arrangement with the source terminals tied together. When the pulse is high, turning on both FETs, current will flow from in to out and will not flow through the P-N junction diodes because the forward voltage is not sufficient enough to turn on BD1 or avalanche BD2. Using the SLG59M610 as an example, RDS(ON) is 22 mΩ. At an I_{DS} of 4 A, the result is a 88 mV drop across the FET. When the gate driver is held low, the two body diodes of the MOSFETs act as reverse blocking components.

The dotted lines labeled in red, illustrating that the current flows when the input or output is greater in voltage potential, are blocked by the diodes of the body in the MOSFET. Since the MOSFETs operate with relatively low voltage, the MOSFETs' body diode reverse breakdown voltage will not be reached or cause the MOSFET's to reach avalanche.

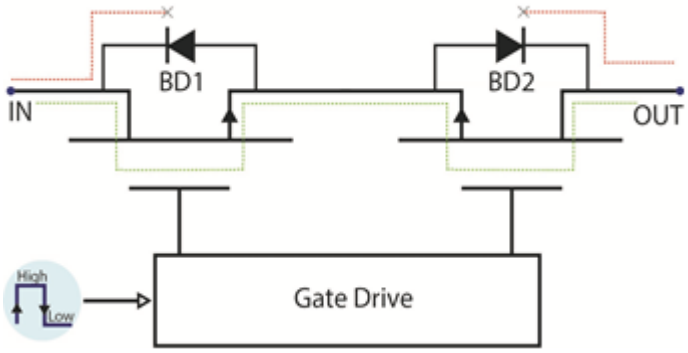

Figure 9: Back-to-Back FET Reverse Blocking

3.2 Using FET Bulk Switching

The more common form of reverse current blocking is known as bulk switching. The reverse voltage detection is implemented across a single MOSFET as shown in Figure 10. The reverse voltage detection, which monitors the drain and source terminals, is active when the ON pin is held low. A closer look of the internal architecture of the FET is illustrated in Figure 11. When the ON pin is high, SW1 switch closes and SW2 opens, thereby connecting the MOSFET's bulk diode to its source terminal. When ON pin is low, the SW1 switch opens and the SW2 switch closes, connecting the body diode's P junction to ground.

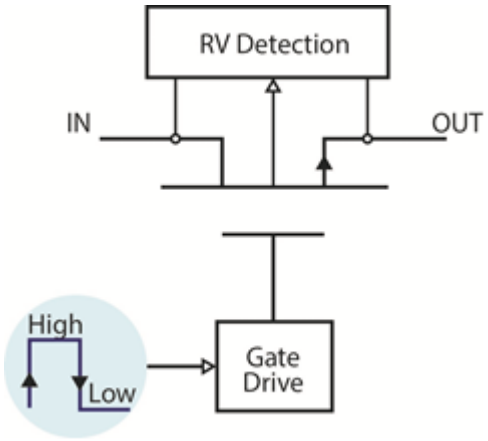

Figure 10: Reverse Voltage Detection

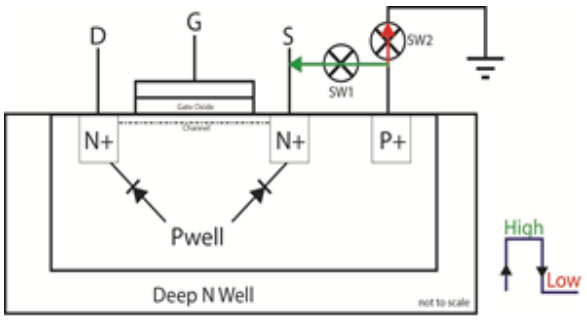

Figure 11: Cross Section of the Bulk Switching FET

3.3 V_{OUT} Slew Rate Control

V_{OUT} slew rate control, or inrush current control, is set by an external capacitor in these GreenFET Load Switches so equipped. The capacitance that is fed through the charge pump, represented in the SLG59M1527 block diagram shown in Figure 12, governs the rate of change from the output in respect to time. The relationship with the slew rate, capacitance value and the output current is given below.

As the capacitance increases, the slew rate decreases and the time which the output transitions low to high is longer.

$$slew\ rate = \frac{dV_{out}}{dt} = \frac{I_{out}}{C}$$

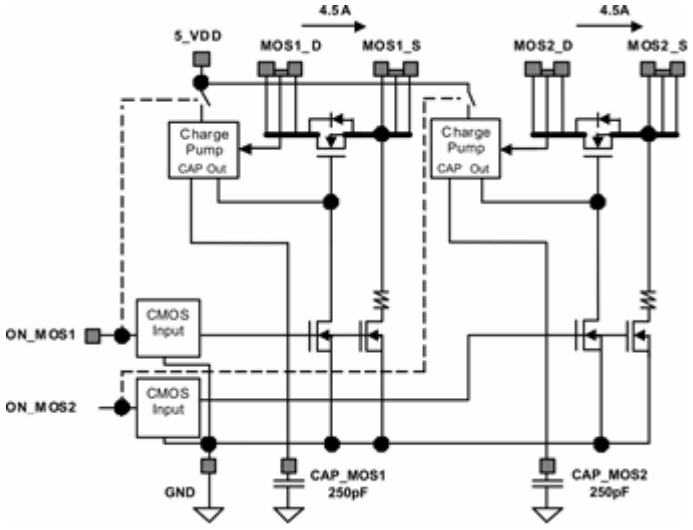

Figure 12: SLG59M1527V Block Diagram

4 Slew Rate Control Sensitivity Analysis

Slew rate control sensitivity analysis is the correlation between the tolerance level of the external components towards the slope of the gate driving signal. The tolerance governs a variation of the slew rate calculated from the nominal value of the capacitor. As noted in Figure 13, the tolerance by the capacitor would yield a slightly different slew rate and may deviate more from the nominal slew rate as the tolerance level increases. Through the charge pump engine, the gate of the FET would be affected. The correspondence of the capacitance and the output may not be 1 to 1 but will indicate a positive relationship.

If the slope increases from the input, the slope for the output would also increase. The I_{CAP} is constant; therefore the main area of controlling the slew rate is the capacitor and its tolerance level.

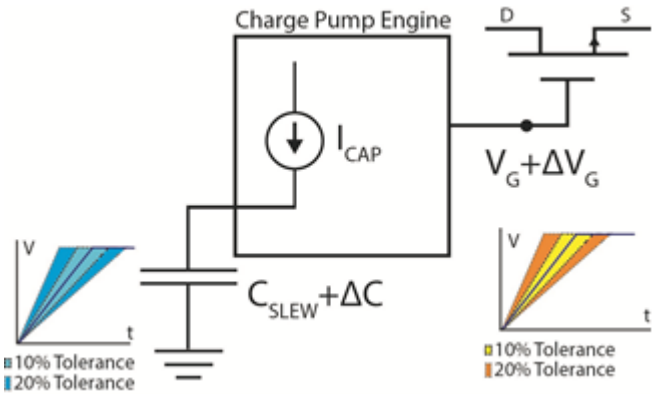

Figure 13: Slew Rate Control Sensitivity Diagram

5 Conclusion

Dialog's GreenFET3 devices are feature-rich switches that include built-in protection circuits. The GreenFET Load Switches' protection circuits such as active current limit operation, thermal protection operation, and short-circuit operation are implemented to protect primarily any circuit downstream in the power path and secondly to protect the Load Switch. Dialog's offers a wide selection of single and dual GreenFET Load Switches, some of which also offer reverse current blocking itself. For more information on GreenFET Load Switches with advanced features, direct your web browser to:

https://www.dialog-semiconductor.com/products/load-switches

Revision History

Revision	Date	Description
1.0	14-Aug-2015	Initial Version

Status Definitions

Status	Definition
DRAFT	The content of this document is under review and subject to formal approval, which may result in modifications or additions.
APPROVED or unmarked	The content of this document has been approved for publication.

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