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RENESAS TECHNICAL UPDATE

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Title	Revised information of S3A7 User's Manual from Rev.1.10		Information Category	Technical Notification		
Applicable Product	Renesas Synergy™ S3 Series S3A7	Lot No. All lots	Reference Document	S3A7 User's Manual: Microcontrollers, Rev.1.10		

1. 39.8.8 ADHSC Bit Rewriting Procedure

[Before]

Before rewriting the A/D conversion select bit (ADCSR.ADHSC) from 0 to 1 or from 1 to 0, the A/D converter must be in the standby state. Carry out steps 1 to 3 in the following section to modify the ADCSR.ADHSC bit. After clearing the sleep bit (ADHVREFCNT.ADSLP) to 0, wait for at least 1 ms and then start A/D conversion.

[After]

Before rewriting the A/D conversion select bit (ADCSR.ADHSC) from 0 to 1 or from 1 to 0, the A/D converter must be in the standby state. Carry out steps 1 to 3 in the following section to modify the ADCSR.ADHSC bit. After clearing the sleep bit (ADHVREFCNT.ADSLP) to 0, wait for at least 1 µs and then start A/D conversion.

2. Table 51.56 A/D internal reference voltage characteristics

[Before]

Conditions: VCC = AVCC0 = VREFH0 = 2.0 to 5.5 V*1

Parameter	Min	Typ	Max	Unit	Test conditions
Internal reference voltage input channel*2	1.36	1.43	1.50	V	-

[After]

Conditions: VCC = AVCC0 = VREFH0 = 2.0 to 5.5 V*1

Parameter	Min	Typ	Max	Unit	Test conditions
Internal reference voltage input channel*2	1.36	1.43	1.50	V	-
Sampling time	5.0	-	-	µs	-

3. 8.2.7 Voltage Monitor 1 Circuit Control Register 0 (LVD1CR0)

[Before]

RN bit (Voltage Monitor 1 Reset Negate Select)

If the RN bit is to be set to 1 (negation follows a stabilization time after assertion of the LVD1 reset signal), set the LOCOCR.LCSTP bit to 0 (the LOCO operates). In addition, if a transition to Software Standby is to be made, the only possible value for the RN bit is 0 (negation follows a stabilization time after VCC > Vdet1 is detected). Do not set the RN bit to 1 (negation follows a stabilization time after assertion of the LVD1 reset signal) when this is the case.

[After]

RN bit (Voltage Monitor 1 Reset Negate Select)

If the RN bit is to be set to 1 (negation follows a stabilization time after assertion of the LVD1 reset signal), set the MOCOCR.MCSTP bit to 0 (the MOCO operates). In addition, if a transition to Software Standby is to be made, the only possible value for the RN bit is 0 (negation follows a stabilization time after VCC > Vdet1 is detected). Do not set the RN bit to 1 (negation follows a stabilization time after assertion of the LVD1 reset signal) when this is the case.

4. 8.2.8 Voltage Monitor 2 Circuit Control Register 0 (LVD2CR0)

[Before]

RN bit (Voltage Monitor 2 Reset Negate Select)

If the RN bit is to be set to 1 (negation follows a stabilization time after the assertion of the LVD2 reset signal), set the LOCOCR.LCSTP bit to 0 (the LOCO operates). Additionally, if a transition to software standby is to be made, the only possible value for the RN bit is 0 (negation follows a stabilization time after VCC > Vdet2 is detected). Do not set the RN bit to 1 (negation follows a stabilization time after the assertion of the LVD2 reset signal) when this is the case.

[After]

RN bit (Voltage Monitor 2 Reset Negate Select)

If the RN bit is to be set to 1 (negation follows a stabilization time after the assertion of the LVD2 reset signal), set the MOCOCR.MCSTP bit to 0 (the MOCO operates). Additionally, if a transition to software standby is to be made, the only possible value for the RN bit is 0 (negation follows a stabilization time after VCC > Vdet2 is detected). Do not set the RN bit to 1 (negation follows a stabilization time after the assertion of the LVD2 reset signal) when this is the case.

5. Table 51.38 SCI timing (2) (1 of 2)

[Before]

Parameter				Symbol	Min	Max	Unit	Test conditions
Simple SPI	Data rise and fall time	Master		t_{Dr}, t_{Df}	-	20	ns	Figure 51.52 to Figure 51.55
		Slave	1.8 V or above		-	20		
			1.6 V or above		-	30		

[After]

Parameter				Symbol	Min	Max	Unit	Test conditions
Simple SPI	Data rise and fall time	Master	1.8 V or above	t_{Dr}, t_{Df}	-	20	ns	Figure 51.52 to Figure 51.55
			1.6 V or above		-	30		
		Slave	1.8 V or above		-	20		
			1.6 V or above		-	30		

6. Table 51.40 SPI timing (2 of 2)

[Before]

Parameter			Symbol	Min	Max	Unit	Test conditions
SPI	Slave access time	2.7 V or above	t_{SA}	-	2 x t_{Pcyc} + 50	ns	Figure 51.62 and Figure 51.63 C = 30pF
		2.4 V or above		-	2 x t_{Pcyc} + 60		
		1.8 V or above		-	2 x t_{Pcyc} + 85		
		1.6 V or above		-	2 x t_{Pcyc} + 110		
	Slave output release time	2.7 V or above	t_{REL}	-	2 x t_{Pcyc} + 50		
		2.4 V or above		-	2 x t_{Pcyc} + 60		
		1.8 V or above		-	2 x t_{Pcyc} + 85		
		1.6 V or above		-	2 x t_{Pcyc} + 110		

[After]

Parameter			Symbol	Min	Max	Unit	Test conditions
SPI	Slave access time	2.4 V or above	t_{SA}	-	2 x t_{Pcyc} + 100	ns	Figure 51.62 and Figure 51.63 C = 30pF
		1.8 V or above		-	2 x t_{Pcyc} + 140		
		1.6 V or above		-	2 x t_{Pcyc} + 180		
	Slave output release time	2.4 V or above	t_{REL}	-	2 x t_{Pcyc} + 100		
		1.8 V or above		-	2 x t_{Pcyc} + 140		
		1.6 V or above		-	2 x t_{Pcyc} + 180		

7. 15.3.9 Bus Error Address Register (BUSnERRADD) (n = 1 to 4)

[Before]

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	BERAD[31:16]															
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	BERAD[15:0]															
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

[After]

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	BERAD[31:16]															
Value after reset	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	BERAD[15:0]															
Value after reset	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x

8. 15.3.10 Bus Error Status Register (BUSnERRSTAT) (n = 1 to 4)

[Before]

	b7	b6	b5	b4	b3	b2	b1	b0
	ERRSTAT	-	-	-	-	-	-	ACCSTAT
Value after reset	0	0	0	0	0	0	0	0

[After]

	b7	b6	b5	b4	b3	b2	b1	b0
	ERRSTAT	-	-	-	-	-	-	ACCSTAT
Value after reset	0	0	0	0	0	0	0	x

9. 37.2.12 SD INFO1 Interrupt Mask Register (SD_INFO1_MASK)

[Before]

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	-	-	-	-	-	-	SDD3INM	SDD3RMM	-	-	-	-	-	ACENDM	-	RSPENDM
Value after reset	0	0	0	0	0	0	0	0	0	0	0	1	1	1	0	1

[After]

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	-	-	-	-	-	-	SDD3INM	SDD3RMM	-	-	-	-	-	ACENDM	-	RSPENDM
Value after reset	0	0	0	0	0	0	1	1	0	0	0	1	1	1	0	1

10. 37.2.15 Transfer Data Length Register (SD_SIZE)

[Before]

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	-	-	-	-	-	-	LEN[9:0]									
Value after reset	0	0	0	0	0	0	1	0	0	0	1	0	0	0	0	0

[After]

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
Value after reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	-	-	-	-	-	-	LEN[9:0]									
Value after reset	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0

11. 37.2.21 SDIO Interrupt Flag Register (SDIO_INFO1)

[Before]

Note 1. The flag value does not change even when set to 1. If 0 is written to this flag, it becomes 0.

[After]

Note 1. Only 0 can be written to clear the bit.

12. Table 19.1 ELC specifications

[Before]

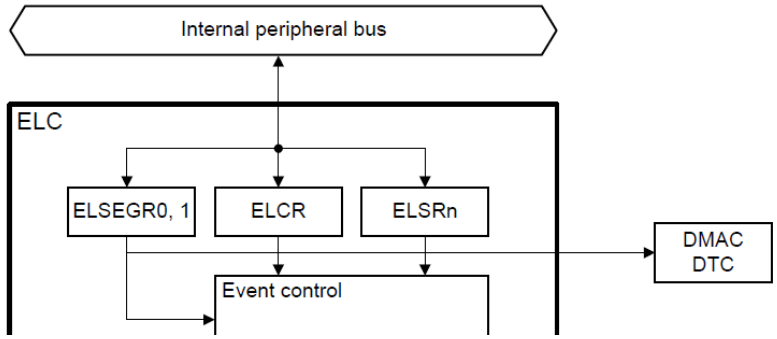
Parameter	Description
Event link function	• 181 types of event signals can be directly connected to modules.The ELC can generate ELC event signal, and events that activate the DMAC and DTC.

[After]

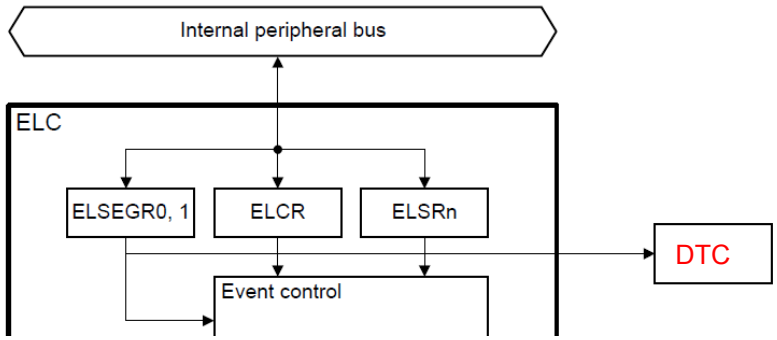
Parameter	Description
Event link function	• 181 types of event signals can be directly connected to modules.The ELC can generate ELC event signal, and events that activate the DTC.

13. Figure 19.1 ELC block diagram (n = 0 to 9, 12 to 18)

[Before]



[After]



14. 19.2.2 Event Link Software Event Generation Register n (ELSEGRn) (n = 0, 1)

[Before]

SEG bit (Software Event Generation)

A software event can trigger a linked DTC and DMAC event.

[After]

SEG bit (Software Event Generation)

A software event can trigger a linked DTC event.

15. Table 19.4 Module operations when event occurs (2 of 2)

[Before]

Module	Operations when event occurs
DMAC/DTC	Starts DMAC data transfer, and starts DTC data transfer

[After]

Module	Operations when event occurs
DTC	Start DTC data transfer

16. Table 51.40 SPI timing (1 of 2)

[Before]

Parameter			Symbol	Min	Max	Unit*1
SPI	RSPCK clock cycle	Master	t_{SPcyc}	2	4096	t_{Pcyc}
		Slave		6	4096	

[After]

Parameter			Symbol	Min	Max	Unit*1
SPI	RSPCK clock cycle	Master	t_{SPcyc}	2*4	4096	t_{Pcyc}
		Slave		6	4096	

Note 4. The upper limit of RSPCK is 16 MHz.

17. Table 51.41 QSPI timing

[Before]

Parameter		Symbol	Min	Max	Unit*1
QSPI	QSPCLK clock cycle	t_{QScyc}	2	48	t_{Pcyc}

[After]

Parameter		Symbol	Min	Max	Unit*1
QSPI	QSPCLK clock cycle	t_{QScyc}	2*4	48	t_{Pcyc}

Note 4. The upper limit of QSPCLK is 16 MHz.