Renesas Synergy™ Platform

S3A1 to S5D5 MCU Group Migration Guide

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Introduction

This Application Note compares hardware peripherals, port select features, and functional differences between the Renesas™ Synergy S3A1 MCU Group and S5D5 MCU Group.

Target Device

Synergy S5D5 MCU Group

Contents

1. About this Document

This document is designed to provide the user with an overview of the functional, hardware, and electrical characteristic differences when migrating from the Synergy S3A1 MCU Group to the S5D5 MCU Group.

2. Audience

This document is intended for users who are designing application systems using the Synergy S5D5 MCU Group devices. Users are expected to have a technical understanding of the peripherals provided in the S3A1 MCU Group. This application note should be used in conjunction with the S5D5 Microcontroller Group User's Manual.

The application note presents two major sections. The first section specifies functional and specification differences between the S3A1 MCU Group and the S5D5 MCU Group, respectively. The second section details the differences in port functionality between the two MCUs.

3. References

Renesas provides the following documents for the Synergy S5 or S3 Series MCUs. Before using any of these documents, visit our web site to obtain the latest versions.

Table 1 Synergy S5 or S3 Series MCU Group Documents

Document Type	Description	Document Title	Document No.
S5D5 MCU Group Datasheet	Overview and electrical characteristics of the MCU	S5D5 Microcontroller Group Datasheet	R01DS0317EU0110
S5D5 MCU Group User's Manual	MCU specifications (pin assignments, memory maps, peripheral functions, electrical characteristics, and timing charts) and operation descriptions	S5D5 Microcontroller Group User's Manual	R01UM0009EU0110
S3A1 MCU Group Datasheet	Overview and electrical characteristics of the MCU	S3A1 Microcontroller Group Datasheet	R01DS0324EU0110
S3A1 MCU Group User's Manual	MCU specifications (pin assignments, memory maps, peripheral functions, electrical characteristics, and timing charts) and operation descriptions	S3A1 Microcontroller Group User's Manual	R01UM0010EU0110
Renesas Synergy Software Package (SSP) User's Manual	API reference and introduction to SSP architecture and programming	Renesas Synergy™ Software Package (SSP) User's Manual	R01US0356EU0103

4. Numbering Notation

The following numbering notation is used throughout this manual.

Table 2 Example of Number Notation

Example	Description
011b	Binary number. For example, the binary equivalent of the number 3 is 011b.
1Fh	Hexadecimal number. For example, the hexadecimal equivalent of the number 31 is described 1Fh. In some cases, a hexadecimal number is shown with the prefix 0x.
1234	Decimal number. A decimal number is followed by this symbol only when the possibility of confusion exists. Decimal numbers are generally shown without a suffix.
Bit 4	Specifies the bit position in field or register.

5. Specification and Hardware Differences

Table 4 compares hardware compatibility and differences between the S3A1 MCU Group and S5D5 MCU Group. The table is ordered with increasing specificity from left to right. The left most column corresponds to a system as noted in the user's manual for the S3A1 MCU Group or S5D5 MCU Group. Values in the S3A1 column represent whether a system, subsystem, or field in register exists/has a certain value. Values in the S5D5 column show the change in hardware, new feature addition, or notes a deprecated feature. The Reference column specifies the section in the S5D5 MCU Group User's Manual that can be referred to for more information.

The following terms describe the functionality of the peripherals mentioned in Table 4.

Table 3 Terms and Functionality of Peripherals

Terms	Description
Exists or Available	The peripheral or function is implemented for the particular MCU Group
Does not exist or Not Available	The peripheral specified has been removed (when compared to the other MCU Group) or does not exist in the MCU Group
Not Applicable	The criteria for comparison is invalid for the MCU Group

Table 4 Specification Difference (1 of 21)

Specification			S3A1	S5D5	S5D5 User's Manual Reference
CPU	Embedded Trace Buffer (ETB)	Buffer Size	1 KB	2 KB	2.1.2
	Maximum Operating Frequency	CPU Core	48 MHz	120 MHz	2.1.3
		4-Bit TPIU Trace Interface	Does Not Exist	60 MHz	2.1.3, 2.3
		SWO Trace Interface	12.5 MHz	60 MHz	2.1.3
		JTAG Interface	12.5 MHz	25 MHz	
		SWD Interface	12.5 MHz	25 MHz	
	CoreSight ROM Table Component at Specific Address	E00F F000h	SCS	NVIC	2.6.3.1
		E00F F004h	DWT	SWT	
	CoreSight Component Register	Initial Value of PID0	0000001Dh	00000015h	2.6.3.2
	Changing a Low power Mode While in OCD Mode	Mode Restriction in Deep Software Standby	Does Not Exist	Applicable	2.11.3.2
Address Space	MCU Supports a 4-GB Linear Address Space Ranging from 0000 0000h to FFFF FFFFh that can Contain Both Program and Data		Refer to Manual	Refer to Manual	Chapter 4
Resets	VBATT-Selected Voltage Power-On Reset		Exists	Does Not Exist	-
	Deep Software Standby Reset		Does Not Exist	Exists	6.1
	Module-Related Registers Initialized by Each Reset Source		Refer to Manual	Refer to Manual	Table 6.3
	States of SOSC and LOCO when a Reset Occurs		Refer to Manual	Refer to Manual	Table 6.4, Table 6.5
	Reset Status Register 0 (RSTSR0)	Bit [7]	Reserved	Deep Software Standby Reset Flag (DPSRSTF)	6.2.1
	Determination of Reset Generation Source		Refer to Manual	Refer to Manual	6.3.9, Figure 6.4

Table 4 Specification Difference (2 of 21)

Specification			S3A1	S5D5	S5D5 User's Manual Reference
Option-Setting Memory	Access Window Setting Control Register (AWSC)		Refer to Manual	Does Not Exist	7.1, 7.2
	Configuration Setting Area	OCD/Serial Programmer ID Setting Register (OSIS)	0101 0018h to 0101 0033h	0100 A150h to 0100 A15Ch	7.1
		Access Window Setting Register (AWS)	0101 0010h to 0101 0013h	0100 A164h to 0100 A167h	
	Option Function Select Register 1 (OFS1)	Bits [1:0]	Reserved	VDSEL0[1:0]	7.2.2
		Bits [5:3]	VDSEL1[2:0]	Reserved	
		Bits [10:9]	Reserved	HOCOFRQ0[1:0]	
		Bits [14:12]	HOCOFRQ1[2:0]	Reserved	
	MPU Registers		Refer to Manual	Does Not Exist	-
	Access Window Setting Register (AWS)	Start Block Address (FAWS)	Spans From Bits [11:0]	Spans from Bits [10:0] (Bit [11] is Reserved)	7.2.3
		Bit [15]	Reserved	Protection of Access Window and Startup Area Select Function (FSPR)	
		End Block Address (FAWE)	Spans From Bits [27:16]	Spans from Bits [26:16] (Bit [27] is Reserved)	
		Bit [31]	Reserved	Startup Area Select Flag (BTFLG)	

Table 4 Specification Difference (3 of 21)

Specification			S3A1	S5D5	S5D5 User's Manual Reference
Low Voltage Detection (LVD)	Digital Filter		Does Not Exist	Refer to Manual	Table 8.1
	Voltage Monitor Circuit Control Register (LVCMPCR)	Deep Software Standby Mode	Not Applicable	When Using Voltage Detection, Do Not Set the DPSBYCR.DEEPCUT [1:0] bits to 11b	8.2.5
	Voltage Detection Level Select Register (LVDLVLR)		Refer to Manual	Refer to Manual	8.2.6
	Voltage Monitor n Circuit Control Register 0 (n= 1, 2) (LVD1CR0 and LVD2CR0)	Bit [1]	Reserved Value after Reset is 0	Digital Filter Disable Mode Select (DFDIS) Value after Reset is 1	8.2.7, 8.2.8
		Bits [5:4]	Reserved	Sampling Clock Reset FSAMP[1:0]	
	VCC Input Voltage Monitor	Procedure to Set Up Monitoring Against Vdet1 and Vdet2	Refer to Manual	Refer to Manual	Table 8.2, Table 8.3
	Interrupt and Reset from Voltage Monitor 1 and 2		Refer to Manual	Refer to Manual	8.5, 8.6
	Interrupt Handling and Event Linking	Deep Software Standby Mode	Not Applicable	For Vdet1 and Vdet2 passage events, event signals are not generated for the ELC	8.7.1

Table 4 Specification Difference (4 of 21)

Specification			S3A1	S5D5	S5D5 User's Manual Reference
Clock Generation Circuit	Main Clock Oscillator (MOSC)	Resonator Frequency	1 MHz to 20 MHz (Up to 5.5 V) 1 MHz to 8 MHz (Up to 2.4 V)	8 to 24 MHz 8, 10, 12, 15, 16, 20, 24 MHz (USB Boot Mode)	Table 9.1, Figure 9.1
		External Clock Input Frequency	Up to 20 MHz	Up to 24 MHz	
	PLL circuit	Input Clock Source	MOSC	MOSC, HOCO	
		Input Frequency	4 MHz to 12.5 MHz	8 MHz to 24 MHz	
		Input Pulse Frequency Division Ratio	Not Applicable	Selectable from 1, 2 and 3	
		Frequency Multiplication Ratio	Selectable from 8 to 31 (1 step) (multiplication frequency is up to 64 MHz)	Selectable from 10 to 30 (0.5 step)	
		Output Pulse Frequency Division Ratio	Selectable from 2, and 4	Not Applicable	
		PLL Output Frequency	24 MHz to 64 MHz (division ratio: 2) 24 MHz to 32 MHz (division ratio: 4)	120 to 240 MHz	
	High-Speed On-Chip Oscillator (HOCO)	Oscillation Frequency	24, 32, 48, 64 MHz	16, 18, 20 MHz	
	Clock Generation Circuit Specifications for the Internal Clocks		Refer to Manual	Refer to Manual	Table 9.2
	Clock Generation Circuit Input/Output Pins	SDRAM Clock (SDCLK)	Does Not Exist	Exists	Table 9.3
	Registers		Refer to Manual	Refer to Manual	9.2
	External Clock Input	XTAL Pin	XTAL Can't Use Any Functions and Cannot be Set by User.	Set in PFS.P213PFS.	9.3.2

Table 4 Specification Difference (5 of 21)

Specification			S3A1	S5D5	S5D5 User's Manual Reference
Clock Generation Circuit (Continued)	Handling of Pins When the Sub-Clock Oscillator Is Not Used		Not Applicable	Refer to Manual	9.4.2
	Oscillation Stop Detection		Detected with SCKSCR.CKSEL[2:0] = 101b	Detected with PLLCCR.PLSRCSEL = 0, SCKSCR.CKSEL[2:0] = 101b	9.5.1
	Internal Clock Sources	Clock the External Bus Controller and External Pin Output for the SDRAM	Not Applicable	SDCLK	9.7, 9.7.5
		Source Clock for the SLCDC	LCDSRCCLK LCD Source Clock	Not Applicable	9.7, 9.7.12
	Specify the Frequency	ICLK, PCLKA, PCLKB, PCLKC, PCLKD, FCLK, BCLK, UCLK	PLLMUL[4:0] and PLODIV[1:0] in PLLCCR2	PLLMUL[5:0] and PLIDIV[1:0] in PLLCCR	9.7.1, 9.7.2, 9.7.3, 9.7.4, 9.7.6
		ICLK, PCLKA, PCLKB, PCLKC, PCLKD, FCLK, BCLK, UCLK, CLKOUT	HOCOFRQ1[2:0] in OFS1	HOCOFRQ[1:0] in OFS1	9.7.1, 9.7.2, 9.7.3, 9.7.4, 9.7.6, 9.7.13
	Usage Notes	Sub-Clock Oscillator for LGA Packages	Not Applicable	Refer to Manual	9.8.5
		Main Clock Oscillator Drive Capability Auto Switching Function	Not Applicable	Refer to Manual	9.8.6
Low Power Modes	Provides Several Functions for Reducing Power Consumption		Excludes Deep Software Standby Mode, Includes Middle-Speed Mode and Low-Voltage Mode, Refer to Manual for Additional Details	Includes Deep Software Standby Mode, Excludes Middle-Speed Mode and Low-Voltage Mode, Refer to Manual for Additional Details	Chapter 11

Table 4 Specification Difference (6 of 21)

Specification			S3A1	S5D5	S5D5 User's Manual Reference
Battery Backup Function	Provides a Battery Backup Function that Maintains Partial Battery Powering in the Event of Power Loss		Includes the RTC, AGT, SOSC, LOCO, Wakeup Control, Backup Memory, VBATT_R Low Voltage Detection and Switch Between VCC and VBATT. Refer to Manual for Additional Details	Includes the RTC, SOSC, Backup Memory, and Switch Between VCC and VBATT. Refer to Manual for Additional Details	Chapter 12
Register Write Protection	Association Between PRCR bits and Registers to be Protected	PRC0	PLLCCR2, MEMWAIT, SLCDSCKCR, USBCKCR	SCKDIVCR2, PLLCCR, SDCKOCR, FLLCR1, FLLCR2	Table 13.1
		PRC1	FLSTOP, PSMCR, VBTCR1, VBTCR2, VBTSR, VBTCMPCR, VBTLVDICR, VBTWCTLR, VBTWCH0OTSR, VBTWCH1OTSR, VBTWCH2OTSR, VBTOCTLR, VBTWTER, VBTWEGR, VBTWFR	DPSBYCR, DPSIER0-3, DPSIFR0-3, DPSIEGR0-2, STCONR	

Table 4 Specification Difference (7 of 21)

Specification			S3A1	S5D5	S5D5 User's Manual Reference
Interrupt Controller Unit (ICU)	Peripheral Function Interrupts	Number of Sources	209	301	Table 14.1
	Interrupt Sources for NVIC		64	96	
	Non-Maskable Interrupt Status Register (NMISR)	Bit [4]	VBATT Monitor Interrupt Status Flag (VBATTST)	Reserved	14.2.2
	Non-Maskable Interrupt Enable Register (NMIER)	Bit [4]	VBATT monitor Interrupt Enable (VBATTEN)	Reserved	14.2.3
	Non-Maskable Interrupt Status Clear Register (NMICLR)	Bit [4]	VBATT Clear (VBATTCLR)	Reserved	14.2.4
	ICU Event Link Setting Register n (IELSRn)	Bits [8:0]	IELS[7:0] ICU Event Link Select Bit 8 is Reserved	IELS[8:0] ICU Event Link Select	14.2.6
	DMAC Event Link Setting Register n (DELSRn)	Bits [8:0]	DELS[7:0] DMAC Event Link Select Bit 8 is Reserved	DELS[8:0] DMAC Event Link Select	14.2.7
	SYS Event Link Setting Register (SELSR0)	Bits [8:0]	SELS[7:0] SYS Event Link Select Bit 8 is Reserved	SELS[8:0] SYS Event Link Select	14.2.8
	Wake Up Interrupt Enable Register (WUPEN)	Bit [20]	VBATT Monitor Interrupt Software Standby Returns Enable (VBATTWUPEN)	Reserved	14.2.9
		Bit [22]	Reserved	ACMPHS0 Interrupt Software Standby Returns Enable (ACMPHS0WUPEN)	
		Bit [23]	ACMPLP0 Interrupt Software Standby Returns Enable (ACMPLP0WUPEN)	Reserved	
	Interrupt Vector Table		Refer to Manual	Refer to Manual	14.3.1, Table 14.3
	Event Numbers		Refer to Manual	Refer to Manual	14.3.2, Table 14.4
	Non-Maskable Interrupt	VBATT monitor interrupt	Exists	Does Not Exist	14.5

Table 4 Specification Difference (8 of 21)

Specification			S3A1	S5D5	S5D5 User's Manual Reference
Buses	Main Bus	ICode Bus DCode Bus	Connected to Code Flash Memory	Connected to Code Flash Memory and SRAMHS	Table 15.1
		ETHER Bus	Does Not Exist	Exists	
	Slave Interface	Memory Bus 2	Does Not Exist	Exists. Connected to SRAMHS	
		Memory Bus 5	Connected to SRAM1	Connected to Standby SRAM	
		Internal Peripheral Bus 3 SRC, TSN	Not Applicable	Connected to SRC, TSN	
		Internal Peripheral Bus 4 IrDA, ETHERC, EDMAC	Not Applicable	Connected to IrDA, ETHERC, EDMAC	
		Internal Peripheral Bus 5 OPAMP, PDC, ACMPLP, DAC8, SLCDC	Connected to OPAMP, ACMPLP, DAC8, SLCDC	Connected to PDC	
	Addresses Assigned	Memory Bus 5	Refer to Manual	Refer to Manual	Table 15.2
	External Bus	Connected to SDRAM	Not Applicable	Yes	Table 15.1, 15.2.3
		External Address Space	4 CS areas (CS0 to CS3)	8 CS areas (CS0 to CS7) and the SDRAM area Address/Data Multiplexed Bus Available	Table 15.3
	All Other Differences		Refer to Manual	Refer to Manual	Chapter 15
Memory Protection Unit (MPU)	Memory protection	Bus Master MPU	Group A: 16 Regions Refer to Manual for Details	Group A: 32 Regions Group B: 8 Regions Refer to Manual for Details	Table 16.1, 16.4.1
	Bus Slave MPU	Register Description	Refer to Manual	Refer to Manual	16.5
	Security MPU	Register Description	Refer to Manual	Refer to Manual	16.6

Table 4 Specification Difference (9 of 21)

Specification			S3A1	S5D5	S5D5 User's Manual Reference
DMA Controller (DMAC)	Number of Channels		4	8	Table 17.1
	Channel Priority		Channel 0 > 1 > ... > 3 (Channel 0: Highest)	Channel 0 > 1 > ... > 7 (Channel 0: Highest)	
	DMAC Execution Cycles	Read and Write Data Transfer	Based on Block Size, Read Destination Access Cycle and Data Write Destination Access Cycle	Based on Block Size, Read Destination Access Cycle, Data Write Destination Access Cycle and SRAMHS	Table 17.7
Data Transfer Controller (DTC)	DTC Module Start Register (DTCST)	Bit 0 - DTCST Bit Must be Set to 0 before transition to Deep Software Standby Mode	Not Applicable	Applicable	18.2.9, 18.10
	DTC Execution Cycles	Read and Write Data Transfer	Based on Block Size, Read Destination Access Cycle and Data Write Destination Access Cycle	Based on Block Size, Read Destination Access Cycle, Data Write Destination Access Cycle and SRAMHS	18.4.8
Event Link Controller (ELC)	Event Link Function	Number of Event Signals Directly Connected to Modules	179	258	Table 19.1
	Associations Between the ELSRn Register and Peripheral Functions		Refer to Manual	Refer to Manual	19.2.3, Table 19.2

Table 4 Specification Difference (10 of 21)

Specification			S3A1	S5D5	S5D5 User's Manual Reference
I/O Ports	Function and Specification	Total Pins	Up to 126	Up to 110	Table 20.1, Table 20.2
		PORT0	P000 to P015	P000 to P009, P014, P015	
		PORT2	P200 to P206, P212 to P215	P200 to P214	
		PORT3	P300 to P315	P300 to P313	
		PORT5	P500 to P507, P511, P512	P500 to P506, P508, P511, P512	
		PORT6	P600 to P606, P608 to P614	P600 to P605, P608 to P614	
		PORT8	P800 to P809	P800, P801	
		PORT9	P900 to P902, P914, P915	Not Available	
		Other	Refer to Manual for Additional Details	Refer to Manual for Additional Details	
	Port Control Register 1 (PCNTR1/PODR/PDR)	Reserved Bit	Bits 16, 30, 31	Bits 0, 16	20.2.1
	Port Control Register 3 (PCNTR3/PORR/POSR)	Reserved Bit	Bits 0, 14, 15 Bit 16, Bit 30, Bit 31	Bits 0, 16	20.2.3
	Port Control Register 4 (PCNTR4/EORR/EOSR)	Reserved Bit	Bits 0, 14, 15 Bit 16, Bit 30, Bit 31	Bits 0, 16	20.2.4
	Port mn Pin Function Select Register (PmnPFS/PmnPFS_HA/PmnPFS_BY) (m = 0 to 8; n = 00 to 15)		Refer to Manual	Refer to Manual	20.2.5
	Ethernet Control Register (PFENET)		Does Not Exist	Exists	20.2.7
	Handling of Unused Pins		Refer to Manual	Refer to Manual	20.4
	I/O Buffer Specification		Refer to Manual	Refer to Manual	20.5.5

Table 4 Specification Difference (11 of 21)

Specification			S3A1	S5D5	S5D5 User's Manual Reference
Port Output Enable for GPT (POEG)	GPT Output Pins Disabled when they Detect a Dead Time Error		Not Available	Available	Table 22.1
	POEG Group n Setting Register (POEGGn) S3A1: n = A, B S5D5: n = A to D	Bits [13:8]	Reserved	CDRE0 TO CDRE5 ACMP_HS Enable	22.2.1
	Interrupt Sources and Conditions	POEG Group n Interrupt S3A1: n = A, B S5D5: n = A to D	Refer to Manual	Refer to Manual	22.4, Table 22.3
General PWM Timer (GPT)	Functions	GPT16 Channels	6 Channels	Not Available	Table 23.1, Table 23.2, Table 23.3, Figure 23.1, Figure 23.2
		GPT32 Channels	4 Channels	6 Channels	
		GPT32E Channels (GPT32 Enhanced)	Not Available	4 Channels Minimum Resolution 8.3ns	
		GPT32EH Channels (GPT32 Enhanced High Resolution)	Not Available	4 Channels Minimum Resolution 8.3ns, Capable of Adjusting PWM Output Duty Cycle in 260ps Increments	
		Generation of A/D Converter Start Triggers	Not Available	Available with GPT32E and GPT32EH Channels	Table 23.1, Table 23.4, 23.5
		Interrupt Skipping Function	Not Available	Available with GPT32E and GPT32EH Channels	Table 23.2
		General PWM Timer Cycle Setting Double-Buffer Register (GTPDBR)	Not Available	Available with GPT32E and GPT32EH Channels	Table 23.2, Table 23.4, 23.2.23
		External Trigger Input Pin	GTETRGA, GTETRGB	GTETRGA, GTETRGB GTETRGC, GTETRGD	Table 23.2, Table 23.3
		Dead Time Buffer	Not Available	Only Available with GPT32E and GPT32EH Channels	Table 23.2, Table 23.4

Table 4 Specification Difference (12 of 21)

Specification			S3A1	S5D5	S5D5 User's Manual Reference
General PWM Timer (GPT) (Continued)	Register Description		Refer to Manual	Refer to Manual	23.2
	Conditions When PWM Delay Generation Circuit is Used		Not Applicable	Reverse the Setting Order of GTIOC Pin Function and Enable GTIOC Pin Output	23.3.1.2, Figure 23.12
	Buffer Operation		Not Applicable	Refer to Manual	23.3.2
	Automatic Dead Time Setting Function		Refer to Manual	Refer to Manual	23.3.4
	Interrupt Sources		Refer to Manual	Refer to Manual	23.4
	Event Signal Output to the ELC		Refer to Manual	Refer to Manual	23.6.1
	Protection Function		Refer to Manual	Refer to Manual	23.8
	Priority Order of Each Event	GTADTRm (m = A, B) GTDVm (m = U, D)	Not Applicable	Applicable	23.9.5
PWM Delay Generation Circuit	The Circuit Controls the Timing with which Signals on the Two PWM Output Pins for Channel 0/1/2/3 Rise and Fall to an Accuracy of up to 1/32 times the Period of the GPT Clock		Does Not Exist	Exists	Chapter 24
Asynchronous General-Purpose Timer (AGT)	Interrupt/Event Link Function	Recovery from Software Standby Mode Using AGTI, AGTCMAI, AGTCMBI	Available	Not Available	Table 25.1
	I/O pins	AGTIO0, AGTIO1, used as input only when assigned as P402 and P403	Available	Not Available	Table 25.2
		AGTIO used in Deep Software Standby Mode	Not Available	Available	
	AGT Mode Register 1 (AGTMR1)	Set AGTSCLK or AGTLCLK as the Count Source	Running AGT in Software Standby Mode Refer to Manual for Details	Running AGT in Software Standby or Deep Software Standby Mode Refer to Manual for Details	25.2.5

Table 4 Specification Difference (13 of 21)

Specification			S3A1	S5D5	S5D5 User's Manual Reference
Asynchronous General-Purpose Timer (AGT) (Continued)	AGT I/O Control Register (AGTIOC)	Condition when Digital Filter Function cannot be used	Event Counter Mode Operation Performed During Software Standby	Event Counter Mode Operation Performed During Software Standby and Deep Software Standby Modes	25.2.7
		When TIOGT[1:0] = 00b Count Control	Not Available	In Deep Software Standby Mode	
	AGT Pin Select Register (AGTIOSEL)		Refer to Manual	Refer to Manual	25.2.10
Realtime Clock (RTC)	Interrupts	Alarm Interrupt Periodic Interrupt	Returns From Software Standby Mode	Returns From Software Standby or Deep Software Standby Mode	Table 26.1
	Alarm Function	Condition in Deep Software Standby Mode	Not Applicable	The MCU Returns from the Deep Software Standby Mode even when the Alarm Interrupt Request is Disabled	26.3.6
Watchdog Timer (WDT)	ICU Event Link Setting Register n (IELSRn) Setting		Setting 25h to the IELSRn.IELS[7:0] bits is Prohibited when Enabling the WDT Reset Assertion (OFS0.WDTRSTIRQS = 0 or WDTRCR.RSTIRQS = 0)	Setting 47h to the IELSRn.IELS[8:0] bits is Prohibited when Enabling the WDT Reset Assertion (OFS0.WDTRSTIRQS = 1 or WDTRCR.RSTIRQS = 1)	27.5.1
Ethernet MAC Controller (ETHERC)	MCU Provides a One-Channel ETHERC Compliant with the Ethernet or IEEE802.3 Media Access Control (MAC) Layer Protocol.		Does Not Exist	Exists	Chapter 29
Ethernet DMA Controller (EDMAC)	MCU Provides One Channel for the EDMAC. EDMAC Controls Data Transmission and Reception for ETHERC.		Does Not Exist	Exists	Chapter 30

Table 4 Specification Difference (14 of 21)

Specification			S3A1	S5D5	S5D5 User's Manual Reference
USB 2.0 Full-Speed Module (USBFS)	MCU Supports Revision 1.2 of the Battery Charging Specification		Available	Not Available	-
	Internal USB Transceiver Powered by USB LDO Regulator		Applicable	Not Applicable	-
	Device Controller Features	Low Speed Transfer	Available at 1.5 Mbps	Not Available	-
	Function	HOCO Clock Can be Used as USB Clock	Available	Not Available	-
	Feature	USB LDO Regulator, VCC_USB_LDO BC Control	Available	Not Available	-
	System Configuration Control Register (SYSCFG)	Bit [3]	D-Line Resistor Control (DMRPU)	Reserved	31.2.1
		Bit [8]	Single-ended Receiver Enable (CNEN)	Reserved	
	System Configuration Status Register 0 (SYSSTS0)	Bit [5]	Reserved	Active Monitor When the Host Controller Is Selected (SOFEA)	31.2.2
	Interrupt Enable Register 1 (INTENB1)	Bit [0]	PDDETINT0 Detection Interrupt Enable (PDDETINTE0)	Reserved	31.2.8
	Interrupt Status Register 1 (INTSTS1)	Bit [0]	PDDET0 Detection Interrupt Status (PDDETINT0)	Reserved	31.2.14
	Device State Change Register (DVCHGR)		Does Not Exist	Exists	31.2.19
	USB Address Register (USBADDR)		Does Not Exist	Exists	31.2.20
	USB Module Control Register (USBMC)		Exists	Does Not Exist	-
	BC Control Register 0 (USBBCCTRL0)		Exists	Does Not Exist	-
	PHY Cross Point Adjustment Register (PHYSLEW)		Does Not Exist	Exists	31.2.36
	Deep Software Standby USB Transceiver Control/Pin Monitor Register (DPUSR0R)		Does Not Exist	Exists	31.2.37

Table 4 Specification Difference (15 of 21)

Specification			S3A1	S5D5	S5D5 User's Manual Reference
USB 2.0 Full-Speed Module (USBFS) (Continued)	Deep Software Standby USB Suspend/Resume Interrupt Register (DPUSR1R)		Does Not Exist	Exists	31.2.38
	Operation		Refer to Manual	Refer to Manual	31.3.1
Serial Communications Interface (SCI)	Event Link function	SCIn_ERI, SCIn_RXI, SCIn_TXI, SCIn_TEI, SCIn_AM	n = 0 to 9	n = 0 to 4, 9	Table 32.1
	I/O Pins		Refer to Manual	Refer to Manual	Table 32.2
IrDA Interface	Sends and receives IrDA data communication waveforms in cooperation with the SCI1 based on the IrDA (Infrared Data Association)		Does Not Exist	Exists	Chapter 33
I2C Bus Interface (IIC)	Transfer Rate		400 kbps	1 Mbps	Table 34.1
	I2C Bus Mode Register 2 (ICMR2)	Data Enable/Acknowledge Enable Time for 1 Mbps Speed	Not Applicable	450 ns	34.2.4
	I2C Bus Function Enable Register (ICFER)	Bit [7]	Reserved	Fast-Mode Plus Enable (FMPE)	34.2.6
	I2C Bus Bit Rate Low-Level Register (ICBRL)	Data Setup Time for 1 Mbps Speed	Not Applicable	50 ns	34.2.15
Controller Area Network (CAN) Module	I/O Pins	CRX1, CTX1	Does Not Exist	Exists	35.1
	Interrupt Generator	CAN1 Reception Complete CAN1 Transmission Complete CAN1 Receive FIFO CAN1 Transmit FIFO CAN1 Error	Does Not Exist Refer to Manual for Details	Exists Refer to Manual for Details	35.1, 35.8
	Settings for the Operating Clock	PCLKA:PCLKB	2:1 Operation Not Guaranteed for Other Settings	No Such Condition	35.9.2

Table 4 Specification Difference (16 of 21)

Specification			S3A1	S5D5	S5D5 User's Manual Reference
Serial Peripheral Interface (SPI)	SPI Sequence Control Register (SPSCR)	SPI1	Not Available	Available	36.2.6
	SPI Sequence Status Register (SPSSR)	SPI1	Not Available	Available	36.2.7
	Data Format	SPI1	128-Bit TX and RX Buffer with up to 4 Frames Transferrable per Round Byte Swap Operating Function Available	32-Bit TX and RX Buffer with only 1 Frame Transferrable per Round	Table 36.1, 36.2.7, 36.2.9
	SPI Data Control Register (SPDCR)	Bit [6]	Reserved	SPI Byte Access Specification (SPBYT)	36.2.9
	SPI Data Control Register 2 (SPDCR2)		Does Not Exist	Exists	36.2.15, Figure 36.1
Quad Serial Peripheral Interface (QSPI)	SPI Bus Reference Cycles	Relationship Among SFMDV[4:0] Bits, Cycle Multiplier, and Serial Clock Frequencies	Refer to Manual	Refer to Manual	Table 37.3
Cyclic Redundancy Check (CRC) Calculator	Snoop Address Register (CRCSAR)	Bits [13:0] CRCSA[13:0]	Refer to Manual	Refer to Manual	38.2.5
Serial Sound Interface Enhanced (SSIE)	Transmit and Receive Audio Data to and from Various Devices that Support Different Audio Data Formats		Refer to Manual	Refer to Manual	Chapter 39
Sampling Rate Converter (SRC)	Used to Convert the Sampling Rate of Data Produced by Various Audio Decoders		Does Not Exist	Refer to Manual	Chapter 40
SD/MMC Host Interface (SDHI)	SD and MMC Shared	Interrupt sources Card access interrupt (SDHI_MMCn_ACCS) SDIO access interrupt (SDHI_MMCn_SDIO) Card detection interrupt (SDHI_MMCn_CARD)	n = 0	n = 0, 1	Table 41.1
	I/O Pins	Channel 1	Does Not Exist	Exists	Table 41.2
Parallel Data Capture Unit (PDC)	Communicates with External I/O Devices		Does Not Exist	Refer to Manual	Chapter 42

Table 4 Specification Difference (17 of 21)

Specification			S3A1	S5D5	S5D5 User's Manual Reference
Boundary Scan	Pins that Cannot be Boundary-Scanned		Power supply pins (VCC, VCL, VSS, VBATT, AVCC0, AVSS0, VCC_USB, and VSS_USB), Clock pins (EXTAL, XTAL, XCIN, and XCOUT), Reset signal (RES), Boundary-scan pins (TCK, TMS, TDI, and TDO), and Mode signal (MD)	Power supply pins (VCC, VCL, VCL0, VSS, VBATT, AVCC0, AVSS0, VCC_USB, and VSS_USB), Analog reference pins (VREFH0, VREFL0, VREFH, VREFL), Clock pins (EXTAL, XTAL, XCIN, and XCOUT), Reset signal (RES), USB-dedicated pins (USB_DP, USB_DM), and Boundary-scan pins (TCK, TMS, TDI, and TDO)	43.4
Secure Cryptographic Engine (SCE)	Provide Security Functions such as Access Management Circuit, Encryption Engine and Random Number Generator		Uses SCE5	Uses SCE7	Chapter 44
	Security Algorithm	Symmetric Algorithm	AES	AES, 3DES, ARC4	
		Asymmetric Algorithm	Not Available	RSA, DSA	
	Additional Features	Hash-Value Generation	GHASH	SHA1, SHA224, SHA256, GHASH	
12-Bit A/D Converter (ADC12)	Provides Successive Approximation A/D Converter		Refer to Manual	Refer to Manual	Chapter 45

Table 4 Specification Difference (18 of 21)

Specification			S3A1	S5D5	S5D5 User's Manual Reference
12-Bit D/A Converter (DAC12)	Output channels		1 Channel	2 Channels	Chapter 46
	D/A Output Amplifier Control Function		Does Not Exist	Exists	Table 46.1, 46.6.5
	D/A Control Register (DACR)	Bit [5]	Reserved	D/A Enable (DAE)	46.2.2
		Bit [7]	Reserved	D/A Output Enable 1 (DAOE1)	
	D/A VREF Control Register (DAVREFCR)		Exists	Does Not Exist	-
	D/A Output Amplifier Control Register (DAAMPCR)		Does Not Exist	Exists	46.2.5
	D/A Amplifier Stabilization Wait Control Register (DAASWCR)		Does Not Exist	Exists	46.2.6
	D/A A/D Synchronous Unit Select Register (DAADUSR)		Does Not Exist	Exists	46.2.7
	Synchronization of DAC12 and ADC12	Need to Set the DAADUSR.AMADSEL1 Bit to 1	DAADUSR Does Not Exist	Yes	46.3.1
	Notes on Using the Internal Reference Voltage as the Reference Voltage		Exists	Does Not Exist	-
	Usage Notes on Event Link Operation	Do Not Use Amplifier Output Function Set DACR.DAE Bit to 0	Not Applicable	Applicable	46.5
Temperature Sensor (TSN)	Used to Determine and Monitor the Die Temperature for Reliable Operation of the Device		Refer to Manual	Refer to Manual	Chapter 47
Operational Amplifier (OPAMP)	Used to Amplify Small Analog Input Voltages and Output the Amplified Voltages		Exists	Does Not Exist	-
High-Speed Analog Comparator (ACMPHS)	Used to Compare a Test Voltage with a Reference Voltage and to Provide a Digital Output Based on the Result of Conversion		Does Not Exist	Exists	Chapter 48
Low Power Analog Comparator (ACMPLP)	Compares a Reference Input Voltage and an Analog Input Voltage		Exists	Does Not Exist	-

Table 4 Specification Difference (19 of 21)

Specification			S3A1	S5D5	S5D5 User's Manual Reference
8-Bit D/A Converter (DAC8)	Provides Successive Approximation A/D Converter		Exists	Does Not Exist	-
Capacitive Touch Sensing Unit (CTSU)	Electrostatic Capacitance Measurement Pins	Channels	27 channels (TS00 to TS13, TS17 to TS22, TS27 to TS31, TS34, TS35)	18 channels (TS00 to TS17)	Chapter 49
SRAM	Capacity	Without ECC	SRAM0: 112 KB SRAM1: 64 KB	SRAM0: 224 KB	Table 47.1
		With ECC	SRAM0: 16 KB	SRAM0: 32 KB	
		SRAMHS	Does Not Exist	128 KB	
	Access		0 Wait	Based on ICLK Frequency Refer to Manual for Details	
	Data Retention		Available	Not Available in Deep Software Standby Mode	
	SRAM Wait State Control Register (SRAMWTSC)		Does Not Exist	Exists	51.2.3
	ECC Protection Register 2 (ECCPRCR2)		Exists	Does Not Exist	-
	Low-Power Functions		Refer to Manual	Refer to Manual	51.3.1
	Access Cycles		Refer to Manual	Refer to Manual	51.3.7
	Wait State Insertion		Does Not Exist	Exists	51.4.3
Standby SRAM	An on-chip SRAM is provided to retain data in Deep Software Standby Mode		Does Not Exist	Exists	Chapter 52

Table 4 Specification Difference (20 of 21)

Specification			S3A1	S5D5	S5D5 User's Manual Reference
Flash Memory	Capacity		Code Flash: 1 MB Data Flash: 8 KB	Code Flash: 1 MB Data Flash: 32 KB	Table 53.1
	Read cycle	Code Flash	32 MHz < ICLK ≤ 48 MHz: Cache hit: 1 cycle Cache miss: 2, 3 cycles ICLK ≤ 32 MHz: Cache hit: 1 cycle Cache miss: 1 cycle	80 MHz < ICLK ≤ 120 MHz: Cache hit: 1 cycle Cache miss: 3 cycles 40 MHz < ICLK ≤ 80 MHz: Cache hit: 1 cycle Cache miss: 2 cycles ICLK ≤ 40 MHz: Cache hit: 1 cycle Cache miss: 1 cycle	
		Data Flash	A Read Operation Takes 6 cycles of FCLK in Bytes (FCLK Frequency is 32 MHz)	A read operation takes 7 cycles of FCLK in words or bytes (FCLK frequency is up to 60 MHz)	
	Value After Erasure	Data Flash	FFh	Undefined	
	Programming/Erasing Method		Handled Through the FCB Commands Specified in the Registers	Handled Through the FACI Commands Specified in the FACI Command Issuing Area (407E 0000h)	
	Units of Programming	Code Flash	64 Bits	128 Bytes	
		Data Flash	8 Bits	4/8/16 Bytes	
	Units of Erasure	Code Flash	2 KB	8/32 KB	
		Data Flash	1 KB	64/128/256 Bytes	
	Background operations (BGOs)	Data Flash Memory can be Read During Code Flash Memory Programming	Not Available	Available	

Table 4 Specification Difference (21 of 21)

Specification			S3A1	S5D5	S5D5 User's Manual Reference
Flash Memory (Continued)	Operation	Set Up Flash Cache and Prepare to Rewrite the Flash Memory	Refer to Manual	Refer to Manual	53.4
	All Other Differences		Refer to Manual	Refer to Manual	Chapter 53
Segment LCD Controller/Driver (SLCDC)	MCU Provides a Controller for LCD Display and Display Pins		Exists	Does Not Exist	-
Internal Voltage Regulator	Does Not Supply Voltage to the Internal Circuits and Memory		I/O, Analog Domain	I/O, Analog, USB, Battery Backup Power Domain	54.1
	LDO Mode Pins Setting Description	VCL Pin	Connect VCL Pin to VSS Through a 4.7-µF Multilayer Ceramic Capacitor. VCL0 Pin Not Available	Connect Each Pin to VSS Through a 0.1-µF Multilayer Ceramic Capacitor	Table 54.1
Electrical Characteristics			Refer to Manual	Refer to Manual	Chapter 55

6. Port Select Function Difference

Table 7 and Table 8 compare the PSEL, ASEL, and ISEL functions for the S3A1 MCU Group and S5D5 MCU Group respectively. For each port number, the first row specifies the bitwise select values. The second row specifies the functionality enabled by the select values on the S3A1 MCU Group. The third column specifies the functionality enabled by the select values on the S5D5. Differences in functionality are notated with bold text and highlighted background. The comments section provides additional details or specifies the migration type from S3A1 MCU Group to S5D5 MCU Group. For more information on the comments column please refer to the Typography Notation table after the contents page in the How to use this Application Note section.

Note: Some pin names have the added suffix of _A, _B, _C, _D, _E and _F. When assigning the GPT, IIC, SPI, SSIE, ETHERC (RMII), SDHI, and GLCDC functionality, select the functional pins with the same suffix. The other pins can be selected regardless of the suffix. Assigning the same function to two or more pins simultaneously is prohibited.

The following typographic notation is used for the pin differences sections of the document to denote the changes happening at the individual ports.

Table 5 Typographic Notation Used in Pin Difference Tables

Example	Description
▲PIXD0_B	The '▲' denotes that signal PIXD0_B is being added to the previously unused/reserved or replacing a deprecated function.
▼ET1_TX_CLK	The '▼' denotes that signal ET1_TX_CLK is being deprecated at the bit position and being replaced by a new signal or remain unused/reserved.

The following gradients visualize whether signals are added, replaced, or removed from the S3A1 and S5D5 MCU Group.

Table 6 Visualization of Gradients to Indicate Added, Replaced, and Removed Signals

Example	Description
	Highlights a bit position where a new function is being added to the previously unused/reserved bit position or highlights a port function with a new pin assignment.
	Highlights a bit position where a new function is replacing an existing function in the bit position.
	Highlights a bit position it is being reserved by deprecating the function that existed at that bit position.

Appendix 1. 100 Pin Package

Table 7 100 Pin Package Difference (1 of 16)

Port	MCU	Select								Comments
P000		PSEL 01100b	ASEL ADC	ASEL CMP	ASEL OPAMP	ISEL				▲IVCMP2 ▲IRQ6-DS ▼TS21 ▼AMP0+ ▼IRQ6
	S3A1	TS21	AN000	-	AMP0+	IRQ6				
	S5D5	-	AN000	IVCMP2	-	IRQ6-DS				
P001		PSEL 01100b	ASEL ADC	ASEL CMP	ASEL OPAMP	ISEL				▲IVCMP2 ▲IRQ7-DS ▼TS22 ▼AMP0- ▼IRQ7
	S3A1	TS22	AN001	-	AMP0-	IRQ7				
	S5D5	-	AN001	IVCMP2	-	IRQ7-DS				
P002		ASEL ADC	ASEL CMP	ASEL OPAMP	ISEL					▲IVCMP2 ▲IRQ8-DS ▼AMP0O ▼IRQ2
	S3A1	AN002	-	AMP0O	IRQ2					
	S5D5	AN002	IVCMP2	-	IRQ8-DS					
P003		ASEL ADC	ASEL OPAMP							▲AN007 ▼AN003 ▼AMP1O
	S3A1	AN003	AMP1O							
	S5D5	AN007	-							
P004		ASEL ADC	ASEL CMP	ASEL OPAMP	ISEL					▲AN100 ▲IVCMP2 ▲IRQ9-DS ▼AN004 ▼AMP2O ▼IRQ3
	S3A1	AN004	-	AMP2O	IRQ3					
	S5D5	AN100	IVCMP2	-	IRQ9-DS					
P005		ASEL ADC	ASEL CMP	ASEL OPAMP	ISEL					▲AN101 ▲IVCMP2 ▲IRQ10-DS ▼AN011 ▼AMP3+ ▼IRQ10
	S3A1	AN011	-	AMP3+	IRQ10					
	S5D5	AN101	IVCMP2	-	IRQ10-DS					
P006		ASEL ADC	ASEL CMP	ASEL OPAMP	ISEL					▲AN102 ▲IVCMP2 ▲IRQ11-DS ▼AN012 ▼AMP3- ▼IRQ11
	S3A1	AN012	-	AMP3-	IRQ11					
	S5D5	AN102	IVCMP2	-	IRQ11-DS					
P007		ASEL ADC	ASEL OPAMP							▲AN107 ▼AN013 ▼AMP3O
	S3A1	AN013	AMP3O							
	S5D5	AN107	-							

Table 7 100 Pin Package Difference (2 of 16)

Port	MCU	Select								Comments
P008		ASEL ADC	ISEL							▲AN003 ▲IRQ12-DS ▼AN014 ▼IRQ12
	S3A1	AN014	IRQ12							
	S5D5	AN003	IRQ12-DS							
P009		ASEL ADC	ISEL							▼AN015 ▼IRQ13
	S3A1	AN015	IRQ13							
	S5D5	-	-							
P010/ VREFH0		PSEL 01100b	ASEL ADC	ASEL OPAMP	ISEL					P010 is only available on S3A1
	S3A1	TS30	AN005	AMP2-	IRQ14					
	S5D5	-	-	-	-					
P011/ VREFL0		PSEL 01100b	ASEL ADC	ASEL OPAMP	ISEL					P011 is only available on S3A1
	S3A1	TS31	AN006	AMP2+	IRQ15					
	S5D5	-	-	-	-					
P012/ VREFH		ASEL ADC	ASEL OPAMP							P012 is only available on S3A1
	S3A1	AN007	AMP1-							
	S5D5	-	-							
P013/ VREFL		ASEL ADC	ASEL OPAMP							P013 is only available on S3A1
	S3A1	AN008	AMP1+							
	S5D5	-	-							
P014		ASEL ADC	ASEL CMP	ASEL DA						▲AN005 ▲AN105 ▲IVREF3 ▼AN009
	S3A1	AN009	-	DA0						
	S5D5	AN005/AN105	IVREF3	DA0						
P015		PSEL 01100b	ASEL ADC	ASEL CMP	ASEL DA	ISEL				▲AN006 ▲AN106 ▲IVCMP1 ▲DA1 ▲IRQ13 ▼TS28 ▼AN010 ▼IRQ7
	S3A1	TS28	AN010	-	-	IRQ7				
	S5D5	-	AN006/AN106	IVCMP1	DA1	IRQ13				

Table 7 100 Pin Package Difference (3 of 16)

Port	MCU	Select								Comments
P100		PSEL 00001b	PSEL 00010b	PSEL 00011b	PSEL 00100b	PSEL 00101b	PSEL 00110b	PSEL 00111b	PSEL 01000b	▲DQ00 ▼VL1 ▼AN022 ▼CMPIN0
	S3A1	AGTIO0	GTETRGA	GTIOC5B	RXD0	SCK1	MISOA	SCL1	KR00	
	S5D5	AGTIO0	GTETRGA	GTIOC5B	RXD0	SCK1	MISOA	SCL1	KR00	
		PSEL 01011b	PSEL 01101b	ASEL ADC	ASEL CMP	ISEL				
	S3A1	D00	VL1	AN022	CMPIN0	IRQ2				
	S5D5	D00/DQ00	-	-	-	IRQ2				
P101		PSEL 00001b	PSEL 00010b	PSEL 00011b	PSEL 00100b	PSEL 00101b	PSEL 00110b	PSEL 00111b	PSEL 01000b	▲DQ01 ▼VL2 ▼AN021 ▼CMPREF0
	S3A1	AGTEE0	GTETRGB	GTIOC5A	TXD0	CTS1	MOSIA	SDA1	KR01	
	S5D5	AGTEE0	GTETRGB	GTIOC5A	TXD0	CTS1	MOSIA	SDA1	KR01	
		PSEL 01011b	PSEL 01101b	ASEL ADC	ASEL CMP	ISEL				
	S3A1	D01	VL2	AN021	CMPREF0	IRQ1				
	S5D5	D01/DQ01	-	-	-	IRQ1				
P102		PSEL 00001b	PSEL 00010b	PSEL 00011b	PSEL 00100b	PSEL 00101b	PSEL 00110b	PSEL 01000b	PSEL 01010b	▲DQ02 ▼TXD2 ▼VL3 ▼AN020 ▼CMPIN1
	S3A1	AGTO0	GTOWLO	GTIOC2B	SCK0	TXD2	RSPCKA	KR02	ADTRG0	
	S5D5	AGTO0	GTOWLO	GTIOC2B	SCK0	-	RSPCKA	KR02	ADTRG0	
		PSEL 01011b	PSEL 01101b	PSEL 10000b	ASEL ADC	ASEL CMP				
	S3A1	D02	VL3	CRX0	AN020	CMPIN1				
	S5D5	D02/DQ02	-	CRX0	-	-				
P103		PSEL 00010b	PSEL 00011b	PSEL 00100b	PSEL 00110b	PSEL 01000b	PSEL 01011b	PSEL 01101b	PSEL 10000b	▲DQ03 ▼VL4 ▼AN019 ▼CMPREF1
	S3A1	GTOWUP	GTIOC2A	CTS0	SSLA0	KR03	D03	VL4	CTX0	
	S5D5	GTOWUP	GTIOC2A	CTS0	SSLA0	KR03	D03/DQ03	-	CTX0	
		ASEL ADC	ASEL CMP							
	S3A1	AN019	CMPREF1							
	S5D5	-	-							

Table 7 100 Pin Package Difference (4 of 16)

Port	MCU	Select								Comments
P104		PSEL 00010b	PSEL 00011b	PSEL 00100b	PSEL 00110b	PSEL 01000b	PSEL 01011b	PSEL 01100b	PSEL 01101b	▲RXD8 ▲DQ04 ▼RXD0 ▼TS13 ▼COM0
	S3A1	GTETRGB	GTIOC1B	RXD0	SSLA1	KR04	D04	TS13	COM0	
	S5D5	GTETRGB	GTIOC1B	RXD8	SSLA1	KR04	D04/DQ04	-	-	
		ISEL								
	S3A1	IRQ1								
	S5D5	IRQ1								
P105		PSEL 00010b	PSEL 00011b	PSEL 00100b	PSEL 00110b	PSEL 01000b	PSEL 01011b	PSEL 01100b	PSEL 01101b	▲TXD8 ▲DQ05 ▼TS34 ▼COM1
	S3A1	GTETRGA	GTIOC1A	-	SSLA2	KR05	D05	TS34	COM1	
	S5D5	GTETRGA	GTIOC1A	TXD8	SSLA2	KR05	D05/DQ05	-	-	
		ISEL								
	S3A1	IRQ0								
	S5D5	IRQ0								
P106		PSEL 00001b	PSEL 00011b	PSEL 00100b	PSEL 00110b	PSEL 01000b	PSEL 01011b	PSEL 01101b		▲AGTOB0 ▲SCK8 ▲DQ06 ▼COM2
	S3A1	-	GTIOC8B	-	SSLA3	KR06	D06	COM2		
	S5D5	AGTOB0	GTIOC8B	SCK8	SSLA3	KR06	D06/DQ06	-		
P107		PSEL 00001b	PSEL 00011b	PSEL 00100b	PSEL 01000b	PSEL 01011b	PSEL 01101b			▲AGTOA0 ▲CTS8 ▲DQ07 ▼COM3
	S3A1	-	GTIOC8A	-	KR07	D07	COM3			
	S5D5	AGTOA0	GTIOC8A	CTS8	KR07	D07/DQ07	-			
P108		PSEL 00000b	PSEL 00010b	PSEL 00011b	PSEL 00101b	PSEL 00110b				
	S3A1	TMS/SWDIO	GTOULO	GTIOC0B	CTS9	SSLB0				
	S5D5	TMS/SWDIO	GTOULO	GTIOC0B	CTS9	SSLB0				

Table 7 100 Pin Package Difference (5 of 16)

Port	MCU	Select								Comments
P109		PSEL 00000b	PSEL 00010b	PSEL 00011b	PSEL 00100b	PSEL 00101b	PSEL 00110b	PSEL 01001b	PSEL 01100b	▼SCK1 ▲CTX1 ▼TS10 ▼SEG52 ▼CTX0
	S3A1	TDO/SWO	GTOVUP	GTIOC1A	SCK1	TXD9	MOSIB	CLKOUT	TS10	
	S5D5	TDO/SWO	GTOVUP	GTIOC1A	-	TXD9	MOSIB	CLKOUT	-	
		PSEL 01101b	PSEL 10000b							
	S3A1	SEG52	CTX0							
	S5D5	-	CTX1							
P110		PSEL 00000b	PSEL 00010b	PSEL 00011b	PSEL 00100b	PSEL 00101b	PSEL 00110b	PSEL 01001b	PSEL 01101b	▲CRX1 ▼SEG53 ▼CRX0
	S3A1	TDI	GTOVLO	GTIOC1B	CTS2	RXD9	MISOB	VCOUT	SEG53	
	S5D5	TDI	GTOVLO	GTIOC1B	CTS2	RXD9	MISOB	VCOUT	-	
		PSEL 10000b	ISEL							
	S3A1	CRX0	IRQ3							
	S5D5	CRX1	IRQ3							
P111		PSEL 00011b	PSEL 00100b	PSEL 00101b	PSEL 00110b	PSEL 01011b	PSEL 01100b	PSEL 01101b	ISEL	▼TS12 ▼CAPH
	S3A1	GTIOC3A	SCK2	SCK9	RSPCKB	A05	TS12	CAPH	IRQ4	
	S5D5	GTIOC3A	SCK2	SCK9	RSPCKB	A05	-	-	IRQ4	
P112		PSEL 00011b	PSEL 00100b	PSEL 00101b	PSEL 00110b	PSEL 01011b	PSEL 01100b	PSEL 01101b	PSEL 10010b	▼TSCAP ▼CAPL
	S3A1	GTIOC3B	TXD2	SCK1	SSLB0	A04	TSCAP	CAPL	SSIBCK0	
	S5D5	GTIOC3B	TXD2	SCK1	SSLB0	A04	-	-	SSIBCK0	
P113		PSEL 00011b	PSEL 00100b	PSEL 01011b	PSEL 01100b	PSEL 01101b	PSEL 10010b			▼TS27 ▼SEG00 ▼COM4
	S3A1	GTIOC2A	RXD2	A03	TS27	SEG00/COM4	SSILRCK0/ SSIFS0			
	S5D5	GTIOC2A	RXD2	A03	-	-	SSILRCK0/ SSIFS0			
P114		PSEL 00011b	PSEL 01011b	PSEL 01100b	PSEL 01101b	PSEL 10010b				▼TS29 ▼SEG24
	S3A1	GTIOC2B	A02	TS29	SEG24	SSIRXD0				
	S5D5	GTIOC2B	A02	-	-	SSIRXD0				

Table 7 100 Pin Package Difference (6 of 16)

Port	MCU	Select								Comments
P115		PSEL 00011b	PSEL 01011b	PSEL 01100b	PSEL 01101b	PSEL 10010b				▼TS35 ▼SEG25
	S3A1	GTIOC4A	A01	TS35	SEG25	SSITXD0				
	S5D5	GTIOC4A	A01	-	-	SSITXD0				
P202		PSEL 00011b	PSEL 00100b	PSEL 00101b	PSEL 00110b	PSEL 01011b	PSEL 01101b	PSEL 10101b	ISEL	▼GTIOC5B ▼SCK2 ▼RXD9 ▼MISOB ▼WR1 ▼BC1 ▼SEG21 ▼SD0DAT6 ▼IRQ3
	S3A1	GTIOC5B	SCK2	RXD9	MISOB	WR1/BC1	SEG21	SD0DAT6	IRQ3	
	S5D5	-	-	-	-	-	-	-	-	
P203		PSEL 00011b	PSEL 00100b	PSEL 00101b	PSEL 00110b	PSEL 01011b	PSEL 01100b	PSEL 01101b	PSEL 10101b	▼GTIOC5A ▼CTS2 ▼TXD9 ▼MOSIB ▼A19 ▼TSCAP ▼SEG22 ▼SD0DAT5 ▼IRQ2
	S3A1	GTIOC5A	CTS2	TXD9	MOSIB	A19	TSCAP	SEG22	SD0DAT5	
	S5D5	-	-	-	-	-	-	-	-	
		ISEL								
	S3A1	IRQ2								
	S5D5	-								
P204		PSEL 00001b	PSEL 00010b	PSEL 00011b	PSEL 00100b	PSEL 00101b	PSEL 00110b	PSEL 00111b	PSEL 01010b	▼AGTIO1 ▼GTIW ▼GTIOC4B ▼SCK4 ▼SCK9 ▼RSPCKB ▼SCL0 ▼CACREF ▼A18 ▼TS00 ▼SEG23 ▼USB_OVRCURB ▼SD0DAT4
	S3A1	AGTIO1	GTIW	GTIOC4B	SCK4	SCK9	RSPCKB	SCL0	CACREF	
	S5D5	-	-	-	-	-	-	-	-	
		PSEL 01011b	PSEL 01100b	PSEL 01101b	PSEL 10011b	PSEL 10101b				
	S3A1	A18	TS00	SEG23	USB_OVRCURB	SD0DAT4				
	S5D5	-	-	-	-	-				

Table 7 100 Pin Package Difference (7 of 16)

Port	MCU	Select								Comments
P205		PSEL 00001b	PSEL 00010b	PSEL 00011b	PSEL 00100b	PSEL 00101b	PSEL 00110b	PSEL 00111b	PSEL 01001b	▲SSIWS0 ▲USB_OVRCURB_A-DS ▲ET0_WOL ▲IRQ1-DS ▼SEG20 ▼IRQ1 ▼USB_OVRCURA ▲SSILRCK0
	S3A1	AGTO1	GTIV	GTIOC4A	TXD4	CTS9	SSLB0	SCL1	CLKOUT	
	S5D5	AGTO1	GTIV	GTIOC4A	TXD4	CTS9	SSLB0	SCL1	CLKOUT	
		PSEL 01011b	PSEL 01100b	PSEL 01101b	PSEL 10010b	PSEL 10011b	PSEL 10101b	PSEL 10110b	PSEL 10111b	
	S3A1	A16	TSCAP	SEG20	-	USB_OVRCURA	SD0DAT3	-	-	
	S5D5	A16	TSCAP	-	SSILRCK0	USB_OVRCURA_A-DS	SD0DAT3	ET0_WOL	ET0_WOL	
		ISEL								
	S3A1	IRQ1								
	S5D5	IRQ1-DS								
P206		PSEL 00010b	PSEL 00100b	PSEL 00110b	PSEL 00111b	PSEL 01011b	PSEL 01100b	PSEL 01101b	PSEL 10010b	▲SSIDATA0 ▲ET0_LINKSTA ▲IRQ0-DS ▼SEG12 ▼IRQ0
	S3A1	GTIU	RXD4	SSLB1	SDA1	WAIT	TS01	SEG12	-	
	S5D5	GTIU	RXD4	SSLB1	SDA1	WAIT	TS01	-	SSIDATA0	
		PSEL 10011b	PSEL 10101b	PSEL 10110b	PSEL 10111b	ISEL				
	S3A1	USB_VBUSEN	SD0DAT2	-	-	IRQ0				
	S5D5	USB_VBUSEN	SD0DAT2	ET0_LINKSTA	ET0_LINKSTA	IRQ0-DS				
P207		PSEL 00110b	PSEL 01011b	PSEL 01100b	PSEL 10001b					P207 is only available on S5D5
	S3A1	-	-	-	-					
	S5D5	SSLB2	A17	TS02	QSSL					
P208		PSEL 00010b	PSEL 01011b	PSEL 10001b	PSEL 10101b	PSEL 10110b	PSEL 10111b	PSEL 11010b		P208 is only available on S5D5
	S3A1	-	-	-	-	-	-	-		
	S5D5	GTOVLO	CS4	QIO3	SD0DAT0	ET0_LINKSTA	ET0_LINKSTA	TDATA3		
P209		PSEL 00010b	PSEL 01011b	PSEL 10001b	PSEL 10101b	PSEL 10110b	PSEL 10111b	PSEL 11010b		P209 is only available on S5D5
	S3A1	-	-	-	-	-	-	-		
	S5D5	GTOVUP	CS5	QIO2	SD0WP	ET0_EXOUT	ET0_EXOUT	TDATA2		

Table 7 100 Pin Package Difference (8 of 16)

Port	MCU	Select								Comments
P210		PSEL 00010b	PSEL 01011b	PSEL 10001b	PSEL 10101b	PSEL 10110b	PSEL 10111b	PSEL 11010b		P210 is only available on S5D5
	S3A1	-	-	-	-	-	-	-		
	S5D5	GTIW	CS6	QIO1	SD0CD	ET0_WOL	ET0_WOL	TDATA1		
P211		PSEL 00010b	PSEL 01011b	PSEL 10001b	PSEL 10101b	PSEL 10110b	PSEL 10111b	PSEL 11010b		P211 is only available on S5D5
	S3A1	-	-	-	-	-	-	-		
	S5D5	GTIV	CS7	QIO0	SD0CMD	ET0_MDIO	ET0_MDIO	TDATA0		
P212/ EXTAL		PSEL 00001b	PSEL 00010b	PSEL 00011b	PSEL 00101b	ISEL				▲GTETRGD ▼GTETRGB
	S3A1	AGTEE1	GTETRGB	GTIOC0B	RXD1	IRQ3				
	S5D5	AGTEE1	GTETRGD	GTIOC0B	RXD1	IRQ3				
P213/ XTAL		PSEL 00010b	PSEL 00011b	PSEL 00101b	PSEL 01010b	ISEL				▲GTETRGC ▲ADTRG1 ▼GTETRGA
	S3A1	GTETRGA	GTIOC0A	TXD1	-	IRQ2				
	S5D5	GTETRGC	GTIOC0A	TXD1	ADTRG1	IRQ2				
P214/ XCOUT		PSEL 00010b	PSEL 10001b	PSEL 10101b	PSEL 10110b	PSEL 10111b	PSEL 11010b			▲GTIU ▲QSPCLK ▲SD0CLK ▲ET0_MDC ▲TCLK
	S3A1	-	-	-	-	-	-			
	S5D5	GTIU	QSPCLK	SD0CLK	ET0_MDC	ET0_MDC	TCLK			
P300		PSEL 00000b	PSEL 00010b	PSEL 00011b	PSEL 00110b					▼GTOUUP
	S3A1	TCK/SWCLK	GTOUUP	GTIOC0A	SSLB1					
	S5D5	TCK/SWCLK	-	GTIOC0A	SSLB1					
P301		PSEL 00001b	PSEL 00010b	PSEL 00011b	PSEL 00100b	PSEL 00101b	PSEL 00110b	PSEL 01011b	PSEL 01100b	▼TS09 ▼SEG01 ▼COM5
	S3A1	AGTIO0	GTOULO	GTIOC4B	RXD2	CTS9	SSLB2	A06	TS09	
	S5D5	AGTIO0	GTOULO	GTIOC4B	RXD2	CTS9	SSLB2	A06	-	
		PSEL 01101b	ISEL							
	S3A1	SEG01/COM5	IRQ6							
	S5D5	-	IRQ6							

Table 7 100 Pin Package Difference (9 of 16)

Port	MCU	Select								Comments
P302		PSEL 00010b	PSEL 00011b	PSEL 00100b	PSEL 00110b	PSEL 01011b	PSEL 01100b	PSEL 01101b	ISEL	▼TS08 ▼SEG02 ▼COM6
	S3A1	GTOUUP	GTIOC4A	TXD2	SSLB3	A07	TS08	SEG02/COM6	IRQ5	
	S5D5	GTOUUP	GTIOC4A	TXD2	SSLB3	A07	-	-	IRQ5	
P303		PSEL 00011b	PSEL 01011b	PSEL 01100b	PSEL 01101b	PSEL 10101b				▼TS02 ▼SEG03 ▼COM7 ▼SD0DAT0
	S3A1	GTIOC7B	A08	TS02	SEG03/COM7	SD0DAT0				
	S5D5	GTIOC7B	A08	-	-	-				
P304		PSEL 00010b	PSEL 00011b	PSEL 00100b	PSEL 01011b	PSEL 01100b	PSEL 01101b	PSEL 10101b	ISEL	▲GTOWLO ▲RXD6 ▼TS11 ▼SEG17 ▼SD0WP
	S3A1	-	GTIOC7A	-	A09	TS11	SEG17	SD0WP	IRQ9	
	S5D5	GTOWLO	GTIOC7A	RXD6	A09	-	-	-	IRQ9	
P305		PSEL 00010b	PSEL 00100b	PSEL 01011b	PSEL 01101b	PSEL 10001b	PSEL 10101b	ISEL		▲GTOWUP ▲TXD6 ▼SEG16 ▼SD0CD
	S3A1	-	-	A10	SEG16	QSPCLK	SD0CD	IRQ8		
	S5D5	GTOWUP	TXD6	A10	-	QSPCLK	-	IRQ8		
P306		PSEL 00010b	PSEL 00100b	PSEL 01011b	PSEL 01101b	PSEL 10001b				▲GTOULO ▲SCK6 ▼SEG15
	S3A1	-	-	A11	SEG15	QSSL				
	S5D5	GTOULO	SCK6	A11	-	QSSL				
P307		PSEL 00010b	PSEL 00100b	PSEL 01011b	PSEL 01101b	PSEL 10001b				▲GTOUUP ▲CTS6 ▼SEG14
	S3A1	-	-	A12	SEG14	QIO0				
	S5D5	GTOUUP	CTS6	A12	-	QIO0				
P400		PSEL 00001b	PSEL 00011b	PSEL 00100b	PSEL 00101b	PSEL 00111b	PSEL 01010b	PSEL 01100b	PSEL 01101b	▲SCK7 ▲ADTRG1 ▲ET0_WOL ▼SCK1 ▼CACREF ▼TS20 ▼SEG04
	S3A1	AGTIO1	GTIOC6A	SCK4	SCK1	SCL0	CACREF	TS20	SEG04	
	S5D5	AGTIO1	GTIOC6A	SCK4	SCK7	SCL0	ADTRG1	-	-	
		PSEL 10010b	PSEL 10110b	PSEL 10111b	ISEL					
	S3A1	AUDIO_CLK	-	-	IRQ0					
	S5D5	AUDIO_CLK	ET0_WOL	ET0_WOL	IRQ0					

Table 7 100 Pin Package Difference (10 of 16)

Port	MCU	Select								Comments
P401		PSEL 00010b	PSEL 00011b	PSEL 00100b	PSEL 00101b	PSEL 00111b	PSEL 01100b	PSEL 01101b	PSEL 10000b	▲TXD7 ▲ET0_MDC ▲IRQ5-DS ▼TXD1 ▼TS19 ▼SEG05 ▼IRQ5
	S3A1	GTETRGA	GTIOC6B	CTS4	TXD1	SDA0	TS19	SEG05	CTX0	
	S5D5	GTETRGA	GTIOC6B	CTS4	TXD7	SDA0	-	-	CTX0	
		PSEL 10110b	PSEL 10111b	ISEL						
	S3A1	-	-	IRQ5						
	S5D5	ET0_MDC	ET0_MDC	IRQ5-DS						
P402		PSEL 00001b	PSEL 00101b	PSEL (don't care)	PSEL 01010b	PSEL 01100b	PSEL 01101b	PSEL 10000b	PSEL 10010b	▲RXD7 ▲ET0_MDIO ▲IRQ4-DS ▲CACREF ▲AUDIO_CLK ▲VSYNC ▼TXD1 ▼TS18 ▼SEG06 ▼IRQ4
	S3A1	AGTIO0_E/AGTIO1	RXD1	RTCIC0	-	TS18	SEG06	CRX0	-	
	S5D5	AGTIO0_B/AGTIO1	RXD7	RTCIC0	CACREF	-	-	CRX0	AUDIO_CLK	
		PSEL 10110b	PSEL 10111b	PSEL 11000b	ISEL					
	S3A1	-	-	-	IRQ4					
	S5D5	ET0_MDIO	ET0_MDIO	VSYNC	IRQ4-DS					
P403		PSEL 00001b	PSEL 00011b	PSEL 00101b	PSEL (don't care)	PSEL 01100b	PSEL 10010b	PSEL 10101b	PSEL 10110b	▲CTS7 ▲ET0_LINKSTA ▲SD1DAT7 ▲PIXD7 ▼CTS1 ▼TS17
	S3A1	AGTIO0_F/AGTIO1	GTIOC3A	CTS1	RTCIC1	TS17	SSIBCK0	-	-	
	S5D5	AGTIO0_C/AGTIO1	GTIOC3A	CTS7	RTCIC1	-	SSIBCK0	SD1DAT7	ET0_LINKSTA	
		PSEL 10111b	PSEL 11000b							
	S3A1	-	-							
	S5D5	ET0_LINKSTA	PIXD7							
P404		PSEL 00011b	PSEL (don't care)	PSEL 10010b	PSEL 10101b	PSEL 10110b	PSEL 10111b	PSEL 11000b		▲SD1DAT6 ▲PIXD6 ▲ET0_EXOUT
	S3A1	GTIOC3B	RTCIC2	SSILRCK0/ SSIFS0	-	-	-	-		
	S5D5	GTIOC3B	RTCIC2	SSILRCK0/ SSIFS0	SD1DAT6	ET0_EXOUT	ET0_EXOUT	PIXD6		

Table 7 100 Pin Package Difference (11 of 16)

Port	MCU	Select								Comments
P405		PSEL 00011b	PSEL 10010b	PSEL 10101b	PSEL 10110b	PSEL 10111b	PSEL 11000b			▲SD1DAT5 ▲PIXD5 ▲ET0_TX_EN ▲RMII0_TXD_EN
	S3A1	GTIOC1A	SSITXD0	-	-	-	-			
	S5D5	GTIOC1A	SSITXD0	SD1DAT5	ET0_TX_EN	RMII0_TXD_EN	PIXD5			
P406		PSEL 00011b	PSEL 00110b	PSEL 10010b	PSEL 10101b	PSEL 10110b	PSEL 10111b	PSEL 11000b		▲SSLB3 ▲SD1DAT4 ▲PIXD4 ▲ET0_RX_ER ▲RMII0_TXD1 ▼SSLA3
	S3A1	GTIOC1B	SSLA3	SSIRXD0	-	-	-	-		
	S5D5	GTIOC1B	SSLB3	SSIRXD0	SD1DAT4	ET0_RX_ER	RMII0_TXD1	PIXD4		
P407/ USB_VBUS		PSEL 00001b	PSEL 00100b	PSEL 00110b	PSEL 00110b	PSEL 01001b	PSEL 01010b	PSEL 01100b	PSEL 01101b	▲ET0_EXOUT ▼SEG11
	S3A1	AGTIO0	CTS4	SSLB3	SDA0	RTCOUT	ADTRG0	TS03	SEG11	
	S5D5	AGTIO0	CTS4	SSLB3	SDA0	RTCOUT	ADTRG0	TS03	-	
		PSEL 10011b	PSEL 10110b	PSEL 10111b						
	S3A1	USB_VBUS	-	-						
	S5D5	USB_VBUS	ET0_EXOUT	ET0_EXOUT						
P408		PSEL 00010b	PSEL 00011b	PSEL 00100b	PSEL 00101b	PSEL 00110b	PSEL 01100b	PSEL 01101b	PSEL 10011b	▲GTIOC10B ▲ET0_CRS ▲RMII0_CRS_DV ▲PIXCLK ▼GTIOC5B ▼CTS1 ▼SEG10
	S3A1	GTOWLO	GTIOC5B	CTS1	RXD3	SCL0	TS04	SEG10	USB_ID	
	S5D5	GTOWLO	GTIOC10B	-	RXD3	SCL0	TS04	-	USB_ID	
		PSEL 10110b	PSEL 10111b	PSEL 11000b	ISEL					
	S3A1	-	-	-	IRQ7					
	S5D5	ET0_CRS	RMII0_CRS_DV	PIXCLK	IRQ7					
P409		PSEL 00010b	PSEL 00011b	PSEL 00101b	PSEL 01100b	PSEL 01101b	PSEL 10011b	PSEL 10110b	PSEL 10111b	▲GTIOC10A ▲ET0_RX_CLK ▲RMIIO_RX_ER ▲HSYNC ▼GTIOC5A ▼SEG09
	S3A1	GTOWUP	GTIOC5A	TXD3	TS05	SEG09	USB_EXICEN	-	-	
	S5D5	GTOWUP	GTIOC10A	TXD3	TS05	-	USB_EXICEN	ET0_RX_CLK	RMII0_RX_ER	
		PSEL 11000b	ISEL							
	S3A1	-	IRQ6							
	S5D5	HSYNC	IRQ6							

Table 7 100 Pin Package Difference (12 of 16)

Port	MCU	Select								Comments
P410		PSEL 00001b	PSEL 00010b	PSEL 00011b	PSEL 00100b	PSEL 00101b	PSEL 00110b	PSEL 01100b	PSEL 01101b	▲ET0_ERXD0 ▲RMII0_RXD1 ▲PIXD0 ▼SEG08
	S3A1	AGTOB1	GTOVLO	GTIOC9B	RXD0	SCK3	MISOA	TS06	SEG08	
	S5D5	AGTOB1	GTOVLO	GTIOC9B	RXD0	SCK3	MISOA	TS06	-	
		PSEL 10101b	PSEL 10110b	PSEL 10111b	PSEL 11000b	ISEL				
	S3A1	SD0DAT1	-	-	-	IRQ5				
	S5D5	SD0DAT1	ET0_ERXD0	RMII0_RXD1	PIXD0	IRQ5				
P411		PSEL 00001b	PSEL 00010b	PSEL 00011b	PSEL 00100b	PSEL 00101b	PSEL 00110b	PSEL 01100b	PSEL 01101b	▲ET0_ERXD1 ▲RMII0_RXD0 ▲PIXD1 ▼SEG07
	S3A1	AGTOA1	GTOVUP	GTIOC9A	TXD0	CTS3	MOSIA	TS07	SEG07	
	S5D5	AGTOA1	GTOVUP	GTIOC9A	TXD0	CTS3	MOSIA	TS07	-	
		PSEL 10101b	PSEL 10110b	PSEL 10111b	PSEL 11000b	ISEL				
	S3A1	SD0DAT0	-	-	-	IRQ4				
	S5D5	SD0DAT0	ET0_ERXD1	RMII0_RXD0	PIXD1	IRQ4				
P412		PSEL 00001b	PSEL 00010b	PSEL 00100b	PSEL 00110b	PSEL 01100b	PSEL 10101b	PSEL 10110b	PSEL 10111b	▲AGTEE1 ▲TS08 ▲ET0_ETXD0 ▲REF50CK0 ▲PIXD2
	S3A1	-	GTOULO	SCK0	RSPCKA	-	SD0CMD	-	-	
	S5D5	AGTEE1	GTOULO	SCK0	RSPCKA	TS08	SD0CMD	ET0_ETXD0	REF50CK0	
		PSEL 11000b								
	S3A1	-								
	S5D5	PIXD2								
P413		PSEL 00010b	PSEL 00100b	PSEL 00110b	PSEL 01100b	PSEL 10101b	PSEL 10110b	PSEL 10111b	PSEL 11000b	▲ET0_ETXD1 ▲RMII0_TXD0 ▲PIXD3 ▲TS09
	S3A1	GTOUUP	CTS0	SSLA0	-	SD0CLK	-	-	-	
	S5D5	GTOUUP	CTS0	SSLA0	TS09	SD0CLK	ET0_ETXD1	RMII0_TXD0	PIXD3	
P414		PSEL 00011b	PSEL 00110b	PSEL 01100b	PSEL 10101b	PSEL 10110b	PSEL 10111b	PSEL 11000b	ISEL	▲ET0_RX_ER ▲RMII0_TXD1 ▲PIXD4 ▲TS10
	S3A1	GTIOC0B	SSLA1	-	SD0WP	-	-	-	IRQ9	
	S5D5	GTIOC0B	SSLA1	TS10	SD0WP	ET0_RX_ER	RMII0_TXD1	PIXD4	IRQ9	

Table 7 100 Pin Package Difference (13 of 16)

Port	MCU	Select								Comments
P415		PSEL 00011b	PSEL 00110b	PSEL 01100b	PSEL 10011b	PSEL 10101b	PSEL 10110b	PSEL 10111b	PSEL 11000b	▲ET0_TX_EN ▲RMII0_TXD_EN ▲TS11 ▲PIXD5 ▲USB_VBUSEN
	S3A1	GTIOC0A	SSLA2	-	-	SD0CD	-	-	-	
	S5D5	GTIOC0A	SSLA2	TS11	USB_VBUSEN	SD0CD	ET0_TX_EN	RMII0_TXD_EN	PIXD5	
		ISEL								
	S3A1	IRQ8								
	S5D5	IRQ8								
P500		PSEL 00001b	PSEL 00010b	PSEL 00011b	PSEL 01101b	PSEL 10001b	PSEL 10011b	PSEL 10101b	ASEL ADC	▲GTIOC11A ▲SD1CLK ▲IVREF0 ▼GTIOC2A ▼SEG48 ▼CMPREF1
	S3A1	AGTOA0	GTIU	GTIOC2A	SEG48	QSPCLK	USB_VBUSEN	-	AN016	
	S5D5	AGTOA0	GTIU	GTIOC11A	-	QSPCLK	USB_VBUSEN	SD1CLK	AN016	
		ASEL CMP								
	S3A1	CMPREF1								
	S5D5	IVREF0								
P501		PSEL 00001b	PSEL 00010b	PSEL 00011b	PSEL 00101b	PSEL 01101b	PSEL 10001b	PSEL 10011b	PSEL 10101b	▲GTIOC11B ▲TXD5 ▲SD1CMD ▲AN116 ▲IVREF1 ▼GTIOC2B ▼TXD3 ▼SEG49 ▼AN017 ▼CMPIN1
	S3A1	AGTOB0	GTIV	GTIOC2B	TXD3	SEG49	QSSL	USB_OVRCURA	-	
	S5D5	AGTOB0	GTIV	GTIOC11B	TXD5	-	QSSL	USB_OVRCURA	SD1CMD	
		ASEL ADC	ASEL CMP	ISEL						
	S3A1	AN017	CMPIN1	IRQ11						
	S5D5	AN116	IVREF1	IRQ11						
P502		PSEL 00010b	PSEL 00011b	PSEL 00101b	PSEL 01101b	PSEL 10001b	PSEL 10011b	PSEL 10101b	ASEL ADC	▲GTIOC12A ▲RXD5 ▲SD1DAT0 ▲AN017 ▲IVCMP0 ▼GTIOC3B ▼RXD3 ▼SEG50 ▼AN018 ▼CMPREF0
	S3A1	GTIW	GTIOC3B	RXD3	SEG50	QIO0	USB_OVRCURB	-	AN018	
	S5D5	GTIW	GTIOC12A	RXD5	-	QIO0	USB_OVRCURB	SD1DAT0	AN017	
		ASEL CMP	ISEL							
	S3A1	CMPREF0	IRQ12							
	S5D5	IVCMP0	IRQ12							

Table 7 100 Pin Package Difference (14 of 16)

Port	MCU	Select								Comments
P503		PSEL 00010b	PSEL 00011b	PSEL 00100b	PSEL 00101b	PSEL 01101b	PSEL 10001b	PSEL 10011b	PSEL 10101b	▲GTETRGC ▲GTIOC12B ▲CTS6 ▲SD1DAT1 ▲AN117 ▲SCK5 ▼GTETRGA ▼CTS2 ▼SEG51 ▼AN023 ▼CMPIN0 ▼SCK3
	S3A1	GTETRGA	-	CTS2	SCK3	SEG51	QIO1	USB_EXICEN	-	
	S5D5	GTETRGC	GTIOC12B	CTS6	SCK5	-	QIO1	USB_EXICEN	SD1DAT1	
		ASEL ADC	ASEL CMP							
	S3A1	AN023	CMPIN0							
	S5D5	AN117	-							
P504		PSEL 00010b	PSEL 00011b	PSEL 00100b	PSEL 00101b	PSEL 01011b	PSEL 10001b	PSEL 10011b	PSEL 10101b	▲GTETRGD ▲GTIOC13A ▲SCK6 ▲SD1DAT2 ▲AN018 ▲CTS5 ▼GTETRGB ▼SCK2 ▼AN024 ▼CTS3
	S3A1	GTETRGB	-	SCK2	CTS3	ALE	QIO2	USB_ID	-	
	S5D5	GTETRGD	GTIOC13A	SCK6	CTS5	ALE	QIO2	USB_ID	SD1DAT2	
		ASEL ADC								
	S3A1	AN024								
	S5D5	AN018								
P505		PSEL 00100b	PSEL 10001b	ASEL ADC	ISEL					▼RXD2 ▼QIO3 ▼AN025 ▼IRQ14
	S3A1	RXD2	QIO3	AN025	IRQ14					
	S5D5	-	-	-	-					
P508		PSEL 00100b	PSEL 00101b	PSEL 10101b	ASEL ADC					P508 is only available on S5D5
	S3A1	-	-	-	-					
	S5D5	SCK6	SCK5	SD1DAT3	AN020					
P600		PSEL 00011b	PSEL 00101b	PSEL 01001b	PSEL 01010b	PSEL 01011b	PSEL 01101b	PSEL 10101b		▲CLKOUT ▲CACREF ▼SEG41 ▼SD0DAT7
	S3A1	GTIOC6B	SCK9	-	-	RD	SEG41	SD0DAT7		
	S5D5	GTIOC6B	SCK9	CLKOUT	CACREF	RD	-	-		
P601		PSEL 00011b	PSEL 00101b	PSEL 01011b	PSEL 01101b	PSEL 10101b				▲DQM0 ▼SEG40 ▼SD0DAT6
	S3A1	GTIOC6A	RXD9	WR/WR0	SEG40	SD0DAT6				
	S5D5	GTIOC6A	RXD9	WR/WR0/DQM0	-	-				

Table 7 100 Pin Package Difference (15 of 16)

Port	MCU	Select								Comments
P602		PSEL 00011b	PSEL 00101b	PSEL 01011b	PSEL 01101b	PSEL 10101b				▲SDCLK ▼SEG39 ▼SD0DAT5
	S3A1	GTIOC7B	TXD9	EBCLK	SEG39	SD0DAT5				
	S5D5	GTIOC7B	TXD9	EBCLK/SDCLK	-	-				
P603		PSEL 00011b	PSEL 00101b	PSEL 01011b	PSEL 01101b	PSEL 10101b				▲DQ13 ▼SEG38 ▼SD0DAT4
	S3A1	GTIOC7A	CTS9	D13	SEG38	SD0DAT4				
	S5D5	-	-	-	-	-				
P608		PSEL 00011b	PSEL 01011b	PSEL 01101b	PSEL 10101b					▲DQM1 ▼SEG28 ▼SD0DAT1
	S3A1	GTIOC4B	A00/BC0	SEG28	SD0DAT1					
	S5D5	GTIOC4B	A00/BC0/DQM1	-	-					
P609		PSEL 00011b	PSEL 01011b	PSEL 01101b	PSEL 10000b	PSEL 10101b				▲CKE ▲CTX1 ▼SEG29 ▼SD0DAT2
	S3A1	GTIOC5A	CS1	SEG29	-	SD0DAT2				
	S5D5	GTIOC5A	CS1/CKE	-	CTX1	-				
P610		PSEL 00011b	PSEL 01011b	PSEL 01101b	PSEL 10000b	PSEL 10101b				▲WE ▲CRX1 ▼SEG30 ▼SD0DAT3
	S3A1	GTIOC5B	CS0	SEG30	-	SD0DAT3				
	S5D5	GTIOC5B	CS0/WE	-	CRX1	-				
P708		PSEL 00101b	PSEL 00110b	PSEL 01010b	PSEL 01100b	PSEL 10010b	PSEL 10110b	PSEL 11000b	ISEL	▲CACREF ▲TS12 ▲AUDIO_CLK ▲ET0_ETXD3 ▲PCKO
	S3A1	RXD1	SSLA3	-	-	-	-	-	IRQ11	
	S5D5	RXD1	SSLA3	CACREF	TS12	AUDIO_CLK	ET0_ETXD3	PCKO	IRQ11	
P808		PSEL 01101b	PSEL 10101b							P808 is only available on S3A1
	S3A1	SEG18	SD0CLK							
	S5D5	-	-							
P809		PSEL 01101b	PSEL 10101b							P809 is only available on S3A1
	S3A1	SEG19	SD0CMD							
	S5D5	-	-							

Table 7 100 Pin Package Difference (16 of 16)

Port	MCU	Select								Comments
P914/ USB_DP		PSEL (don't care)								P914 is only available on S3A1
	S3A1	USB_DP								
	S5D5	-								
P915/ USB_DM		PSEL (don't care)								P915 is only available on S3A1
	S3A1	USB_DM								
	S5D5	-								

Appendix 2. 144 Pin Package

Table 8 144 Pin Package Difference (1 of 21)

Port	MCU	Select								Comments
P000		PSEL 01100b	ASEL ADC	ASEL CMP	ASEL OPAMP	ISEL				▲IVCMP2 ▲IRQ6-DS ▼TS21 ▼AMP0+ ▼IRQ6
	S3A1	TS21	AN000	-	AMP0+	IRQ6				
	S5D5	-	AN000	IVCMP2	-	IRQ6-DS				
P001		PSEL 01100b	ASEL ADC	ASEL CMP	ASEL OPAMP	ISEL				▲IVCMP2 ▲IRQ7-DS ▼TS22 ▼AMP0- ▼IRQ7
	S3A1	TS22	AN001	-	AMP0-	IRQ7				
	S5D5	-	AN001	IVCMP2	-	IRQ7-DS				
P002		ASEL ADC	ASEL CMP	ASEL OPAMP	ISEL					▲IVCMP2 ▲IRQ8-DS ▼AMP0O ▼IRQ2
	S3A1	AN002	-	AMP0O	IRQ2					
	S5D5	AN002	IVCMP2	-	IRQ8-DS					
P003		ASEL ADC	ASEL OPAMP							▲AN007 ▼AN003 ▼AMP1O
	S3A1	AN003	AMP1O							
	S5D5	AN007	-							
P004		ASEL ADC	ASEL CMP	ASEL OPAMP	ISEL					▲AN100 ▲IVCMP2 ▲IRQ9-DS ▼AN004 ▼AMP2O ▼IRQ3
	S3A1	AN004	-	AMP2O	IRQ3					
	S5D5	AN100	IVCMP2	-	IRQ9-DS					
P005		ASEL ADC	ASEL CMP	ASEL OPAMP	ISEL					▲AN101 ▲IVCMP2 ▲IRQ10-DS ▼AN011 ▼AMP3+ ▼IRQ10
	S3A1	AN011	-	AMP3+	IRQ10					
	S5D5	AN101	IVCMP2	-	IRQ10-DS					
P006		ASEL ADC	ASEL CMP	ASEL OPAMP	ISEL					▲AN102 ▲IVCMP2 ▲IRQ11-DS ▼AN012 ▼AMP3- ▼IRQ11
	S3A1	AN012	-	AMP3-	IRQ11					
	S5D5	AN102	IVCMP2	-	IRQ11-DS					
P007		ASEL ADC	ASEL OPAMP							▲AN107 ▼AN013 ▼AMP3O
	S3A1	AN013	AMP3O							
	S5D5	AN107	-							

Table 8 144 Pin Package Difference (2 of 21)

Port	MCU	Select								Comments
P008		ASEL ADC	ISEL							▲AN003 ▲IRQ12-DS ▼AN014 ▼IRQ12
	S3A1	AN014	IRQ12							
	S5D5	AN003	IRQ12-DS							
P009		ASEL ADC	ISEL							▲AN004 ▲IRQ13-DS ▼AN015 ▼IRQ13
	S3A1	AN015	IRQ13							
	S5D5	AN004	IRQ13-DS							
P010/ VREFH0		PSEL 01100b	ASEL ADC	ASEL OPAMP	ISEL					P010 is only available on S3A1
	S3A1	TS30	AN005	AMP2-	IRQ14					
	S5D5	-	-	-	-					
P011/ VREFL0		PSEL 01100b	ASEL ADC	ASEL OPAMP	ISEL					P011 is only available on S3A1
	S3A1	TS31	AN006	AMP2+	IRQ15					
	S5D5	-	-	-	-					
P012/ VREFH		ASEL ADC	ASEL OPAMP							P012 is only available on S3A1
	S3A1	AN007	AMP1-							
	S5D5	-	-							
P013/ VREFL		ASEL ADC	ASEL OPAMP							P013 is only available on S3A1
	S3A1	AN008	AMP1+							
	S5D5	-	-							
P014		ASEL ADC	ASEL CMP	ASEL DA						▲AN005 ▲AN105 ▲IVREF3 ▼AN009
	S3A1	AN009	-	DA0						
	S5D5	AN005/AN105	IVREF3	DA0						
P015		PSEL 01100b	ASEL ADC	ASEL CMP	ASEL DA	ISEL				▲AN006 ▲AN106 ▲IVCMP1 ▲DA1 ▲IRQ13 ▼TS28 ▼AN010 ▼IRQ7
	S3A1	TS28	AN010	-	-	IRQ7				
	S5D5	-	AN006/AN106	IVCMP1	DA1	IRQ13				

Table 8 144 Pin Package Difference (3 of 21)

Port	MCU	Select								Comments
P100		PSEL 00001b	PSEL 00010b	PSEL 00011b	PSEL 00100b	PSEL 00101b	PSEL 00110b	PSEL 00111b	PSEL 01000b	▲DQ00 ▼VL1 ▼AN022 ▼CMPIN0
	S3A1	AGTIO0	GTETRGA	GTIOC5B	RXD0	SCK1	MISOA	SCL1	KR00	
	S5D5	AGTIO0	GTETRGA	GTIOC5B	RXD0	SCK1	MISOA	SCL1	KR00	
		PSEL 01011b	PSEL 01101b	ASEL ADC	ASEL CMP	ISEL				
	S3A1	D00	VL1	AN022	CMPIN0	IRQ2				
	S5D5	D00/DQ00	-	-	-	IRQ2				
P101		PSEL 00001b	PSEL 00010b	PSEL 00011b	PSEL 00100b	PSEL 00101b	PSEL 00110b	PSEL 00111b	PSEL 01000b	▲DQ01 ▼VL2 ▼AN021 ▼CMPREF0
	S3A1	AGTEE0	GTETRGB	GTIOC5A	TXD0	CTS1	MOSIA	SDA1	KR01	
	S5D5	AGTEE0	GTETRGB	GTIOC5A	TXD0	CTS1	MOSIA	SDA1	KR01	
		PSEL 01011b	PSEL 01101b	ASEL ADC	ASEL CMP	ISEL				
	S3A1	D01	VL2	AN021	CMPREF0	IRQ1				
	S5D5	D01/DQ01	-	-	-	IRQ1				
P102		PSEL 00001b	PSEL 00010b	PSEL 00011b	PSEL 00100b	PSEL 00101b	PSEL 00110b	PSEL 01000b	PSEL 01010b	▲DQ02 ▼TXD2 ▼VL3 ▼AN020 ▼CMPIN1
	S3A1	AGTO0	GTOWLO	GTIOC2B	SCK0	TXD2	RSPCKA	KR02	ADTRG0	
	S5D5	AGTO0	GTOWLO	GTIOC2B	SCK0	-	RSPCKA	KR02	ADTRG0	
		PSEL 01011b	PSEL 01101b	PSEL 10000b	ASEL ADC	ASEL CMP				
	S3A1	D02	VL3	CRX0	AN020	CMPIN1				
	S5D5	D02/DQ02	-	CRX0	-	-				
P103		PSEL 00010b	PSEL 00011b	PSEL 00100b	PSEL 00110b	PSEL 01000b	PSEL 01011b	PSEL 01101b	PSEL 10000b	▲DQ03 ▼VL4 ▼AN019 ▼CMPREF1
	S3A1	GTOWUP	GTIOC2A	CTS0	SSLA0	KR03	D03	VL4	CTX0	
	S5D5	GTOWUP	GTIOC2A	CTS0	SSLA0	KR03	D03/DQ03	-	CTX0	
		ASEL ADC	ASEL CMP							
	S3A1	AN019	CMPREF1							
	S5D5	-	-							

Table 8 144 Pin Package Difference (4 of 21)

Port	MCU	Select								Comments
P104		PSEL 00010b	PSEL 00011b	PSEL 00100b	PSEL 00110b	PSEL 01000b	PSEL 01011b	PSEL 01100b	PSEL 01101b	▲RXD8 ▲DQ04 ▼RXD0 ▼TS13 ▼COM0
	S3A1	GTETRGB	GTIOC1B	RXD0	SSLA1	KR04	D04	TS13	COM0	
	S5D5	GTETRGB	GTIOC1B	RXD8	SSLA1	KR04	D04/DQ04	-	-	
		ISEL								
	S3A1	IRQ1								
	S5D5	IRQ1								
P105		PSEL 00010b	PSEL 00011b	PSEL 00100b	PSEL 00110b	PSEL 01000b	PSEL 01011b	PSEL 01100b	PSEL 01101b	▲TXD8 ▲DQ05 ▼TS34 ▼COM1
	S3A1	GTETRGA	GTIOC1A	-	SSLA2	KR05	D05	TS34	COM1	
	S5D5	GTETRGA	GTIOC1A	TXD8	SSLA2	KR05	D05/DQ05	-	-	
		ISEL								
	S3A1	IRQ0								
	S5D5	IRQ0								
P106		PSEL 00001b	PSEL 00011b	PSEL 00100b	PSEL 00110b	PSEL 01000b	PSEL 01011b	PSEL 01101b		▲AGTOB0 ▲SCK8 ▲DQ06 ▼COM2
	S3A1	-	GTIOC8B	-	SSLA3	KR06	D06	COM2		
	S5D5	AGTOB0	GTIOC8B	SCK8	SSLA3	KR06	D06/DQ06	-		
P107		PSEL 00001b	PSEL 00011b	PSEL 00100b	PSEL 01000b	PSEL 01011b	PSEL 01101b			▲AGTOA0 ▲CTS8 ▲DQ07 ▼COM3
	S3A1	-	GTIOC8A	-	KR07	D07	COM3			
	S5D5	AGTOA0	GTIOC8A	CTS8	KR07	D07/DQ07	-			
P108		PSEL 00000b	PSEL 00010b	PSEL 00011b	PSEL 00101b	PSEL 00110b				
	S3A1	TMS/SWDIO	GTOULO	GTIOC0B	CTS9	SSLB0				
	S5D5	TMS/SWDIO	GTOULO	GTIOC0B	CTS9	SSLB0				

Table 8 144 Pin Package Difference (5 of 21)

Port	MCU	Select								Comments
P109		PSEL 00000b	PSEL 00010b	PSEL 00011b	PSEL 00100b	PSEL 00101b	PSEL 00110b	PSEL 01001b	PSEL 01100b	▼SCK1 ▲CTX1 ▼TS10 ▼SEG52 ▼CTX0
	S3A1	TDO/SWO	GTOVUP	GTIOC1A	SCK1	TXD9	MOSIB	CLKOUT	TS10	
	S5D5	TDO/SWO	GTOVUP	GTIOC1A	-	TXD9	MOSIB	CLKOUT	-	
		PSEL 01101b	PSEL 10000b							
	S3A1	SEG52	CTX0							
	S5D5	-	CTX1							
P110		PSEL 00000b	PSEL 00010b	PSEL 00011b	PSEL 00100b	PSEL 00101b	PSEL 00110b	PSEL 01001b	PSEL 01101b	▲CRX1 ▼SEG53 ▼CRX0
	S3A1	TDI	GTOVLO	GTIOC1B	CTS2	RXD9	MISOB	VCOUT	SEG53	
	S5D5	TDI	GTOVLO	GTIOC1B	CTS2	RXD9	MISOB	VCOUT	-	
		PSEL 10000b	ISEL							
	S3A1	CRX0	IRQ3							
	S5D5	CRX1	IRQ3							
P111		PSEL 00011b	PSEL 00100b	PSEL 00101b	PSEL 00110b	PSEL 01011b	PSEL 01100b	PSEL 01101b	ISEL	▼TS12 ▼CAPH
	S3A1	GTIOC3A	SCK2	SCK9	RSPCKB	A05	TS12	CAPH	IRQ4	
	S5D5	GTIOC3A	SCK2	SCK9	RSPCKB	A05	-	-	IRQ4	
P112		PSEL 00011b	PSEL 00100b	PSEL 00101b	PSEL 00110b	PSEL 01011b	PSEL 01100b	PSEL 01101b	PSEL 10010b	▼TSCAP ▼CAPL
	S3A1	GTIOC3B	TXD2	SCK1	SSLB0	A04	TSCAP	CAPL	SSIBCK0	
	S5D5	GTIOC3B	TXD2	SCK1	SSLB0	A04	-	-	SSIBCK0	
P113		PSEL 00011b	PSEL 00100b	PSEL 01011b	PSEL 01100b	PSEL 01101b	PSEL 10010b			▼TS27 ▼SEG00 ▼COM4
	S3A1	GTIOC2A	RXD2	A03	TS27	SEG00/COM4	SSILRCK0/ SSIFS0			
	S5D5	GTIOC2A	RXD2	A03	-	-	SSILRCK0/ SSIFS0			

Table 8 144 Pin Package Difference (6 of 21)

Port	MCU	Select								Comments
P114		PSEL 00011b	PSEL 01011b	PSEL 01100b	PSEL 01101b	PSEL 10010b				▼TS29 ▼SEG24
	S3A1	GTIOC2B	A02	TS29	SEG24	SSIRXD0				
	S5D5	GTIOC2B	A02	-	-	SSIRXD0				
P115		PSEL 00011b	PSEL 01011b	PSEL 01100b	PSEL 01101b	PSEL 10010b				▼TS35 ▼SEG25
	S3A1	GTIOC4A	A01	TS35	SEG25	SSITXD0				
	S5D5	GTIOC4A	A01	-	-	SSITXD0				
P202		PSEL 00011b	PSEL 00100b	PSEL 00101b	PSEL 00110b	PSEL 01011b	PSEL 01101b	PSEL 10000b	PSEL 10101b	▲CRX0 ▲ET0_ERXD2 ▲IRQ3-DS ▼SEG21 ▼IRQ3
	S3A1	GTIOC5B	SCK2	RXD9	MISOB	WR1/BC1	SEG21	-	SD0DAT6	
	S5D5	GTIOC5B	SCK2	RXD9	MISOB	WR1/BC1	-	CRX0	SD0DAT6	
		PSEL 10110b	ISEL							
	S3A1	-	IRQ3							
	S5D5	ET0_ERXD2	IRQ3-DS							
P203		PSEL 00011b	PSEL 00100b	PSEL 00101b	PSEL 00110b	PSEL 01011b	PSEL 01100b	PSEL 01101b	PSEL 10000b	▲CTX0 ▲ET0_COL ▲IRQ2-DS ▼SEG22 ▼IRQ2
	S3A1	GTIOC5A	CTS2	TXD9	MOSIB	A19	TSCAP	SEG22	-	
	S5D5	GTIOC5A	CTS2	TXD9	MOSIB	A19	TSCAP	-	CTX0	
		PSEL 10101b	PSEL 10110b	ISEL						
	S3A1	SD0DAT5	-	IRQ2						
	S5D5	SD0DAT5	ET0_COL	IRQ2-DS						
P204		PSEL 00001b	PSEL 00010b	PSEL 00011b	PSEL 00100b	PSEL 00101b	PSEL 00110b	PSEL 00111b	PSEL 01010b	▲SSIBCK0 ▲USB_OVRCURB_A-DS ▲ET0_RX_DV ▼SEG23 ▼USB_OVRCURB
	S3A1	AGTIO1	GTIW	GTIOC4B	SCK4	SCK9	RSPCKB	SCL0	CACREF	
	S5D5	AGTIO1	GTIW	GTIOC4B	SCK4	SCK9	RSPCKB	SCL0	CACREF	
		PSEL 01011b	PSEL 01100b	PSEL 01101b	PSEL 10010b	PSEL 10011b	PSEL 10101b	PSEL 10110b		
	S3A1	A18	TS00	SEG23	-	USB_OVRCURB	SD0DAT4	-		
	S5D5	A18	TS00	-	SSIBCK0	USB_OVRCURB_A-DS	SD0DAT4	ET0_RX_DV		

Table 8 144 Pin Package Difference (7 of 21)

Port	MCU	Select								Comments
P205		PSEL 00001b	PSEL 00010b	PSEL 00011b	PSEL 00100b	PSEL 00101b	PSEL 00110b	PSEL 00111b	PSEL 01001b	▲SSIWS0 ▲USB_OVRCURB_A-DS ▲ET0_WOL ▲IRQ1-DS ▼SEG20 ▼IRQ1 ▼USB_OVRCURA ▲SSILRCK0
	S3A1	AGTO1	GTIV	GTIOC4A	TXD4	CTS9	SSLB0	SCL1	CLKOUT	
	S5D5	AGTO1	GTIV	GTIOC4A	TXD4	CTS9	SSLB0	SCL1	CLKOUT	
		PSEL 01011b	PSEL 01100b	PSEL 01101b	PSEL 10010b	PSEL 10011b	PSEL 10101b	PSEL 10110b	PSEL 10111b	
	S3A1	A16	TSCAP	SEG20	-	USB_OVRCURA	SD0DAT3	-	-	
	S5D5	A16	TSCAP	-	SSILRCK0	USB_OVRCURA_A-DS	SD0DAT3	ET0_WOL	ET0_WOL	
		ISEL								
	S3A1	IRQ1								
	S5D5	IRQ1-DS								
P206		PSEL 00010b	PSEL 00100b	PSEL 00110b	PSEL 00111b	PSEL 01011b	PSEL 01100b	PSEL 01101b	PSEL 10010b	▲SSIDATA0 ▲ET0_LINKSTA ▲IRQ0-DS ▼SEG12 ▼IRQ0
	S3A1	GTIU	RXD4	SSLB1	SDA1	WAIT	TS01	SEG12	-	
	S5D5	GTIU	RXD4	SSLB1	SDA1	WAIT	TS01	-	SSIDATA0	
		PSEL 10011b	PSEL 10101b	PSEL 10110b	PSEL 10111b	ISEL				
	S3A1	USB_VBUSEN	SD0DAT2	-	-	IRQ0				
	S5D5	USB_VBUSEN	SD0DAT2	ET0_LINKSTA	ET0_LINKSTA	IRQ0-DS				
P207		PSEL 00110b	PSEL 01011b	PSEL 01100b	PSEL 10001b					P207 is only available on S5D5
	S3A1	-	-	-	-					
	S5D5	SSLB2	A17	TS02	QSSL					
P208		PSEL 00010b	PSEL 01011b	PSEL 10001b	PSEL 10101b	PSEL 10110b	PSEL 10111b	PSEL 11010b		P208 is only available on S5D5
	S3A1	-	-	-	-	-	-	-		
	S5D5	GTOVLO	CS4	QIO3	SD0DAT0	ET0_LINKSTA	ET0_LINKSTA	TDATA3		
P209		PSEL 00010b	PSEL 01011b	PSEL 10001b	PSEL 10101b	PSEL 10110b	PSEL 10111b	PSEL 11010b		P209 is only available on S5D5
	S3A1	-	-	-	-	-	-	-		
	S5D5	GTOVUP	CS5	QIO2	SD0WP	ET0_EXOUT	ET0_EXOUT	TDATA2		

Table 8 144 Pin Package Difference (8 of 21)

Port	MCU	Select								Comments
P210		PSEL 00010b	PSEL 01011b	PSEL 10001b	PSEL 10101b	PSEL 10110b	PSEL 10111b	PSEL 11010b		P210 is only available on S5D5
	S3A1	-	-	-	-	-	-	-		
	S5D5	GTIW	CS6	QIO1	SD0CD	ET0_WOL	ET0_WOL	TDATA1		
P211		PSEL 00010b	PSEL 01011b	PSEL 10001b	PSEL 10101b	PSEL 10110b	PSEL 10111b	PSEL 11010b		P211 is only available on S5D5
	S3A1	-	-	-	-	-	-	-		
	S5D5	GTIV	CS7	QIO0	SD0CMD	ET0_MDIO	ET0_MDIO	TDATA0		
P212/ EXTAL		PSEL 00001b	PSEL 00010b	PSEL 00011b	PSEL 00101b	ISEL				▲GTETRGD ▼GTETRGB
	S3A1	AGTEE1	GTETRGB	GTIOC0B	RXD1	IRQ3				
	S5D5	AGTEE1	GTETRGD	GTIOC0B	RXD1	IRQ3				
P213/ XTAL		PSEL 00010b	PSEL 00011b	PSEL 00101b	PSEL 01010b	ISEL				▲GTETRGC ▲ADTRG1 ▼GTETRGA
	S3A1	GTETRGA	GTIOC0A	TXD1	-	IRQ2				
	S5D5	GTETRGC	GTIOC0A	TXD1	ADTRG1	IRQ2				
P214/ XCOUT		PSEL 00010b	PSEL 10001b	PSEL 10101b	PSEL 10110b	PSEL 10111b	PSEL 11010b			▲GTIU ▲QSPCLK ▲SD0CLK ▲ET0_MDC ▲TCLK
	S3A1	-	-	-	-	-	-			
	S5D5	GTIU	QSPCLK	SD0CLK	ET0_MDC	ET0_MDC	TCLK			
P300		PSEL 00000b	PSEL 00010b	PSEL 00011b	PSEL 00110b					▼GTOUUP
	S3A1	TCK/SWCLK	GTOUUP	GTIOC0A	SSLB1					
	S5D5	TCK/SWCLK	-	GTIOC0A	SSLB1					
P301		PSEL 00001b	PSEL 00010b	PSEL 00011b	PSEL 00100b	PSEL 00101b	PSEL 00110b	PSEL 01011b	PSEL 01100b	▼TS09 ▼SEG01 ▼COM5
	S3A1	AGTIO0	GTOULO	GTIOC4B	RXD2	CTS9	SSLB2	A06	TS09	
	S5D5	AGTIO0	GTOULO	GTIOC4B	RXD2	CTS9	SSLB2	A06	-	
		PSEL 01101b	ISEL							
	S3A1	SEG01/COM5	IRQ6							
	S5D5	-	IRQ6							

Table 8 144 Pin Package Difference (9 of 21)

Port	MCU	Select								Comments
P302		PSEL 00010b	PSEL 00011b	PSEL 00100b	PSEL 00110b	PSEL 01011b	PSEL 01100b	PSEL 01101b	ISEL	▼TS08 ▼SEG02 ▼COM6
	S3A1	GTOUUP	GTIOC4A	TXD2	SSLB3	A07	TS08	SEG02/COM6	IRQ5	
	S5D5	GTOUUP	GTIOC4A	TXD2	SSLB3	A07	-	-	IRQ5	
P303		PSEL 00011b	PSEL 01011b	PSEL 01100b	PSEL 01101b	PSEL 10101b				▼TS02 ▼SEG03 ▼COM7 ▼SD0DAT0
	S3A1	GTIOC7B	A08	TS02	SEG03/COM7	SD0DAT0				
	S5D5	GTIOC7B	A08	-	-	-				
P304		PSEL 00010b	PSEL 00011b	PSEL 00100b	PSEL 01011b	PSEL 01100b	PSEL 01101b	PSEL 10101b	ISEL	▲GTOWLO ▲RXD6 ▼TS11 ▼SEG17 ▼SD0WP
	S3A1	-	GTIOC7A	-	A09	TS11	SEG17	SD0WP	IRQ9	
	S5D5	GTOWLO	GTIOC7A	RXD6	A09	-	-	-	IRQ9	
P305		PSEL 00010b	PSEL 00100b	PSEL 01011b	PSEL 01101b	PSEL 10001b	PSEL 10101b	ISEL		▲GTOWUP ▲TXD6 ▼SEG16 ▼SD0CD
	S3A1	-	-	A10	SEG16	QSPCLK	SD0CD	IRQ8		
	S5D5	GTOWUP	TXD6	A10	-	QSPCLK	-	IRQ8		
P306		PSEL 00010b	PSEL 00100b	PSEL 01011b	PSEL 01101b	PSEL 10001b				▲GTOULO ▲SCK6 ▼SEG15
	S3A1	-	-	A11	SEG15	QSSL				
	S5D5	GTOULO	SCK6	A11	-	QSSL				
P307		PSEL 00010b	PSEL 00100b	PSEL 01011b	PSEL 01101b	PSEL 10001b				▲GTOUUP ▲CTS6 ▼SEG14
	S3A1	-	-	A12	SEG14	QIO0				
	S5D5	GTOUUP	CTS6	A12	-	QIO0				
P308		PSEL 01011b	PSEL 01101b	PSEL 10001b						▼SEG13
	S3A1	A13	SEG13	QIO1						
	S5D5	A13	-	QIO1						
P309		PSEL 00101b	PSEL 01011b	PSEL 10001b						
	S3A1	RXD3	A14	QIO2						
	S5D5	RXD3	A14	QIO2						

Table 8 144 Pin Package Difference (10 of 21)

Port	MCU	Select								Comments
P310		PSEL 00001b	PSEL 00101b	PSEL 01011b	PSEL 10001b					
	S3A1	AGTEE1	TXD3	A15	QIO3					
	S5D5	AGTEE1	TXD3	A15	QIO3					
P311		PSEL 00001b	PSEL 00101b	PSEL 01011b						▲RAS
	S3A1	AGTOB1	SCK3	CS2						
	S5D5	AGTOB1	SCK3	CS2/RAS						
P312		PSEL 00001b	PSEL 00101b	PSEL 01011b						▲CAS
	S3A1	AGTOA1	CTS3	CS3						
	S5D5	AGTOA1	CTS3	CS3/CAS						
P313		PSEL 01011b	PSEL 10101b	PSEL 10110b						▲ET0_ERXD3
	S3A1	A20	SD0DAT7	-						
	S5D5	A20	SD0DAT7	ET0_ERXD3						
P314		PSEL 01010b	PSEL 01011b							P314 is only available on S3A1
	S3A1	ADTRG0	A21							
	S5D5	-	-							
P315		PSEL 00100b	PSEL 01011b							P315 is only available on S3A1
	S3A1	RXD4	A22							
	S5D5	-	-							
P400		PSEL 00001b	PSEL 00011b	PSEL 00100b	PSEL 00101b	PSEL 00111b	PSEL 01010b	PSEL 01100b	PSEL 01101b	▲SCK7 ▲ADTRG1 ▲ET0_WOL ▼SCK1 ▼CACREF ▼TS20 ▼SEG04
	S3A1	AGTIO1	GTIOC6A	SCK4	SCK1	SCL0	CACREF	TS20	SEG04	
	S5D5	AGTIO1	GTIOC6A	SCK4	SCK7	SCL0	ADTRG1	-	-	
		PSEL 10010b	PSEL 10110b	PSEL 10111b	ISEL					
	S3A1	AUDIO_CLK	-	-	IRQ0					
	S5D5	AUDIO_CLK	ET0_WOL	ET0_WOL	IRQ0					

Table 8 144 Pin Package Difference (11 of 21)

Port	MCU	Select								Comments
P401		PSEL 00010b	PSEL 00011b	PSEL 00100b	PSEL 00101b	PSEL 00111b	PSEL 01100b	PSEL 01101b	PSEL 10000b	▲TXD7 ▲ET0_MDC ▲IRQ5-DS ▼TXD1 ▼TS19 ▼SEG05 ▼IRQ5
	S3A1	GTETRGA	GTIOC6B	CTS4	TXD1	SDA0	TS19	SEG05	CTX0	
	S5D5	GTETRGA	GTIOC6B	CTS4	TXD7	SDA0	-	-	CTX0	
		PSEL 10110b	PSEL 10111b	ISEL						
	S3A1	-	-	IRQ5						
	S5D5	ET0_MDC	ET0_MDC	IRQ5-DS						
P402		PSEL 00001b	PSEL 00101b	PSEL (don't care)	PSEL 01010b	PSEL 01100b	PSEL 01101b	PSEL 10000b	PSEL 10010b	▲RXD7 ▲ET0_MDIO ▲IRQ4-DS ▲CACREF ▲AUDIO_CLK ▲VSYNC ▼TXD1 ▼TS18 ▼SEG06 ▼IRQ4
	S3A1	AGTIO0_E/AGTIO1	RXD1	RTCIC0	-	TS18	SEG06	CRX0	-	
	S5D5	AGTIO0_B/AGTIO1	RXD7	RTCIC0	CACREF	-	-	CRX0	AUDIO_CLK	
		PSEL 10110b	PSEL 10111b	PSEL 11000b	ISEL					
	S3A1	-	-	-	IRQ4					
	S5D5	ET0_MDIO	ET0_MDIO	VSYNC	IRQ4-DS					
P403		PSEL 00001b	PSEL 00011b	PSEL 00101b	PSEL (don't care)	PSEL 01100b	PSEL 10010b	PSEL 10101b	PSEL 10110b	▲CTS7 ▲ET0_LINKSTA ▲SD1DAT7 ▲PIXD7 ▼CTS1 ▼TS17
	S3A1	AGTIO0_F/AGTIO1	GTIOC3A	CTS1	RTCIC1	TS17	SSIBCK0	-	-	
	S5D5	AGTIO0_C/AGTIO1	GTIOC3A	CTS7	RTCIC1	-	SSIBCK0	SD1DAT7	ET0_LINKSTA	
		PSEL 10111b	PSEL 11000b							
	S3A1	-	-							
	S5D5	ET0_LINKSTA	PIXD7							
P404		PSEL 00011b	PSEL (don't care)	PSEL 10010b	PSEL 10101b	PSEL 10110b	PSEL 10111b	PSEL 11000b		▲SD1DAT6 ▲PIXD6 ▲ET0_EXOUT
	S3A1	GTIOC3B	RTCIC2	SSILRCK0/SSIFS0	-	-	-	-		
	S5D5	GTIOC3B	RTCIC2	SSILRCK0/SSIFS0	SD1DAT6	ET0_EXOUT	ET0_EXOUT	PIXD6		

Table 8 144 Pin Package Difference (12 of 21)

Port	MCU	Select								Comments
P405		PSEL 00011b	PSEL 10010b	PSEL 10101b	PSEL 10110b	PSEL 10111b	PSEL 11000b			▲SD1DAT5 ▲PIXD5 ▲ET0_TX_EN ▲RMII0_TXD_EN
	S3A1	GTIOC1A	SSITXD0	-	-	-	-			
	S5D5	GTIOC1A	SSITXD0	SD1DAT5	ET0_TX_EN	RMII0_TXD_EN	PIXD5			
P406		PSEL 00011b	PSEL 00110b	PSEL 10010b	PSEL 10101b	PSEL 10110b	PSEL 10111b	PSEL 11000b		▲SSLB3 ▲SD1DAT4 ▲PIXD4 ▲ET0_RX_ER ▲RMII0_TXD1 ▼SSLA3
	S3A1	GTIOC1B	SSLA3	SSIRXD0	-	-	-	-		
	S5D5	GTIOC1B	SSLB3	SSIRXD0	SD1DAT4	ET0_RX_ER	RMII0_TXD1	PIXD4		
P407/ USB_VBUS		PSEL 00001b	PSEL 00100b	PSEL 00110b	PSEL 00110b	PSEL 01001b	PSEL 01010b	PSEL 01100b	PSEL 01101b	▲ET0_EXOUT ▼SEG11
	S3A1	AGTIO0	CTS4	SSLB3	SDA0	RTCOUT	ADTRG0	TS03	SEG11	
	S5D5	AGTIO0	CTS4	SSLB3	SDA0	RTCOUT	ADTRG0	TS03	-	
		PSEL 10011b	PSEL 10110b	PSEL 10111b						
	S3A1	USB_VBUS	-	-						
	S5D5	USB_VBUS	ET0_EXOUT	ET0_EXOUT						
P408		PSEL 00010b	PSEL 00011b	PSEL 00100b	PSEL 00101b	PSEL 00110b	PSEL 01100b	PSEL 01101b	PSEL 10011b	▲GTIOC10B ▲ET0_CRS ▲RMII0_CRS_DV ▲PIXCLK ▼GTIOC5B ▼CTS1 ▼SEG10
	S3A1	GTOWLO	GTIOC5B	CTS1	RXD3	SCL0	TS04	SEG10	USB_ID	
	S5D5	GTOWLO	GTIOC10B	-	RXD3	SCL0	TS04	-	USB_ID	
		PSEL 10110b	PSEL 10111b	PSEL 11000b	ISEL					
	S3A1	-	-	-	IRQ7					
	S5D5	ET0_CRS	RMII0_CRS_DV	PIXCLK	IRQ7					
P409		PSEL 00010b	PSEL 00011b	PSEL 00101b	PSEL 01100b	PSEL 01101b	PSEL 10011b	PSEL 10110b	PSEL 10111b	▲GTIOC10A ▲ET0_RX_CLK ▲RMIIO_RX_ER ▲HSYNC ▼GTIOC5A ▼SEG09
	S3A1	GTOWUP	GTIOC5A	TXD3	TS05	SEG09	USB_EXICEN	-	-	
	S5D5	GTOWUP	GTIOC10A	TXD3	TS05	-	USB_EXICEN	ET0_RX_CLK	RMII0_RX_ER	
		PSEL 11000b	ISEL							
	S3A1	-	IRQ6							
	S5D5	HSYNC	IRQ6							

Table 8 144 Pin Package Difference (13 of 21)

Port	MCU	Select								Comments
P410		PSEL 00001b	PSEL 00010b	PSEL 00011b	PSEL 00100b	PSEL 00101b	PSEL 00110b	PSEL 01100b	PSEL 01101b	▲ET0_ERXD0 ▲RMII0_RXD1 ▲PIXD0 ▼SEG08
	S3A1	AGTOB1	GTOVLO	GTIOC9B	RXD0	SCK3	MISOA	TS06	SEG08	
	S5D5	AGTOB1	GTOVLO	GTIOC9B	RXD0	SCK3	MISOA	TS06	-	
		PSEL 10101b	PSEL 10110b	PSEL 10111b	PSEL 11000b	ISEL				
	S3A1	SD0DAT1	-	-	-	IRQ5				
	S5D5	SD0DAT1	ET0_ERXD0	RMII0_RXD1	PIXD0	IRQ5				
P411		PSEL 00001b	PSEL 00010b	PSEL 00011b	PSEL 00100b	PSEL 00101b	PSEL 00110b	PSEL 01100b	PSEL 01101b	▲ET0_ERXD1 ▲RMII0_RXD0 ▲PIXD1 ▼SEG07
	S3A1	AGTOA1	GTOVUP	GTIOC9A	TXD0	CTS3	MOSIA	TS07	SEG07	
	S5D5	AGTOA1	GTOVUP	GTIOC9A	TXD0	CTS3	MOSIA	TS07	-	
		PSEL 10101b	PSEL 10110b	PSEL 10111b	PSEL 11000b	ISEL				
	S3A1	SD0DAT0	-	-	-	IRQ4				
	S5D5	SD0DAT0	ET0_ERXD1	RMII0_RXD0	PIXD1	IRQ4				
P412		PSEL 00001b	PSEL 00010b	PSEL 00100b	PSEL 00110b	PSEL 01100b	PSEL 10101b	PSEL 10110b	PSEL 10111b	▲AGTEE1 ▲TS08 ▲ET0_ETXD0 ▲REF50CK0 ▲PIXD2
	S3A1	-	GTOULO	SCK0	RSPCKA	-	SD0CMD	-	-	
	S5D5	AGTEE1	GTOULO	SCK0	RSPCKA	TS08	SD0CMD	ET0_ETXD0	REF50CK0	
		PSEL 11000b								
	S3A1	-								
	S5D5	PIXD2								
P413		PSEL 00010b	PSEL 00100b	PSEL 00110b	PSEL 01100b	PSEL 10101b	PSEL 10110b	PSEL 10111b	PSEL 11000b	▲ET0_ETXD1 ▲RMII0_TXD0 ▲PIXD3 ▲TS09
	S3A1	GTOUUP	CTS0	SSLA0	-	SD0CLK	-	-	-	
	S5D5	GTOUUP	CTS0	SSLA0	TS09	SD0CLK	ET0_ETXD1	RMII0_TXD0	PIXD3	
P414		PSEL 00011b	PSEL 00110b	PSEL 01100b	PSEL 10101b	PSEL 10110b	PSEL 10111b	PSEL 11000b	ISEL	▲ET0_RX_ER ▲RMII0_TXD1 ▲PIXD4 ▲TS10
	S3A1	GTIOC0B	SSLA1	-	SD0WP	-	-	-	IRQ9	
	S5D5	GTIOC0B	SSLA1	TS10	SD0WP	ET0_RX_ER	RMII0_TXD1	PIXD4	IRQ9	

Table 8 144 Pin Package Difference (14 of 21)

Port	MCU	Select								Comments
P415		PSEL 00011b	PSEL 00110b	PSEL 01100b	PSEL 10011b	PSEL 10101b	PSEL 10110b	PSEL 10111b	PSEL 11000b	▲ET0_TX_EN ▲RMII0_TXD_EN ▲TS11 ▲PIXD5 ▲USB_VBUSEN
	S3A1	GTIOC0A	SSLA2	-	-	SD0CD	-	-	-	
	S5D5	GTIOC0A	SSLA2	TS11	USB_VBUSEN	SD0CD	ET0_TX_EN	RMII0_TXD_EN	PIXD5	
		ISEL								
	S3A1	IRQ8								
	S5D5	IRQ8								
P500		PSEL 00001b	PSEL 00010b	PSEL 00011b	PSEL 01101b	PSEL 10001b	PSEL 10011b	PSEL 10101b	ASEL ADC	▲GTIOC11A ▲SD1CLK ▲IVREF0 ▼GTIOC2A ▼SEG48 ▼CMPREF1
	S3A1	AGTOA0	GTIU	GTIOC2A	SEG48	QSPCLK	USB_VBUSEN	-	AN016	
	S5D5	AGTOA0	GTIU	GTIOC11A	-	QSPCLK	USB_VBUSEN	SD1CLK	AN016	
		ASEL CMP								
	S3A1	CMPREF1								
	S5D5	IVREF0								
P501		PSEL 00001b	PSEL 00010b	PSEL 00011b	PSEL 00101b	PSEL 01101b	PSEL 10001b	PSEL 10011b	PSEL 10101b	▲GTIOC11B ▲TXD5 ▲SD1CMD ▲AN116 ▲IVREF1 ▼GTIOC2B ▼TXD3 ▼SEG49 ▼AN017 ▼CMPIN1
	S3A1	AGTOB0	GTIV	GTIOC2B	TXD3	SEG49	QSSL	USB_OVRCURA	-	
	S5D5	AGTOB0	GTIV	GTIOC11B	TXD5	-	QSSL	USB_OVRCURA	SD1CMD	
		ASEL ADC	ASEL CMP	ISEL						
	S3A1	AN017	CMPIN1	IRQ11						
	S5D5	AN116	IVREF1	IRQ11						
P502		PSEL 00010b	PSEL 00011b	PSEL 00101b	PSEL 01101b	PSEL 10001b	PSEL 10011b	PSEL 10101b	ASEL ADC	▲GTIOC12A ▲RXD5 ▲SD1DAT0 ▲AN017 ▲IVCMP0 ▼GTIOC3B ▼RXD3 ▼SEG50 ▼AN018 ▼CMPREF0
	S3A1	GTIW	GTIOC3B	RXD3	SEG50	QIO0	USB_OVRCURB	-	AN018	
	S5D5	GTIW	GTIOC12A	RXD5	-	QIO0	USB_OVRCURB	SD1DAT0	AN017	
		ASEL CMP	ISEL							
	S3A1	CMPREF0	IRQ12							
	S5D5	IVCMP0	IRQ12							

Table 8 144 Pin Package Difference (15 of 21)

Port	MCU	Select								Comments
P503		PSEL 00010b	PSEL 00011b	PSEL 00100b	PSEL 00101b	PSEL 01101b	PSEL 10001b	PSEL 10011b	PSEL 10101b	▲GTETRGC ▲GTIOC12B ▲CTS6 ▲SD1DAT1 ▲AN117 ▲SCK5 ▼GTETRGA ▼CTS2 ▼SEG51 ▼AN023 ▼CMPIN0 ▼SCK3
	S3A1	GTETRGA	-	CTS2	SCK3	SEG51	QIO1	USB_EXICEN	-	
	S5D5	GTETRGC	GTIOC12B	CTS6	SCK5	-	QIO1	USB_EXICEN	SD1DAT1	
		ASEL ADC	ASEL CMP							
	S3A1	AN023	CMPIN0							
	S5D5	AN117	-							
P504		PSEL 00010b	PSEL 00011b	PSEL 00100b	PSEL 00101b	PSEL 01011b	PSEL 10001b	PSEL 10011b	PSEL 10101b	▲GTETRGD ▲GTIOC13A ▲SCK6 ▲SD1DAT2 ▲AN018 ▲CTS5 ▼GTETRGB ▼SCK2 ▼AN024 ▼CTS3
	S3A1	GTETRGB	-	SCK2	CTS3	ALE	QIO2	USB_ID	-	
	S5D5	GTETRGD	GTIOC13A	SCK6	CTS5	ALE	QIO2	USB_ID	SD1DAT2	
		ASEL ADC								
	S3A1	AN024								
	S5D5	AN018								
P505		PSEL 00011b	PSEL 00100b	PSEL 10001b	PSEL 10101b	ASEL ADC	ISEL			▲GTIOC13B ▲RXD6 ▲SD1DAT3 ▲AN118 ▼RXD2 ▼AN025
	S3A1	-	RXD2	QIO3	-	AN025	IRQ14			
	S5D5	GTIOC13B	RXD6	QIO3	SD1DAT3	AN118	IRQ14			
P506		PSEL 00100b	PSEL 10101b	ASEL ADC	ISEL					▲TXD6 ▲SD1CD ▲AN019 ▼TXD2 ▼AN026
	S3A1	TXD2	-	AN026	IRQ15					
	S5D5	TXD6	SD1CD	AN019	IRQ15					
P507		PSEL 00100b	PSEL 00101b	PSEL 10101b	ASEL ADC					P507 is only available on S3A1
	S3A1	-	-	-	AN027					
	S5D5	-	-	-	-					
P508		PSEL 00100b	PSEL 00101b	PSEL 10101b	ASEL ADC					P508 is only available on S5D5
	S3A1	-	-	-	-					
	S5D5	SCK6	SCK5	SD1DAT3	AN020					

Table 8 144 Pin Package Difference (16 of 21)

Port	MCU	Select								Comments
P511		PSEL 00011b	PSEL 00100b	PSEL 00111b	PSEL 10000b	PSEL 11000b	ISEL			▲CRX1 ▲PCKO ▼CRX0
	S3A1	GTIOC0B	RXD4	SDA2	CRX0	-	IRQ15			
	S5D5	GTIOC0B	RXD4	SDA2	CRX1	PCKO	IRQ15			
P512		PSEL 00011b	PSEL 00100b	PSEL 00111b	PSEL 10000b	PSEL 11000b	ISEL			▲CTX1 ▲VSYNC ▼CTX0
	S3A1	GTIOC0A	TXD4	SCL2	CTX0	-	IRQ14			
	S5D5	GTIOC0A	TXD4	SCL2	CTX1	VSYNC	IRQ14			
P600		PSEL 00011b	PSEL 00101b	PSEL 01001b	PSEL 01010b	PSEL 01011b	PSEL 01101b	PSEL 10101b		▲CLKOUT ▲CACREF ▼SEG41 ▼SD0DAT7
	S3A1	GTIOC6B	SCK9	-	-	RD	SEG41	SD0DAT7		
	S5D5	GTIOC6B	SCK9	CLKOUT	CACREF	RD	-	-		
P601		PSEL 00011b	PSEL 00101b	PSEL 01011b	PSEL 01101b	PSEL 10101b				▲DQM0 ▼SEG40 ▼SD0DAT6
	S3A1	GTIOC6A	RXD9	WR/WR0	SEG40	SD0DAT6				
	S5D5	GTIOC6A	RXD9	WR/WR0/DQM0	-	-				
P602		PSEL 00011b	PSEL 00101b	PSEL 01011b	PSEL 01101b	PSEL 10101b				▲SDCLK ▼SEG39 ▼SD0DAT5
	S3A1	GTIOC7B	TXD9	EBCLK	SEG39	SD0DAT5				
	S5D5	GTIOC7B	TXD9	EBCLK/SDCLK	-	-				
P603		PSEL 00011b	PSEL 00101b	PSEL 01011b	PSEL 01101b	PSEL 10101b				▲DQ13 ▼SEG38 ▼SD0DAT4
	S3A1	GTIOC7A	CTS9	D13	SEG38	SD0DAT4				
	S5D5	GTIOC7A	CTS9	D13/DQ13	-	-				
P604		PSEL 00011b	PSEL 01011b	PSEL 01101b						▲DQ12 ▼SEG37
	S3A1	GTIOC8B	D12	SEG37						
	S5D5	GTIOC8B	D12/DQ12	-						
P605		PSEL 00011b	PSEL 01011b	PSEL 01101b						▲DQ11 ▼SEG36
	S3A1	GTIOC8A	D11	SEG36						
	S5D5	GTIOC8A	D11/DQ11	-						

Table 8 144 Pin Package Difference (17 of 21)

Port	MCU	Select								Comments
P606		PSEL 01001b	PSEL 01101b							P606 is only available on S3A1
	S3A1	RTCOUT	SEG35							
	S5D5	-	-							
P608		PSEL 00011b	PSEL 01011b	PSEL 01101b	PSEL 10101b					▲DQM1 ▼SEG28 ▼SD0DAT1
	S3A1	GTIOC4B	A00/BC0	SEG28	SD0DAT1					
	S5D5	GTIOC4B	A00/BC0/DQM1	-	-					
P609		PSEL 00011b	PSEL 01011b	PSEL 01101b	PSEL 10000b	PSEL 10101b				▲CKE ▲CTX1 ▼SEG29 ▼SD0DAT2
	S3A1	GTIOC5A	CS1	SEG29	-	SD0DAT2				
	S5D5	GTIOC5A	CS1/CKE	-	CTX1	-				
P610		PSEL 00011b	PSEL 01011b	PSEL 01101b	PSEL 10000b	PSEL 10101b				▲WE ▲CRX1 ▼SEG30 ▼SD0DAT3
	S3A1	GTIOC5B	CS0	SEG30	-	SD0DAT3				
	S5D5	GTIOC5B	CS0/WE	-	CRX1	-				
P611		PSEL 00101b	PSEL 01001b	PSEL 01010b	PSEL 01011b	PSEL 01101b				▲CTS7 ▲CLKOUT ▲CACREF ▲SDCS ▼SEG31
	S3A1	-	-	-	-	SEG31				
	S5D5	CTS7	CLKOUT	CACREF	SDCS	-				
P612		PSEL 00101b	PSEL 01011b	PSEL 01101b						▲SCK7 ▲DQ08 ▼SEG32
	S3A1	-	D08	SEG32						
	S5D5	SCK7	D08/DQ08	-						
P613		PSEL 00101b	PSEL 01011b	PSEL 01101b						▲TXD7 ▲DQ09 ▼SEG33
	S3A1	-	D09	SEG33						
	S5D5	TXD7	D09/DQ09	-						
P614		PSEL 00101b	PSEL 01011b	PSEL 01101b						▲RXD7 ▲DQ10 ▼SEG34
	S3A1	-	D10	SEG34						
	S5D5	RXD7	D10/DQ10	-						

Table 8 144 Pin Package Difference (18 of 21)

Port	MCU	Select								Comments
P700		PSEL 00011b	PSEL 00110b	PSEL 10101b	PSEL 10110b	PSEL 10111b	PSEL 11000b			▲MISOB ▲SD1DAT3 ▲ET0_ETXD1 ▲PIXD3 ▲RMII0_TXD0 ▼MISOA
	S3A1	GTIOC5A	MISOA	-	-	-	-			
	S5D5	GTIOC5A	MISOB	SD1DAT3	ET0_ETXD1	RMII0_TXD0	PIXD3			
P701		PSEL 00011b	PSEL 00110b	PSEL 10101b	PSEL 10110b	PSEL 10111b	PSEL 11000b			▲MOSIB ▲SD1DAT2 ▲ET0_ERXD1 ▲PIXD3 ▲REF50CK0 ▼MOSIA
	S3A1	GTIOC5B	MOSIA	-	-	-	-			
	S5D5	GTIOC5B	MOSIB	SD1DAT2	ET0_ETXD0	REF50CK0	PIXD2			
P702		PSEL 00011b	PSEL 00110b	PSEL 10101b	PSEL 10110b	PSEL 10111b	PSEL 11000b			▲RSPCKB ▲SD1DAT1 ▲ET0_ERXD1 ▲PIXD1 ▲RMII0_RXD0 ▼RSPCKA
	S3A1	GTIOC6A	RSPCKA	-	-	-	-			
	S5D5	GTIOC6A	RSPCKB	SD1DAT1	ET0_ERXD1	RMII0_RXD0	PIXD1			
P703		PSEL 00011b	PSEL 00110b	PSEL 01001b	PSEL 10101b	PSEL 10110b	PSEL 10111b	PSEL 11000b		▲SSLB0 ▲SD1DAT0 ▲ET0_ERXD0 ▲PIXD0 ▲RMII0_RXD1 ▼SSLA0
	S3A1	GTIOC6B	SSLA0	VCOUT	-	-	-	-		
	S5D5	GTIOC6B	SSLB0	VCOUT	SD1DAT0	ET0_ERXD0	RMII0_RXD1	PIXD0		
P704		PSEL 00001b	PSEL 00110b	PSEL 10000b	PSEL 10101b	PSEL 10110b	PSEL 10111b	PSEL 11000b		▲SSLB1 ▲SD1CLK ▲CTX0 ▲ET0_RX_CLK ▲HYSYNC ▲RMII0_RX_ER ▼SSLA1
	S3A1	AGTO0	SSLA1	-	-	-	-	-		
	S5D5	AGTO0	SSLB1	CTX0	SD1CLK	ET0_RX_CLK	RMII0_RX_ER	HSYNC		
P705		PSEL 00001b	PSEL 00110b	PSEL 10000b	PSEL 10101b	PSEL 10110b	PSEL 10111b	PSEL 11000b		▲SSLB2 ▲CRX0 ▲SD1CMD ▲ET0_CRS ▲PIXCLK ▲RMII0_CRS_DV ▼SSLA2
	S3A1	AGTIO0	SSLA2	-	-	-	-	-		
	S5D5	AGTIO0	SSLB2	CRX0	SD1CMD	ET0_CRS	RMII0_CRS_DV	PIXCLK		
P708		PSEL 00101b	PSEL 00110b	PSEL 01010b	PSEL 01100b	PSEL 10010b	PSEL 10110b	PSEL 11000b	ISEL	▲CACREF ▲TS12 ▲AUDIO_CLK ▲ET0_ETXD3 ▲PCKO
	S3A1	RXD1	SSLA3	-	-	-	-	-	IRQ11	
	S5D5	RXD1	SSLA3	CACREF	TS12	AUDIO_CLK	ET0_ETXD3	PCKO	IRQ11	
P709		PSEL 00101b	PSEL 01100b	PSEL 10110b	ISEL					▲TS13 ▲ET0_ETXD2
	S3A1	TXD1	-	-	IRQ10					
	S5D5	TXD1	TS13	ET0_ETXD2	IRQ10					

Table 8 144 Pin Package Difference (19 of 21)

Port	MCU	Select								Comments
P710		PSEL 00101b	PSEL 01011b	PSEL 01100b	PSEL 10110b					▲TS14 ▲ET0_TX_ER ▼A17
	S3A1	SCK1	A17	-	-					
	S5D5	SCK1	-	TS14	ET0_TX_ER					
P711		PSEL 00001b	PSEL 00101b	PSEL 01100b	PSEL 10110b					▲TS15 ▲ET0_TX_CLK
	S3A1	AGTEE0	CTS1	-	-					
	S5D5	AGTEE0	CTS1	TS15	ET0_TX_CLK					
P712		PSEL 00001b	PSEL 00011b	PSEL 01100b						▲TS16
	S3A1	AGTOB0	GTIOC2B	-						
	S5D5	AGTOB0	GTIOC2B	TS16						
P713		PSEL 00001b	PSEL 00011b	PSEL 01100b						▲TS17
	S3A1	AGTOA0	GTIOC2A	-						
	S5D5	AGTOA0	GTIOC2A	TS17						
P800		PSEL 01011b	PSEL 01101b							▲DQ14 ▼SEG44
	S3A1	D14	SEG44							
	S5D5	D14/DQ14	-							
P801		PSEL 01011b	PSEL 01101b							▲DQ15 ▼SEG45
	S3A1	D15	SEG45							
	S5D5	D15/DQ15	-							
P802		PSEL 01101b								P802 is only available on S3A1
	S3A1	SEG46								
	S5D5	-								
P803		PSEL 01101b								P803 is only available on S3A1
	S3A1	SEG47								
	S5D5	-								

Table 8 144 Pin Package Difference (20 of 21)

Port	MCU	Select								Comments
P804		PSEL 00011b	PSEL 01101b							P804 is only available on S3A1
	S3A1	GTIOC9B	SEG43							
	S5D5	-	-							
P805		PSEL 00011b	PSEL 01101b							P805 is only available on S3A1
	S3A1	GTIOC9A	SEG42							
	S5D5	-	-							
P806		PSEL 01101b								P806 is only available on S3A1
	S3A1	SEG26								
	S5D5	-								
P807		PSEL 01101b								P807 is only available on S3A1
	S3A1	SEG27								
	S5D5	-								
P808		PSEL 01101b	PSEL 10101b							P808 is only available on S3A1
	S3A1	SEG18	SD0CLK							
	S5D5	-	-							
P809		PSEL 01101b	PSEL 10101b							P809 is only available on S3A1
	S3A1	SEG19	SD0CMD							
	S5D5	-	-							
P900		PSEL 00100b	PSEL 01011b							P900 is only available on S3A1
	S3A1	TXD4	A23							
	S5D5	-	-							
P901		PSEL 00001b	PSEL 00100b							P901 is only available on S3A1
	S3A1	AGTIO1	SCK4							
	S5D5	-	-							

Table 8 144 Pin Package Difference (21 of 21)

Port	MCU	Select								Comments
P902		PSEL 00001b	PSEL 00100b							P902 is only available on S3A1
	S3A1	AGTO1	CTS4							
	S5D5	-	-							
P914/ USB_DP		PSEL (don't care)								P914 is only available on S3A1
	S3A1	USB_DP								
	S5D5	-								
P915/ USB_DM		PSEL (don't care)								P915 is only available on S3A1
	S3A1	USB_DM								
	S5D5	-								

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Revision History

Rev.	Date	Description	
		Page	Summary
1.00	Jun 29, 2018	—	First release document

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