Renesas Synergy™ Platform

S3A7 to S5D5 MCU Group Migration Guide

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Introduction

This Application Note compares hardware peripherals, port select features, and functional differences between the Renesas Synergy™ Microcontrollers S3A7 MCU Group and the S5D5 MCU Group.

Target Device

Synergy S5D5 MCU Group

Contents

1. About this Document

This document is designed to provide the user with an overview of the functional, hardware, and electrical characteristic differences when migrating from the S3A7 MCU Group to the S5D5 MCU Group.

2. Audience

This document is intended for users who are designing application systems using the Synergy S3A7 MCU Group devices. Users are expected to have a technical understanding of the peripherals provided in the S3A7 MCU Group. This application note should be used with the *S3A7 MCU Group User's Manual: Microcontrollers*.

The application note presents two major sections. The first section specifies functional and specification differences between the S3A7 MCU Group and the S5D5 MCU Group's, respectively. The second section details the differences in port functionality between the two MCU's.

3. References

Renesas provides the following documents for the Synergy S3 and S5 Series MCUs. Before using any of these documents, see the Website and Support section. This section lists locations where you can find the latest document versions to use.

Table 3.1 Synergy S3 and S5 Series MCU Group Documents

Document Type	Description	Description Title	Description No.
Datasheet S3A7 MCU Group	Overview and electrical characteristics of MCU.	S3A7 MCU Group Datasheet	R01DS0263EU0100
S3A7 User's Manual: Microcontrollers	MCU specifications (pin assignments, memory maps, peripheral functions, electrical characteristics, and timing charts) and operation descriptions.	S3A7 MCU Group User's Manual: Microcontrollers	R01UM0002EU0120
Datasheet S5D5 MCU Group	Overview and electrical characteristics of MCU.	S5D5 MCU Group Datasheet	R01DS0317EU0110
S5D5 MCU Group User's Manual: Microcontrollers	MCU specifications (pin assignments, memory maps, peripheral functions, electrical characteristics, and timing charts) and operation descriptions.	S5D5 MCU Group User's Manual: Microcontrollers	R01UM0009EU0110
Renesas Synergy Software Package (SSP)	API reference and introduction to SSP architecture and programming.	Renesas Synergy Software Package (SSP) User's Manual	R01US0315EU0100

4. Numbering Notation

The following numbering notation is used throughout this manual:

Table 4.1 Example of number notation

Example	Description
011b	Binary number. For example, the binary equivalent of the number 3 is 011b
1Fh	Hexadecimal number. For example, the hexadecimal equivalent of the number 31 is described 1Fh. In some cases, a hexadecimal number is shown with the prefix 0x.
1234	Decimal number. A decimal number is followed by this symbol only when the possibility of confusion exists. Decimal numbers are generally shown without a suffix.
Bit 4	Specifies the bit position in field or register.

5. Specification and Hardware Differences

Table 5.2 specifies hardware compatibility and differences between the S3A7 MCU Group and S5D5 MCU Group. The table is ordered with increasing specifics from left to right. The leftmost column corresponds to a system as noted in the user's manual for the Synergy S3A7 MCU Group or S5D5 MCU Group. Values in the S5D5 column represent a system, subsystem, or field in register exists and has a certain value. Values in the S3A7 column show the change in hardware, new feature addition, or notes a main feature. The Reference column specifies the section in the *S5D5 MCU Group User's Manua*l that can be referred to for more information.

The following terms are used to compare the functionality of peripherals in the specification differences table.

Table 5.1 Terms and functionality of peripherals

Terms	Description
Exists or Available	The peripheral or function is implemented for a MCU Group
Does Not Exist or Not Available	The peripheral specified has been removed (when compared to the other MCU Group) or does not exist in the MCU Group
Not Applicable	The criteria for comparison is invalid for the MCU Group

Table 5.2 Specification Difference (1 of 23)

SPECIFICATION			S3A7	S5D5	S5D5 HWM REFERENCE
CPU	Embedded Trace Buffer	Buffer Size	All reset sources	Only VBATT_POR	2.1.2
	Maximum Operating Frequency	CPU Core	48 MHz	120 MHz	2.1.3
		4-Bit TPIU Trace Interface	Does Not Exist	60 MHz	2.1.3, 2.3
		SWO Trace Interface	12.5 MHz	60 MHz	2.1.3
		JTAG Interface	12.5 MHz	25 MHz	
		SWD Interface	12.5 MHz	25 MHz	
	CoreSight ROM Table	ROM Entries	Refer to Manual	Refer to Manual	2.6.3.1
	Changing a Low power Mode While in OCD Mode	Mode Restriction Deep Software Standby	Does Not Exist	Refer to Manual	2.11.3.2
Address Space	MCU Supports a 4-GB Linear Address Space Ranging from 0000 0000h to FFFF FFFFh that can Contain Both Program and Data		Refer to Manual	Refer to Manual	Chapter 4
Memory Mirror Function	MMSFR.MEMMIRADDR Address	Application Code Ver1	0010 0000h	DB10 0000h	5.3.2
		Application Code Ver2	0011 0000h	DB11 0000h	5.3.2
		Application Code Ver3	0012 0000h	DB12 0000h	5.3.2
Resets	VBATT-Selected Voltage Power-On Reset		Exists	Does Not Exist	
	Deep Software Standby Reset		Does Not Exist	Exists	6.1
	Module-Related Registers Initialized by Each Reset Source		Refer to Manual	Refer to Manual	Table 6.3
	States of SOSC and LOCO when a Reset Occurs		Refer to Manual	Refer to Manual	Table 6.4, Table 6.5
	Reset Status Register 0 (RSTSR0)	Bit 7	Reserved	Deep Software Standby Reset Flag	6.2.1

Table 5.3 Specification Difference (2 of 23)

SPECIFICATION			S3A7	S5D5	S5D5 HWM REFERENCE
Option-Setting Memory	Configuration Setting Area	OCD/Serial Programmer ID Setting Register (OSIS)	0101 0018h to 0101 0033h	0100 A150h to 0100 A15Ch	7.1
		Access Window Setting Register (AWS)	0101 0010h to 0101 0013h	0100 A164h to 0100 A167h	
	Option Function Select Register 1 (OFS1)	Bits [1:0]	Reserved	VDSEL0[1:0]	7.2.2
		Bits [5:3]	VDSEL1[2:0]	Reserved	
		Bits [9:8]	Reserved	HOCOFRQ0[1:0]	
		Bits [14:12]	HOCOFRQ1[2:0]	Reserved	
	MPU Registers		Refer to Manual	Does Not Exist	
	Access Window Setting Control Register (AWSC)		Refer to Manual	Does Not Exist	
	Access Window Setting Register (AWS)	Start Block Address (FAWS)	Spans Bits [11:0]	Spans Bits [10:0] Bit 11 is Reserved	7.2.3
		Bit 15	Reserved	FSPR Bit	
		End Block Address (FAWE)	Spans Bits [27:16]	Spans Bits [26:16] Bit 27 is Reserved	
		Bit 31	Reserved	BTFLG Bit	

Table 5.4 Specification Difference (3 of 23)

SPECIFICATION			S3A7	S5D5	S5D5 HWM REFERENCE
Low Voltage Detection (LVD)	Voltage Monitor Circuit Control Register (LVCMPCR)	Deep Software Standby Mode	Not Applicable	For Voltage Detection, Do Not Set DPSBYCR.DEEPCUT [1:0] to 11b	8.2.5
	Voltage Detection Level Select Register (LVDLVLR)		Refer to Manual	Refer to Manual	8.2.6
	Voltage Monitor n Circuit Control Register 0 (n = 1, 2) (LVD1CR0 and LVD2CR0)	Bit 1	Reserved Value After Reset is 0	Digital Filter Disable Mode Select (DFDIS) Value After Reset is 1	8.2.7 8.2.8
		Bit 3	Value After Reset is 0	Value After Reset is Undefined	
		Bits [5:4]	Reserved	Sampling Clock Reset FSAMP[1:0]	
	VCC Input Voltage Monitor	Procedure to Set Up Monitoring Against Vdet1 and Vdet2	Refer to Manual	Refer to Manual	Table 8.2 Table 8.3
	Interrupt and Reset from Voltage Monitor 1 and 2		Refer to Manual	Refer to Manual	8.5, 8.6
	Interrupt Handling and Event Linking	Deep Software Standby Mode	Not Applicable	For Vdet1 and Vdet2 passage events, event signals are not generated for the ELC	8.7.1

Table 5.5 Specification Difference (4 of 23)

SPECIFICATION			S3A7	S5D5	S5D5 HWM REFERENCE
Clock Generation Circuit	Main Clock Oscillator (MOSC)	Resonator Frequency	1 MHz to 20 MHz (Up to 5.5 V) 1 MHz to 8 MHz (Up to 2.4 V) 4, 6, 8, 12 MHz (USB boot mode)	8 to 24 MHz 8, 10, 12, 15, 16, 20, 24 MHz (USB Boot Mode)	
		External Clock Input Frequency	Up to 20 MHz	Up to 24 MHz	
	PLL Circuit	Input Clock Source	MOSC	MOSC, HOCO	Table 9.1
		Input Frequency	4 MHz to 12.5 MHz	8 MHz to 24 MHz	
		Input Pulse Frequency Division Ratio	Not Applicable	Select between 1, 2 and 3	
		Frequency Multiplication Ratio	Select between 8 and 31, Step Size 1, Multiplication Frequency up to 64 MHz	Select between 10 and 30, Step Size 0.5	
		Output Pulse Frequency Division Ratio	Select between 1, 2, and 4	Not Applicable	
		PLL Output Frequency	48 MHz to 64 MHz (Division Ratio: 1) 24 MHz to 64 MHz (Division Ratio: 2) 24 MHz to 32 MHz (Division Ratio: 4)	120 to 240 MHz	
	High-Speed On-Chip Oscillator (HOCO)	Oscillation Frequency	24, 32, 48, 64 MHz	16, 18, 20 MHz	
	Clock Generation Circuit Specifications for the Internal Clocks		Refer to Manual	Refer to Manual	Table 9.2

Table 5.6 Specification Difference (5 of 23)

SPECIFICATION			S3A7	S5D5	S5D5 HWM REFERENCE
Clock Generation Circuit (Continued)	Registers		Refer to Manual	Refer to Manual	9.2
	External Clock Input	XTAL Pin	Cannot be Set by User	Set in PFS.P213PFS	9.3.2
	Handling of Pins When the Sub-Clock Oscillator Is Not Used		Not Applicable	Refer to Manual	9.4.2
	Oscillation Stop Detection		Detected when SCKSCR.CKSEL[2:0] = 101b	Detected when PLLCCR.PLSRCSEL = 0 and SCKSCR.CKSEL[2:0] = 101b	9.5.1
	Oscillation Stop Detection Interrupts		When triggered, write to ICSR6.OSTSTF flag	When triggered, write to POEGGn.OSTPF flag	9.5.2
	Internal Clock Sources	Clock for the External Bus Controller and External Pin Output for the SDRAM	Not Applicable	SDCLK	9.7, 9.7.5
		Source Clock for the SLCDC	LCDSRCCLK	Not Applicable	9.7, 9.7.12
	Specify the Frequency	ICLK, PCLKA, PCLKB, PCLKC, PCLKD, FCLK, BCLK, UCLK	PLLMUL[4:0] and PLODIV[1:0] in PLLCCR2	PLLMUL[5:0] and PLIDIV[1:0] in PLLCCR	9.7.1, 9.7.2, 9.7.3, 9.7.4, 9.7.6
		CLKOUT	PLLMUL[4:0] and PLODIV[1:0] in PLLCCR2	Cannot be Set Using PLLCCR	9.7.13
		ICLK, PCLKA, PCLKB, PCLKC, PCLKD, FCLK, BCLK, UCLK, CLKOUT	HOCOFRQ1[2:0] in OFS1	HOCOFRQ[1:0] in OFS1	9.7.1, 9.7.2, 9.7.3, 9.7.4, 9.7.6, 9.7.13
	Usage Notes	Sub-Clock Oscillator for LGA Packages	Not Applicable	Refer to Manual	9.8.5
		Main Clock Oscillator Drive Capability Auto Switching Function	Not Applicable	Refer to Manual	9.8.6

Table 5.7 Specification Difference (6 of 23)

SPECIFICATION			S3A7	S5D5	S5D5 HWM REFERENCE
Low Power Modes	Provides Several Functions for Reducing Power Consumption		Missing Deep Software Standby Mode, Has Middle-Speed Mode and Low-Voltage Mode, Refer to Manual for Additional Details	Has Deep Software Standby Mode, Missing Middle-Speed Mode and Low-Voltage Mode, Refer to Manual for Additional Details	Chapter 11
Battery Backup Function	Provides a Battery Backup Function that Maintains Partial Battery Powering in the Event of Power Loss		Includes the RTC, AGT, SOSC, LOCO, Wakeup Control, Backup Memory, VBATT_R Low Voltage Detection and Switch Between VCC and VBATT. Refer to Manual for Additional Details	Includes the RTC, SOSC, Backup Memory, and Switch Between VCC and VBATT. Refer to Manual for Additional Details	Chapter 12
Register Write Protection	Association Between PRCR bits and Protected Registers	PRC0	PLLCCR2, MEMWAIT, SLCDSCKCR	SCKDIVCR2, PLLCCR, SDCKOCR, FLLCR1, FLLCR2	Table 13.1
		PRC1	FLSTOP, PSMCR, VBTCR1, VBTCR2, VBTSR, VBTCMPCR, VBTLVDICR, VBTWCTLR, VBTWCH0OTSR, VBTWCH1OTSR, VBTWCH2OTSR, VBTOCTLR, VBTWTER, VBTWEGR, VBTWFR	DPSBYCR, DPSIER0-3, DPSIFR0-3, DPSIEGR0-2, STCONR	

Table 5.8 Specification Difference (7 of 23)

SPECIFICATION			S3A7	S5D5	S5D5 HWM REFERENCE
Interrupt Controller Unit (ICU)	Peripheral Function Interrupts	Number of Sources	205	301	Table 14.1
	Interrupt Sources for NVIC		64	96	
	Non-Maskable Interrupt Status Register (NMISR)	Bit 4	VBATTST VBATT Monitor Interrupt Status Flag	Reserved	14.2.2
	Non-Maskable Interrupt Enable Register (NMIER)	Bit 4	VBATTEN VBATT monitor Interrupt Enable	Reserved	14.2.3
	Non-Maskable Interrupt Status Clear Register (NMICLR)	Bit 4	VBATTCLR VBATT Clear	Reserved	14.2.4
	DMAC Event Link Setting Register n (DELSRn) (n = 0 to 7)	Bit 16	Does Not Exist Refer to Manual for Additional Differences	IR Interrupt Status Flag Refer to Manual for Additional Differences	14.2.7
	Wake Up Interrupt Enable Register (WUPEN)	Bit 20	Reserved	VBATTWUPEN VBATT Monitor Interrupt Software Standby Returns Enable	14.2.7
		Bit 22	ACMPHS0WUPEN ACMPHS0 Interrupt Software Standby Returns Enable	Reserved	
		Bit 23	Reserved	ACMPLP0WUPEN ACMPLP0 Interrupt Software Standby Returns Enable	

Table 5.9 Specification Difference (8 of 23)

SPECIFICATION			S3A7	S5D5	S5D5 HWM REFERENCE
Interrupt Controller Unit (ICU) (Continued)	Interrupt Vector Table		Refer to Manual	Refer to Manual	14.3.1, Table 14.3
	Event Numbers		Refer to Manual	Refer to Manual	14.3.2, Table 14.4
	Non-Maskable Interrupt	VBATT monitor interrupt	Exists	Does Not Exist	14.5
Buses	Main Bus	ICode Bus DCode Bus	Connected to Code Flash Memory	Connected to Code Flash Memory and SRAMHS	Table 15.1
		ETHER Bus	Does Not Exist	Exists	
	Slave Interface	Memory Bus 2	Does Not Exist	Exists. Connected to SRAMHS	
		Internal Peripheral Bus 3 SRC, TSN	Not Applicable	Connected to SRC, TSN	
		Internal Peripheral Bus 4 GPT, ETHERC, EDMAC	Not Applicable	Connected to GPT, ETHERC, EDMAC	
		Internal Peripheral Bus 5 OPAMP, PDC, ACMPLP	Connected to OPAMP, ACMPLP	Connected to PDC	
		Internal Peripheral Bus 7 SCE7	Not Applicable	Connected to SCE7	
	Addresses Assigned	Memory Bus 5	20020000h to 2002FFFFh Area: SRAM1	20040000h to 200FFFFFh Area: Standby SRAM	Table 15.2
	External Bus	Connected to SDRAM	Not Applicable	Yes	Table 15.1, 15.2.3
		External Address Space	4 CS areas (CS0 to CS3)	8 CS areas (CS0 to CS7) and SDRAM area Address/Data Multiplexed Bus Available	Table 15.3
	All Other Differences		Refer to Manual	Refer to Manual	Chapter 15

Table 5.10 Specification Difference (9 of 23)

SPECIFICATION			S3A7	S5D5	S5D5 HWM REFERENCE
Memory Protection Unit MPU	Memory protection	Bus Master MPU	Group A: 16 Regions Refer to Manual for Details	Group A: 32 Regions Group B: 8 Regions Refer to Manual for Details	Table 16.1 16.4.1
	Security MPU - Protects Accesses from Non-Secure Programs to the Secure Regions		2 Regions (PC) 1 Region (Code Flash)	2 Regions (PC) 4 Regions (Code Flash, SRAM, 2 Secure Functions)	Table 16.1 16.6.2.1
	Bus Slave MPU	Register Description	Refer to Manual	Refer to Manual	16.5
	Security MPU	Register Description	Refer to Manual	Refer to Manual	16.6

Table 5.11 Specification Difference (10 of 23)

SPECIFICATION			S3A7	S5D5	S5D5 HWM REFERENCE
DMA Controller (DMAC)	Number of Channels		4	8	Table 17.1
	Channel Priority		Channels 0 > 1 > … > 3 (Channel 0: Highest)	Channels 0 > 1 > … > 7 (Channel 0: Highest)	
	DMAC Execution Cycles	Read and Write Data Transfer	Based on Block Size, Read Destination Access Cycle and Data Write Destination Access Cycle	Based on Block Size, Read Destination Access Cycle, Data Write Destination Access Cycle and SRAMHS	Table 17.7
Data Transfer Controller (DTC)	DTC Module Start Register (DTCST)	Read and Write Data Transfer	Not Applicable	Applicable	18.2.9 18.10
	DTC Execution Cycles	Bit 0 - DTCST Bit Must be Set to 0 before transition to Deep Software Standby Mode	Based on Block Size, Read Destination Access Cycle and Data Write Destination Access Cycle	Based on Block Size, Read Destination Access Cycle, Data Write Destination Access Cycle and SRAMHS	18.4.8
Event Link Controller (ELC)	Event Link Function	Number of Event Signals Directly Connected to Modules	181	258	Table 19.1
	Associations Between the ELSRn Register and Peripheral Functions		Refer to Manual	Refer to Manual	19.2.3 Table 19.2

Table 5.12 Specification Difference (11 of 23)

SPECIFICATION			S3A7	S5D5	S5D5 HWM REFERENCE
I/O Ports	Function and Specification	Total Pins	Up to 124	Up to 110	Table 20.1 Table 20.2
		PORT0	P000 to P015	P000 to P009, P014, P015	
		PORT2	P200 to P206, P212 to P215	P200 to P214	
		PORT3	P300 to P315	P300 to P313	
		PORT5	P500 to P507, P511, P512	P500 to P506, P508, P511, P512	
		PORT6	P600 to P606, P608 to P614	P600 to P605, P608 to P614	
		PORT8	P800 to P809	P800, P801	
		PORT9	P900 to P902	Not Available	
			Refer to Manual for Additional Details	Refer to Manual for Additional Details	
	Port Control Register 1 (PCNTR1/PODR/PDR)	Input Only Port	P200, P214, P215	P200	20.2.1
		Reserved Bit	Bits 0, 14, 15	Bits 0, 16	
	Port Control Register 3 (PCNTR3/PORR/POSR)	Reserved Bit	Bits 0, 14, 15, 16, 30, 31	Bits 0, 16	20.2.3
	Port Control Register 4 (PCNTR4/EORR/EOSR)	Reserved Bit	Bits 0, 14, 15, 16, 30, 31	Bits 0, 16	20.2.4
	Port mn Pin Function Select Register (PmnPFS/PmnPFS_HA/PmnPFS_BY) (m = 0 to 8; n = 00 to 15)		DSCR - Port Drive Capability is Bit 10 Refer to Manual for Details	DSCR - Port Drive Capability is Bit 10, Bit 11 Refer to Manual for Details	20.2.5
	Ethernet Control Register (PFENET)		Does Not Exist	Exists	20.2.7
	Handling of Unused Pins		Refer to Manual	Refer to Manual	20.4
	I/O Buffer Specification		Refer to Manual	Refer to Manual	20.5.5

Table 5.13 Specification Difference (12 of 23)

SPECIFICATION			S3A7	S5D5	S5D5 HWM REFERENCE
Port Output Enable for GPT (POEG)	GPT Output Pins Disabled when they Detect a Dead Time Error		Not Available	Available	Table 20.1
	POEG Group n Setting Register (POEGGn) (n = A to D)	Bits [13:10]	Reserved	CDRE2 TO CDRE5 ACMP_HS Enable	22.2.1
General PWM Timer (GPT)	Functions	GPT32 Channels	10 Channels	6 Channels	Table 23.1 Table 23.2 Table 23.3
		GPT32E Channels (GPT32 Enhanced)	Not Available	4 Channels Min Resolution: 8.3 ns	
		GPT2EH Channels (GPT32 Enhanced High Resolution)	Not Available	4 Channels Min Resolution: 8.3 ns, Capable of Adjusting PWM Output Duty Cycle in 260 ps Increments	
		Generation of A/D Converter Start Triggers	Not Available	Available with GPT32E and GPT32EH Channels	
	Register Description		Refer to Manual	Refer to Manual	23.2
	Buffer Operation for GTPDBR, GTADTRA, GTADTBRA, GTADTDBRA, GTADTRB, GTADTBRB, GTADTDBRB		Not Available	Set by GTBER	23.3.2 23.3.2.3
	Buffer Operation for GTDVU, GTDBU, GTDBD		Not Available	Set by GTDTCR	23.3.2
	Automatic Dead Time Setting Function		Refer to Manual	Refer to Manual	23.3.4
	Interrupt Sources		Refer to Manual	Refer to Manual	23.4
	Event Signal Output to the ELC	GPTn_UDF (n = 0 to 13) GPTn_ADTRGA GPTn_ADTRGB (n = 0 to 7)	Not Available	Available	23.6.1
	Protection Function		Refer to Manual	Refer to Manual	23.8
	Priority Order of Each Event	GTADTRm (m = A, B) GTDVm (m = U, D)	Not Applicable	Applicable	23.9.5

Table 5.14 Specification Difference (13 of 23)

SPECIFICATION			S3A7	S5D5	S5D5 HWM REFERENCE
PWM Delay Generation Circuit	The Circuit Controls the Timing with which Signals on the Two PWM Output Pins for Channel 0/1/2/3 Rise and Fall to an Accuracy of up to 1/32 times the Period of the GPT Clock		Does Not Exist	Exists	Chapter 24
Asynchronous General-Purpose Timer (AGT)	Count Source	PCLKB, PCLKB/2	Not Available	Available	Table 25.1 25.2.5
	Interrupt/Event Link Function	Recovery from Software Standby Mode Using AGTI, AGTCMAI, AGTCMBI	Available	Not Available	Table 25.1
	I/O pins	AGTIO0, AGTIO1 Used as Input during AGT Operation Using VBATT Pin Voltage	Available	Not Available	Table 25.2
		AGTIO Used in Deep Software Standby Mode	Not Available	Available	
	AGT Counter Register (AGT)	AGTMR1 Register Setting	001B Refer to Manual for Details	001B or 011B Refer to Manual for Details	25.2.1
	AGT Mode Register 1 (AGTMR1)	Bit 6 to Bit 4 - TCK[2:0] Count Source	0 0 0: Reserved 0 0 1: PCLKB/8 0 1 1: Prohibited	0 0 0: PCLKB 0 0 1: PCLKB/8 0 1 1: PCLKB/2	25.2.5
		Set AGTSCLK or AGTLCLK as the Count Source	Running AGT in Software Standby Mode	Running AGT in Software Standby or Deep Software Standby Mode	
	AGT Pin Select Register (AGTIOSEL)		Refer to Manual	Refer to Manual	25.2.10
	Usage Notes When Count Source Clock Frequency is over 32 kHz		Applicable	Not Applicable	

Table 5.15 Specification Difference (14 of 23)

SPECIFICATION			S3A7	S5D5	S5D5 HWM REFERENCE
Realtime Clock (RTC)	Interrupts	Alarm Interrupt Periodic Interrupt	Returns From Software Standby Mode	Returns From Software Standby or Deep Software Standby Mode	Table 26.1
	Alarm Function	Condition in Deep Software Standby Mode	Not Applicable	The MCU Returns from the Deep Software Standby Mode even when the Alarm Interrupt Request is Disabled	26.3.6
Watchdog Timer (WDT)	ICU Event Link Setting Register n (IELSRn) Setting		Setting IELSRn.IELS[7:0] = 18h is Prohibited when Enabling WDT Reset Assertion (OFS0.WDTRSTIRQS = 0 or WDTRCR.RSTIRQS = 0)	Setting IELSRn.IELS[8:0] = 47h is Prohibited when Enabling WDT Reset Assertion (OFS0.WDTRSTIRQS = 1 or WDTRCR.RSTIRQS = 1)	27.5.1
Ethernet MAC Controller (ETHERC)	MCU Provides One Channel ETHERC Compliant with Ethernet or IEEE802.3 Media Access Control (MAC) Layer Protocol		Does Not Exist	Exists	Chapter 29
Ethernet DMA Controller (EDMAC)	MCU Provides One Channel for the EDMAC EDMAC Controls Data Transmission and Reception for ETHERC		Does Not Exist	Exists	Chapter 30
Ethernet DMA Controller (EDMAC)	MCU Provides One Channel for the EDMAC EDMAC Controls Data Transmission and Reception for ETHERC		Does Not Exist	Exists	Chapter 30

Table 5.16 Specification Difference (15 of 23)

SPECIFICATION			S3A7	S5D5	S5D5 HWM REFERENCE
USB 2.0 Full-Speed Module (USBFS)	MCU Supports Revision 1.2 of the Battery Charging Specification		Available	Not Available	
	Internal USB Transceiver Powered by USB LDO Regulator		Applicable	Not Applicable	
	Low Speed Transfer		1.5 Mbps	Not Available	
	System Configuration Control Register (SYSCFG)	Bit 3	DMRPU D-Line Resistor Control	Reserved	31.2.1
		Bit 8	CNEN - Single End Receiver Enable	Reserved	
	System Configuration Status Register 0 (SYSSTS0)	Bit 5	Reserved	SOFEA - Active Monitor When the Host Controller Is Selected	31.2.2
	Interrupt Enable Register 1 (INTENB1)	Bit 0	PDDETINTE0 PDDETINT0 Detection Interrupt Enable	Reserved	31.2.8
	Interrupt Status Register 1 (INTSTS1)	Bit 0	PDDETINT0 - PDDET0 Detection Interrupt Status	Reserved	31.2.14
	Device State Change Register (DVCHGR)		Does Not Exist	Exists	31.2.19
	USB Address Register (USBADDR)		Does Not Exist	Exists	31.2.20
	USB Module Control Register (USBMC)		Exists	Does Not Exist	
	BC Control Register 0 (USBBCCTRL0)		Exists	Does Not Exist	
	PHY Cross Point Adjustment Register (PHYSLEW)		Does Not Exist	Exists	31.2.36
	Deep Software Standby USB Transceiver Control/Pin Monitor Register (DPUSR0R)		Does Not Exist	Exists	31.2.37
	Deep Software Standby USB Suspend/Resume Interrupt Register (DPUSR1R)		Does Not Exist	Exists	31.2.38
	Operation		Refer to Manual	Refer to Manual	31.3.1
	Portable Device Detection Interrupt		Exists	Does Not Exist	
	Battery Charging Detection Processing		Available	Not Available	

Table 5.17 Specification Difference (16 of 23)

SPECIFICATION			S3A7	S5D5	S5D5 HWM REFERENCE
Serial Communications Interface (SCI)	Event Link function	SCIn_ERI, SCIn_RXI, SCIn_TXI, SCIn_TEI, SCIn_AM	n = 0 to 9	n = 0 to 4, 9	Table 32.1
	I/O Pins		Refer to Manual	Refer to Manual	Table 32.2
	SCI Initialization		Refer to Manual	Refer to Manual	32.6.5
I2C Bus Interface (IIC)	Transfer Rate		400 Kbps	1 Mbps	Table 34.1
	I2C Bus Mode Register 2 (ICMR2)	Data Enable/Acknowledge Enable Time for 1 Mbps Speed	Not Applicable	450 ns	34.2.4
	I2C Bus Function Enable Register (ICFER)	Bit 7	Reserved	FMPE Fast-Mode Plus Enable	34.2.6
	I2C-Bus Wakeup Unit Register 2 (ICWUR2)		Reserved	Refer to Manual	34.2.12 34.15
	I2C Bus Bit Rate Low-Level Register (ICBRL)	Data Setup Time for 1 Mbps Speed	Not Applicable	50 ns	34.2.15
Controller Area Network (CAN)	I/O Pins	CRX1, CTX1	Does Not Exist	Exists	35.1
	Interrupt Generator	CAN1 Reception Complete CAN1 Transmission Complete CAN1 Receive FIFO CAN1 Transmit FIFO CAN1 Error	Does Not Exist Refer to Manual for Details	Exists Refer to Manual for Details	35.1 35.8
	Settings for the Operating Clock	PCLKA:PCLKB	2:1 Operation Not Guaranteed for Other Settings	No Such Condition	35.9.2

Table 5.18 Specification Difference (17 of 23)

SPECIFICATION			S3A7	S5D5	S5D5 HWM REFERENCE
Serial Peripheral Interface (SPI)	Bit rate	Slave Mode Max RSPCK Frequency	PCLK/6	PCLK/4	Table 36.1
		Slave Mode Width at High/Low Level	3 PCLKA Cycles	2 PCLKA Cycles	
	SPI Data Control Register (SPDCR)	Bit 6	Reserved	SPBYT - SPI Byte Access Specification	36.2.9
	SPI Data Control Register 2 (SPDCR2)		Does Not Exist	Exists	36.2.15
Quad Serial Peripheral Interface (QSPI)	SPI Bus Reference Cycles	Relationship Among SFMDV[4:0] Bits, Cycle Multiplier, and Serial Clock Frequencies	Refer to Manual	Refer to Manual	Table 37.3
Cyclic Redundancy Check (CRC) Calculator	Snoop Address Register (CRCSAR)	Bit 13 to Bit 0 CRCSA[13:0]	Refer to Manual	Refer to Manual	38.2.5
Serial Sound Interface Enhanced (SSIE)	Transmit and Receive Audio Data to and from Various Devices that Support Different Audio Data Formats		Refer to Manual	Refer to Manual	Chapter 39
Sampling Rate Converter (SRC)	Used to Convert the Sampling Rate of Data Produced by Various Audio Decoders		Does Not Exist	Refer to Manual	Chapter 40

Table 5.19 Specification Difference (18 of 23)

SPECIFICATION			S3A7	S5D5	S5D5 HWM REFERENCE
SD/MMC Host Interface (SDHI)	SD and MMC Shared	Interrupt Sources Card Access Interrupt (SDHI_MMCn_ACCS) SDIO Access Interrupt (SDHI_MMCn_SDIO) Card Detection Interrupt (SDHI_MMCn_CARD)	n = 0	n = 0, 1	Table 41.1
	I/O Pins	Channel 1	Does Not Exist	Exists	Table 41.2
	SD Card Interrupt Flag Register 1 (SD_INFO1)	Bit 3	Reserved	SDCDRM SDnCD Removal Flag	41.2.10
		Bit 4	Reserved	SDCDIN SDnCD Insertion Flag	
		Bit 5	Reserved Value After Reset is 1	SDCDMON SDnCD Pin Monitor Flag Value After Reset is Undefined	
	SD INFO1 Interrupt Mask Register (SD_INFO1_MASK)	Bit 3	Reserved	SDCDRMM SDnCD Removal Interrupt Request Mask	41.2.12
		Bit 4	Reserved	SDCDINM SDnCD Insertion Interrupt Request Mask	
	SD Card Access Control Option Register (SD_OPTION)	Bit 3 to Bit 0	Reserved	CTOP[3:0] Card Detection Time Counter	41.2.16
	SDIO Interrupt Flag Register (SDIO_INFO1)	Bit 1, Bit 2	Write Value is 1	Write Value is 0	41.2.21
		Bit 13 to Bit 3 Bit 31 to Bit 16	Read Only	Write Value is 0	
	Card Detect		Refer to Manual	Refer to Manual	41.3.2.1

Table 5.20 Specification Difference (19 of 23)

SPECIFICATION			S3A7	S5D5	S5D5 HWM REFERENCE
Parallel Data Capture Unit (PDC)	Communicates with External I/O Devices		Does Not Exist	Refer to Manual	Chapter 42
Boundary Scan	Usage Notes	BDSL Needs to be Configured	No	Yes	43.4
		Pins that Cannot be Boundary-Scanned	Mode Signal (MD)	VCL0, VREFH0, VREFL0, VREFH, VREFL	
Secure Cryptographic Engine (SCE)	Provide Security Functions such as Access Management Circuit, Encryption Engine and Random Number Generator		Uses SCE5	Uses SCE7	Chapter 44
	Security Algorithm	Symmetric Algorithm	AES	AES, 3DES, ARC4	
		Asymmetric Algorithm	Not Available	RSA, DSA	
	Additional Features	Hash-Value Generation	GHASH	SHA1, SHA224, SHA256, GHASH	
12-Bit A/D Converter (ADC12)	Provides Successive Approximation A/D Converter		Refer to Manual	Refer to Manual	Chapter 45

Table 5.21 Specification Difference (20 of 23)

SPECIFICATION			S3A7	S5D5	S5D5 HWM REFERENCE
12-Bit D/A Converter (DAC12)	D/A Output Amplifier Control Function		Does Not Exist	Exists	Table 46.1 46.6.5
	D/A Control Register (DACR)	Bit 5	Reserved	DAE D/A Enable	46.2.2
	D/A VREF Control Register (DAVREFCR)		Exists	Does Not Exist	
	D/A Output Amplifier Control Register (DAAMPCR)		Does Not Exist	Exists	46.2.5
	D/A Amplifier Stabilization Wait Control Register (DAASWCR)		Does Not Exists	Exists	46.2.6
	D/A A/D Synchronous Unit Select Register (DAADUSR)		Does Not Exists	Exists	46.2.7
	Synchronization of DAC12 and ADC12	Set DAADUSR.AMADSEL1 = 1b	DAADUSR Does Not Exist	Exists	46.3.1
	Notes on Using the Internal Reference Voltage as the Reference Voltage		Exists	Does Not Exist	
	Usage Notes on Event Link Operation	Do Not Use the Amplifier Output Function Set DACR.DAE = 0b	Not Applicable	Applicable	46.5

Table 5.22 Specification Difference (21 of 23)

SPECIFICATION			S3A7	S5D5	S5D5 HWM REFERENCE
Temperature Sensor (TSN)	Used to Determine and Monitor the Die Temperature for Reliable Operation of the Device		Refer to Manual	Refer to Manual	Chapter 47
Operational Amplifier (OPAMP)	Used to Amplify Small Analog Input Voltages and Output the Amplified Voltages		Exists	Does Not Exist	
High-Speed Analog Comparator (ACMPHS)	Used to Compare a Test Voltage with a Reference Voltage and to Provide a Digital Output Based on the Result of Conversion		Refer to Manual	Refer to Manual	Chapter 48
Low Power Analog Comparator (ACMPLP)	Compares a Reference Input Voltage and an Analog Input Voltage		Exists	Does Not Exist	
SRAM	Capacity	Without ECC	SRAM0: 112 KB SRAM1: 64 KB	SRAM0: 224 KB	Table 47.1
		With ECC	SRAM0: 16 KB	SRAM0: 32 KB	
		SRAMHS	Does Not Exist	128 KB	
	Access		0 Wait	Based on ICLK Frequency Refer to Manual for Details	
	Data Retention		Not Available	Available	
	Error Checking	With ECC	1-bit Error Correction and Up to 2-bit Error Detection	Up to 2-bit errors	
	SRAM Wait State Control Register (SRAMWTSC)		Does Not Exist	Exists	51.2.3
	ECC 1-Bit Error Information Update Enable Register (ECC1STSEN)		No Such Condition	Bit 0 - E1STSEN Set to 1 when the ECC Function is Enabled	51.2.6
	ECC Protection Register 2 (ECCPRCR2)		Exists	Does Not Exist	
	Low-Power Functions		Refer to Manual	Refer to Manual	51.3.1
	Access Cycles		Refer to Manual	Refer to Manual	51.3.7
	Store Buffer of SRAM		Does Not Exist	Exists	51.4.3

Table 5.23 Specification Difference (22 of 23)

SPECIFICATION			S3A7	S5D5	S5D5 HWM REFERENCE
Standby SRAM	An on-chip SRAM is provided to retain data in Deep Software Standby Mode		Does Not Exist	Exists	Chapter 52
Flash Memory	Capacity		Code Flash: 1 MB Data Flash: 16 KB	Code Flash: 1 MB Data Flash: 32 KB	Table 53.1
	Read cycle	Code Flash	32 MHz < ICLK ≤ 48 MHz: Cache hit: 1 cycle Cache miss: 2, 3 cycles ICLK ≤ 32 MHz: Cache hit: 1 cycle Cache miss: 1 cycle	80 MHz < ICLK ≤ 120 MHz: Cache hit: 1 cycle Cache miss: 3 cycles 40 MHz < ICLK ≤ 80 MHz: Cache hit: 1 cycle Cache miss: 2 cycles ICLK ≤ 40 MHz: Cache hit: 1 cycle Cache miss: 1 cycle	
		Data Flash	A Read Operation Takes 6 cycles of FCLK in Bytes (FCLK Frequency is 32 MHz)	A read operation takes 7 cycles of FCLK in words or bytes (FCLK frequency is up to 60 MHz)	
	Value After Erasure	Data Flash	FFh	Undefined	
	Programming/Erasing Method	Handled Through FCB Commands Specified in Registers	Handled Through FACI Commands Specified in FACI Command Issuing Area (407E 0000h)	Programming/Erasing Method	
	Units of Programming	Code Flash	64 Bit	128 Byte	
		Data Flash	8 Bit	4/8/16 Byte	
		Data Flash	8 Bit	4/8/16 Byte	

Table 5.24 Specification Difference (23 of 23)

SPECIFICATION			S3A7	S5D5	S5D5 HWM REFERENCE
Flash Memory (Continued)	Units of Erasure	Code Flash	64 Bit	128 Byte	Table 53.1
		Data Flash	8 Bit	4/8/16 Byte	
	Background operations (BGOs)	Data Flash Memory can be Read during Code Flash Memory Programming	Not Available	Available	
	Operation	Setup Flash Cache and Prepare to Rewrite Flash Memory	Refer to Manual	Refer to Manual	53.4
	All Other Differences		Refer to Manual	Refer to Manual	Chapter 53
Internal Voltage Regulator	Does Not Supply Voltage to the Internal Circuits and Memory		I/O, Analog Domain	I/O, Analog, USB, Battery Backup Power Domain	54.1
	LDO Mode Pins Setting Description	VCL Pin	Connect VCL Pin to VSS Through a 4.7-µF Multilayer Ceramic Capacitor. VCL0 Pin Not Available	Connect Each Pin to VSS Through a 0.1-µF Multilayer Ceramic Capacitor	Table 54.1
Electrical Characteristics			Refer to Manual	Refer to Manual	Chapter 55

6. Port Select Function Difference

Appendix A and B include tables that compare the PSEL, ASEL, and ISEL functions for the S3A7 MCU Group and S5D5 MCU Group, respectively. For each port number, the first row specifies the bitwise select values. The second row specifies the functionality enabled by the select values on the S3A7 MCU Group. The third column specifies the functionality enabled by the select values on the S5D5. Differences in functionality are notated with bold text and highlighted background. The comments section provides additional details or specifies the migration type from S3A7 MCU Group to S5D5 MCU Group. For more information on the comments column, refer to the following Typography Notation table.

Note: Some pin names have the added suffix of _A, _B, _C, _D, _E and _F. When assigning the GPT, IIC, SPI, SSIE, ETHERC (RMII), SDHI, and GLCDC functionality, select the functional pins with the same suffix. The other pins can be selected regardless of the suffix. **Assigning the same function to two or more pins simultaneously is prohibited.**

The following typographic notation is used for the pin differences sections of the document to denote the changes happening at the individual ports:

Example	Description
▲PIXD0_B	The '▲' denotes that signal PIXD0_B is being added to the previously unused/reserved or replacing a deprecated function.
▼ET1_TX_CLK	The '▼' denotes that signal ET1_TX_CLK is being deprecated at the bit position and being replaced by a new signal or remain unused/reserved.

The following gradients visualize whether signals are added, replaced, or removed from the Synergy S3A7 MCU and S5D5 MCU Group**.**

Example	Description
	Highlights a bit position where a new function is being added to the previously unused/reserved bit position.
	Highlights a bit position where a new function is replacing an existing function in the bit position.
	Highlights a bit position it is being reserved by deprecating the function that existed at that bit position.

Appendix A 100 Pin Package

Table A 100-Pin Package Difference (1 of 14)

PORT	MCU	SELECT								COMMENTS
P000		PSEL 01100B	ASEL ADC	ASEL CMP	ISEL					▲IVCMP2, ▲IRQ6DS, ▼TS21, ▼IVREF0, ▼IVCMP0
	S3A7	TS21	AN000	IVREF0/IVCMP0	IRQ6					
	S5D5	-	AN000	IVCMP2	IRQ6DS					
P001		PSEL 01100B	ASEL ADC	ASEL CMP	ISEL					▲IVCMP2, ▲IRQ7DS, ▼TS22, ▼IVREF1, ▼IVCMP1
	S3A7	TS22	AN001	IVREF1/IVCMP1	IRQ7					
	S5D5	-	AN001	IVCMP2	IRQ7DS					
P002		ASEL ADC	ASEL CMP	ISEL						▲IRQ8DS ▼IVREF2 ▼IVREF2/IVCMP2 ▼IRQ8
	S3A7	AN002	IVREF2/IVCMP2	IRQ8						
	S5D5	AN002	IVCMP2	IRQ8DS						
P003		ASEL ADC	ASEL CMP							▲AN007, ▼AN003, ▼IVREF3, ▼IVCMP3
	S3A7	AN003	IVREF3/IVCMP3							
	S5D5	AN007	-							
P004		ASEL ADC	ASEL CMP	ISEL						▲AN100 ▲IVCMP2 ▲IRQ9DS ▼AN004 ▼IVCMP0
	S3A7	AN004	IVCMP0	IRQ9						
	S5D5	AN100	IVCMP2	IRQ9DS						
P005		PSEL 01100B	ASEL ADC	ASEL CMP	ISEL					▲AN101 ▲IVMP2 ▲IRQ10DS ▼TS26 ▼AN005 ▼IVREF0
	S3A7	TS26	AN005	IVREF0	IRQ10					
	S5D5	-	AN101	IVCMP2	IRQ10DS					
P006		PSEL 01100B	ASEL ADC	ASEL CMP	ISEL					▲AN102 ▲IVCMP2 ▲IRQ11DS ▼TS27 ▼AN006 ▼IVREF1
	S3A7	TS27	AN006	IVREF4/IVREF1	IRQ11					
	S5D5	-	AN102	IVCMP2	IRQ11DS					

Table A 100 Pin Package Difference (2 of 14)

PORT	MCU	SELECT								COMMENTS
P007		ASEL ADC	ASEL CMP							▲AN107 ▼AN007 ▼IVCMP4 ▼IVCMP1
	S3A7	AN007	IVCMP4/IVCMP1							
	S5D5	AN107	-							
P008		PSEL 01100B	ASEL ADC	ISEL						▲AN003 ▲IRQ12DS ▼TS29 ▼AN008
	S3A7	TS29	AN008	IRQ12						
	S5D5	-	AN003	IRQ12DS						
P010/VREFH0		PSEL 01100B	ASEL ADC	ISEL						▼TS30 ▼AN010 ▼IRQ14
	S3A7	TS30	AN010	IRQ14						
VREFH0	S5D5	-	-	-						
P011/VREFL0		PSEL 01100B	ASEL ADC	ISEL						▼TS31 ▼AN011 ▼IRQ15
	S3A7	TS31	AN011	IRQ15						
VREFL0	S5D5	-	-	-						
P012/VREFH		ASEL ADC								▼AN012
	S3A7	AN012								
VREFH	S5D5	-								
P013/VREFL		ASEL ADC								▼AN013
	S3A7	AN013								
VREFL	S5D5	-								
P014		ASEL ADC	ASEL CMP	ASEL DA						▲AN005 ▲AN105 ▲IVREF3 ▼AN014 ▼IVREF5 ▼IVREF2
	S3A7	AN014	IVREF5/IVREF2	DA0						
	S5D5	AN005/AN105	IVREF3	DA0						
P015		ASEL ADC	ASEL CMP	ASEL DA	ISEL					▲AN006 ▲AN106 ▲IVCMP1 ▼AN015 ▼IVCMP5 ▼IVCMP2
	S3A7	AN015	IVCMP5/IVCMP2	DA1	IRQ13					
	S5D5	AN006/AN106	IVCMP1	DA1	IRQ13					

Table A 100 Pin Package Difference (3 of 14)

PORT	MCU	SELECT								COMMENTS
P100		PSEL 00001B	PSEL 00010B	PSEL 00011B	PSEL 00100B	PSEL 00101B	PSEL 00110B	PSEL 00111B	PSEL 01000B	▲GTIOC5B ▲DQ0 ▼AN027 ▼CMPIN0
	S3A7	AGTIO0	GTETRGA	-	RXD0	SCK1	MISOA	SCL1	KR00	
	S5D5	AGTIO0	GTETRGA	GTIOC5B	RXD0	SCK1	MISOA	SCL1	KR00	
		PSEL 01011B	ASEL ADC	ASEL CMP	ISEL					
	S3A7	D0	AN027	CMPIN0	IRQ2					
	S5D5	D0/DQ0	-	-	IRQ2					
P101		PSEL 00001B	PSEL 00010B	PSEL 00011B	PSEL 00100B	PSEL 00101B	PSEL 00110B	PSEL 00111B	PSEL 01000B	▲GTIOC5A ▲DQ1 ▼AN026 ▼CMPREF0
	S3A7	AGTEE0	GTETRGB	-	TXD0	CTS1	MOSIA	SDA1	KR01	
	S5D5	AGTEE0	GTETRGB	GTIOC5A	TXD0	CTS1	MOSIA	SDA1	KR01	
		PSEL 01011B	ASEL ADC	ASEL CMP	ISEL					
	S3A7	D1	AN026	CMPREF0	IRQ1					
	S5D5	D1/DQ1	-	-	IRQ1					
P102		PSEL 00001B	PSEL 00010B	PSEL 00011B	PSEL 00100B	PSEL 00110B	PSEL 01000B	PSEL 01010B	PSEL 01011B	▲DQ2 ▲CRX0 ▼AN025 ▼CMPIN1
	S3A7	AGTO0	GTOWLO	GTIOC2B	SCK0	RSPCKA	KR02	ADTRG0	D2	
	S5D5	AGTO0	GTOWLO	GTIOC2B	SCK0	RSPCKA	KR02	ADTRG0	D2/DQ2	
		PSEL 10000B	ASEL ADC	ASEL CMP						
	S3A7	-	AN025	CMPIN1						
	S5D5	CRX0	-	-						
P103		PSEL 00010B	PSEL 00011B	PSEL 00100B	PSEL 00110B	PSEL 01000B	PSEL 01011B	PSEL 10000B	ASEL ADC	▲DQ3 ▲CTX0 ▼AN024 ▼CMPREF1
	S3A7	GTOWUP	GTIOC2A	CTS0	SSLA0	KR03	D3	-	AN024	
	S5D5	GTOWUP	GTIOC2A	CTS0	SSLA0	KR03	D3/DQ3	CTX0	-	
		ASEL CMP								
	S3A7	CMPREF1								
	S5D5	-								

Table A 100 Pin Package Difference (4 of 14)

PORT	MCU	SELECT								COMMENTS
P104		PSEL 00010B	PSEL 00011B	PSEL 00100B	PSEL 00110B	PSEL 01000B	PSEL 01011B	ISEL		▲GTIOC1B ▲RXD8 ▲DQ4
	S3A7	GTETRGB	-	-	SSLA1	KR04	D4	IRQ1		
	S5D5	GTETRGB	GTIOC1B	RXD8	SSLA1	KR04	D4/DQ4	IRQ1		
P105		PSEL 00010B	PSEL 00011B	PSEL 00100B	PSEL 00110B	PSEL 01000B	PSEL 01011B	ISEL		▲GTIOC1A ▲TXD8 ▲DQ5
	S3A7	GTETRGA	-	-	SSLA2	KR05	D5	IRQ0		
	S5D5	GTETRGA	GTIOC1A	TXD8	SSLA2	KR05	D5/DQ5	IRQ0		
P106		PSEL 00001B	PSEL 00011B	PSEL 00100B	PSEL 00110B	PSEL 01000B	PSEL 01011B			▲AGTOB0 ▲SCK8 ▲DQ6
	S3A7	-	GTIOC8B	-	SSLA3	KR06	D6			
	S5D5	AGTOB0	GTIOC8B	SCK8	SSLA3	KR06	D6/DQ6			
P107		PSEL 00001B	PSEL 00011B	PSEL 00100B	PSEL 01000B	PSEL 01011B				▲AGTOB0 ▲CTS8 ▲DQ7
	S3A7	-	GTIOC8A	-	KR07	D7				
	S5D5	AGTOA0	GTIOC8A	CTS8	KR07	D7/DQ7				
P108		PSEL 00000B	PSEL 00010B	PSEL 00011B	PSEL 00101B	PSEL 00110B				▲GTOULO
	S3A7	TMS/SWDIO	-	GTIOC0B	CTS9	SSLB0				
	S5D5	TMS/SWDIO	GTOULO	GTIOC0B	CTS9	SSLB0				
P109		PSEL 00000B	PSEL 00010B	PSEL 00011B	PSEL 00101B	PSEL 00110B	PSEL 01001B	PSEL 10000B		▲CTX1
	S3A7	TDO/TRACESWO	GTOVUP	GTIOC1A	TXD9	MOSIB	CLKOUT	-		
	S5D5	TDO/TRACESWO	GTOVUP	GTIOC1A	TXD9	MOSIB	CLKOUT	CTX1		
P110		PSEL 00000B	PSEL 00010B	PSEL 00011B	PSEL 00100B	PSEL 00101B	PSEL 00110B	PSEL 01001B	PSEL 10000B	▲CRX1
	S3A7	TDI	GTOVLO	GTIOC1B	CTS2	RXD9	MISOB	VCOUT	-	
	S5D5	TDI	GTOVLO	GTIOC1B	CTS2	RXD9	MISOB	VCOUT	CRX1	
		ISEL								
	S3A7	IRQ3								
	S5D5	IRQ3								

Table A 100 Pin Package Difference (5 of 14)

PORT	MCU	SELECT								COMMENTS
P111		PSEL 00010B	PSEL 00011B	PSEL 00100B	PSEL 00101B	PSEL 00110B	PSEL 01011B	ISEL		▲HRMON0 ▼A5
	S3A7	-	GTIOC3A	SCK2	SCK9	RSPCKB	A5	IRQ4		
	S5D5	HRMON0	GTIOC3A	SCK2	SCK9	RSPCKB	-	IRQ4		
P112		PSEL 00010B	PSEL 00011B	PSEL 00100B	PSEL 00101B	PSEL 00110B	PSEL 01011B	PSEL 10010B		▲HRMON1 ▼A4
	S3A7	-	GTIOC3B	TXD2	-	-	A4	SSISCK0		
	S5D5	HRMON1	GTIOC3B	TXD2	SCK1	SSLB0	-	SSISCK0		
P113		PSEL 00011B	PSEL 00100B	PSEL 01011B	PSEL 10010B					▲GTIOC2A ▼A3
	S3A7	-	RXD2	A3	SSIWS0					
	S5D5	GTIOC2A	RXD2	-	SSIWS0					
P114		PSEL 00011B	PSEL 01011B	PSEL 10010B						▲GTIOC2B ▼A2
	S3A7	-	A2	SSIRXD0						
	S5D5	GTIOC2B	-	SSIRXD0						
P115		PSEL 00011B	PSEL 01011B	PSEL 10010B						▲GTIOC4A ▼A1
	S3A7	-	A1	SSITXD0						
	S5D5	GTIOC4A	-	SSITXD0						
P202		PSEL 00011B	PSEL 00100B	PSEL 00101B	PSEL 00110B	PSEL 01011B	PSEL 10000B	PSEL 10101B	PSEL 10110B	▲ET0_ERXD2 ▲IRQ3DS
	S3A7	GTIOC5B	SCK2	RXD9	MISOB	WR1/BC1	CRX0	SD0DAT6	-	
	S5D5	GTIOC5B	SCK2	RXD9	MISOB	WR1/BC1	CRX0	SD0DAT6	ET0_ERXD2	
		ISEL								
	S3A7	IRQ3								
	S5D5	IRQ3DS								

Table A 100 Pin Package Difference (6 of 14)

PORT	MCU	SELECT								COMMENTS
P203		PSEL 00011B	PSEL 00100B	PSEL 00101B	PSEL 00110B	PSEL 01011B	PSEL 01100B	PSEL 10000B	PSEL 10101B	▲ET0_COL ▲IRQ2DS
	S3A7	GTIOC5A	CTS2	TXD9	MOSIB	A19	TSCAP	CTX0	SD0DAT5	
	S5D5	GTIOC5A	CTS2	TXD9	MOSIB	A19	TSCAP	CTX0	SD0DAT5	
		PSEL 10110B	ISEL							
	S3A7	-	IRQ2							
	S5D5	ET0_COL	IRQ2DS							
P204		PSEL 00001B	PSEL 00010B	PSEL 00011B	PSEL 00100B	PSEL 00101B	PSEL 00110B	PSEL 00111B	PSEL 01010B	▲USB_OVRCURB_ ADS ▲ET0_RX_DV
	S3A7	AGTIO1	GTIW	GTIOC4B	SCK4	SCK9	RSPCKB	SCL0	CACREF	
	S5D5	AGTIO1	GTIW	GTIOC4B	SCK4	SCK9	RSPCKB	SCL0	CACREF	
		PSEL 01011B	PSEL 01100B	PSEL 10010B	PSEL 10011B	PSEL 10101B	PSEL 10110B			
	S3A7	A18	TS0	SSISCK1	USB_OVRCURB	SD0DAT4	-			
	S5D5	A18	TS0	SSISCK0	USB_OVRCURB_ADS	SD0DAT4	ET0_RX_DV			
P205		PSEL 00001B	PSEL 00010B	PSEL 00011B	PSEL 00100B	PSEL 00101B	PSEL 00110B	PSEL 00111B	PSEL 01001B	▲SSIWS0 ▲USB_OVRCURA_ ADS ▲ET0_WOL ▲IRQ1DS
	S3A7	AGTO1	GTIV	GTIOC4A	TXD4	CTS9	SSLB0	SCL1	CLKOUT	
	S5D5	AGTO1	GTIV	GTIOC4A	TXD4	CTS9	SSLB0	SCL1	CLKOUT	
		PSEL 01011B	PSEL 01100B	PSEL 10010B	PSEL 10011B	PSEL 10101B	PSEL 10110B	PSEL 10111B	ISEL	
	S3A7	A16	TSCAP	SSIWS1	USB_OVRCURA	SD0DAT3	-	-	IRQ1	
	S5D5	A16	TSCAP	SSIWS0	USB_OVRCURA_ADS	SD0DAT3	ET0_WOL	ET0_WOL	IRQ1DS	
P206		PSEL 00010B	PSEL 00100B	PSEL 00110B	PSEL 00111B	PSEL 01011B	PSEL 01100B	PSEL 10010B	PSEL 10011B	▲SSIDATA0 ▲ET0_LINKSTA ▲IRQ0DS ▼SSIDATA1
	S3A7	GTIU	RXD4	SSLB1	SDA1	WAIT	TS1	SSIDATA1	USB_VBUSEN	
	S5D5	GTIU	RXD4	SSLB1	SDA1	WAIT	TS1	SSIDATA0	USB_VBUSEN	
		PSEL 10101B	PSEL 10110B	PSEL 10111B	ISEL					
	S3A7	SD0DAT2	-	-	IRQ0					
	S5D5	SD0DAT2	ET0_LINKSTA	ET0_LINKSTA	IRQ0DS					

Table A 100 Pin Package Difference (7 of 14)

PORT	MCU	SELECT								COMMENTS
		PSEL 00110B	PSEL 01011B	PSEL 01100B	PSEL 10001B					▲QSSL ▲TS2 ▲A17 ▲SSLB2
VCC_USB_LDO	S3A7	-	-	-	-					
P207	S5D5	SSLB2	A17	TS2	QSSL					
		PSEL 00001B	PSEL 00010B	PSEL 00011B	PSEL 00101B	ISEL				▲GTIOC0B
P212/EXTAL	S3A7	AGTEE1	GTETRGD	-	RXD1	IRQ3				
	S5D5	AGTEE1	GTETRGD	GTIOC0B	RXD1	IRQ3				
		PSEL 00000B	PSEL 00010B	PSEL 00011B	PSEL 00110B					▲GTOUUP
P300	S3A7	TCK/SWCLK	-	GTIOC0A	SSLB1					
	S5D5	TCK/SWCLK	GTOUUP	GTIOC0A	SSLB1					
		PSEL 00001B	PSEL 00010B	PSEL 00011B	PSEL 00100B	PSEL 00101B	PSEL 00110B	PSEL 01011B	ISEL	▲CTS9 ▲AGTIO0 ▼A6
P301	S3A7	-	GTOULO	GTIOC4B	RXD2	-	SSLB2	A6	IRQ6	
	S5D5	AGTIO0	GTOULO	GTIOC4B	RXD2	CTS9	SSLB2	-	IRQ6	
		PSEL 00010B	PSEL 00011B	PSEL 00100B	PSEL 00110B	PSEL 01011B	ISEL			▼A7
P302	S3A7	GTOUUP	GTIOC4A	TXD2	SSLB3	A7	IRQ5			
	S5D5	GTOUUP	GTIOC4A	TXD2	SSLB3	-	IRQ5			
		PSEL 00011B	PSEL 01011B							▼A8
P303	S3A7	GTIOC7B	A8							
	S5D5	GTIOC7B	-							
		PSEL 00010B	PSEL 00011B	PSEL 00100B	PSEL 01011B	ISEL				▲GTOWLO ▲RXD6 ▼A9
P304	S3A7	-	GTIOC7A	-	A9	IRQ9				
	S5D5	GTOWLO	GTIOC7A	RXD6		IRQ9				

Table A 100 Pin Package Difference (8 of 14)

PORT	MCU	SELECT								COMMENTS
P305		PSEL 00010B	PSEL 00100B	PSEL 01011B	PSEL 10001B	ISEL				▲GTOWUP ▲TXD6 ▲QSPCLK ▼A10
	S3A7	-	-	A10	-	IRQ8				
	S5D5	GTOWUP	TXD6	-	QSPCLK	IRQ8				
P306		PSEL 00010B	PSEL 00100B	PSEL 01011B	PSEL 10001B					▲GTOULO ▲SCK6 ▲A11 ▼QSSL
	S3A7	-	-	A11	-					
	S5D5	GTOULO	SCK6	-	QSSL					
P307		PSEL 00010B	PSEL 00100B	PSEL 01011B	PSEL 10001B					▲GTOUUP ▲CTS6 ▲QIO0 ▼A12
	S3A7	-	-	A12	-					
	S5D5	GTOUUP	CTS6	-	QIO0					
P400		PSEL 00001B	PSEL 00011B	PSEL 00100B	PSEL 00101B	PSEL 00111B	PSEL 01010B	PSEL 01100B	PSEL 10010B	▲AGTIO1 ▲SCK7 ▲ADTRG1 ▲ET0_WOL ▼TS20
	S3A7	-	GTIOC6A	SCK4	-	SCL0	-	TS20	AUDIO_CLK	
	S5D5	AGTIO1	GTIOC6A	SCK4	SCK7	SCL0	ADTRG1	-	AUDIO_CLK	
		PSEL 10110B	PSEL 10111B	ISEL						
	S3A7	-	-	IRQ0						
	S5D5	ET0_WOL	ET0_WOL	IRQ0						
P401		PSEL 00010B	PSEL 00011B	PSEL 00100B	PSEL 00101B	PSEL 00111B	PSEL 01100B	PSEL 10000B	PSEL 10110B	▲TXD7 ▲IRQ5DS ▲ET0_WOL ▼TS19
	S3A7	GTETRGA	GTIOC6B	CTS4	-	SDA0	TS19	CTX0	-	
	S5D5	GTETRGA	GTIOC6B	CTS4	TXD7	SDA0	-	CTX0	ET0_MDC	
		PSEL 10111B	ISEL							
	S3A7	-	IRQ5							
	S5D5	ET0_MDC	IRQ5DS							

Table A 100 Pin Package Difference (9 of 14)

PORT	MCU	SELECT								COMMENTS
P402		PSEL 00001B	PSEL 00101B	PSEL 01001B	PSEL 01010B	PSEL 01100B	PSEL 10000B	PSEL 10010B	PSEL 10110B	▲RXD7 ▲CACREF ▲AUDIO_CLK ▲ET0_MDIO ▲VSYNC ▲IRQ4DS ▼TS18
	S3A7	AGTIO0_B/AGTIO1	-	RTCIC0	-	TS18	CRX0	-	-	
	S5D5	AGTIO0_B/AGTIO1	RXD7	RTCIC0	CACREF	-	CRX0	AUDIO_CLK	ET0_MDIO	
		PSEL 10111B	PSEL 11000B	ISEL						
	S3A7	-	-	IRQ4						
	S5D5	ET0_MDIO	VSYNC	IRQ4DS						
P403		PSEL 00001B	PSEL 00011B	PSEL 00101B	PSEL 01001B	PSEL 01100B	PSEL 10010B	PSEL 10101B	PSEL 10110B	▲CTS7 ▲SD1DAT7 ▲ET0_LINKSTA ▲PIXD7 ▼TS17
	S3A7	AGTIO0_C/AGTIO1	GTIOC3A	-	RTCIC1	TS17	SSISCK0	-	-	
	S5D5	AGTIO0_C/AGTIO1	GTIOC3A	CTS7	RTCIC1	-	SSISCK0	SD1DAT7	ET0_LINKSTA	
		PSEL 10111B	PSEL 11000B							
	S3A7	-	-							
	S5D5	ET0_LINKSTA	PIXD7							
P404		PSEL 00011B	PSEL 01001B	PSEL 01100B	PSEL 10010B	PSEL 10101B	PSEL 10110B	PSEL 10111B	PSEL 11000B	▲SD1DAT6 ▲ET0_EXOUT ▲PIXD6 ▼TS16
	S3A7	GTIOC3B	RTCIC2	TS16	SSIWS0	-	-	-	-	
	S5D5	GTIOC3B	RTCIC2	-	SSIWS0	SD1DAT6	ET0_EXOUT	ET0_EXOUT	PIXD6	
P405		PSEL 00011B	PSEL 01100B	PSEL 10010B	PSEL 10101B	PSEL 10110B	PSEL 10111B	PSEL 11000B		▲SD1DAT5 ▲ET0_TX_EN ▲RMII0_TXD_EN ▲PIXD5 ▼TS15
	S3A7	GTIOC1A	TS15	SSITXD0	-	-	-	-		
	S5D5	GTIOC1A	-	SSITXD0	SD1DAT5	ET0_TX_EN	RMII0_TXD_EN	PIXD5		
P406		PSEL 00011B	PSEL 00110B	PSEL 01100B	PSEL 10010B	PSEL 10101B	PSEL 10110B	PSEL 10111B	PSEL 11000B	▲SSLB3 ▲SD1DAT4 ▲ET0_RX_ER ▲RMIIO_TXD1 ▲PIXD4 ▼TS14
	S3A7	GTIOC1B	-	TS14	SSIRXD0	-	-	-	-	
	S5D5	GTIOC1B	SSLB3	-	SSIRXD0	SD1DAT4	ET0_RX_ER	RMII0_TXD1	PIXD4	

Table A 100 Pin Package Difference (10 of 14)

PORT	MCU	SELECT								COMMENTS
		PSEL 00001B	PSEL 00100B	PSEL 00110B	PSEL 00111B	PSEL 01001B	PSEL 01010B	PSEL 01100B	PSEL 10011B	▲AGTIO0 ▲ET0_EXOUT
P407/USB_VBUS	S3A7	-	CTS4	SSLB3	SDA0	RTCOUT	ADTRG0	TS3	USB_VBUS	
P407	S5D5	AGTIO0	CTS4	SSLB3	SDA0	RTCOUT	ADTRG0	TS3	USB_VBUS	
		PSEL 10110B	PSEL 10111B							
P407/USB_VBUS	S3A7	-	-							
P407	S5D5	ET0_EXOUT	ET0_EXOUT							
P408		PSEL 00010B	PSEL 00011B	PSEL 00101B	PSEL 00111B	PSEL 01100B	PSEL 10011B	PSEL 10110B	PSEL 10111B	▲GTIOC10B ▲SCL0 ▲ET0_CRS ▲RMII0_CRS_DV ▲PIXCLK
	S3A7	GTOWLO	-	RXD3	-	TS4	USB_ID	-	-	
	S5D5	GTOWLO	GTIOC10B	RXD3	SCL0	TS4	USB_ID	ET0_CRS	RMII0_CRS_DV	
		PSEL 11000B	ISEL							
	S3A7	-	IRQ7							
	S5D5	PIXCLK	IRQ7							
P409		PSEL 00010B	PSEL 00011B	PSEL 00101B	PSEL 01100B	PSEL 10011B	PSEL 10110B	PSEL 10111B	PSEL 11000B	▲GTIOC10A ▲ET0_RX_CLK ▲RMII0_RX_ER ▲HSYNC
	S3A7	GTOWUP	-	TXD3	TS5	USB_EXICEN	-	-	-	
	S5D5	GTOWUP	GTIOC10A	TXD3	TS5	USB_EXICEN	ET0_RX_CLK	RMII0_RX_ER	HSYNC	
		ISEL								
	S3A7	IRQ6								
	S5D5	IRQ6								
P410		PSEL 00001B	PSEL 00010B	PSEL 00011B	PSEL 00100B	PSEL 00101B	PSEL 00110B	PSEL 01100B	PSEL 10101B	▲ET_ERXD0 ▲RMII0_RXD1 ▲PIXD0
	S3A7	AGTOB1	GTOVLO	GTIOC9B	RXD0	SCK3	MISOA	TS6	SD0DAT1	
	S5D5	AGTOB1	GTOVLO	GTIOC9B	RXD0	SCK3	MISOA	TS6	SD0DAT1	
		PSEL 10110B	PSEL 10111B	PSEL 11000B	ISEL					
	S3A7	-	-	-	IRQ5					
	S5D5	ET0_ERXD0	RMII0_RXD1	PIXD0	IRQ5					

Table A 100 Pin Package Difference (11 of 14)

PORT	MCU	SELECT								COMMENTS
P411		PSEL 00001B	PSEL 00010B	PSEL 00011B	PSEL 00100B	PSEL 00101B	PSEL 00110B	PSEL 01100B	PSEL 10101B	▲ET_ERXD1 ▲RMII0_RXD0 ▲PIXD1
	S3A7	AGTOA1	GTOVUP	GTIOC9A	TXD0	CTS3	MOSIA	TS7	SD0DAT0	
	S5D5	AGTOA1	GTOVUP	GTIOC9A	TXD0	CTS3	MOSIA	TS7	SD0DAT0	
		PSEL 10110B	PSEL 10111B	PSEL 11000B	ISEL					
	S3A7	-	-	-	IRQ4					
	S5D5	ET0_ERXD1	RMII0_RXD0	PIXD1	IRQ4					
P412		PSEL 00001B	PSEL 00010B	PSEL 00100B	PSEL 00110B	PSEL 01100B	PSEL 10101B	PSEL 10110B	PSEL 10111B	▲AGTEE1 ▲ET0_ETXD0 ▲REF50CK0 ▲PIXD2
	S3A7	-	GTOULO	SCK0	RSPCKA	TS8	SD0CMD	-	-	
	S5D5	AGTEE1	GTOULO	SCK0	RSPCKA	TS8	SD0CMD	ET0_ETXD0	REF50CK0	
		PSEL 11000B								
	S3A7	-								
	S5D5	PIXD2								
P413		PSEL 00010B	PSEL 00100B	PSEL 00110B	PSEL 01100B	PSEL 10101B	PSEL 10110B	PSEL 10111B	PSEL 11000B	▲ET0_ETXD1 ▲RMII0_TXD0 ▲PIXD3
	S3A7	GTOUUP	CTS0	SSLA0	TS9	SD0CLK	-	-	-	
	S5D5	GTOUUP	CTS0	SSLA0	TS9	SD0CLK	ET0_ETXD1	RMII0_TXD0	PIXD3	
P414		PSEL 00011B	PSEL 00110B	PSEL 01100B	PSEL 10101B	PSEL 10110B	PSEL 10111B	PSEL 11000B	ISEL	▲GTIOC0B ▲IRQ9 ▲ET0_RX_ER ▲RMII0_TXD1 ▲PIXD4
	S3A7	-	SSLA1	TS10	SD0WP	-	-	-	-	
	S5D5	GTIOC0B	SSLA1	TS10	SD0WP	ET0_RX_ER	RMII0_TXD1	PIXD4	IRQ9	
P415		PSEL 00011B	PSEL 00110B	PSEL 01100B	PSEL 10011B	PSEL 10101B	PSEL 10110B	PSEL 10111B	PSEL 11000B	▲GTIOC0A ▲USB_VBUSEN ▲SC0CD ▲ET0_TX_EN ▲RMII0_TXD_EN ▲PIXD5 ▲IRQ8
	S3A7	-	SSLA2	TS11	-	-	-	-	-	
	S5D5	GTIOC0A	SSLA2	TS11	USB_VBUSEN	SD0CD	ET0_TX_EN	RMII0_TXD_EN	PIXD5	
		ISEL								
	S3A7	-								
	S5D5	IRQ8								

Table A 100 Pin Package Difference (12 of 14)

PORT	MCU	SELECT								COMMENTS
P500		PSEL 00001B	PSEL 00010B	PSEL 00011B	PSEL 10001B	PSEL 10011B	PSEL 10101B	ASEL ADC	ASEL CMP	▲GTIOC11A ▲SD1CMD ▲IVREF0
	S3A7	AGTOA0	GTIU	-	QSPCLK	USB_VBUSEN	-	AN016	-	
	S5D5	AGTOA0	GTIU	GTIOC11A	QSPCLK	USB_VBUSEN	SD1CLK	AN016	IVREF0	
P501		PSEL 00001B	PSEL 00010B	PSEL 00011B	PSEL 00101B	PSEL 10001B	PSEL 10011B	PSEL 10101B	ASEL ADC	▲GTIOC11B ▲TXD5 ▲SD1CMD ▲AN116 ▲IVREF1 ▼AN017
	S3A7	AGTOB0	GTIV	-	-	QSSL	USB_OVRCURA	-	AN017	
	S5D5	AGTOB0	GTIV	GTIOC11B	TXD5	QSSL	USB_OVRCURA	SD1CMD	AN116	
		ASEL CMP	ISEL							
	S3A7	-	IRQ11							
	S5D5	IVREF1	IRQ11							
P502		PSEL 00010B	PSEL 00011B	PSEL 00101B	PSEL 10001B	PSEL 10011B	PSEL 10101B	ASEL ADC	ASEL CMP	▲GTIOC12A ▲RXD5 ▲SD1DAT0 ▲AN017 ▲IVCMP0 ▼AN018
	S3A7	GTIW	-	-	QIO0	USB_OVRCURB	-	AN018	-	
	S5D5	GTIW	GTIOC12A	RXD5	QIO0	USB_OVRCURB	SD1DAT0	AN017	IVCMP0	
		ISEL								
	S3A7	IRQ12								
	S5D5	IRQ12								
P503		PSEL 00010B	PSEL 00011B	PSEL 00100B	PSEL 00101B	PSEL 10001B	PSEL 10011B	PSEL 10101B	ASEL ADC	▲GTIOC12B ▲CTS6 ▲SCK5 ▲SDADAT1 ▲AN117 ▼AN019
	S3A7	GTETRGC	-	-	-	QIO1	USB_EXICEN	-	AN019	
	S5D5	GTETRGC	GTIOC12B	CTS6	SCK5	QIO1	USB_EXICEN	SD1DAT1	AN117	
P504		PSEL 00010B	PSEL 00011B	PSEL 00100B	PSEL 00101B	PSEL 01011B	PSEL 10001B	PSEL 10011B	PSEL 10101B	▲GTIOC13A ▲SCK6 ▲CTS5 ▲ALE ▲SD1DAT2 ▲AN018 ▼AN020
	S3A7	GTETRGD	-	-	-	-	QIO2	USB_ID	-	
	S5D5	GTETRGD	GTIOC13A	SCK6	CTS5	ALE	QIO2	USB_ID	SD1DAT2	
		ASEL ADC								
	S3A7	AN020								
	S5D5	AN018								

Table A 100 Pin Package Difference (13 of 14)

PORT	MCU	SELECT								COMMENTS
P505		PSEL 00011B	PSEL 00100B	PSEL 10001B	PSEL 10101B	ASEL ADC	ISEL			▲GTIOC13B ▲RXD6 ▲SD1DAT3 ▲AN118 ▼AN021
	S3A7	-	-	QIO3	-	AN021	IRQ14			
	S5D5	GTIOC13B	RXD6	QIO3	SD1DAT3	AN118	IRQ14			
P600		PSEL 00011B	PSEL 00101B	PSEL 01001B	PSEL 01010B	PSEL 01011B				▲GTIOC6B ▲SCK9 ▲CLKOUT ▲CACREF
	S3A7	-	-	-	-	RD				
	S5D5	GTIOC6B	SCK9	CLKOUT	CACREF	RD				
P601		PSEL 00011B	PSEL 00101B	PSEL 01011B						▲GTIOC6A ▲RXD9 ▲DQM0
	S3A7	-	-	WR/WR0						
	S5D5	GTIOC6A	RXD9	WR/WR0/DQM0						
P602		PSEL 00011B	PSEL 00101B	PSEL 01011B						▲GTIOC7B ▲TXD9 ▲SDCLK
	S3A7	-	-	BCLK						
	S5D5	GTIOC7B	TXD9	BCLK/SDCLK						
P603		PSEL 00011B	PSEL 00101B	PSEL 01011B						▲GTIOC7A ▲CTS9 ▲DQ13
	S3A7	-	-	D13						
	S5D5	GTIOC7A	CTS9	D13/DQ13						
P608		PSEL 00011B	PSEL 01011B							▲GTIOC4B ▲DQM1
	S3A7	-	A0/BC0							
	S5D5	GTIOC4B	A0/BC0/DQM1							
P609		PSEL 00011B	PSEL 01011B	PSEL 10000B						▲GTIOC5A ▲CKE ▲CTX1
	S3A7	-	CS1#	-						
	S5D5	GTIOC5A	CS1#/CKE	CTX1						
P610		PSEL 00011B	PSEL 01011B	PSEL 10000B						▲GTIOC5B ▲WE ▲CRX1
	S3A7	-	CS0#	-						
	S5D5	GTIOC5B	CS0#/WE	CRX1						

Table A 100 Pin Package Difference (14 of 14)

PORT	MCU	SELECT								COMMENTS
P708		PSEL 00101B	PSEL 00110B	PSEL 01010B	PSEL 01100B	PSEL 10010B	PSEL 10110B	PSEL 11000B	ISEL	▲AUDIO_CLK ▲ET0_ETXD3 ▲PCKO
	S3A7	RXD1	SSLA3	CACREF	TS12	-	-	-	IRQ11	
	S5D5	RXD1	SSLA3	CACREF	TS12	AUDIO_CLK	ET0_ETXD3	PCKO	IRQ11	

Appendix B 144 Pin Package

Table B 144 Pin Package Difference (1 of 18)

PORT	MCU	SELECT								COMMENTS
P000		PSEL 01100B	ASEL ADC	ASEL CMP	ISEL					▲IVCMP2, ▲IRQ6DS, ▼TS21, ▼IVREF0, ▼IVCMP0
	S3A7	TS21	AN000	IVREF0/IVCMP0	IRQ6					
	S5D5	-	AN000	IVCMP2	IRQ6DS					
P001		PSEL 01100B	ASEL ADC	ASEL CMP	ISEL					▲IVCMP2, ▲IRQ7DS, ▼TS22, ▼IVREF1, ▼IVCMP1
	S3A7	TS22	AN001	IVREF1/IVCMP1	IRQ7					
	S5D5	-	AN001	IVCMP2	IRQ7DS					
P002		ASEL ADC	ASEL CMP	ISEL						▲IRQ8DS ▼IVREF2
	S3A7	AN002	IVREF2/IVCMP2	IRQ8						
	S5D5	AN002	IVCMP2	IRQ8DS						
P003		ASEL ADC	ASEL CMP							▲AN007, ▼AN003, ▼IVREF3, ▼IVCMP3
	S3A7	AN003	IVREF3/IVCMP3							
	S5D5	AN007	-							
P004		ASEL ADC	ASEL CMP	ISEL						▲AN100 ▲IVCMP2 ▲IRQ9DS ▼AN004 ▼IVCMP0
	S3A7	AN004	IVCMP0	IRQ9						
	S5D5	AN100	IVCMP2	IRQ9DS						
P005		PSEL 01100B	ASEL ADC	ASEL CMP	ISEL					▲AN101 ▲IVMP2 ▲IRQ10DS ▼TS26 ▼AN005 ▼IVREF0
	S3A7	TS26	AN005	IVREF0	IRQ10					
	S5D5	-	AN101	IVCMP2	IRQ10DS					
P006		PSEL 01100B	ASEL ADC	ASEL CMP	ISEL					▲AN102 ▲IVCMP2 ▲IRQ11DS ▼TS27 ▼AN006 ▼IVREF1
	S3A7	TS27	AN006	IVREF4/IVREF1	IRQ11					
	S5D5	-	AN102	IVCMP2	IRQ11DS					

Table B 144 Pin Package Difference (2 of 18)

PORT	MCU	SELECT								COMMENTS
P007		ASEL ADC	ASEL CMP							▲AN107 ▼AN007 ▼IVCMP4 ▼IVCMP1
	S3A7	AN007	IVCMP4/IVCMP1							
	S5D5	AN107	-							
P008		PSEL 01100B	ASEL ADC	ISEL						▲AN003 ▲IRQ12DS ▼TS29 ▼AN008
	S3A7	TS29	AN008	IRQ12						
	S5D5	-	AN003	IRQ12DS						
P009		ASEL ADC	ISEL							▲AN004 ▲IRQ13DS ▼AN009
	S3A7	AN009	IRQ13							
	S5D5	AN004	IRQ13DS							
P010/VREFH0 VREFH0		PSEL 01100B	ASEL ADC	ISEL						▼TS30 ▼AN010 ▼IRQ14
	S3A7	TS30	AN010	IRQ14						
	S5D5	-	-	-						
P011/VREFL0 VREFL0		PSEL 01100B	ASEL ADC	ISEL						▼TS31 ▼AN011 ▼IRQ15
	S3A7	TS31	AN011	IRQ15						
	S5D5	-	-	-						
P012/VREFH VREFH		ASEL ADC								▼AN012
	S3A7	AN012								
	S5D5	-								
P013/VREFL VREFL		ASEL ADC								▼AN013
	S3A7	AN013								
	S5D5	-								
P014		ASEL ADC	ASEL CMP	ASEL DA						▲AN005 ▲AN105 ▲IVREF3 ▼AN014 ▼IVREF5 ▼IVREF2
	S3A7	AN014	IVREF5/IVREF2	DA0						
	S5D5	AN005/AN105	IVREF3	DA0						

Table B 144 Pin Package Difference (3 of 18)

PORT	MCU	SELECT								COMMENTS
P015		ASEL ADC	ASEL CMP	ASEL DA	ISEL					▲AN006 ▲AN106 ▲IVCMP1 ▼AN015 ▼IVCMP5 ▼IVCMP2
	S3A7	AN015	IVCMP5/IVCMP2	DA1	IRQ13					
	S5D5	AN006/AN106	IVCMP1	DA1	IRQ13					
P100		PSEL 00001B	PSEL 00010B	PSEL 00011B	PSEL 00100B	PSEL 00101B	PSEL 00110B	PSEL 00111B	PSEL 01000B	▲GTIOC5B ▲DQ0 ▼AN027 ▼CMPIN0
	S3A7	AGTIO0	GTETRGA	-	RXD0	SCK1	MISOA	SCL1	KR00	
	S5D5	AGTIO0	GTETRGA	GTIOC5B	RXD0	SCK1	MISOA	SCL1	KR00	
		PSEL 01011B	ASEL ADC	ASEL CMP	ISEL					
	S3A7	D0	AN027	CMPIN0	IRQ2					
	S5D5	D0/DQ0	-	-	IRQ2					
P101		PSEL 00001B	PSEL 00010B	PSEL 00011B	PSEL 00100B	PSEL 00101B	PSEL 00110B	PSEL 00111B	PSEL 01000B	▲GTIOC5A ▲DQ1 ▼AN026 ▼CMPREF0
	S3A7	AGTEE0	GTETRGB	-	TXD0	CTS1	MOSIA	SDA1	KR01	
	S5D5	AGTEE0	GTETRGB	GTIOC5A	TXD0	CTS1	MOSIA	SDA1	KR01	
		PSEL 01011B	ASEL ADC	ASEL CMP	ISEL					
	S3A7	D1	AN026	CMPREF0	IRQ1					
	S5D5	D1/DQ1	-	-	IRQ1					
P102		PSEL 00001B	PSEL 00010B	PSEL 00011B	PSEL 00100B	PSEL 00110B	PSEL 01000B	PSEL 01010B	PSEL 01011B	▲DQ2 ▲CRX0 ▼AN025 ▼CMPIN1
	S3A7	AGTO0	GTOWLO	GTIOC2B	SCK0	RSPCKA	KR02	ADTRG0	D2	
	S5D5	AGTO0	GTOWLO	GTIOC2B	SCK0	RSPCKA	KR02	ADTRG0	D2/DQ2	
		PSEL 10000B	ASEL ADC	ASEL CMP						
	S3A7	-	AN025	CMPIN1						
	S5D5	CRX0	-	-						

Table B 144 Pin Package Difference (4 of 18)

PORT	MCU	SELECT								COMMENTS
P103		PSEL 00010B	PSEL 00011B	PSEL 00100B	PSEL 00110B	PSEL 01000B	PSEL 01011B	PSEL 10000B	ASEL ADC	▲DQ3 ▲CTX0 ▼AN024 ▼CMPREF1
	S3A7	GTOWUP	GTIOC2A	CTS0	SSLA0	KR03	D3	-	AN024	
	S5D5	GTOWUP	GTIOC2A	CTS0	SSLA0	KR03	D3/DQ3	CTX0	-	
		ASEL CMP								
	S3A7	CMPREF1								
	S5D5	-								
P104		PSEL 00010B	PSEL 00011B	PSEL 00100B	PSEL 00110B	PSEL 01000B	PSEL 01011B	ISEL		▲GTIOC1B ▲RXD8 ▲DQ4
	S3A7	GTETRGB	-	-	SSLA1	KR04	D4	IRQ1		
	S5D5	GTETRGB	GTIOC1B	RXD8	SSLA1	KR04	D4/DQ4	IRQ1		
P105		PSEL 00010B	PSEL 00011B	PSEL 00100B	PSEL 00110B	PSEL 01000B	PSEL 01011B	ISEL		▲GTIOC1A ▲TXD8 ▲DQ5
	S3A7	GTETRGA	-	-	SSLA2	KR05	D5	IRQ0		
	S5D5	GTETRGA	GTIOC1A	TXD8	SSLA2	KR05	D5/DQ5	IRQ0		
P106		PSEL 00001B	PSEL 00011B	PSEL 00100B	PSEL 00110B	PSEL 01000B	PSEL 01011B			▲AGTOB0 ▲SCK8 ▲DQ6
	S3A7	-	GTIOC8B	-	SSLA3	KR06	D6			
	S5D5	AGTOB0	GTIOC8B	SCK8	SSLA3	KR06	D6/DQ6			
P107		PSEL 00001B	PSEL 00011B	PSEL 00100B	PSEL 01000B	PSEL 01011B				▲AGTOB0 ▲CTS8 ▲DQ7
	S3A7	-	GTIOC8A	-	KR07	D7				
	S5D5	AGTOA0	GTIOC8A	CTS8	KR07	D7/DQ7				
P108		PSEL 00000B	PSEL 00010B	PSEL 00011B	PSEL 00101B	PSEL 00110B				▲GTOULO
	S3A7	TMS/SWDIO	-	GTIOC0B	CTS9	SSLB0				
	S5D5	TMS/SWDIO	GTOULO	GTIOC0B	CTS9	SSLB0				
P109		PSEL 00000B	PSEL 00010B	PSEL 00011B	PSEL 00101B	PSEL 00110B	PSEL 01001B	PSEL 10000B		▲CTX1
	S3A7	TDO/TRACESWO	GTOVUP	GTIOC1A	TXD9	MOSIB	CLKOUT	-		
	S5D5	TDO/TRACESWO	GTOVUP	GTIOC1A	TXD9	MOSIB	CLKOUT	CTX1		

Table B 144 Pin Package Difference (5 of 18)

PORT	MCU	SELECT								COMMENTS
P110		PSEL 00000B	PSEL 00010B	PSEL 00011B	PSEL 00100B	PSEL 00101B	PSEL 00110B	PSEL 01001B	PSEL 10000B	▲CRX1
	S3A7	TDI	GTOVLO	GTIOC1B	CTS2	RXD9	MISOB	VCOUT	-	
	S5D5	TDI	GTOVLO	GTIOC1B	CTS2	RXD9	MISOB	VCOUT	CRX1	
		ISEL								
	S3A7	IRQ3								
	S5D5	IRQ3								
P111		PSEL 00010B	PSEL 00011B	PSEL 00100B	PSEL 00101B	PSEL 00110B	PSEL 01011B	ISEL		▲HRMON0 ▼A5
	S3A7	-	GTIOC3A	SCK2	SCK9	RSPCKB	A5	IRQ4		
	S5D5	HRMON0	GTIOC3A	SCK2	SCK9	RSPCKB	-	IRQ4		
P112		PSEL 00010B	PSEL 00011B	PSEL 00100B	PSEL 00101B	PSEL 00110B	PSEL 01011B	PSEL 10010B		▲HRMON1 ▼A4
	S3A7	-	GTIOC3B	TXD2	-	-	A4	SSISCK0		
	S5D5	HRMON1	GTIOC3B	TXD2	SCK1	SSLB0	-	SSISCK0		
P113		PSEL 00011B	PSEL 00100B	PSEL 01011B	PSEL 10010B					▲GTIOC2A ▼A3
	S3A7	-	RXD2	A3	SSIWS0					
	S5D5	GTIOC2A	RXD2	-	SSIWS0					
P114		PSEL 00011B	PSEL 01011B	PSEL 10010B						▲GTIOC2B ▼A2
	S3A7	-	A2	SSIRXD0						
	S5D5	GTIOC2B	-	SSIRXD0						
P115		PSEL 00011B	PSEL 01011B	PSEL 10010B						▲GTIOC4A ▼A1
	S3A7	-	A1	SSITXD0						
	S5D5	GTIOC4A	-	SSITXD0						

Table B 144 Pin Package Difference (6 of 18)

PORT	MCU	SELECT								COMMENTS
P202		PSEL 00011B	PSEL 00100B	PSEL 00101B	PSEL 00110B	PSEL 01011B	PSEL 10000B	PSEL 10101B	PSEL 10110B	▲ET0_ERXD2 ▲IRQ3DS
	S3A7	GTIOC5B	SCK2	RXD9	MISOB	WR1/BC1	CRX0	SD0DAT6	-	
	S5D5	GTIOC5B	SCK2	RXD9	MISOB	WR1/BC1	CRX0	SD0DAT6	ET0_ERXD2	
		ISEL								
	S3A7	IRQ3								
	S5D5	IRQ3DS								
P203		PSEL 00011B	PSEL 00100B	PSEL 00101B	PSEL 00110B	PSEL 01011B	PSEL 01100B	PSEL 10000B	PSEL 10101B	▲ET0_COL ▲IRQ2DS
	S3A7	GTIOC5A	CTS2	TXD9	MOSIB	A19	TSCAP	CTX0	SD0DAT5	
	S5D5	GTIOC5A	CTS2	TXD9	MOSIB	A19	TSCAP	CTX0	SD0DAT5	
		PSEL 10110B	ISEL							
	S3A7	-	IRQ2							
	S5D5	ET0_COL	IRQ2DS							
P204		PSEL 00001B	PSEL 00010B	PSEL 00011B	PSEL 00100B	PSEL 00101B	PSEL 00110B	PSEL 00111B	PSEL 01010B	▲USB_OVRCURB_ ADS ▲ET0_RX_DV
	S3A7	AGTIO1	GTIW	GTIOC4B	SCK4	SCK9	RSPCKB	SCL0	CACREF	
	S5D5	AGTIO1	GTIW	GTIOC4B	SCK4	SCK9	RSPCKB	SCL0	CACREF	
		PSEL 01011B	PSEL 01100B	PSEL 10010B	PSEL 10011B	PSEL 10101B	PSEL 10110B			
	S3A7	A18	TS0	SSISCK1	USB_OVRCURB	SD0DAT4	-			
	S5D5	A18	TS0	SSISCK0	USB_OVRCURB_ADS	SD0DAT4	ET0_RX_DV			
P205		PSEL 00001B	PSEL 00010B	PSEL 00011B	PSEL 00100B	PSEL 00101B	PSEL 00110B	PSEL 00111B	PSEL 01001B	▲SSIWS0 ▲USB_OVRCURA_ ADS ▲ET0_WOL ▲IRQ1DS
	S3A7	AGTO1	GTIV	GTIOC4A	TXD4	CTS9	SSLB0	SCL1	CLKOUT	
	S5D5	AGTO1	GTIV	GTIOC4A	TXD4	CTS9	SSLB0	SCL1	CLKOUT	
		PSEL 01011B	PSEL 01100B	PSEL 10010B	PSEL 10011B	PSEL 10101B	PSEL 10110B	PSEL 10111B	ISEL	
	S3A7	A16	TSCAP	SSIWS1	USB_OVRCURA	SD0DAT3	-	-	IRQ1	
	S5D5	A16	TSCAP	SSIWS0	USB_OVRCURA_ADS	SD0DAT3	ET0_WOL	ET0_WOL	IRQ1DS	

Table B 144 Pin Package Difference (7 of 18)

PORT	MCU	SELECT								COMMENTS
P206		PSEL 00010B	PSEL 00100B	PSEL 00110B	PSEL 00111B	PSEL 01011B	PSEL 01100B	PSEL 10010B	PSEL 10011B	▲SSIDATA0 ▲ET0_LINKSTA ▲IRQ0DS ▼SSIDATA1
	S3A7	GTIU	RXD4	SSLB1	SDA1	WAIT	TS1	SSIDATA1	USB_VBUSEN	
	S5D5	GTIU	RXD4	SSLB1	SDA1	WAIT	TS1	SSIDATA0	USB_VBUSEN	
		PSEL 10101B	PSEL 10110B	PSEL 10111B	ISEL					
	S3A7	SD0DAT2	-	-	IRQ0					
	S5D5	SD0DAT2	ET0_LINKSTA	ET0_LINKSTA	IRQ0DS					
VCC_USB_LDO P207		PSEL 00110B	PSEL 01011B	PSEL 01100B	PSEL 10001B					▲QSSL ▲TS2 ▲A17 ▲SSLB2
	S3A7	-	-	-	-					
	S5D5	SSLB2	A17	TS2	QSSL					
VCC(IO) P208		PSEL 00010B	PSEL 01011B	PSEL 10001B	PSEL 10101B	PSEL 10110B	PSEL 10111B	PSEL 11010B		▲GTOVLO ▲CS4# ▲QIO3 ▲SD0DAT0 ▲ETO_LINKSTA ▲TDATA3
	S3A7	-	-	-	-	-	-	-		
	S5D5	GTOVLO	CS4#	QIO3	SD0DAT0	ET0_LINKSTA	ET0_LINKSTA	TDATA3		
VSS(IO) P209		PSEL 00010B	PSEL 01011B	PSEL 10001B	PSEL 10101B	PSEL 10110B	PSEL 10111B	PSEL 11010B		▲GTOVUP ▲CS5# ▲QIO2 ▲SD0WP ▲ETO_EXOUT ▲TDATA2
	S3A7	-	-	-	-	-	-	-		
	S5D5	GTOVUP	CS5#	QIO2	SD0WP	ET0_EXOUT	ET0_EXOUT	TDATA2		
P902 P210		PSEL 00010B	PSEL 01011B	PSEL 10001B	PSEL 10101B	PSEL 10110B	PSEL 10111B	PSEL 11010B		▲GTIW ▲CS6# ▲QIO1 ▲SD0CD ▲ETO_WOL ▲TDATA1
	S3A7	-	-	-	-	-	-	-		
	S5D5	GTIW	CS6#	QIO1	SD0CD	ET0_WOL	ET0_WOL	TDATA1		
P901 P211		PSEL 00010B	PSEL 01011B	PSEL 10001B	PSEL 10101B	PSEL 10110B	PSEL 10111B	PSEL 11010B		▲GTIV ▲CS7# ▲QIO0 ▲SD0CMD ▲ETO_MDIO ▲TDATA0
	S3A7	-	-	-	-	-	-	-		
	S5D5	GTIV	CS7#	QIO0	SD0CMD	ET0_MDIO	ET0_MDIO	TDATA0		
P212/EXTAL		PSEL 00001B	PSEL 00010B	PSEL 00011B	PSEL 00101B	ISEL				▲GTIOC0B
	S3A7	AGTEE1	GTETRGD	-	RXD1	IRQ3				
	S5D5	AGTEE1	GTETRGD	GTIOC0B	RXD1	IRQ3				

Table B 144 Pin Package Difference (8 of 18)

PORT	MCU	SELECT								COMMENTS
P213/XTAL		PSEL 00010B	PSEL 00011B	PSEL 00101B	PSEL 01010B	ISEL				▲GTIOC0A ▲ADTRG1
	S3A7	GTETRGC	-	TXD1	-	IRQ2				
	S5D5	GTETRGC	GTIOC0A	TXD1	ADTRG1	IRQ2				
P900 P214		PSEL 00010B	PSEL 01011B	PSEL 10001B	PSEL 10101B	PSEL 10110B	PSEL 10111B	PSEL 11010B		▲GTIU ▲QSPCLK ▲SD0CLK ▲ET0_MDC ▲TCLK ▼A23
	S3A7	-	A23	-	-	-	-	-		
	S5D5	GTIU	-	QSPCLK	SD0CLK	ET0_MDC	ET0_MDC	TCLK		
P300		PSEL 00000B	PSEL 00010B	PSEL 00011B	PSEL 00110B					▲GTOUUP
	S3A7	TCK/SWCLK	-	GTIOC0A	SSLB1					
	S5D5	TCK/SWCLK	GTOUUP	GTIOC0A	SSLB1					
P301		PSEL 00001B	PSEL 00010B	PSEL 00011B	PSEL 00100B	PSEL 00101B	PSEL 00110B	PSEL 01011B	ISEL	▲CTS9 ▲AGTIO0 ▼A6
	S3A7	-	GTOULO	GTIOC4B	RXD2	-	SSLB2	A6	IRQ6	
	S5D5	AGTIO0	GTOULO	GTIOC4B	RXD2	CTS9	SSLB2	-	IRQ6	
P302		PSEL 00010B	PSEL 00011B	PSEL 00100B	PSEL 00110B	PSEL 01011B	ISEL			▼A7
	S3A7	GTOUUP	GTIOC4A	TXD2	SSLB3	A7	IRQ5			
	S5D5	GTOUUP	GTIOC4A	TXD2	SSLB3	-	IRQ5			
P303		PSEL 00011B	PSEL 01011B							▼A8
	S3A7	GTIOC7B	A8							
	S5D5	GTIOC7B	-							
P304		PSEL 00010B	PSEL 00011B	PSEL 00100B	PSEL 01011B	ISEL				▲GTOWLO ▲RXD6 ▼A9
	S3A7	-	GTIOC7A	-	A9	IRQ9				
	S5D5	GTOWLO	GTIOC7A	RXD6		IRQ9				
P305		PSEL 00010B	PSEL 00100B	PSEL 01011B	PSEL 10001B	ISEL				▲GTOWUP ▲TXD6 ▲QSPCLK ▼A10
	S3A7	-	-	A10	-	IRQ8				
	S5D5	GTOWUP	TXD6	-	QSPCLK	IRQ8				

Table B 144 Pin Package Difference (9 of 18)

PORT	MCU	SELECT								COMMENTS
P306		PSEL 00010B	PSEL 00100B	PSEL 01011B	PSEL 10001B					▲GTOULO ▲SCK6 ▲A11 ▼QSSL
	S3A7	-	-	A11	-					
	S5D5	GTOULO	SCK6	-	QSSL					
P307		PSEL 00010B	PSEL 00100B	PSEL 01011B	PSEL 10001B					▲GTOUUP ▲CTS6 ▲QIO0 ▼A12
	S3A7	-	-	A12	-					
	S5D5	GTOUUP	CTS6	-	QIO0					
P308		PSEL 01011B	PSEL 10001B							▲QIO1 ▼A13
	S3A7	A13	-							
	S5D5	-	QIO1							
P309		PSEL 00101B	PSEL 01011B	PSEL 10001B						▲RXD3 ▲QIO2 ▼A14
	S3A7	-	A14	-						
	S5D5	RXD3	-	QIO2						
P310		PSEL 00001B	PSEL 00101B	PSEL 01011B	PSEL 10001B					▲AGTEE1 ▲TXD3 ▲QIO3 ▼A15
	S3A7	-	-	A15	-					
	S5D5	AGTEE1	TXD3	-	QIO3					
P311		PSEL 00001B	PSEL 00101B	PSEL 01011B						▲AGTOB1 ▲SCK3 ▲RAS
	S3A7	-	-	CS2#						
	S5D5	AGTOB1	SCK3	CS2#/RAS						
P312		PSEL 00001B	PSEL 00101B	PSEL 01011B						▲AGTOA1 ▲CTS3 ▲CAS
	S3A7	-	-	CS3#						
	S5D5	AGTOA1	CTS3	CS3#/CAS						
P313		PSEL 01011B	PSEL 10101B	PSEL 10110B						▲ET0_ERXD3
	S3A7	A20	SD0DAT7	-						
	S5D5	A20	SD0DAT7	ET0_ERXD3						

Table B 144 Pin Package Difference (10 of 18)

PORT	MCU	SELECT								COMMENTS
P314 VSS(IO)		PSEL 01011B								▼A21
	S3A7	A21								
	S5D5	-								
P315 VCC(IO)		PSEL 01011B								▼A22
	S3A7	A22								
	S5D5	-								
P400		PSEL 00001B	PSEL 00011B	PSEL 00100B	PSEL 00101B	PSEL 00111B	PSEL 01010B	PSEL 01100B	PSEL 10010B	▲AGTIO1 ▲SCK7 ▲ADTRG1 ▲ET0_WOL ▼TS20
	S3A7	-	GTIOC6A	SCK4	-	SCL0	-	TS20	AUDIO_CLK	
	S5D5	AGTIO1	GTIOC6A	SCK4	SCK7	SCL0	ADTRG1	-	AUDIO_CLK	
		PSEL 10110B	PSEL 10111B	ISEL						
	S3A7	-	-	IRQ0						
	S5D5	ET0_WOL	ET0_WOL	IRQ0						
P401		PSEL 00010B	PSEL 00011B	PSEL 00100B	PSEL 00101B	PSEL 00111B	PSEL 01100B	PSEL 10000B	PSEL 10110B	▲TXD7 ▲IRQ5DS ▲ET0_WOL ▼TS19
	S3A7	GTETRGA	GTIOC6B	CTS4	-	SDA0	TS19	CTX0	-	
	S5D5	GTETRGA	GTIOC6B	CTS4	TXD7	SDA0	-	CTX0	ET0_MDC	
		PSEL 10111B	ISEL							
	S3A7	-	IRQ5							
	S5D5	ET0_MDC	IRQ5DS							
P402		PSEL 00001B	PSEL 00101B	PSEL 01001B	PSEL 01010B	PSEL 01100B	PSEL 10000B	PSEL 10010B	PSEL 10110B	▲RXD7 ▲CACREF ▲AUDIO_CLK ▲ET0_MDIO ▲VSYNC ▲IRQ4DS ▼TS18
	S3A7	AGTIO0_B/AGTIO1	-	RTCIC0	-	TS18	CRX0	-	-	
	S5D5	AGTIO0_B/AGTIO1	RXD7	RTCIC0	CACREF	-	CRX0	AUDIO_CLK	ET0_MDIO	
		PSEL 10111B	PSEL 11000B	ISEL						
	S3A7	-	-	IRQ4						
	S5D5	ET0_MDIO	VSYNC	IRQ4DS						

Table B 144 Pin Package Difference (11 of 18)

PORT	MCU	SELECT								COMMENTS
P403		PSEL 00001B	PSEL 00011B	PSEL 00101B	PSEL 01001B	PSEL 01100B	PSEL 10010B	PSEL 10101B	PSEL 10110B	▲CTS7 ▲SD1DAT7 ▲ET0_LINKSTA ▲PIXD7 ▼TS17
	S3A7	AGTIO0_C/AGTIO1	GTIOC3A	-	RTCIC1	TS17	SSISCK0	-	-	
	S5D5	AGTIO0_C/AGTIO1	GTIOC3A	CTS7	RTCIC1	-	SSISCK0	SD1DAT7	ET0_LINKSTA	
		PSEL 10111B	PSEL 11000B							
	S3A7	-	-							
	S5D5	ET0_LINKSTA	PIXD7							
P404		PSEL 00011B	PSEL 01001B	PSEL 01100B	PSEL 10010B	PSEL 10101B	PSEL 10110B	PSEL 10111B	PSEL 11000B	▲SD1DAT6 ▲ET0_EXOUT ▲PIXD6 ▼TS16
	S3A7	GTIOC3B	RTCIC2	TS16	SSIWS0	-	-	-	-	
	S5D5	GTIOC3B	RTCIC2	-	SSIWS0	SD1DAT6	ET0_EXOUT	ET0_EXOUT	PIXD6	
P405		PSEL 00011B	PSEL 01100B	PSEL 10010B	PSEL 10101B	PSEL 10110B	PSEL 10111B	PSEL 11000B		▲SD1DAT5 ▲ET0_TX_EN ▲RMII0_TXD_EN ▲PIXD5 ▼TS15
	S3A7	GTIOC1A	TS15	SSITXD0	-	-	-	-		
	S5D5	GTIOC1A	-	SSITXD0	SD1DAT5	ET0_TX_EN	RMII0_TXD_EN	PIXD5		
P406		PSEL 00011B	PSEL 00110B	PSEL 01100B	PSEL 10010B	PSEL 10101B	PSEL 10110B	PSEL 10111B	PSEL 11000B	▲SSLB3 ▲SD1DAT4 ▲ET0_RX_ER ▲RMIIO_TXD1 ▲PIXD4 ▼TS14
	S3A7	GTIOC1B	-	TS14	SSIRXD0	-	-	-	-	
	S5D5	GTIOC1B	SSLB3	-	SSIRXD0	SD1DAT4	ET0_RX_ER	RMII0_TXD1	PIXD4	
		PSEL 00001B	PSEL 00100B	PSEL 00110B	PSEL 00111B	PSEL 01001B	PSEL 01010B	PSEL 01100B	PSEL 10011B	▲AGTIO0 ▲ET0_EXOUT
P407/USB_VBUS	S3A7	-	CTS4	SSLB3	SDA0	RTCOUT	ADTRG0	TS3	USB_VBUS	
P407	S5D5	AGTIO0	CTS4	SSLB3	SDA0	RTCOUT	ADTRG0	TS3	USB_VBUS	
		PSEL 10110B	PSEL 10111B							
P407/USB_VBUS	S3A7	-	-							
P407	S5D5	ET0_EXOUT	ET0_EXOUT							

Table B 144 Pin Package Difference (12 of 18)

PORT	MCU	SELECT								COMMENTS
P408		PSEL 00010B	PSEL 00011B	PSEL 00101B	PSEL 00111B	PSEL 01100B	PSEL 10011B	PSEL 10110B	PSEL 10111B	▲GTIOC10B ▲SCL0 ▲ET0_CRS ▲RMII0_CRS_DV ▲PIXCLK
	S3A7	GTOWLO	-	RXD3	-	TS4	USB_ID	-	-	
	S5D5	GTOWLO	GTIOC10B	RXD3	SCL0	TS4	USB_ID	ET0_CRS	RMII0_CRS_DV	
		PSEL 11000B	ISEL							
	S3A7	-	IRQ7							
	S5D5	PIXCLK	IRQ7							
P409		PSEL 00010B	PSEL 00011B	PSEL 00101B	PSEL 01100B	PSEL 10011B	PSEL 10110B	PSEL 10111B	PSEL 11000B	▲GTIOC10A ▲ET0_RX_CLK ▲RMII0_RX_ER ▲HSYNC
	S3A7	GTOWUP	-	TXD3	TS5	USB_EXICEN	-	-	-	
	S5D5	GTOWUP	GTIOC10A	TXD3	TS5	USB_EXICEN	ET0_RX_CLK	RMII0_RX_ER	HSYNC	
		ISEL								
	S3A7	IRQ6								
	S5D5	IRQ6								
P410		PSEL 00001B	PSEL 00010B	PSEL 00011B	PSEL 00100B	PSEL 00101B	PSEL 00110B	PSEL 01100B	PSEL 10101B	▲ET_ERXD0 ▲RMII0_RXD1 ▲PIXD0
	S3A7	AGTOB1	GTOVLO	GTIOC9B	RXD0	SCK3	MISOA	TS6	SD0DAT1	
	S5D5	AGTOB1	GTOVLO	GTIOC9B	RXD0	SCK3	MISOA	TS6	SD0DAT1	
		PSEL 10110B	PSEL 10111B	PSEL 11000B	ISEL					
	S3A7	-	-	-	IRQ5					
	S5D5	ET0_ERXD0	RMII0_RXD1	PIXD0	IRQ5					
P411		PSEL 00001B	PSEL 00010B	PSEL 00011B	PSEL 00100B	PSEL 00101B	PSEL 00110B	PSEL 01100B	PSEL 10101B	▲ET_ERXD1 ▲RMII0_RXD0 ▲PIXD1
	S3A7	AGTOA1	GTOVUP	GTIOC9A	TXD0	CTS3	MOSIA	TS7	SD0DAT0	
	S5D5	AGTOA1	GTOVUP	GTIOC9A	TXD0	CTS3	MOSIA	TS7	SD0DAT0	
		PSEL 10110B	PSEL 10111B	PSEL 11000B	ISEL					
	S3A7	-	-	-	IRQ4					
	S5D5	ET0_ERXD1	RMII0_RXD0	PIXD1	IRQ4					

Table B 144 Pin Package Difference (13 of 18)

PORT	MCU	SELECT								COMMENTS
P412		PSEL 00001B	PSEL 00010B	PSEL 00100B	PSEL 00110B	PSEL 01100B	PSEL 10101B	PSEL 10110B	PSEL 10111B	▲AGTEE1 ▲ET0_ETXD0 ▲REF50CK0 ▲PIXD2
	S3A7	-	GTOULO	SCK0	RSPCKA	TS8	SD0CMD	-	-	
	S5D5	AGTEE1	GTOULO	SCK0	RSPCKA	TS8	SD0CMD	ET0_ETXD0	REF50CK0	
		PSEL 11000B								
	S3A7	-								
	S5D5	PIXD2								
P413		PSEL 00010B	PSEL 00100B	PSEL 00110B	PSEL 01100B	PSEL 10101B	PSEL 10110B	PSEL 10111B	PSEL 11000B	▲ET0_ETXD1 ▲RMII0_TXD0 ▲PIXD3
	S3A7	GTOUUP	CTS0	SSLA0	TS9	SD0CLK	-	-	-	
	S5D5	GTOUUP	CTS0	SSLA0	TS9	SD0CLK	ET0_ETXD1	RMII0_TXD0	PIXD3	
P414		PSEL 00011B	PSEL 00110B	PSEL 01100B	PSEL 10101B	PSEL 10110B	PSEL 10111B	PSEL 11000B	ISEL	▲GTIOC0B ▲IRQ9 ▲ET0_RX_ER ▲RMII0_TXD1 ▲PIXD4
	S3A7	-	SSLA1	TS10	SD0WP	-	-	-	-	
	S5D5	GTIOC0B	SSLA1	TS10	SD0WP	ET0_RX_ER	RMII0_TXD1	PIXD4	IRQ9	
P415		PSEL 00011B	PSEL 00110B	PSEL 01100B	PSEL 10011B	PSEL 10101B	PSEL 10110B	PSEL 10111B	PSEL 11000B	▲GTIOC0A ▲USB_VBUSEN ▲SC0CD ▲ET0_TX_EN ▲RMII0_TXD_EN ▲PIXD5 ▲IRQ8
	S3A7	-	SSLA2	TS11	-	-	-	-	-	
	S5D5	GTIOC0A	SSLA2	TS11	USB_VBUSEN	SD0CD	ET0_TX_EN	RMII0_TXD_EN	PIXD5	
		ISEL								
	S3A7	-								
	S5D5	IRQ8								
P500		PSEL 00001B	PSEL 00010B	PSEL 00011B	PSEL 10001B	PSEL 10011B	PSEL 10101B	ASEL ADC	ASEL CMP	▲GTIOC11A ▲SD1CMD ▲IVREF0
	S3A7	AGTOA0	GTIU	-	QSPCLK	USB_VBUSEN	-	AN016	-	
	S5D5	AGTOA0	GTIU	GTIOC11A	QSPCLK	USB_VBUSEN	SD1CLK	AN016	IVREF0	

Table B 144 Pin Package Difference (14 of 18)

PORT	MCU	SELECT								COMMENTS
P501		PSEL 00001B	PSEL 00010B	PSEL 00011B	PSEL 00101B	PSEL 10001B	PSEL 10011B	PSEL 10101B	ASEL ADC	▲GTIOC11B ▲TXD5 ▲SD1CMD ▲AN116 ▲IVREF1 ▼AN017
	S3A7	AGTOB0	GTIV	-	-	QSSL	USB_OVRCURA	-	AN017	
	S5D5	AGTOB0	GTIV	GTIOC11B	TXD5	QSSL	USB_OVRCURA	SD1CMD	AN116	
		ASEL CMP	ISEL							
	S3A7	-	IRQ11							
	S5D5	IVREF1	IRQ11							
P502		PSEL 00010B	PSEL 00011B	PSEL 00101B	PSEL 10001B	PSEL 10011B	PSEL 10101B	ASEL ADC	ASEL CMP	▲GTIOC12A ▲RXD5 ▲SD1DAT0 ▲AN017 ▲IVCMP0 ▼AN018
	S3A7	GTIW	-	-	QIO0	USB_OVRCURB	-	AN018	-	
	S5D5	GTIW	GTIOC12A	RXD5	QIO0	USB_OVRCURB	SD1DAT0	AN017	IVCMP0	
		ISEL								
	S3A7	IRQ12								
	S5D5	IRQ12								
P503		PSEL 00010B	PSEL 00011B	PSEL 00100B	PSEL 00101B	PSEL 10001B	PSEL 10011B	PSEL 10101B	ASEL ADC	▲GTIOC12B ▲CTS6 ▲SCK5 ▲SDADAT1 ▲AN117 ▼AN019
	S3A7	GTETRGC	-	-	-	QIO1	USB_EXICEN	-	AN019	
	S5D5	GTETRGC	GTIOC12B	CTS6	SCK5	QIO1	USB_EXICEN	SD1DAT1	AN117	
P504		PSEL 00010B	PSEL 00011B	PSEL 00100B	PSEL 00101B	PSEL 01011B	PSEL 10001B	PSEL 10011B	PSEL 10101B	▲GTIOC13A ▲SCK6 ▲CTS5 ▲ALE ▲SD1DAT2 ▲AN018 ▼AN020
	S3A7	GTETRGD	-	-	-	-	QIO2	USB_ID	-	
	S5D5	GTETRGD	GTIOC13A	SCK6	CTS5	ALE	QIO2	USB_ID	SD1DAT2	
		ASEL ADC								
	S3A7	AN020								
	S5D5	AN018								
P505		PSEL 00011B	PSEL 00100B	PSEL 10001B	PSEL 10101B	ASEL ADC	ISEL			▲GTIOC13B ▲RXD6 ▲SD1DAT3 ▲AN118 ▼AN021
	S3A7	-	-	QIO3	-	AN021	IRQ14			
	S5D5	GTIOC13B	RXD6	QIO3	SD1DAT3	AN118	IRQ14			

Table B 144 Pin Package Difference (15 of 18)

PORT	MCU	SELECT								COMMENTS
P506		PSEL 00100B	PSEL 10101B	ASEL ADC	ISEL					▲TXD6 ▲SD1CD ▲AN019 ▼AN022
	S3A7	-	-	AN022	IRQ15					
	S5D5	TXD6	SD1CD	AN019	IRQ15					
P507		PSEL 00100B	PSEL 00101B	PSEL 10101B	ASEL ADC					▲SCK6 ▲SD1DAT3 ▲AN020 ▲SCK5 ▼AN023
	S3A7	-	-	-	AN023					
P508	S5D5	SCK6	SCK5	SD1DAT3	AN020					
P511		PSEL 00011B	PSEL 00100B	PSEL 00111B	PSEL 10000B	PSEL 11000B	ISEL			▲CRX1 ▲PCKO
	S3A7	GTIOC0B	RXD4	SDA2	-	-	IRQ15			
	S5D5	GTIOC0B	RXD4	SDA2	CRX1	PCKO	IRQ15			
P512		PSEL 00011B	PSEL 00100B	PSEL 00111B	PSEL 10000B	PSEL 11000B	ISEL			▲CTX1 ▲VSYNC
	S3A7	GTIOC0A	TXD4	SCL2	-	-	IRQ14			
	S5D5	GTIOC0A	TXD4	SCL2	CTX1	VSYNC	IRQ14			
P600		PSEL 00011B	PSEL 00101B	PSEL 01001B	PSEL 01010B	PSEL 01011B				▲GTIOC6B ▲SCK9 ▲CLKOUT ▲CACREF
	S3A7	-	-	-	-	RD				
	S5D5	GTIOC6B	SCK9	CLKOUT	CACREF	RD				
P601		PSEL 00011B	PSEL 00101B	PSEL 01011B						▲GTIOC6A ▲RXD9 ▲DQM0
	S3A7	-	-	WR/WR0						
	S5D5	GTIOC6A	RXD9	WR/WR0/DQM0						
P602		PSEL 00011B	PSEL 00101B	PSEL 01011B						▲GTIOC7B ▲TXD9 ▲SDCLK
	S3A7	-	-	BCLK						
	S5D5	GTIOC7B	TXD9	BCLK/SDCLK						
P603		PSEL 00011B	PSEL 00101B	PSEL 01011B						▲GTIOC7A ▲CTS9 ▲DQ13
	S3A7	-	-	D13						
	S5D5	GTIOC7A	CTS9	D13/DQ13						

Table B 144 Pin Package Difference (16 of 18)

PORT	MCU	SELECT								COMMENTS
P604		PSEL 00011B	PSEL 01011B							▲GTIOC8B ▲DQ12
	S3A7	-	D12							
	S5D5	GTIOC8B	D12/DQ12							
P605		PSEL 00011B	PSEL 01011B							▲GTIOC8A ▲DQ11
	S3A7	-	D11							
	S5D5	GTIOC8A	D11/DQ11							
P608		PSEL 00011B	PSEL 01011B							▲GTIOC4B ▲DQM1
	S3A7	-	A0/BC0							
	S5D5	GTIOC4B	A0/BC0/DQM1							
P609		PSEL 00011B	PSEL 01011B	PSEL 10000B						▲GTIOC5A ▲CKE ▲CTX1
	S3A7	-	CS1#	-						
	S5D5	GTIOC5A	CS1#/CKE	CTX1						
P610		PSEL 00011B	PSEL 01011B	PSEL 10000B						▲GTIOC5B ▲WE ▲CRX1
	S3A7	-	CS0#	-						
	S5D5	GTIOC5B	CS0#/WE	CRX1						
P611		PSEL 00101B	PSEL 01001B	PSEL 01010B	PSEL 01011B					▲CTS7 ▲SDCS ▲CLKOUT ▲CACREF
	S3A7	-	-	-	-					
	S5D5	CTS7	CLKOUT	CACREF	SDCS					
P612		PSEL 00101B	PSEL 01011B							▲SCK7 ▲DQ8
	S3A7	-	D8							
	S5D5	SCK7	D8/DQ8							
P613		PSEL 00101B	PSEL 01011B							▲TXD7 ▲DQ9
	S3A7	-	D9							
	S5D5	TXD7	D9/DQ9							

Table B 144 Pin Package Difference (17 of 18)

PORT	MCU	SELECT								COMMENTS
P614		PSEL 00101B	PSEL 01011B							▲RXD7 ▲DQ10
	S3A7	-	D10							
	S5D5	RXD7	D10/DQ10							
P700		PSEL 00011B	PSEL 00110B	PSEL 01100B	PSEL 10101B	PSEL 10110B	PSEL 10111B	PSEL 11000B		▲MISOB ▲PIXD3 ▲SD1DAT3 ▲ET0_ETXD1 ▲RMII0_TXD0 ▼TS32
	S3A7	GTIOC5A	-	TS32	-	-	-	-		
	S5D5	GTIOC5A	MISOB	-	SD1DAT3	ET0_ETXD1	RMII0_TXD0	PIXD3		
P701		PSEL 00011B	PSEL 00110B	PSEL 01100B	PSEL 10101B	PSEL 10110B	PSEL 10111B	PSEL 11000B		▲MISOB ▲PIXD2 ▲SD1DAT2 ▲ET0_ETXD0 ▲REF50CK0 ▼TS33
	S3A7	GTIOC5B	-	TS33	-	-	-	-		
	S5D5	GTIOC5B	MOSIB	-	SD1DAT2	ET0_ETXD0	REF50CK0	PIXD2		
P702		PSEL 00011B	PSEL 00110B	PSEL 01100B	PSEL 10101B	PSEL 10110B	PSEL 10111B	PSEL 11000B		▲RSPCKB ▲PIXD1 ▲SD1DAT1 ▲ET0_ERXD1 ▲RMIIO_RXD0 ▼TS34
	S3A7	GTIOC6A	-	TS34	-	-	-	-		
	S5D5	GTIOC6A	RSPCKB	-	SD1DAT1	ET0_ERXD1	RMII0_RXD0	PIXD1		
P703		PSEL 00011B	PSEL 00110B	PSEL 01001B	PSEL 10101B	PSEL 10110B	PSEL 10111B	PSEL 11000B		▲PIXD0 ▲VCOUT ▲SD1DAT0 ▲SSLB0 ▲ET0_ERXD0 ▲RMII0_RXD1
	S3A7	GTIOC6B	-	-	-	-	-	-		
	S5D5	GTIOC6B	SSLB0	VCOUT	SD1DAT0	ET0_ERXD0	RMII0_RXD1	PIXD0		
P704		PSEL 00001B	PSEL 00110B	PSEL 10000B	PSEL 10101B	PSEL 10110B	PSEL 10111B	PSEL 11000B		▲AGTO0 ▲CTX0 ▲SSLB1 ▲HSYNC ▲SD1CLK ▲ETO_RX_CLK ▲RMII0_RX_ER
	S3A7	-	-	-	-	-	-	-		
	S5D5	AGTO0	SSLB1	CTX0	SD1CLK	ET0_RX_CLK	RMII0_RX_ER	HSYNC		
P705		PSEL 00001B	PSEL 00110B	PSEL 10000B	PSEL 10101B	PSEL 10110B	PSEL 10111B	PSEL 11000B		▲AGTIO0 ▲CRX0 ▲SSLB2 ▲PIXCLK ▲SD1CMD ▲SEO_CRS ▲RMII0_CRS_DV
	S3A7	-	-	-	-	-	-	-		
	S5D5	AGTIO0	SSLB2	CRX0	SD1CMD	ET0_CRS	RMII0_CRS_DV	PIXCLK		
P708		PSEL 00101B	PSEL 00110B	PSEL 01010B	PSEL 01100B	PSEL 10010B	PSEL 10110B	PSEL 11000B	ISEL	▲AUDIO_CLK ▲ET0_ETXD3 ▲PCKO
	S3A7	RXD1	SSLA3	CACREF	TS12	-	-	-	IRQ11	
	S5D5	RXD1	SSLA3	CACREF	TS12	AUDIO_CLK	ET0_ETXD3	PCKO	IRQ11	

Table B 144 Pin Package Difference (18 of 18)

PORT	MCU	SELECT								COMMENTS
P709		PSEL 00101B	PSEL 01100B	PSEL 10110B	ISEL					▲ET0_ETXD2
	S3A7	TXD1	TS13	-	IRQ10					
	S5D5	TXD1	TS13	ET0_ETXD2	IRQ10					
P710		PSEL 00101B	PSEL 01100B	PSEL 10110B						▲TS14 ▲ETO_TX_ER ▼TS35
	S3A7	SCK1	TS35	-						
	S5D5	SCK1	TS14	ET0_TX_ER						
P711		PSEL 00001B	PSEL 00101B	PSEL 01100B	PSEL 10110B					▲AGTEE0 ▲TS15 ▲ET0_TX_CLK
	S3A7	-	CTS1	-	-					
	S5D5	AGTEE0	CTS1	TS15	ET0_TX_CLK					
P712		PSEL 00001B	PSEL 00011B	PSEL 01100B						▲AGTOB0 ▲TS16
	S3A7	-	GTIOC2B	-						
	S5D5	AGTOB0	GTIOC2B	TS16						
P713		PSEL 00001B	PSEL 00011B	PSEL 01100B						▲AGTOA0 ▲TS17
	S3A7	-	GTIOC2A	-						
	S5D5	AGTOA0	GTIOC2A	TS17						
P800		PSEL 01011B								▲DQ14
	S3A7	D14								
	S5D5	D14/DQ14								
P801		PSEL 01011B								▲DQ15
	S3A7	D15								
	S5D5	D15/DQ15								

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Revision History

		Description	
Rev.	**Date**	**Page**	**Summary**
1.00	Oct 24, 2017	—	Initial version
1.01	Oct 31, 2017	18, 22-23	Minor data corrections made

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