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R8C/27 Group

Timer RC in PWM Mode

1. Abstract

This document describes how to set up and use timer RC in PWM mode in the R8C/27 Group.

2. Introduction

The application example described in this document is applied to the following MCU and parameter(s):

• MCU: R8C/27 Group

This program can be used with other R8C/Tiny Series which have the same special function registers (SFRs) as the R8C/27 Group. Check the manual for any additions and modifications to functions. Careful evaluation is recommended before using this application note.

3. Applications

3.1 Timer RC

Timer RC is a 16-bit timer with four I/O pins.
Timer RC uses either f1 or fOCO40M as its operation clock. Table 3.1 lists the Timer RC Operation Clock.

Table 3.1 Timer RC Operation Clock

Condition	Timer RC Operation Clock
Count source is f1, f2, f4, f8, f32, or TRCCLK input (bits TCK2 to TCK0 in TRCCR1 register are set to a value from 000b to 101b)	f1
Count source is fOCO40M (bits TCK2 to TCK0 in TRCCR1 register are set to 110b)	fOCO40M

Table 3.2 lists the Timer RC I/O Pins, and Figure 3.1 shows a Timer RC Block Diagram.
Timer RC has three modes:

- Timer mode
  - Input capture function — The counter value is captured to a register, using an external signal as the trigger.
  - Output compare function — Matches between the counter and register values are detected. (Pin output state changes when a match is detected.)

The following two modes use the output compare function:

- PWM mode — Pulses of a given width are output continuously.
- PWM2 mode — A one-shot waveform or PWM waveform is output following the trigger after the wait time has elapsed.

Input capture function, output compare function, and PWM mode settings may be specified independently for each pin.
In PWM2 mode, waveforms are output based on a combination of the counter and the register. Pin function is decided by the mode.

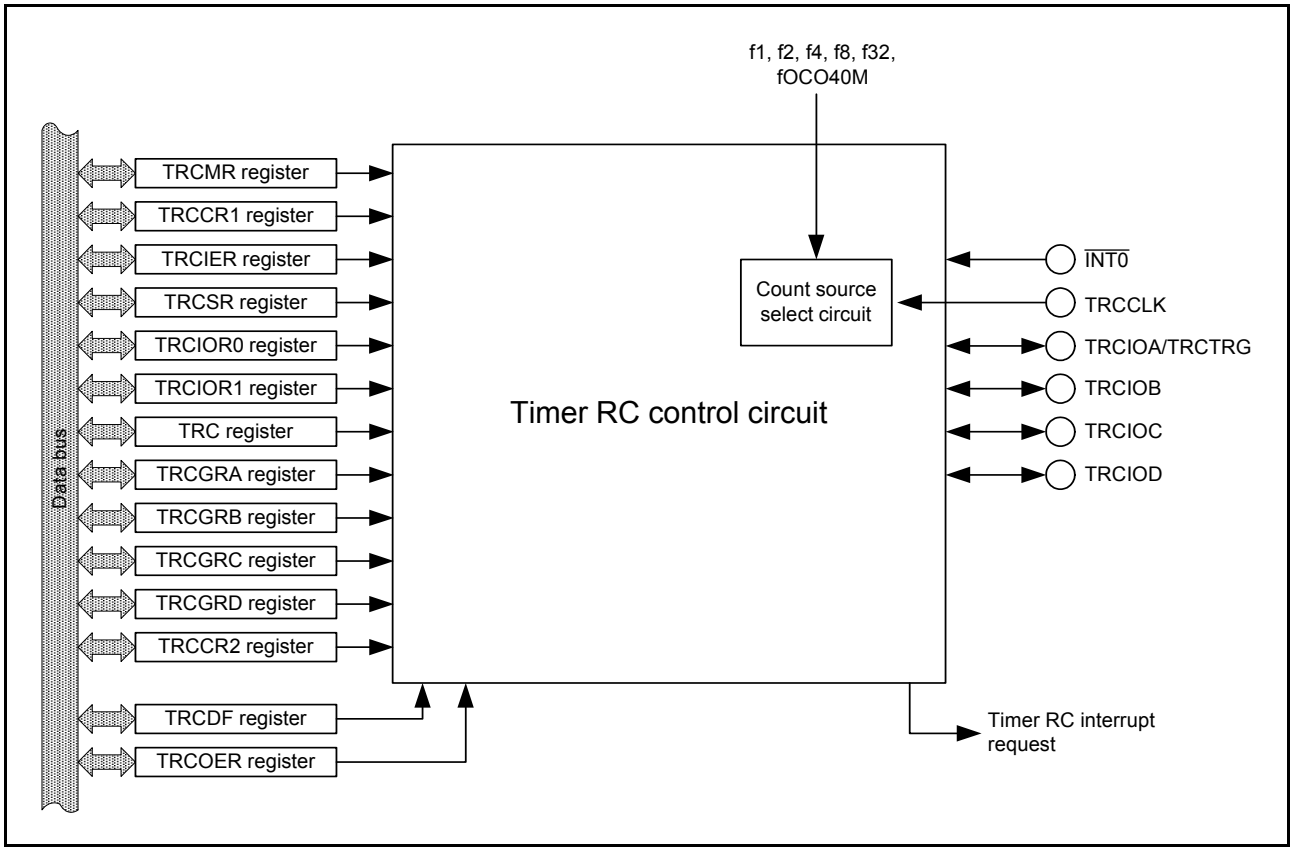


Figure 3.1 Timer RC Block Diagram

Table 3.2 Timer RC I/O Pins

Pin Name	I/O	Function
TRCIOA(P1_1) TRCIOB(P1_2) TRCIOC(P5_3 or P3_4)(1) TRCIOD(P5_4 or P3_5)(1)	I/O	Function differs according to the mode. Refer to descriptions of individual modes for details.
TRCCLK(P3_3)	Input	External clock input
TRCTRG(P1_1)	Input	PWM2 mode external trigger input

NOTE:
1. The pins used for TRCIOC and TRCIOD are selectable. Refer to the description of bits TRCIOCSEL and TRCIODSEL in the PINSR3 register in the **R8C/27 Group Hardware Manual** for details.

3.2 Registers Associated with Timer RC

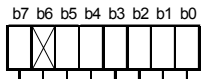
Table 3.3 lists the Registers Associated with Timer RC. Figures 3.2 to 3.11 show details of the registers associated with timer RC.

Table 3.3 Registers Associated with Timer RC

Address	Symbol	Mode				Related Information
		Timer		PWM	PWM2	
		Input Capture Function	Output Compare Function			
0120h	TRCMR	Valid	Valid	Valid	Valid	Timer RC mode register Figure 3.2 TRCMR Register
0121h	TRCCR1	Valid	Valid	Valid	Valid	Timer RC control register 1 Figure 3.3 TRCCR1 Register Figure 3.15 TRCCR1 Register for PWM Mode
0122h	TRCIER	Valid	Valid	Valid	Valid	Timer RC interrupt enable register Figure 3.4 TRCIER Register
0123h	TRCSR	Valid	Valid	Valid	Valid	Timer RC status register Figure 3.5 TRCSR Register
0124h	TRCIOR0	Valid	Valid	–	–	Timer RC I/O control register 0, timer RC I/O control register 1 Figure 3.11 Registers TRCIOR0 and TRCIOR1
0125h	TRCIOR1					
0126h 0127h	TRC	Valid	Valid	Valid	Valid	Timer RC counter Figure 3.6 TRC Register
0128h 0129h	TRCGRA	Valid	Valid	Valid	Valid	Timer RC general registers A, B, C, and D Figure 3.7 Registers TRCGRA, TRCGRB, TRCGRC, and TRCGRD
012Ah 012Bh	TRCGRB					
012Ch 012Dh	TRCGRC					
012Eh 012Fh	TRCGRD					
0130h	TRCCR2	–	–	–	Valid	Timer RC control register 2 Figure 3.8 TRCCR2 Register
0131h	TRCDF	Valid	–	–	Valid	Timer RC digital filter function select register Figure 3.9 TRCDF Register
0132h	TRCOER	–	Valid	Valid	Valid	Timer RC output mask enable register Figure 3.10 TRCOER Register

– : Invalid

Timer RC Mode Register(1)



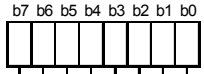
Symbol	Address	After Reset
TRCMR	0120h	01001000b

Bit Symbol	Bit Name	Function	RW
PWMB	PWM mode of TRCIOB select bit(2)	0: Timer mode 1: PWM mode	RW
PWMC	PWM mode of TRCIOC select bit(2)	0: Timer mode 1: PWM mode	RW
PWMD	PWM mode of TRCIOD select bit(2)	0: Timer mode 1: PWM mode	RW
PWM2	PWM2 mode select bit	0: PWM 2 mode 1: Timer mode or PWM mode	RW
BFC	TRCGRC register function select bit(3)	0: General register 1: Buffer register of TRCGRA register	RW
BFD	TRCGRD register function select bit	0: General register 1: Buffer register of TRCGRB register	RW
— (b6)	Nothing is assigned. If necessary, set to 0. When read, the content is 1.		—
TSTART	TRC count start bit	0: Count stops 1: Count starts	RW

NOTES:
1. For notes on PWM2 mode, refer to the **R8C/27 Group Hardware Manual**.
2. These bits are enabled when the PWM2 bit is set to 1 (timer mode or PWM mode).
3. Set the BFC bit to 0 (general register) in PWM2 mode.

Figure 3.2 TRCMR Register

Timer RC Control Register 1



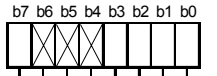
Symbol	Address	After Reset
TRCCR1	0121h	00h

Bit Symbol	Bit Name	Function	RW
TOA	TRCIOA output level select bit(1)	Function varies according to the operating mode (function).(2)	RW
TOB	TRCIOB output level select bit(1)		RW
TOC	TRCIOC output level select bit(1)		RW
TOD	TRCIOD output level select bit(1)		RW
TCK0	Count source select bits(1)	b6 b5 b4 0 0 0: f1 0 0 1: f2 0 1 0: f4 0 1 1: f8 1 0 0: f32 1 0 1: TRCCLK input rising edge 1 1 0: fOCO40M 1 1 1: Do not set.	RW
TCK1			RW
TCK2			RW
CCLR	TRC counter clear select bit(2, 3)	0: Disable clear (free-running operation) 1: Clear by compare match in the TRCGRA register	RW

NOTES:
1. Set to these bits when the TSTART bit in the TRCMR register is set to 0 (count stops).
2. Bits CCLR, TOA, TOB, TOC and TOD are disabled for the input capture function of the timer mode.
3. The TRC counter performs free-running operation for the input capture function of the timer mode independent of the CCLR bit setting.

Figure 3.3 TRCCR1 Register

Timer RC Interrupt Enable Register

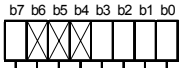


Symbol	Address	After Reset
TRCIER	0122h	01110000b

Bit Symbol	Bit Name	Function	RW
IMIEA	Input capture/compare match interrupt enable bit A	0: Disable interrupt (IMIA) by the IMFA bit 1: Enable interrupt (IMIA) by the IMFA bit	RW
IMIEB	Input capture/compare match interrupt enable bit B	0: Disable interrupt (IMIB) by the IMFB bit 1: Enable interrupt (IMIB) by the IMFB bit	RW
IMIEC	Input capture/compare match interrupt enable bit C	0: Disable interrupt (IMIC) by the IMFC bit 1: Enable interrupt (IMIC) by the IMFC bit	RW
IMIED	Input capture/compare match interrupt enable bit D	0: Disable interrupt (IMID) by the IMFD bit 1: Enable interrupt (IMID) by the IMFD bit	RW
— (b6 - b4)	Nothing is assigned. If necessary, set to 0. When read, the content is 1.		—
OVIE	Overflow interrupt enable bit	0: Disable interrupt (OVI) by the OVF bit 1: Enable interrupt (OVI) by the OVF bit	RW

Figure 3.4 TRCIER Register

Timer RC Status Register



Symbol	Address	After Reset
TRCSR	0123h	01110000b

Bit Symbol	Bit Name	Function	RW
IMFA	Input capture/compare match flag A	[Source for setting this bit to 0] Write 0 after read(1). [Source for setting this bit to 1] Refer to the table below.	RW
IMFB	Input capture/compare match flag B		RW
IMFC	Input capture/compare match flag C		RW
IMFD	Input capture/compare match flag D		RW
— (b6 - b4)	Nothing is assigned. If necessary, set to 0. When read, the content is 1.		—
OVF	Overflow flag	[Source for setting this bit to 0] Write 0 after read(1). [Source for setting this bit to 1] Refer to the table below.	RW

NOTE:
1. The writing results are as follows:
   - This bit is set to 0 when the read result is 1 and 0 is written to the same bit.
   - This bit remains unchanged even if the read result is 0 and 0 is written to the same bit. (This bit remains 1 even if it is set to 1 from 0 after reading, and writing 0.)
   - This bit remains unchanged if 1 is written to it.

Bit Symbol	Timer Mode		PWM Mode	PWM2 Mode
	Input capture Function	Output Compare Function		
IMFA	TRCIOA pin input edge(1)	When the values of the registers TRC and TRCGRA match.		
IMFB	TRCIOB pin input edge(1)	When the values of the registers TRC and TRCGRB match.		
IMFC	TRCIOC pin input edge(1)	When the values of the registers TRC and TRCGRC match.(2)		
IMFD	TRCIOD pin input edge(1)	When the values of the registers TRC and TRCGRD match.(2)		
OVF	When the TRC register overflows.			

NOTES:
1. Edge selected by bits IOj1 to IOj0 (j = A, B, C, or D).
2. Includes the condition that bits BFC and BFD are set to 1 (buffer registers of registers TRCGRA and TRCGRB).

Figure 3.5 TRCSR Register

Timer RC Counter(1)

(b15) (b8) b7 b0 b7 b0

Symbol	Address	After Reset
TRC	0127h-0126h	0000h

Function	Setting Range	RW
Count a count source. Count operation is incremented. When an overflow occurs, the OVF bit in the TRCSR register is set to 1.	0000h to FFFFh	RW

NOTE:
1. Access the TRC register in 16-bit units. Do not access it in 8-bit units.

Figure 3.6 TRC Register

Timer RC General Registers A, B, C and D(1)

(b15) (b8) b7 b0 b7 b0

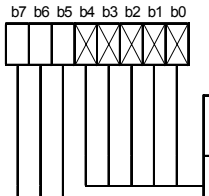
Symbol	Address	After Reset
TRCGRA	0129h-0128h	FFFFh
TRCGRB	012Bh-012Ah	FFFFh
TRCGRC	012Dh-012Ch	FFFFh
TRCGRD	012Fh-012Eh	FFFFh

Function	RW
Function varies according to the operating mode.	RW

NOTE:
1. Access registers TRCGRA to TRCGRD in 16-bit units. Do not access them in 8-bit units.

Figure 3.7 Registers TRCGRA, TRCGRB, TRCGRC, and TRCGRD

Timer RC Control Register 2



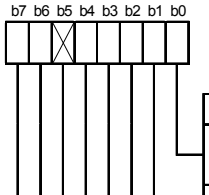
Symbol	Address	After Reset
TRCCR2	0130h	00011111b

Bit Symbol	Bit Name	Function	RW
— (b4 - b0)	Nothing is assigned. If necessary, set to 0. When read, the content is 1.		—
CSEL	TRC count operation select bit(1, 2)	0: Count continues at compare match with the TRCGRA register	RW
		1: Count stops at compare match with the TRCGRA register	RW
TCEG0	TRCTRG input edge select bits(3)	b7 b6 0 0: Disable the trigger input from the TRCTRG pin	RW
TCEG1		0 1: Rising edge selected 1 0: Falling edge selected 1 1: Both edges selected	RW

NOTES:
1. For notes on PWM2 mode, refer to the **R8C/27 Hardware Manual**.
2. In timer mode and PWM mode, this bit is disabled (the count operation continues independent of the CSEL bit setting).
3. In timer mode and PWM mode, these bits are disabled.

Figure 3.8 TRCCR2 Register

Timer RC Digital Filter Function Select Register



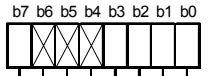
Symbol	Address	After Reset
TRCDF	0131h	00h

Bit Symbol	Bit Name	Function	RW
DFA	TRCIOA pin digital filter function select bit(1)	0: Function is not used 1: Function is used	RW
DFB	TRCIOB pin digital filter function select bit(1)		RW
DFC	TRCIOC pin digital filter function select bit(1)		RW
DFD	TRCIOD pin digital filter function select bit(1)		RW
DFTRG	TRCTRG pin digital filter function select bit(2)		RW
— (b5)	Nothing is assigned. If necessary, set to 0. When read, the content is 0.		—
DFCK0	Clock select bits for digital filter function(1, 2)	b7 b6 0 0: f32 0 1: f8 1 0: f1	RW
DFCK1		1 1: Count source (clock selected by bits TCK2 to TCK0 in the TRCCR1 register)	RW

NOTES:
1. These bits are enabled for the input capture function.
2. These bits are enabled when in PWM2 mode and bits TCEG1 to TCEG0 in the TRCCR2 register are set to 01b, 10b, or 11b (TRCTRG trigger input enabled).

Figure 3.9 TRCDF Register

Timer RC Output Master Enable Register



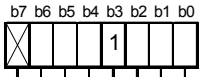
Symbol	Address	After Reset
TRCOER	0132h	01111111b

Bit Symbol	Bit Name	Function	RW
EA	TRCIOA output disable bit(1)	0: Enable output 1: Disable output (TRCIOA pin as a programmable I/O port.)	RW
EB	TRCIOB output disable bit(1)	0: Enable output 1: Disable output (TRCIOB pin as a programmable I/O port.)	RW
EC	TRCIOC output disable bit(1)	0: Enable output 1: Disable output (TRCIOC pin as a programmable I/O port.)	RW
ED	TRCIOD output disable bit(1)	0: Enable output 1: Disable output (TRCIOD pin as a programmable I/O port.)	RW
— (b6 - b4)	Nothing is assigned. If necessary, set to 0. When read, the content is 1.		—
PTO	$\overline{INT0}$ of pulse output forced cutoff signal input enabled bit	0 : Pulse output forced cutoff input disabled 1 : Pulse output forced cutoff input enabled (Bits EA, EB, EC, and ED are set to 1 (disable output) when “L” is applied to the $\overline{INT0}$ pin)	RW

NOTE:
1. These bits are disabled for input pins set to the input capture function.

Figure 3.10 TRCOER Register

Timer RC I/O Control Register 0(1)

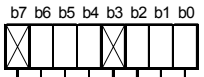


Symbol	Address	After Reset
TRCIOR0	0124h	10001000b

Bit Symbol	Bit Name	Function	RW
IOA0	TRCGRA control bits	Function varies according to the operating mode (function).	RW
IOA1			RW
IOA2	TRCGRA mode select bit(2)	0: Output compare function 1: Input capture function	RW
— (b3)	Reserved bit	Set to 1.	RW
IOB0	TRCGRB control bits	Function varies according to the operating mode (function).	RW
IOB1			RW
IOB2	TRCGRB mode select bit(3)	0: Output compare function 1: Input capture function	RW
— (b7)	Nothing is assigned. If necessary, set to 0. When read, the content is 1.		—

NOTES:
1. The TRCIOR0 register is enabled in timer mode. It is disabled in modes PWM and PWM2.
2. When the BFC bit in the TRCMR register is set to 1 (buffer register of TRCGRA register), set the IOC2 bit in the TRCIOR1 register to the same value as the IOA2 bit in the TRCIOR0 register.
3. When the BFD bit in the TRCMR register is set to 1 (buffer register of TRCGRB register), set the IOD2 bit in the TRCIOR1 register to the same value as the IOB2 bit in the TRCIOR0 register.

Timer RC I/O Control Register 1(1)



Symbol	Address	After Reset
TRCIOR1	0125h	10001000b

Bit Symbol	Bit Name	Function	RW
IOC0	TRCGRC control bits	Function varies according to the operating mode (function).	RW
IOC1			RW
IOC2	TRCGRC mode select bit(2)	0: Output compare function 1: Input capture function	RW
— (b3)	Nothing is assigned. If necessary, set to 0. When read, the content is 1.		—
IOD0	TRCGRD control bits	Function varies according to the operating mode (function).	RW
IOD1			RW
IOD2	TRCGRD mode select bit(3)	0: Output compare function 1: Input capture function	RW
— (b7)	Nothing is assigned. If necessary, set to 0. When read, the content is 1.		—

NOTES:
1. The TRCIOR1 register is enabled in timer mode. It is disabled in modes PWM and PWM2.
2. When the BFC bit in the TRCMR register is set to 1 (buffer register of TRCGRA register), set the IOC2 bit in the TRCIOR1 register to the same value as the IOA2 bit in the TRCIOR0 register.
3. When the BFD bit in the TRCMR register is set to 1 (buffer register of TRCGRB register), set the IOD2 bit in the TRCIOR1 register to the same value as the IOB2 bit in the TRCIOR0 register.

Figure 3.11 Registers TRCIOR0 and TRCIOR1

3.3 Common Items for Multiple Modes

3.3.1 Count Source

The method of selecting the count source is common to all modes.
Table 3.4 lists the Count Source Selection, and Figure 3.12 shows a Count Source Block Diagram

Table 3.4 Count Source Selection

Count Source	Selection Method
f1, f2, f4, f8, f32	Count source selected using bits TCK2 to TCK0 in TRCCR1 register
fOCO40M	FRA00 bit in FRA0 register set to 1 (high-speed on-chip oscillator on) and bits TCK2 to TCK0 in TRCCR1 register are set to 110b (fOCO40M)
External signal input to TRCCLK pin	Bits TCK2 to TCK0 in TRCCR1 register are set to 101b (count source is rising edge of external clock) and PD3_3 bit in PD3 register is set to 0 (input mode)

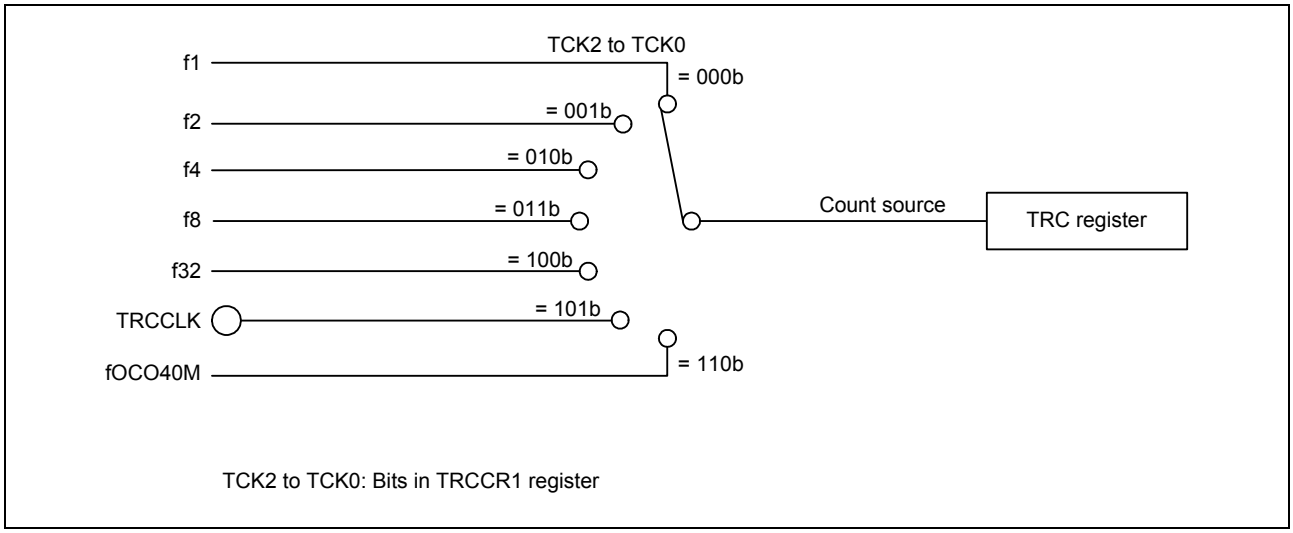


Figure 3.12 Count Source Block Diagram

The pulse width of the external clock input to the TRCCLK pin should be three cycles or more of the timer RC operation clock (see **Table 3.1 Timer RC Operation Clock**).
To select fOCO40M as the count source, set the FRA00 bit in the FRA0 register to 1 (high-speed on-chip oscillator on), and then set bits TCK2 to TCK0 in the TRCCR1 register to 110b (fOCO40M).

3.3.2 Buffer Operation

Bits BFC and BFD in the TRCMR register are used to select the TRCGRC or TRCGRD register as the buffer register for the TRCGRA or TRCGRB register.

- Buffer register for TRCGRA register: TRCGRC register
- Buffer register for TRCGRB register: TRCGRD register

Buffer operation differs depending on the mode.
Table 3.5 lists the Buffer Operation in Each Mode.

Table 3.5 Buffer Operation in Each Mode

Function, Mode	Transfer Timing	Transfer Destination Register
Input capture function	Input capture signal input	Contents of TRCGRA (TRCGRB) register are transferred to buffer register
Output compare function PWM mode	Compare match between TRC register and TRCGRA (TRCGRB) register	Contents of buffer register are transferred to TRCGRA (TRCGRB) register
PWM2 mode	• Compare match between TRC register and TRCGRA register • TRCTRG pin trigger input	Contents of buffer register (TRCGRD) are transferred to TRCGRB register

The output compare function, PWM mode, or PWM2 mode, and the TRCGRC or TRCGRD register is functioning as a buffer register, the IMFC bit or IMFD bit in the TRCSR register is set to 1 when a compare match with the TRC register occurs.

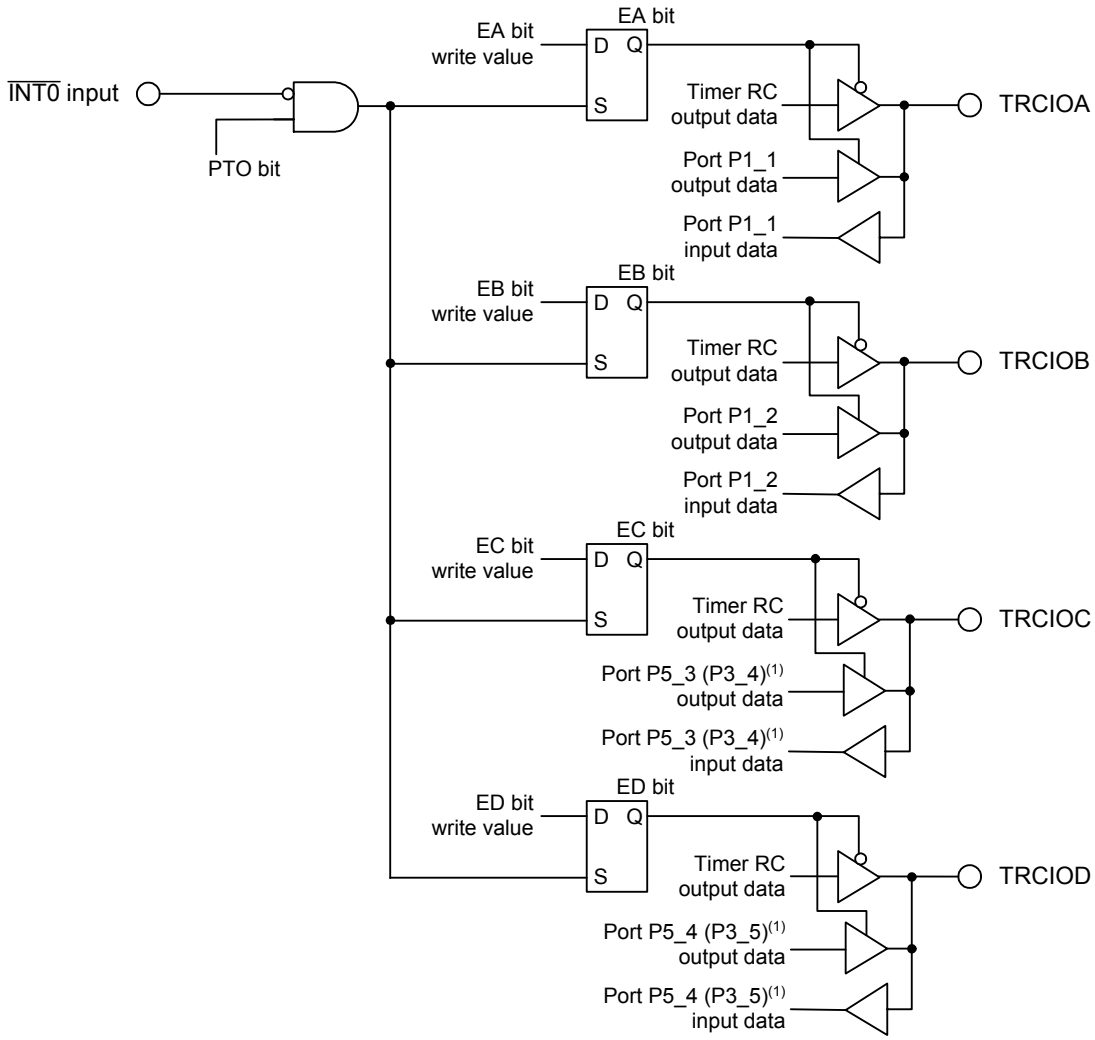
3.3.3 Forced Cutoff of Pulse Output

When using the timer mode's output compare function, the PWM mode, or the PWM2 mode, pulse output from the TRCIOj (j = A, B, C, or D) output pin can be forcibly cut off and the TRCIOj pin set to function as a programmable I/O port by means of input to the $\overline{\text{INT0}}$ pin.
A pin used for output by the timer mode's output compare function, the PWM mode, or the PWM2 mode can be set to function as the timer RC output pin by setting the Ej bit in the TRCOER register to 0 (timer RC output enabled). If "L" is input to the $\overline{\text{INT0}}$ pin while the PTO bit in the TRCOER register is set to 1 (pulse output forced cutoff signal input $\overline{\text{INT0}}$ enabled), bits EA, EB, EC, and ED in the TRCOER register are all set to 1 (timer RC output disabled, TRCIOj output pin functions as the programmable I/O port). When one or two cycles of the timer RC operation clock after "L" input to the $\overline{\text{INT0}}$ pin (refer to **Table 3.1 Timer RC Operation Clock**) has elapsed, the TRCIOj output pin becomes a programmable I/O port.

Make the following settings to use this function:

- Set the pin state following forced cutoff of pulse output (high impedance (input), "L" output, or "H" output). (Refer to the **R8C/27 Group Hardware Manual**.)
- Set the INT0EN bit to 1 ($\overline{\text{INT0}}$ input enabled) and the INT0PL bit to 0 (one edge) in the INTEN register.
- Set the PD4_5 bit in the PD4 register to 0 (input mode).
- Select the $\overline{\text{INT0}}$ digital filter by means of bits INT0F1 to INT0F0 in the INTF register.
- Set the PTO bit in the TRCOER register to 1 (pulse output forced cutoff signal input $\overline{\text{INT0}}$ enabled).

The IR bit in the INT0IC register is set to 1 (interrupt request) in accordance with the setting of the POL bit and a change in the $\overline{\text{INT0}}$ pin input (refer to the **R8C/27 Group Hardware Manual**).
For details on interrupts, refer to the **R8C/27 Group Hardware Manual**.



EA, EB, EC, ED, PTO: Bits in TRCOER register

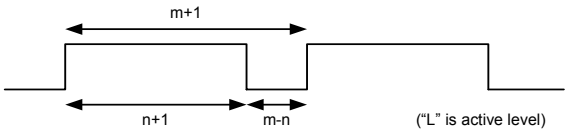
NOTE:
1. Pins in parentheses ( ) can be assigned by a program.

Figure 3.13 Forced Cutoff of Pulse Output

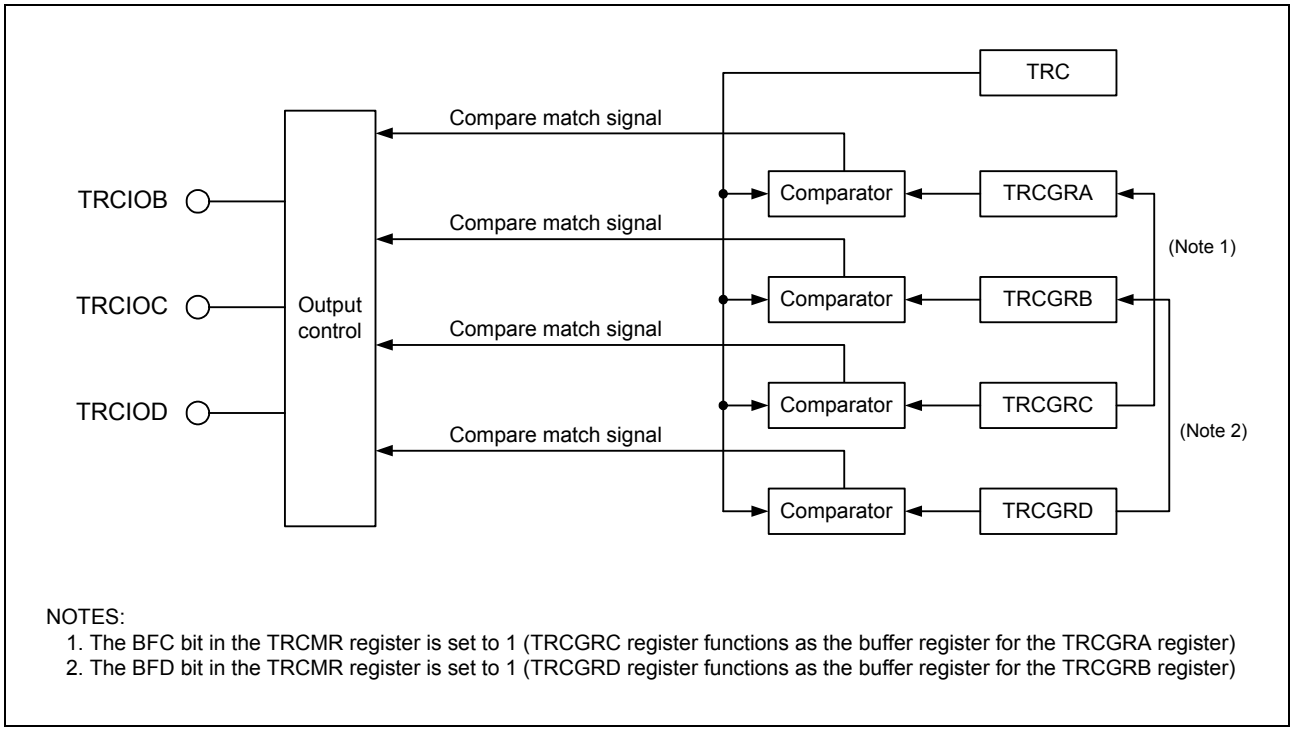
3.4 PWM Mode

This mode outputs PWM waveforms. A maximum of three PWM waveforms with the same period are output. The PWM mode, or the timer mode, can be selected for each individual pin. (However, since the TRCGRA register is used when using any pin for the PWM mode, the TRCGRA register cannot be used for the timer mode.)
Table 3.6 lists the Specifications of PWM Mode, Figure 3.14 shows a Block Diagram of PWM Mode, Figure 3.15 shows the registers associated with the PWM mode, Table 3.7 lists the Functions of TRCGRj Register in PWM Mode, and Figures 3.16 and 3.17 show Operating Examples of PWM Mode.

Table 3.6 Specifications of PWM Mode

Item	Specification
Count source	f1, f2, f4, f8, f32, fOCO40M, or external signal (rising edge) input to TRCCLK pin
Count operation	Increment
PWM waveform	PWM period: 1/fk × (m + 1) Active level width: 1/fk × (m - n) Inactive width: 1/fk × (n + 1) fk: Count source frequency m: TRCGRA register setting value n: TRCGRj register setting value 
Count start condition	1 (count starts) is written to the TSTART bit in the TRCMR register.
Count stop condition	0 (count stops) is written to the TSTART bit in the TRCMR register. PWM output pin retains output level before count stops, TRC register retains value before count stops.
Interrupt request generation timing	• Compare match (contents of registers TRC and TRCGRj match) • The TRC register overflows.
TRCIOA pin function	Programmable I/O port
TRCIOB, TRCIOC, and TRCIOD pin functions	Programmable I/O port or PWM output (selectable individually by pin)
$\overline{\text{INT0}}$ pin function	Programmable I/O port, pulse output forced cutoff signal input, or $\overline{\text{INT0}}$ interrupt input
Read from timer	The count value can be read by reading the TRC register.
Write to timer	The TRC register can be written to.
Select functions	• One to three pins selectable as PWM output pins per channel One or more of pins TRCIOB, TRCIOC, and TRCIOD • Active level selectable by individual pins • Buffer operation (refer to **3.3.2 Buffer Operation**) • Pulse output forced cutoff signal input (refer to **3.3.3 Forced Cutoff of Pulse Output**)

j = A, B, C, or D



NOTES:
1. The BFC bit in the TRCMR register is set to 1 (TRCGRC register functions as the buffer register for the TRCGRA register)
2. The BFD bit in the TRCMR register is set to 1 (TRCGRD register functions as the buffer register for the TRCGRB register)

Figure 3.14 Block Diagram of PWM Mode

Timer RC Control Register 1

b7 b6 b5 b4 b3 b2 b1 b0

Symbol	Address	After Reset
TRCCR1	0121h	00h

Bit Symbol	Bit Name	Function	RW
TOA	TRCIOA output level select bit(1)	Disabled in PWM mode	RW
TOB	TRCIOB output level select bit(1)	0: Active level "H" (Initial output "L" "H" output by compare match in the TRCGRj register "L" output by compare match in the TRCGRA register) 1: Active level "L" (Initial output "H" "L" output by compare match in the TRCGRj register "H" output by compare match in the TRCGRA register)	RW
TOC	TRCIOC output level select bit(1)		RW
TOD	TRCIOD output level select bit(1)		RW
TCK0	Count source select bits(1)	b6 b5 b4 0 0 0: f1 0 0 1: f2 0 1 0: f4 0 1 1: f8 1 0 0: f32 1 0 1: TRCCLK input rising edge 1 1 0: fOCO40M 1 1 1: Do not set.	RW
TCK1			RW
TCK2			RW
CCLR	TRC counter clear select bit	0: Disable clear (free-running operation) 1: Clear by compare match in the TRCGRA register	RW

j = B, C or D

NOTE:

1. Set to these bits when the TSTART bit in the TRCMR register is set to 0 (count stops).

Figure 3.15 TRCCR1 Register for PWM Mode

Table 3.7 Functions of TRCGRj Register in PWM Mode

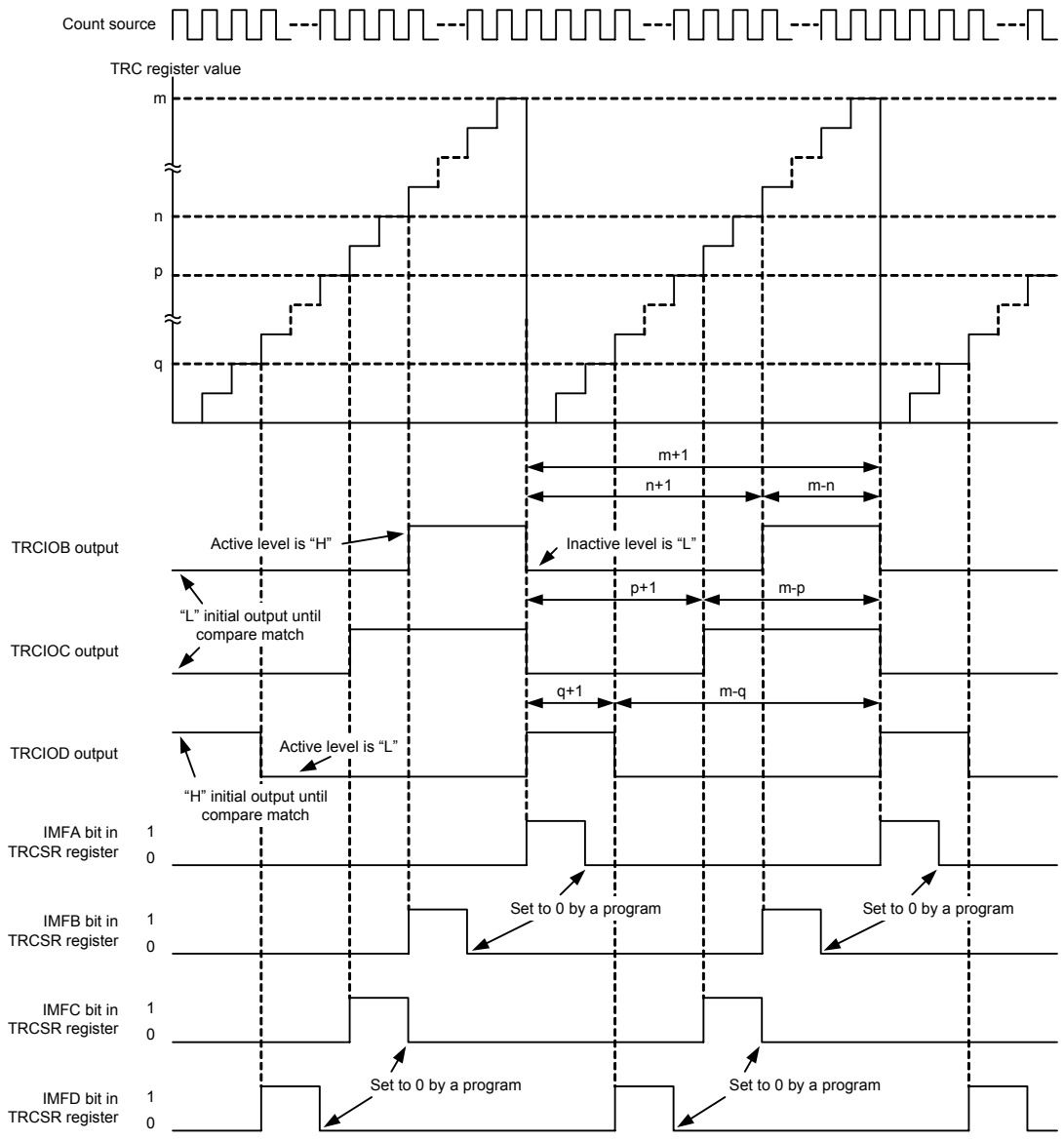
Register	Setting	Register Function	PWM Output Pin
TRCGRA	–	General register. Set the PWM period.	–
TRCGRB	–	General register. Set the PWM output change point.	TRCIOB
TRCGRC	BFC = 0	General register. Set the PWM output change point.	TRCIOC
TRCGRD	BFD = 0		TRCIOD
TRCGRC	BFC = 1	Buffer register. Set the next PWM period (refer to **3.3.2 Buffer Operation**).	–
TRCGRD	BFD = 1	Buffer register. Set the next PWM output change point (refer to **3.3.2 Buffer Operation**).	TRCIOB

j = A, B, C, or D

BFC, BFD: Bits in TRCMR register

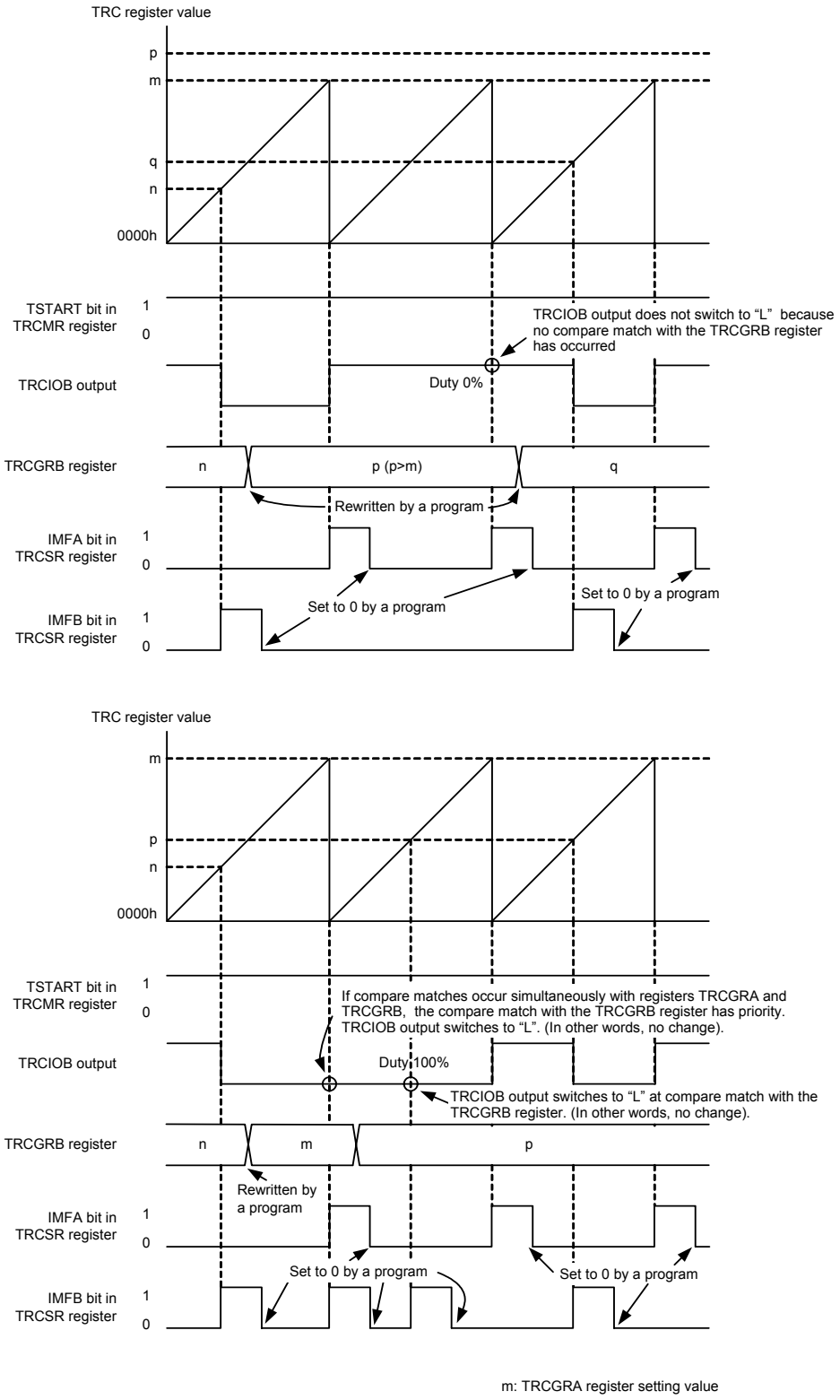
NOTE:

1. The output level does not change even when a compare match occurs if the TRCGRA register value (PWM period) is the same as the TRCGRB, TRCGRC, or TRCGRD register value.



The above applies under the following conditions:
- Bits BFC and BFD in the TRCMR register are set to 0 (registers TRCGRC and TRCGRD do not operate as buffers).
- Bits EB, EC, and ED in the TRCOER register are set to 0 (output from TRCIOB, TRCIOC, and TRCIOD enabled).
- In the TRCCR1 register, bits TOB and TOC are set to 0 (active level is “H”) and the TOD bit is set to 1 (active level is “L”).

Figure 3.16 Operating Example of PWM Mode



The above applies under the following conditions:
- The EB bit in the TRCOER register is set to 0 (output from TRCIOB enabled).
- The TOB bit in the TRCCR1 register is set to 1 (active level is "L").

Figure 3.17 Operating Example of PWM Mode (Duty 0% and Duty 100%)

3.5 Timer RC Interrupt

Timer RC generates a timer RC interrupt request from five sources. The timer RC interrupt uses a single TRCIC register (bits IR and ILVL0 to ILVL2) and a single vector.
Table 3.8 lists the Registers Associated with Timer RC Interrupt, and Figure 3.18 is a Timer RC Interrupt Block Diagram.

Table 3.8 Registers Associated with Timer RC Interrupt

Timer RC Status Register	Timer RC Interrupt Enable Register	Timer RC Interrupt Control Register
TRCSR0	TRCIER	TRCIC

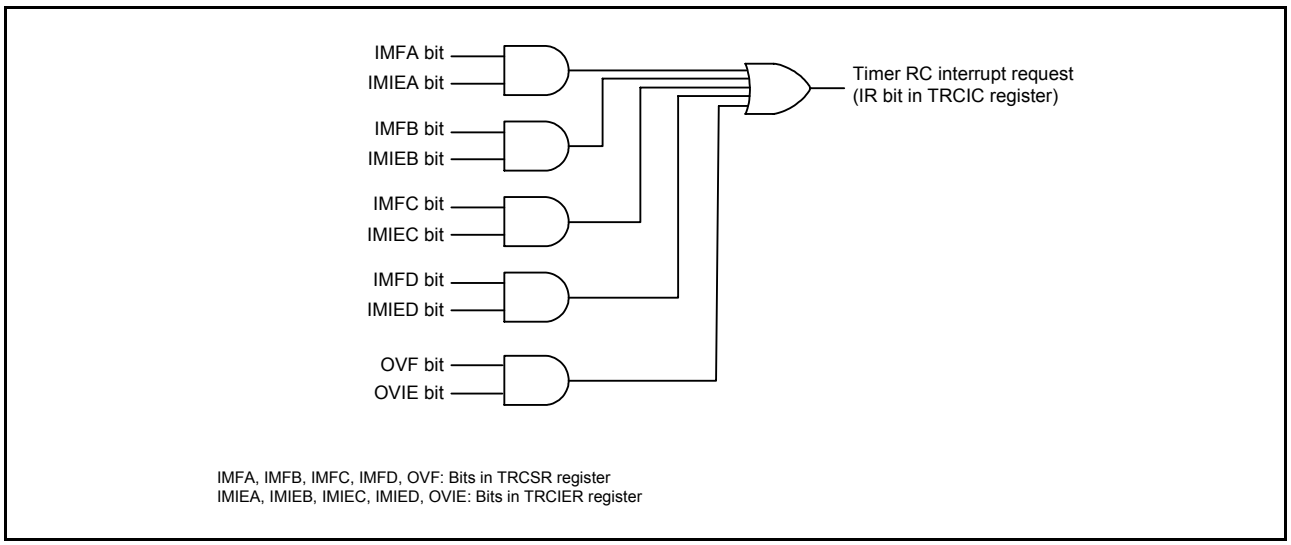


Figure 3.18 Timer RC Interrupt Block Diagram

Like other maskable interrupts, the timer RC interrupt is controlled by the combination of the I flag, IR bit, bits ILVL0 to ILVL2, and IPL. However, it differs from other maskable interrupts in the following respects because a single interrupt source (timer RC interrupt) is generated from multiple interrupt request sources.

- The IR bit in the TRCIC register is set to 1 (interrupt requested) when a bit in the TRCSR register is set to 1 and the corresponding bit in the TRCIER register is also set to 1 (interrupt enabled).
- The IR bit is set to 0 (no interrupt request) when the bit in the TRCSR register or the corresponding bit in the TRCIER register is set to 0, or both are set to 0. In other words, the interrupt request is not maintained if the IR bit is once set to 1, but the interrupt is not acknowledged.
- If after the IR bit is set to 1, another interrupt source is triggered, the IR bit remains set to 1 and does not change.
- If multiple bits in the TRCIER register are set to 1, use the TRCSR register to determine the source of the interrupt request.
- The bits in the TRCSR register are not automatically set to 0 when an interrupt is acknowledged. Set them to 0 within the interrupt routine. Refer to **Figure 3.5 TRCSR Register** for the procedure for setting these bits to 0.

Refer to **Figure 3.4 TRCIER Register**, for details on the TRCIER register.
Refer to the **R8C/27 Group Hardware Manual** for details on the TRCIC register and for information on interrupt vectors.

3.6 Notes on Timer RC

3.6.1 TRC Register

- The following note applies when the CCLR bit in the TRCCR1 register is set to 1 (clear TRC register at compare match with TRCGRA register).
  When using a program to write a value to the TRC register while the TSTART bit in the TRCMR register is set to 1 (count starts), ensure that the write does not overlap with the timing with which the TRC register is set to 0000h.
  If the timing of the write to the TRC register and the setting of the TRC register to 0000h coincide, the write value will not be written to the TRC register and the TRC register will be set to 0000h.

- Reading from the TRC register immediately after writing to it can result in the value previous to the write being read out. To prevent this, execute the JMP.B instruction between the read and the write instructions.

```
Program Example     MOV.W   #XXXXh, TRC     ;Write
                    JMP.B   L1              ;JMP.B instruction
                L1: MOV.W   TRC,DATA        ;Read
```

3.6.2 TRCSR Register

Reading from the TRCSR register immediately after writing to it can result in the value previous to the write being read out. To prevent this, execute the JMP.B instruction between the read and the write instructions.

```
Program Example     MOV.B   #XXh, TRCSR     ;Write
                    JMP.B   L1              ;JMP.B instruction
                L1: MOV.B   TRCSR,DATA      ;Read
```

3.6.3 Count Source Switching

- Stop the count before switching the count source.

Switching procedure:

(1) Set the TSTART bit in the TRCMR register to 0 (count stops).
(2) Change the settings of bits TCK2 to TCK0 in the TRCCR1 register.

- After switching the count source from fOCO40M to another clock, allow a minimum of two cycles of f1 to elapse after changing the clock setting before stopping fOCO40M.

Switching procedure:

(1) Set the TSTART bit in the TRCMR register to 0 (count stops).
(2) Change the settings of bits TCK2 to TCK0 in the TRCCR1 register.
(3) Wait for a minimum of two cycles of f1.
(4) Set the FRA00 bit in the FRA0 register to 0 (high-speed on-chip oscillator off).

4. Program Overview

This program can be used on timer RC to output a compare match signal between timer RC counter and general registers (TRCIOB, TRCIOC, and TRCIOD) at the PWM period (100 µs). The output signals are as follows.

TRCIOB pin: inactive level (“L”) 25 µs = 40 MHz × (TRCGRB + 1) = 25 ns × 1000
active level (“H”) 75 µs = 40 MHz × ((TRCGRA + 1) – (TRCGRB + 1))
= 25 ns × (4000 – 1000) = 25 ns × 3000

TRCIOC pin: inactive level (“L”) 50 µs = 40 MHz × (TRCGRC + 1) = 25 ns × 2000
active level (“H”) 50 µs = 40 MHz × ((TRCGRA + 1) – (TRCGRC + 1))
= 25 ns × (4000 – 2000) = 25 ns × 2000

TRCIOC pin: inactive level (“L”) 75 µs = 40 MHz × (TRCGRD + 1) = 25 ns × 3000
active level (“H”) 25 µs = 40 MHz × ((TRCGRA + 1) – (TRCGRD + 1))
= 25 ns × (4000 – 3000) = 25 ns × 1000

Set TRCGRA to the PWM period (100 µs).
100 µs = 40 MHz (TRCGRA + 1)
= 25 ns × 4000

The setting conditions of this program are as follows:
- Select the high-speed on-chip oscillator (fOCOM40M) as count source.
- Select P3_4 for TRCIOC pin.
- Select P3_5 for TRCIOD pin.
- Clear timer RC counter (TRC) by compare match with TRCGRA.
- For the TRCIOB pin, set the output level to active (“H”) and the initial level to inactive (“L”)
- For the TRCIOC pin, set the output level to active (“H”) and the initial level to inactive (“L”)
- For the TRCIOD pin, set the output level to active (“H”) and the initial level to inactive (“L”)
- Output an active level signal (“H”) from the TRCIOB output pin at compare match between TRC and TRCGRB.
- Output an active level signal (“H”) from the TRCIOC output pin at compare match between TRC and TRCGRC.
- Output an active level signal (“H”) from the TRCIOD output pin at compare match between TRC and TRCGRD.
- Output an inactive level signal (“L”) from the TRCIOB, TRCIOC, and TRCIOD output pins at compare match between TRC and TRCGRA.
- Do not use the pulse output forced cutoff input function.

Figure 4.1 shows the Pin Used.

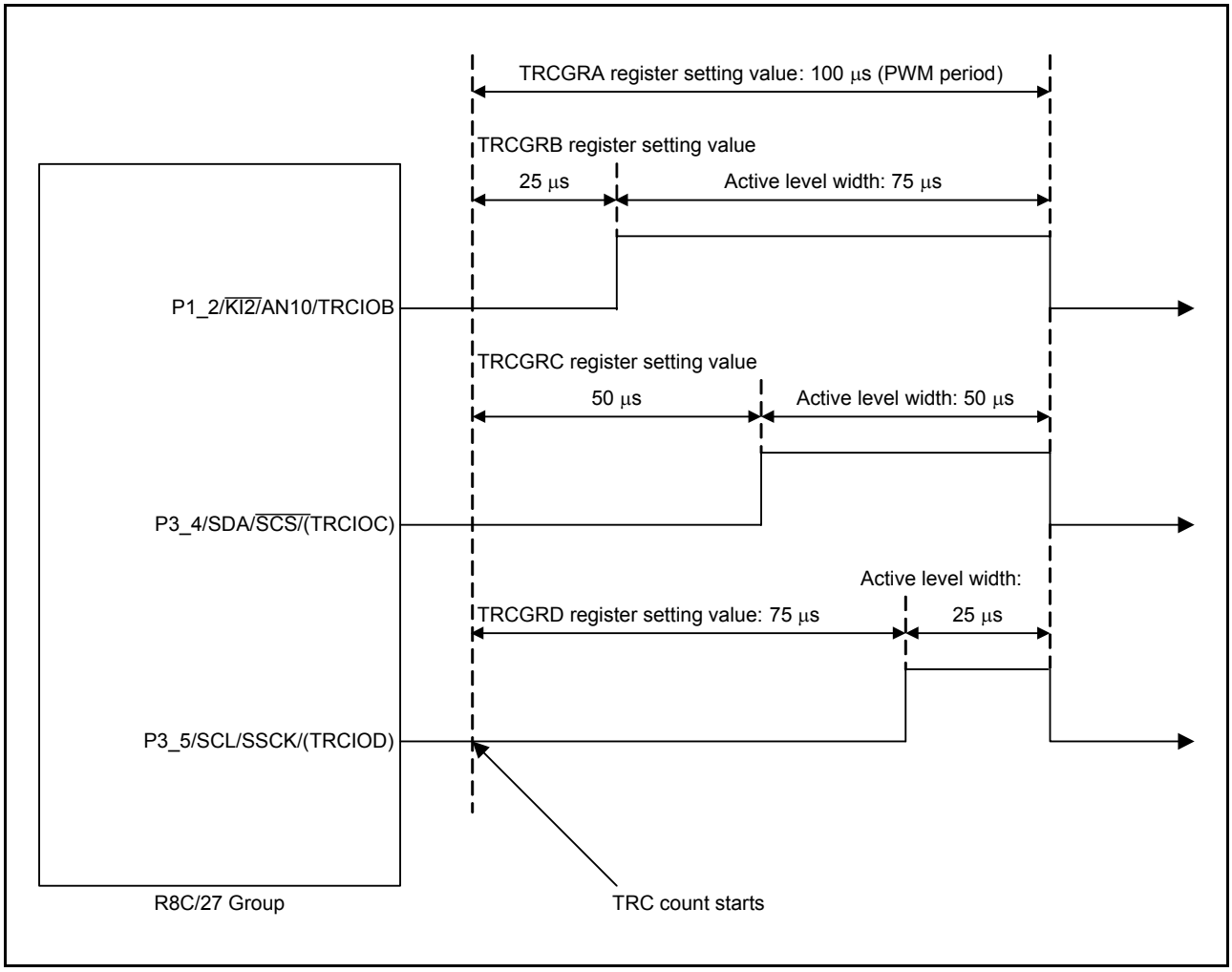


Figure 4.1 Pin Used

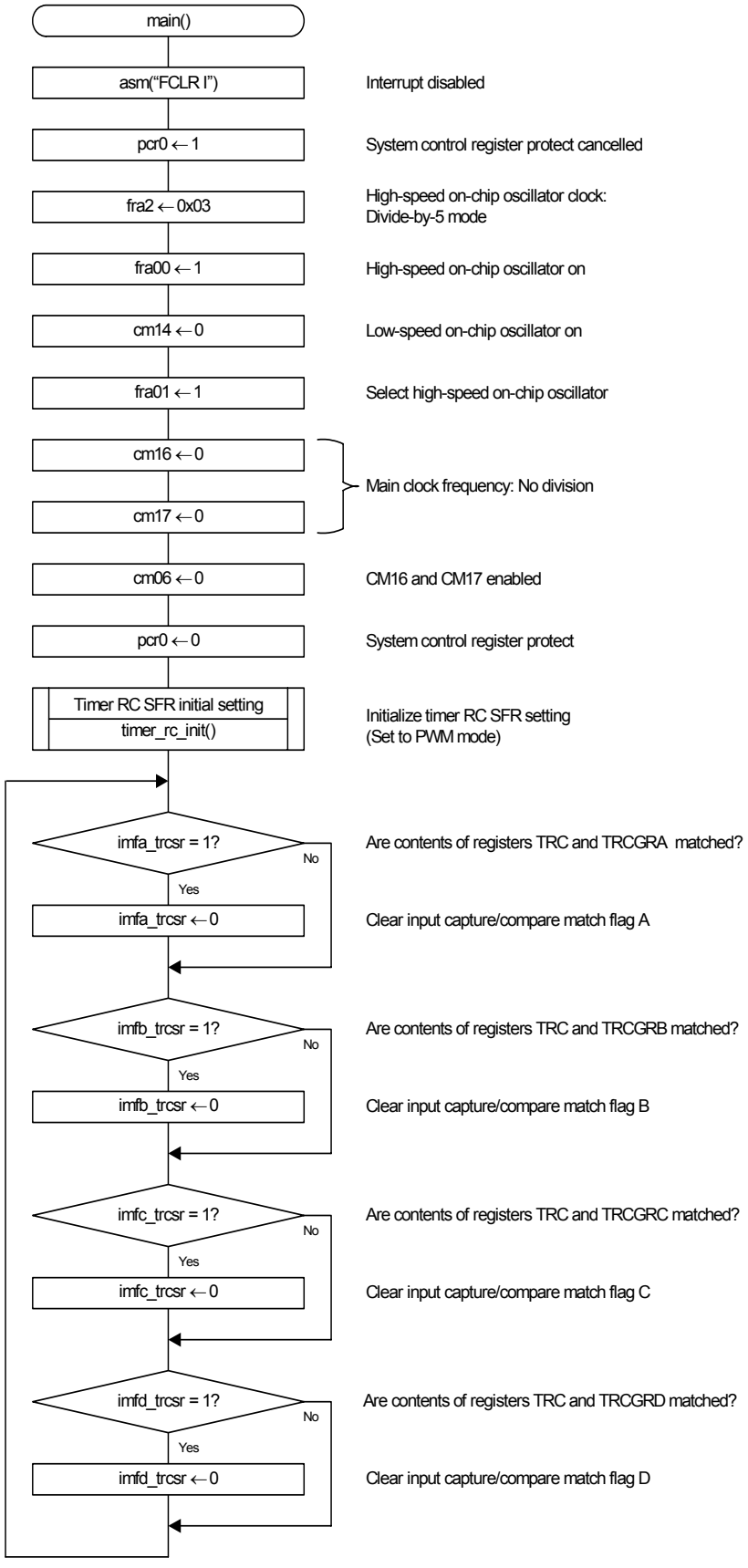
4.1 Function Table

Table 4.1

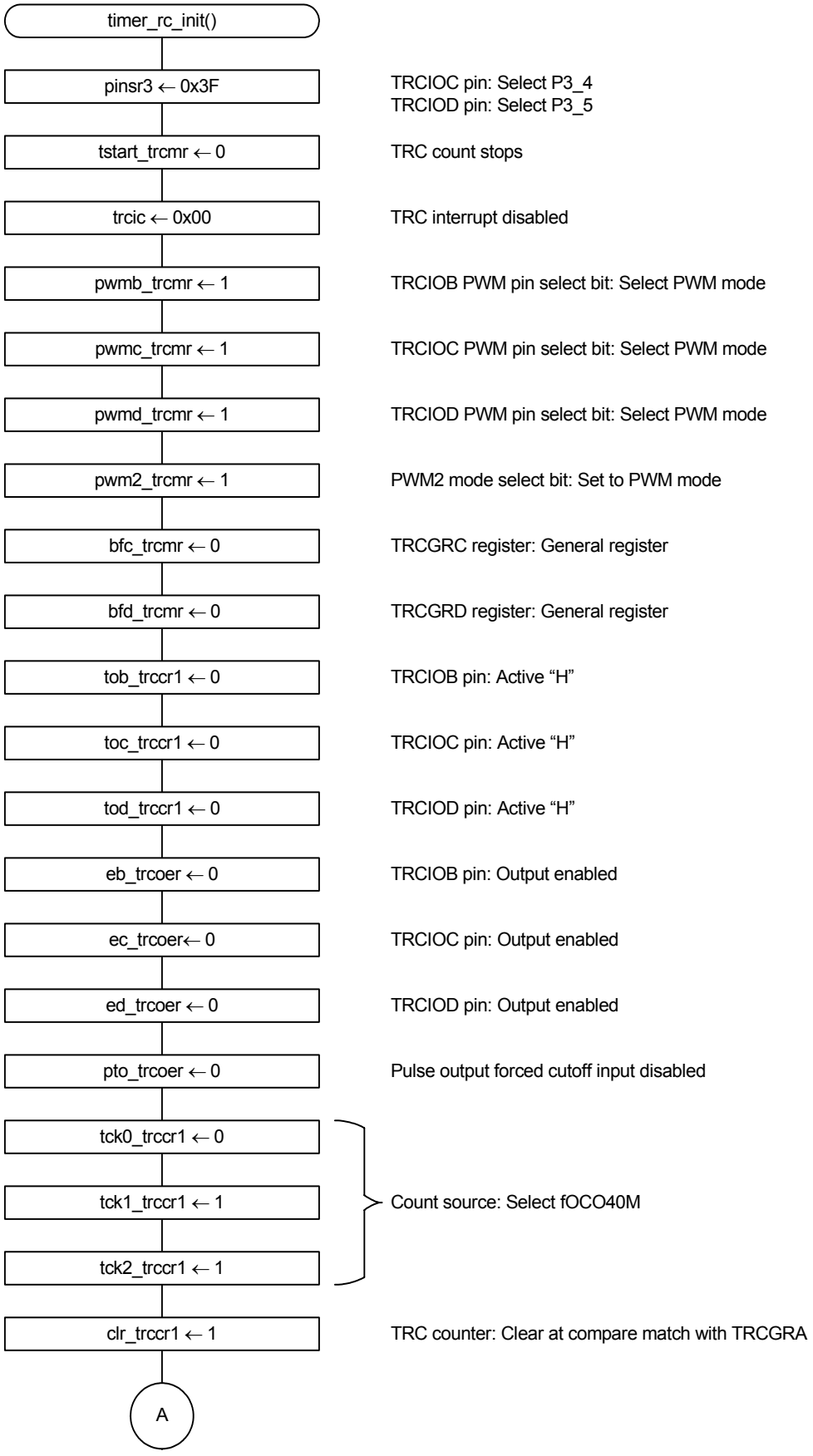
Declaration	void timer_rc_init(void)		
Overview	SFR initial setting associated with timer RC		
Argument	Argument name		Meaning
	None		
Variable used (global)	Variable name		Usage
	None		
Return value	Type	Value	Meaning
	None		
Function	Initialize the SFR registers associated with timer RC		

4.2 Flow chart

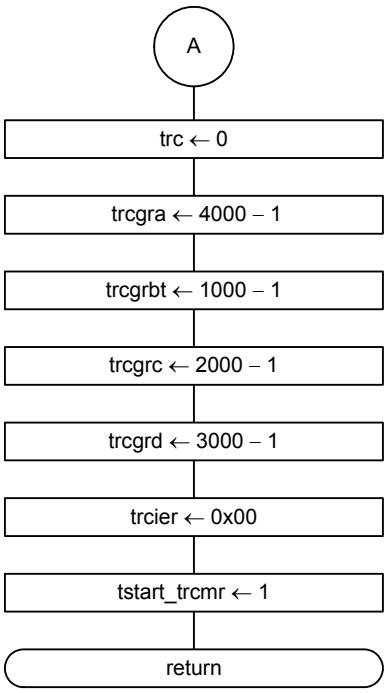
4.2.1 Main Function



4.2.2 Timer RC SER Initial Setting 1



4.2.3 Timer RC SER Initial Setting 2



Initialize TRC register count value to 0

Count period:
Set to 100 μs (25 ns × 4000 = 100 μs)

PWM output change point for TRCIOB pin:
Set to 25 μs (25 ns × 1000 = 25 μs)

PWM output change point for TRCIOC pin:
Set to 50 μs (25 ns × 2000 = 50 μs)

PWM output change point for TRCIOD pin:
Set to 75 μs (25 ns × 3000 = 75 μs)

Interrupt disabled

TRC count starts

5. Sample Programming Code

A sample program can be downloaded from the Renesas Technology website.
To download, click “Application Notes” in the left-hand side menu on the R8C/Tiny Series page.

6. Reference Documents

Hardware Manual
R8C/27 Group Hardware Manual
The latest version can be downloaded from the Renesas Technology website.

Technical Update/Technical News
The latest information can be downloaded from the Renesas Technology website.

Website and Support

Renesas Technology website
http://www.renesas.com/

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REVISION HISTORY	R8C/27 Group Timer RC in PWM Mode

Rev.	Date	Description	
		Page	Summary
1.00	Dec 01, 2006	–	First Edition issued
1.10	Oct 09, 2008	27	Flowchart revised
		–	Sample program revised

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