RL78/I1D

Power Supply Voltage Monitoring CC-RL

R01AN3417EJ0100
Rev. 1.00
Jan. 31, 2017

Introduction

This application note explains how to implement power supply voltage monitoring when selecting an internal reference voltage as the positive-side reference voltage of the A/D converter.

Target Device

RL78/I1D

When applying the sample program covered in this application note to another microcomputer, modify the program according to the specifications for the target microcomputer and conduct an extensive evaluation of the modified program.

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1. Specifications

1.1 Approaches to Measuring Power Supply Voltage

In this application note, an internal reference voltage is selected as the positive-side reference voltage of the A/D converter, and an external input voltage that has been resistively divided is measured using the A/D converter.

Table 1.1 shows the peripheral functions to be used and their usage. Figure 1.1 shows the basic circuit under measurement.

Table 1.1 Peripheral Functions to be Used and Their Usage

Peripheral Function	Usage
A/D converter	Measures resistive-divided power supply voltages.
12-bit interval timer	Triggers A/D conversion.
Timer array unit channel 1	Drives the LED. (0.5 sec period)

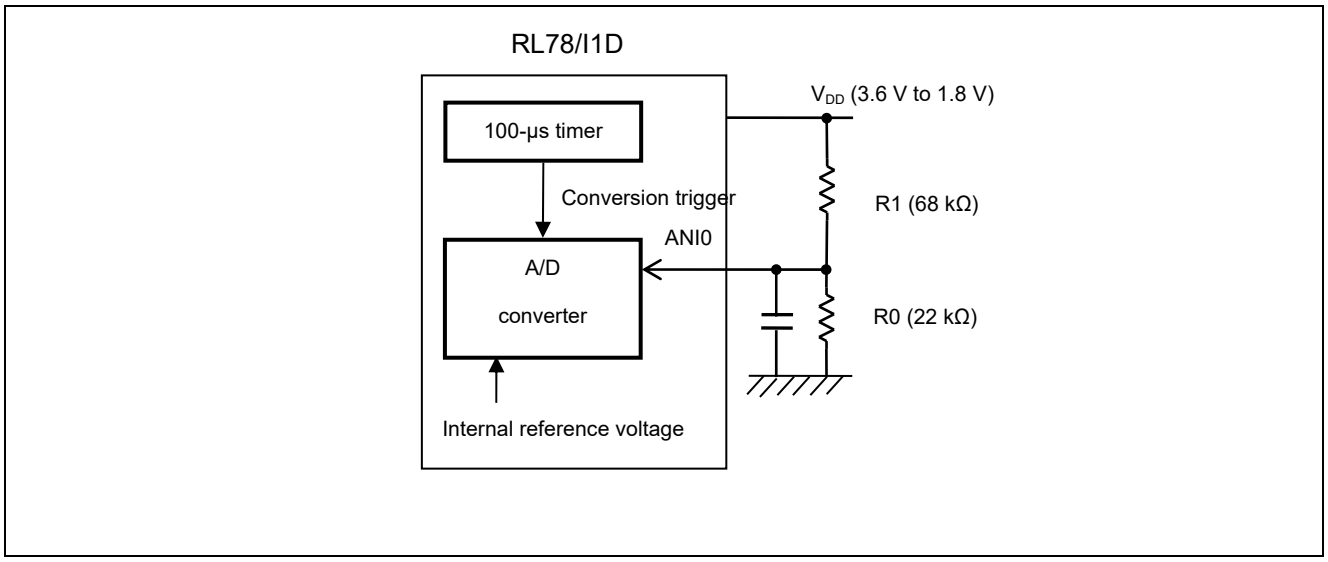

Figure 1.1 Basic Circuit

The input voltage to the ANI0 pin must be at or below the internal reference voltage (typ. 1.45 V). Hence a voltage obtained by resistive dividing of the power supply voltage is input to the ANI0 pin, as in figure 1.1.

In this application note, when the power supply voltage has fallen to 2.2 V or below, that is, when the voltage input to the ANI0 pin is at 0.54 V or lower, the voltage is judged to be low.

Moreover, in order to achieve the above specifications, the RL78/I1D is used in LS mode at an operating frequency of 8 MHz.

1.2 Analog Input Voltage Measurement Method

When selecting an internal reference voltage as the positive-side reference voltage of the A/D converter, while in the conversion-stopped state (ADCS = 0, ADCE = 0), set (ADREFP1, ADREFP0) = (1, 0). Then, after waiting for a stabilization wait time of at least 10 μs, set ADCE=1. In this application note, a hardware trigger wait mode is used, and so there is no need to count to the reference voltage stabilization wait time count B. Select ANI0 in the ADS register and wait for the A/D conversion start trigger.

In this application note, 8-bit resolution is selected. Further, it is assumed that power supply voltage changes are not sudden, and interrupts by a 12-bit interval timer at every 100 μs are used as the trigger for starting A/D conversion.

1.3 Evaluation of Conversion Result

In this application note, when the power supply voltage falls to 2.2 V or lower, that is, when the voltage input to the ANI0 pin drops to 0.54 V or below, the voltage is judged to be low. The internal reference voltage is typical 1.45 V, and so when the A/D conversion result is 0x5F or lower, an A/D conversion end interrupt is generated.

Moreover, after the A/D conversion end interrupt has been generated, the TO01 output causes an LED to blink.

1.4 Acquiring Data Flash Library

Before compiling, download the latest version of the data flash library, and copy the library files to a folder below the folder r01an3417_ad of this sample code.

Copy "pfdl.h", "pfdl.inc", and "pfdl_types.h" to the "incrl78" folder.

Copy "pfdl.lib" to the "librl78" folder.

The data flash library can be obtained from the Renesas Electronics website.

Please contact a Renesas Electronics sales office for details.

2. Conditions for Confirming Operations

The sample code operations described in this application note are confirmed under the following conditions.

Table 2.1 Operation Check Conditions

Item	Description
Microcontroller used	RL78/I1D (R5F117GC)
Operating frequency	- High-speed on-chip oscillator (HOCO) clock: 8 MHz - CPU/peripheral hardware clock: 8 MHz
Operation voltage	3 V (Operation is possible over a voltage range of 1.8 V to 3.6 V.) LVD operation (V_{LVD11}): Reset mode MIN. 1.8 V
Integrated development environment (CS+)	CS+ for CC V3.03.00 from Renesas Electronics Corp.
C compiler (CS+)	CC-RL V1.02.00 from Renesas Electronics Corp.
Integrated development environment (e^2 studio)	e^2 studio V4.0.0.26 from Renesas Electronics Corp.
C compiler (e^2 studio)	CC-RL V1.02.00 from Renesas Electronics Corp.
Data flash library (Type, Ver)	FDLRL78 Type04, Ver.1.05[Note]

Note: The latest version should be downloaded and evaluated before usage.

3. Related Application Notes

The application notes related to this application note are listed below for reference.

RL78/G13 Data Flash Library Type04 CC-RL (R01AN2827E) Application Note

4. Hardware Descriptions

4.1 Hardware Configuration Example

Figure 4.1 shows an example of the hardware configuration described in this application note.

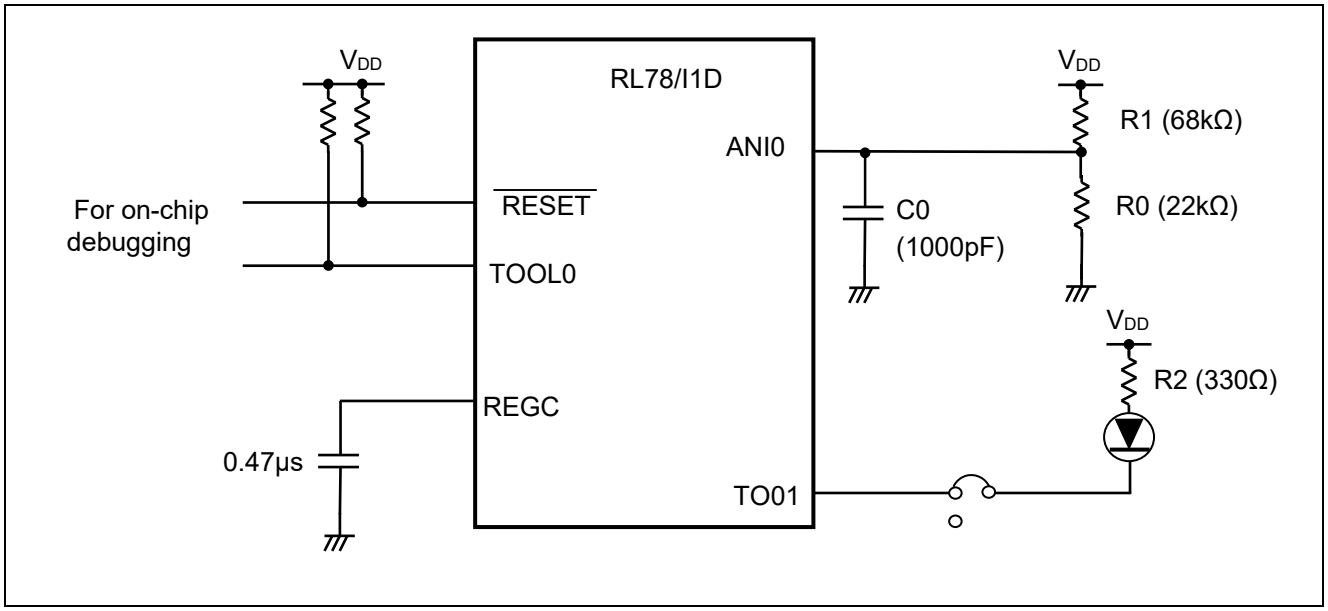

Figure 4.1 Hardware Configuration

Cautions: 1. This circuit diagram is simplified in order to show a summary of connections. When actually creating the circuit, pin processing and the like should be optimized and the circuit designed so as to satisfy the required electrical characteristics (input-only ports should be each connected to V_{DD} or V_{SS} via a resistor).

2. V_{DD} should be made equal to or higher than the reset release voltage (V_{LVD}) set using LVD.

4.2 List of Pins Used

Table 4.1 lists the pins used and their functions.

Table 4.1 Pins Used and their Functions

Pin Name	I/O	Function
P10/ANI0/AVREFP	Input	Analog input port
P30/TI00/TO01/VREF0	Output	Output for LED1 control

5. Software Descriptions

5.1 Operation Summary

In this application note, an internal reference voltage is selected as the positive-side reference voltage of the A/D converter, and an external input voltage that has been resistively divided is measured using the A/D converter.

A voltage input to the ANI0 pin every 100 μs is A/D-converted.

When the A/D conversion result falls to 0x5F or lower (when the power supply voltage is 2.2 V or below), an A/D conversion end interrupt is generated.

When the A/D conversion end interrupt is generated, the conversion result at that time is written to data flash memory. Also, the TO01 output is used to cause the LED1 to blink with a 0.5 s period.

(1) Set the initial A/D converter settings.

<A/D converter>

- The P10/ANI0 pin is used for analog input.
- Select mode is used to select the A/D conversion channel.
- The one-shot conversion mode is used as the A/D conversion operation mode.
- The hardware trigger wait mode is used as the A/D conversion trigger mode.

(2) The voltage input to the ANI0 pin every 100 μs is A/D-converted. As the hardware trigger signal, a 12-bit interval timer interrupt signal is used.

(3) When the A/D conversion result falls to 0x5F or lower, an A/D conversion end interrupt (INTAD) is generated.

(4) When the A/D conversion end interrupt is generated, the conversion result at that time is written to data flash memory. Further, the TO01 output is used to cause the LED1 to blink with a 0.5 sec period.

5.2 List of Option Byte Settings

Table 5.1 shows the settings of the option bytes.

Table 5.1 Option Byte Settings

Address	Setting Value	Description
000C0H	11101111B	Watchdog timer is stopped. (Counting stopped after a reset release)
000C1H	00111111B	LVD reset mode; 1.88 V (1.84 V to 1.88 V)
000C2H	11101010B	HS mode; High-speed on-chip oscillator: 8 MHz
000C3H	10000100B	On-chip debugging is enabled.

5.3 List of Constants

Table 5.2 lists the constants used in sample codes.

Table 5.2 Constants Used in Sample Codes

Constant	Setting	Content
TARGET_BLOCK	0	Target block for writing Note
BLOCK_SIZE	0x400	Size of one block (byte)
WRITE_SIZE	1	Size of write data (byte)
MAX_VALUE	0xFF	Maximum value of data flash write data
MAX_ADDRESS	(TARGET_BLOCK+1) * BLOCK_SIZE -1	Maximum value of data flash write address
PFDL_NG	1	Abnormal termination of data flash library processing
FDL_FRQ	8	Frequency setting [MHz]
FDL_VOL	0x00	Voltage mode (full-speed mode)

Note: The valid range for TARGET_BLOCK is 0 to 3. If a value outside this range is set, an error occurs during build. The relation between the setting for TARGET_BLOCK and the block for writing is described below.

0: The block for writing is block 0 of data flash memory (address 0xF1000 to 0xF13FF)

1: The block for writing is block 1 of data flash memory (address 0xF1400 to 0xF17FF)

2: The block for writing is block 2 of data flash memory (address 0xF1800 to 0xF1BFF)

3: The block for writing is block 3 of data flash memory (address 0xF1C00 to 0xF1FFF)

5.4 List of Variables

Table 5.3 lists the global variables.

Table 5.3 Global Variables

Type	Variable Name	Contents	Function Used
uint8_t	g_result_buffer	AD conversion result storage buffer	main r_adc_interrupt
uint8_t	g_read_value	Read value	R_FDL_Read R_FDL_ExecuteWrite
uint8_t	g_write_value	Write value	main R_FDL_Read R_FDL_ExecuteWrite R_FDL_Write r_adc_interrupt
uint16_t	g_write_address	Target address for writing	R_FDL_BlankCheck R_FDL_Read R_FDL_Write R_FDL_ChangeAddress

5.5 List of Functions

Table 5.4 lists the functions used.

Table 5.4 Functions

Function Name	Summary
R_ADC_Set_OperationOn	Enables A/D voltage comparator operation
R_ADC_Start	Starts A/D conversion.
R_ADC_Stop	Stops A/D conversion.
r_adc_interrupt	Processes A/D conversion end interrupt.
R_IT_Start	Starts 12-bit interval timer.
R_IT_Stop	Stops 12-bit interval timer.
R_TAU0_Channel1_Start	TAU0 channel 1 operation start setting
R_TAU0_Channel1_Stop	TAU0 channel 1 operation stop setting

5.6 Function Specifications

The following gives the specifications of the functions used in the sample code.

[Function name] R_ADC_Set_OperationOn

Summary	Enables A/D voltage comparator operation.
Header	r_cg_adc.h, r_cg_userdefine.h
Declaration	void R_ ADC_Set_OperationOn(void)
Description	Enables A/D voltage comparator operation.
Arguments	None
Return values	None
Remarks	None

[Function name] R_ADC_Start

Summary	Starts A/D conversion.
Header	r_cg_adc.h, r_cg_userdefine.h
Declaration	void R_ ADC_Start(void)
Description	Starts A/D conversion.
Arguments	None
Return values	None
Remarks	None

[Function name] R_ADC_Stop

Summary	Stops A/D conversion.
Header	r_cg_adc.h, r_cg_userdefine.h
Declaration	void R_ ADC_Stop(void)
Description	Stops A/D conversion.
Arguments	None
Return values	None
Remarks	None

[Function name] r_adc_interrupt

Summary	Processes A/D conversion end interrupt.
Header	r_cg_adc.h, r_cg_userdefine.h
Declaration	static void __near r_adc_interrupt_error(void)
Description	This interrupt processing is performed when A/D conversion result is 0x5f or lower.
Arguments	None
Return values	None
Remarks	None

[Function name] R_IT_Start

Summary	Starts 12-bit interval timer.
Header	r_cg_it.h, r_cg_userdefine.h
Declaration	void R_IT_Start (void)
Description	Starts 12-bit interval timer operation.
Arguments	None
Return values	None
Remarks	None

[Function name] R_IT_Stop

Summary	Stops 12-bit interval timer.
Header	r_cg_it.h, r_cg_userdefine.h
Declaration	void R_TAU0_Channel1_Stop (void)
Description	Stops 12-bit interval timer operation.
Arguments	None
Return values	None
Remarks	None

[Function name] R_TAU0_Channel1_Start

Summary	TAU0 channel 1 operation start setting
Header	r_cg_tau.h, r_cg_userdefine.h
Declaration	void R_TAU0_Channel1_Start (void)
Description	Cancels TAU0 channel 1 interrupt mask.
Arguments	None
Return values	None
Remarks	None

[Function name] R_TAU0_Channel1_Stop

Summary	TAU0 channel 1 operation stop setting
Header	r_cg_tau.h, r_cg_userdefine.h
Declaration	void R_TAU0_Channel1_Stop (void)
Description	Masks TAU0 channel 1 interrupts.
Arguments	None
Return values	None
Remarks	None

5.7 Flowcharts

Figure 5.1 shows the overall flow of the process described in this application note.

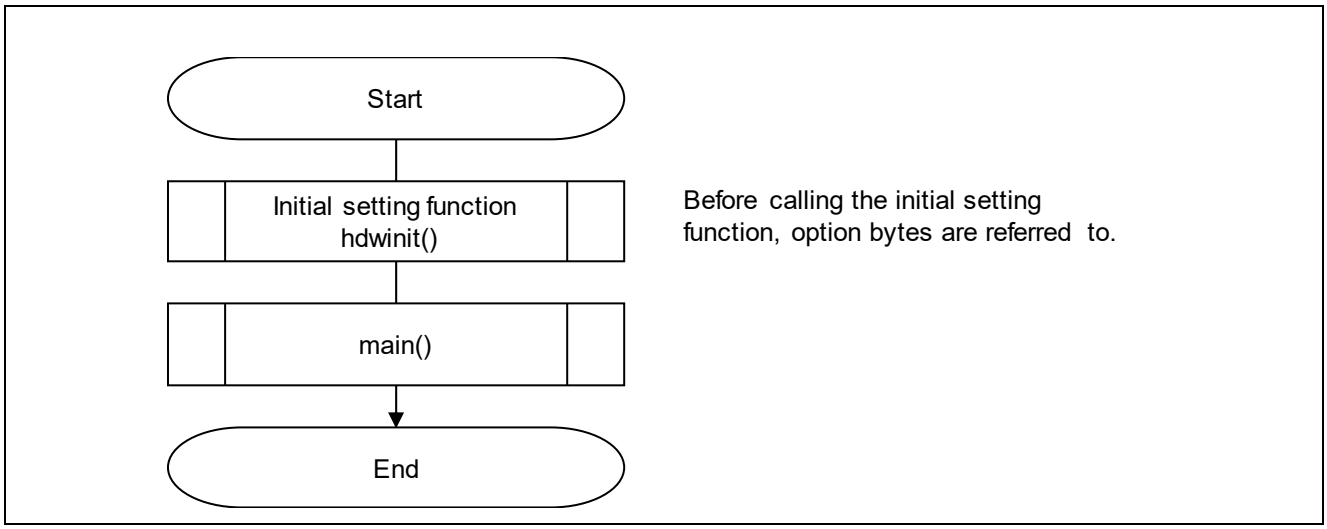

Figure 5.1 Overall Flow

Note: The start-up routine is executed before and after the initial setting function.

5.7.1 Initial Setting Function

Figure 5.2 shows the flowchart of the initial setting function.

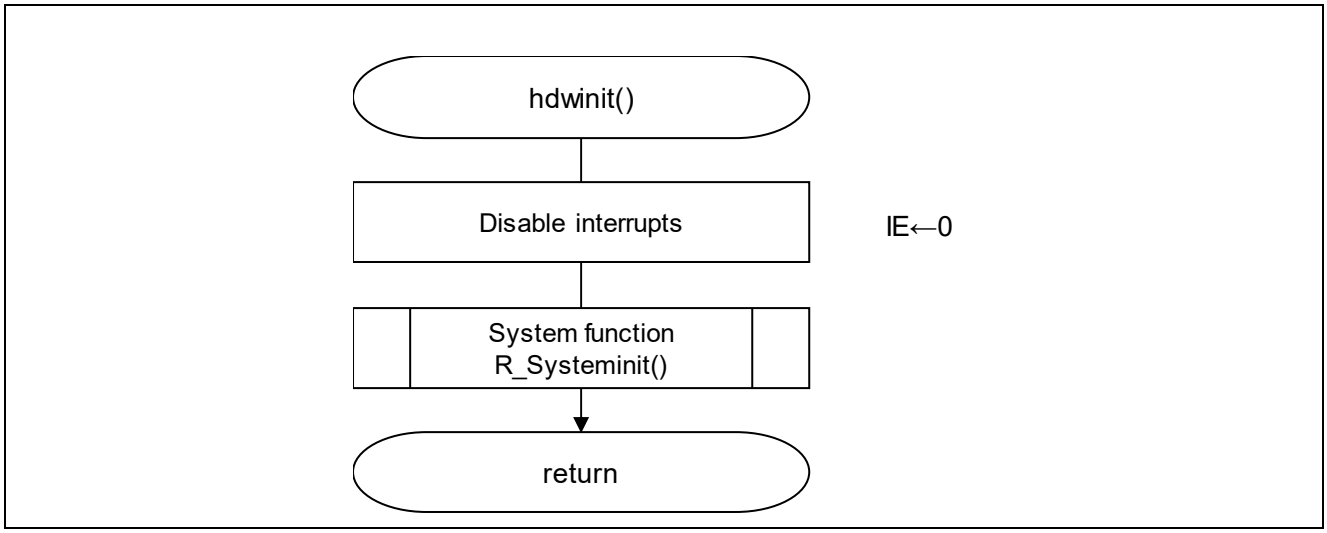

Figure 5.2 Initial Setting Function

5.7.2 System Function

Figure 5.3 shows the flowchart of the system function.

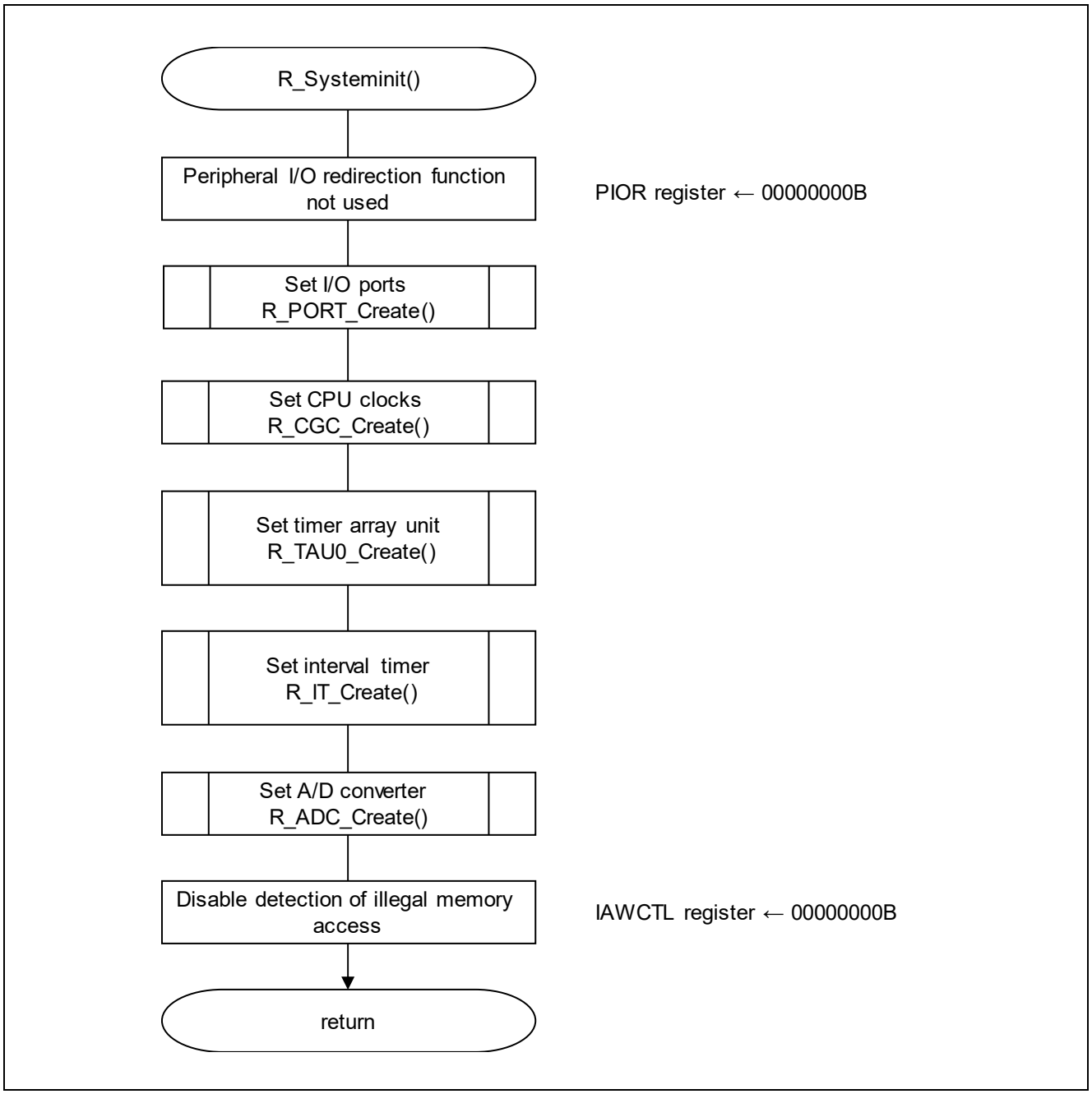

Figure 5.3 System Function

5.7.3 Setting I/O Ports

Figure 5.4 shows the flowchart for setting the I/O ports.

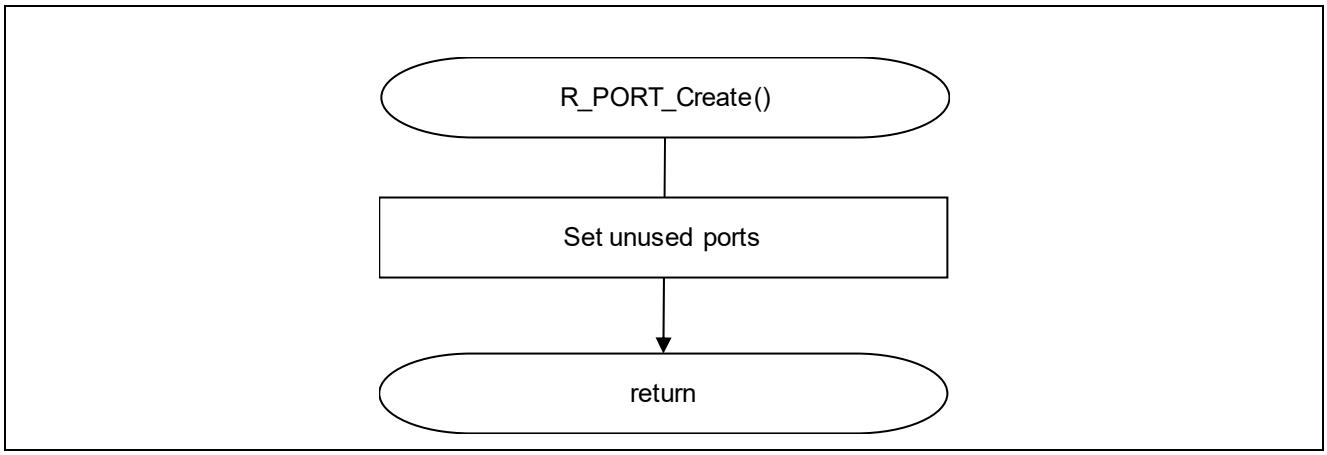

Figure 5.4 Setting I/O Ports

Note: For settings of unused ports, refer to the RL78/I1D User's Manual: Hardware.

Caution: Unused ports should be designed so that the electrical characteristics are satisfied by appropriately treating the pertinent pins. Separately connect unused input-only ports to VDD or VSS via a resistor.

5.7.4 Setting CPU Clocks

Figure 5.5 shows the flowchart for setting the CPU clocks.

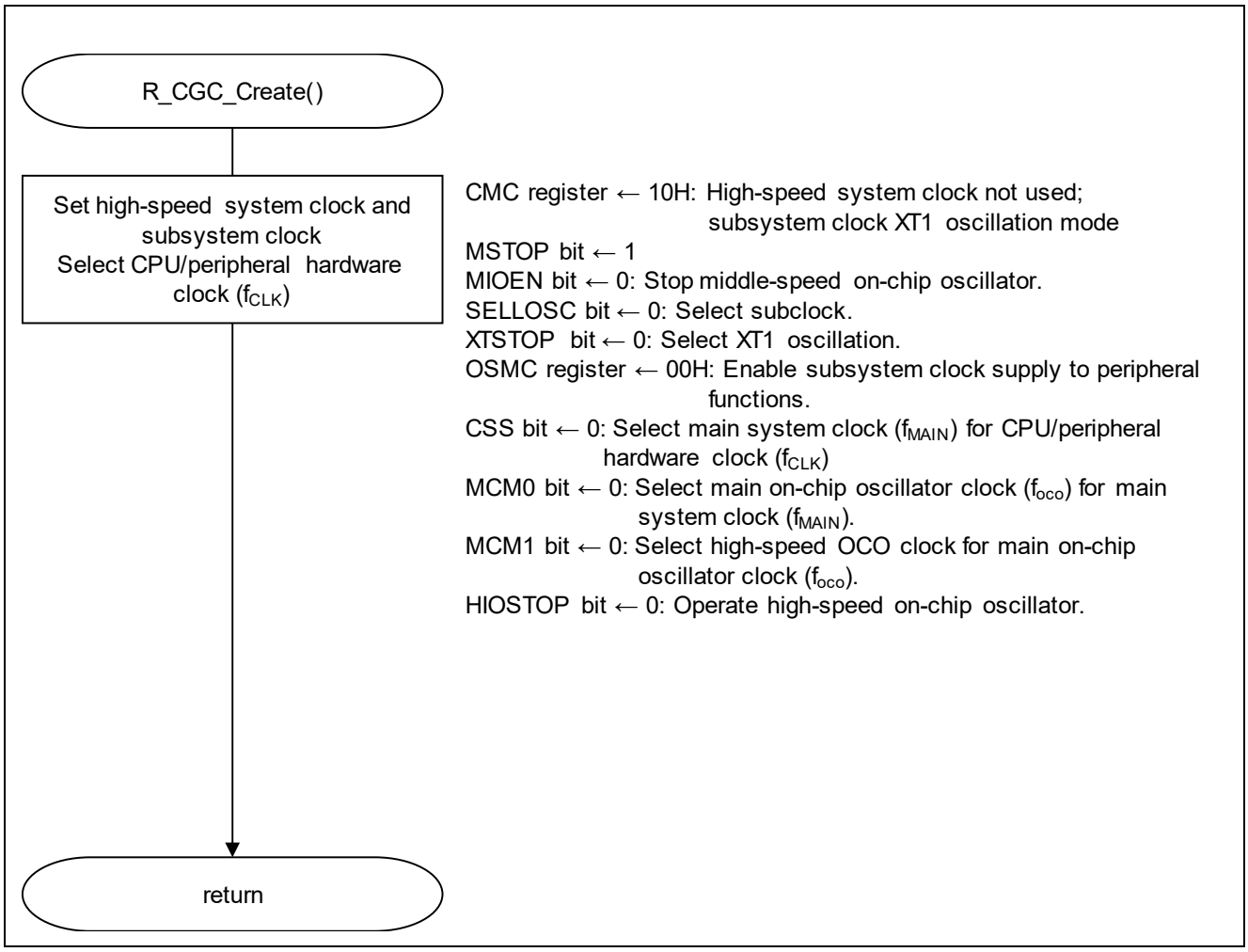

Figure 5.5 Setting CPU Clocks

5.7.5 Setting A/D Converter

Figure 5.6 shows the flowchart for setting the A/D converter.

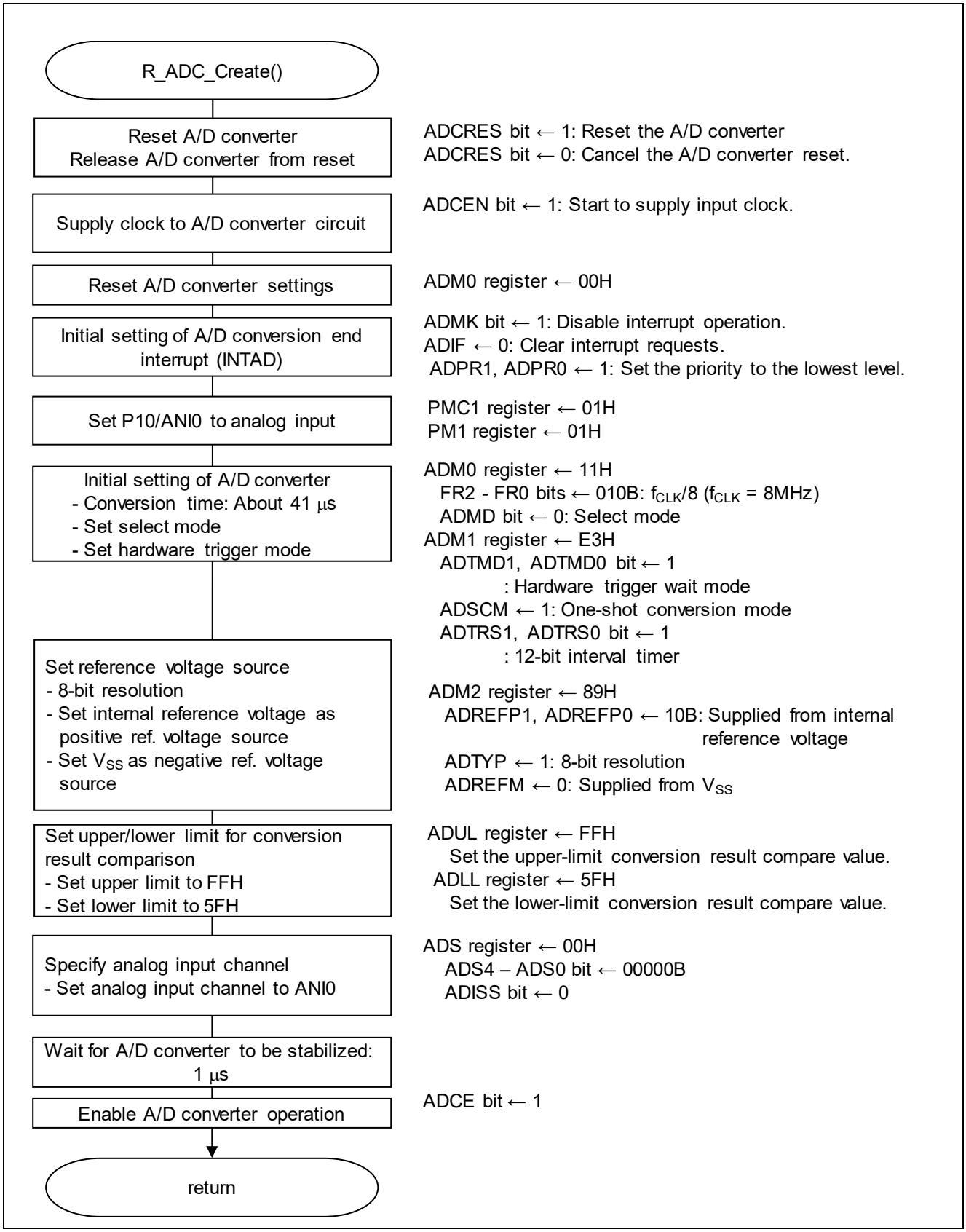

Figure 5.6 Setting A/D Converter

Controlling reset of A/D converter

- Peripheral reset control register 0 (PRR0)

Control reset of the A/D converter.

Symbol: PRR0

7	6	5	4	3	2	1	0
0	0	ADCRES	0	0	SAU0RES	0	TAU0RES
0	0	**1/0**	0	0	x	0	x

Bit 5

ADCRES	Reset control of A/D converter
0	**A/D converter reset release**
1	**A/D converter reset state**

Starting clock supply to A/D converter

- Peripheral enable register 0 (PER0)

Start supplying clock to the A/D converter.

Symbol: PER0

7	6	5	4	3	2	1	0
RTCEN	0	ADCEN	0	0	SAU0EN	0	TAU0EN
x	0	**1**	0	0	x	0	x

Bit 5

ADCEN	Control of A/D converter input clock supply
0	Stops input clock supply.
1	**Enables input clock supply.**

Setting A/D conversion time and operation mode

- A/D converter mode register 0 (ADM0)

Control the A/D conversion operation.

Set the A/D conversion channel select mode.

Symbol: ADM0

7	6	5	4	3	2	1	0
ADCS	ADMD	FR2	FR1	FR0	LV1	LV0	ADCE
x	**0**	**0**	**1**	**0**	**0**	**0**	x

Bit 6

ADMD	Specification of A/D conversion channel selection mode
0	**Select mode**
1	Scan mode

Note: For details of register settings, refer to the RL78/I1D User's Manual: Hardware.

Symbol: ADM0

7	6	5	4	3	2	1	0
ADCS	ADMD	FR2	FR1	FR0	LV1	LV0	ADCE
x	**0**	**0**	**1**	**0**	**0**	**0**	x

Bits 5 to 1

ADM0					Conv clock (f_{AD})	A/D power supply stabili-zation wait clock	No. of conv. clock (Samp-ling clock)	Conv. time	Conversion time selection				
FR2	FR1	FR0	LV1	LV2					f_{CLK}= 1 MHz	f_{CLK}= 4 MHz	f_{CLK}= 8 MHz	f_{CLK}= 16 MHz	f_{CLK}= 24 MHz
0	0	0	**0**	**0**	$f_{CLK}/32$	**4 f_{CLK}**	**41 f_{AD} (Samp-ling: 11 f_{AD})**	$1316/f_{CLK}$	Setting prohibited	Setting prohibited	Setting prohibited	Setting prohibited	54.8333µs
0	0	1			$f_{CLK}/16$			$660/f_{CLK}$				41.25µs	27.5µs
0	**1**	**0**			**$f_{CLK}/8$**			**$332/f_{CLK}$**			**41.5µs**	20.75µs	13.8333µs
0	1	1			$f_{CLK}/6$			$250/f_{CLK}$			31.25µs	15.625µs	10.4167µs
1	0	0			$f_{CLK}/5$			$209/f_{CLK}$			26.125µs	13.0625µs	8.7083µs
1	0	1			$f_{CLK}/4$			$168/f_{CLK}$		42µs	21µs	10.5µs	7µs
1	1	0			$f_{CLK}/2$			$86/f_{CLK}$		21.5µs	10.75µs	5.375µs	3.5833µs
1	1	1			$f_{CLK}/1$	2 f_{CLK}		$43/f_{CLK}$	43µs	10.75µs	5.375µs	2.6875µs	Setting prohibited
0	0	0	0	1	$f_{CLK}/32$	58 f_{CLK}	53 f_{AD} (Samp-ling clock: 23 f_{AD})	$1754/f_{CLK}$	Setting prohibited	Setting prohibited	Setting prohibited	Setting prohibited	73.0833µs
0	0	1			$f_{CLK}/16$			$906/f_{CLK}$				55.625µs	37.75µs
0	1	0			$f_{CLK}/8$			$482/f_{CLK}$			60.25µs	30.125µs	20.0833µs
0	1	1			$f_{CLK}/6$			$376/f_{CLK}$			47µs	23.5µs	15.6667µs
1	0	0			$f_{CLK}/5$			$323/f_{CLK}$			40.375µs	20.1875µs	13.4583µs
1	0	1			$f_{CLK}/4$			$270/f_{CLK}$		67.5µs	33.75µs	16.875µs	11.25µs
1	1	0			$f_{CLK}/2$			$164/f_{CLK}$		41µs	20.5µs	10.25µs	6.833µs
1	1	1			$f_{CLK}/1$	29 f_{CLK}		$82/f_{CLK}$	82µs	20.5µs	10.25µs	5.125µs	Setting prohibited
0	0	0	1	0	$f_{CLK}/32$	15 f_{CLK}	63 f_{AD} (Samp-ling clock: 33 f_{AD})	$2031/f_{CLK}$	Setting prohibited	Setting prohibited	Setting prohibited	Setting prohibited	84.625µs
0	0	1			$f_{CLK}/16$			$1023/f_{CLK}$				63.975µs	42.625µs
0	1	0			$f_{CLK}/8$			$519/f_{CLK}$			64.875µs	32.4375µs	21.625µs
0	1	1			$f_{CLK}/6$			$393/f_{CLK}$			49.125µs	24.5625µs	16.375µs
1	0	0			$f_{CLK}/5$			$330/f_{CLK}$			41.25µs	20.625µs	13.75µs
1	0	1			$f_{CLK}/4$			$264/f_{CLK}$		66.75µs	33.375µs	16.6875µs	11.125µs
1	1	0			$f_{CLK}/2$			$141/f_{CLK}$		35.25µs	17.625µs	8.8125µs	5.875µs
1	1	1			$f_{CLK}/1$			$78/f_{CLK}$	78µs	19.5µs	9.75µs	4.875µs	Setting prohibited
0	0	0	1	1	$f_{CLK}/32$	8 f_{CLK}	217 f_{AD} (Samp-ling clock: 187 f_{AD})	$6952/f_{CLK}$	Setting prohibited	Setting prohibited	Setting prohibited	Setting prohibited	289.67µs
0	0	1			$f_{CLK}/16$			$3480/f_{CLK}$				217.5µs	145µs
0	1	0			$f_{CLK}/8$			$1744/f_{CLK}$			218µs	109µs	72.67µs
0	1	1			$f_{CLK}/6$			$1310/f_{CLK}$			163.75µs	81.875µs	54.58µs
1	0	0			$f_{CLK}/5$			$1093/f_{CLK}$			136.625µs	68.3125µs	45.54µs
1	0	1			$f_{CLK}/4$			$876/f_{CLK}$		219µs	109.5µs	54.75µs	36.5µs
1	1	0			$f_{CLK}/2$			$442/f_{CLK}$		110.5µs	55.25µs	27.625µs	18.42µs
1	1	1			$f_{CLK}/1$			$225/f_{CLK}$	225µs	56.25µs	28.125µs	14.0625µs	Setting prohibited

Note: For details of register settings, refer to the RL78/I1D User's Manual: Hardware.

Setting A/D conversion trigger mode

- A/D converter mode register 1 (ADM1)
  Select the A/D conversion trigger mode.
  Specify the A/D conversion operation mode
  Select the hardware trigger signal.

Symbol: ADM1

7	6	5	4	3	2	1	0
ADTMD1	ADTMD0	ADSCM	0	0	0	ADTRS1	ADTRS0
1	**1**	**1**	0	0	0	**1**	**1**

Bits 7 and 6

ADTMD1	ADTMD0	Selection of A/D conversion trigger mode
0	x	Software trigger mode
1	0	Hardware trigger no-wait mode
1	**1**	**Hardware trigger wait mode**

Bit 5

ADSCM	Specification of A/D conversion mode
0	Sequential conversion mode
1	**One-shot conversion mode**

Bits 1 and 0

ADTRS1	ADTRS0	Selection of hardware trigger signal
0	0	End of timer channel 1 count or capture interrupt signal (INTTM01)
0	1	Event signal selected by ELC
1	0	Real-time clock 2 interrupt signal (INTRTC)
1	**1**	**12-bit interval timer interrupt signal (INTIT)**

Note: For details of register settings, refer to the RL78/I1D User's Manual: Hardware.

Setting reference voltage source

- A/D converter mode register 2 (ADM2)

Select the A/D converter positive-side reference voltage source.
Select the A/D converter negative-side reference voltage source.
Check the conversion result upper-limit/lower-limit value
Set SNOOZE mode.
Select A/D conversion resolution.

Symbol: ADM2

7	6	5	4	3	2	1	0
ADREFP1	ADREFP0	ADREFM	0	ADRCK	AWC	0	ADTYP
1	**0**	**0**	0	**1**	**0**	0	**1**

Bits 7 and 6

ADREFP1	ADREFP0	Selection of + side reference voltage source of A/D converter
0	0	Supplied from V_{DD}
0	1	Supplied from AV_{REFP}/ANI0
1	**0**	**Supplied from internal reference voltage (1.45 V)**
1	1	Setting prohibited

Bit 5

ADREFM	Selection of – side reference voltage source of A/D converter
0	**Supplied from V_{SS}**
1	Supplied from AV_{REFM}/ANI1

Bit 3

ADRCK	Checking upper limit and lower limit conversion result values
0	Interrupt signal (INTAD) is generated when the ADLL register ≤ the ADCR register ≤ the ADUL register.
1	**Interrupt signal (INTAD) is generated when ADCR register < ADLL register, ADUL register < ADCR register.**

Bit 2

AWC	Specification of SNOOZE mode
0	**Do not use the SNOOZE mode function.**
1	Use the SNOOZE mode function.

Bit 0

ADTYP	Selection of A/D conversion resolution
0	10-**bit resolution**
1	**8-bit resolution**

Note: For details of register settings, refer to the RL78/I1D User's Manual: Hardware.

Setting upper limit and lower limit values for conversion result comparison

- Conversion result comparison upper limit setting register (ADUL)
- Conversion result comparison lower limit setting register (ADLL)

Set the upper limit and lower limit conversion result compare values.

Symbol: ADUL

7	6	5	4	3	2	1	0
ADUL7	ADUL6	ADUL5	ADUL4	ADUL3	ADUL2	ADUL1	ADUL0
1	**1**	**1**	**1**	**1**	**1**	**1**	**1**

Symbol: ADLL

7	6	5	4	3	2	1	0
ADLL7	ADLL6	ADLL5	ADLL4	ADLL3	ADLL2	ADLL1	ADLL0
0	**1**	**0**	**1**	**1**	**1**	**1**	**1**

Note: For details of register settings, refer to the RL78/I1D User's Manual: Hardware.

Setting input channel

- Analog input channel specification register (ADS)
  Specify the input channel of analog voltage to be converted.

Symbol: ADS

7	6	5	4	3	2	1	0
ADISS	0	0	ADS4	ADS3	ADS2	ADS1	ADS0
0	x	x	**0**	**0**	**0**	**0**	**0**

Bits 7, 4 to 0

ADISS	ADS4	ADS3	ADS2	ADS1	ADS0	Analog input channel	Input source
0	**0**	**0**	**0**	**0**	**0**	**ANI0**	**P10/ANI0/AV_{REFP} pin**
0	0	0	0	0	1	ANI1	P11/ANI1/AV_{REFM} pin
0	0	0	0	1	0	ANI2	P12/ANI2 pin
0	0	0	0	1	1	ANI3	P13/ANI3 pin
0	0	0	1	0	0	ANI4	P14/ANI4 pin
0	0	0	1	0	1	ANI5	P15/ANI5 pin
0	0	0	1	1	0	ANI6	P16/ANI6 pin
0	0	0	1	1	1	ANI7	P17/ANI7 pin
0	0	1	0	0	0	ANI8	P25/ANI8 pin
0	0	1	0	0	1	ANI9	P24/ANI9 pin
0	0	1	0	1	0	ANI10	P23/ANI10 pin
0	0	1	0	1	1	ANI11	P22/ANI11 pin
0	0	1	1	0	0	ANI12	P21/ANI12 pin
0	0	1	1	0	1	ANI13	P20/ANI13 pin
0	0	1	1	1	0	ANI16	P02/ANI16 pin
0	0	1	1	1	1	ANI17	P03/ANI17 pin
0	1	0	0	0	0	ANI18	P04/ANI18 pin
1 Note 1	0	0	0	0	0 Note 2	—	Temperature sensor output voltage
1 Note 1	0	0	0	0	1 Note 3	—	Internal reference voltage (1.45V)
Other than the above						Setting prohibited	

Note 1: When setting the ADISS bit to 1 after having previously set it to 1 (i.e. in the sequence ADISS = 1 → 0 → 1), at least 300 µs must elapse after the setting of the ADISS bit was 1 before it is again set to 1.

Note 2: When setting the ADS0 bit to 0 after having previously set it to 0 while the setting of the ADISS bit is 1 (i.e. in the sequence (ADISS, ADS0) = (1,0) → (1,1) → (1,0)), at least 100 µs must elapse after the setting of the ADS0 bit was 0 before it is again set to 0.

Note 3: When setting the ADS0 bit to 1 after having previously set it to 1 while the setting of the ADISS bit is 1 (i.e. in the sequence (ADISS, ADS0) = (1,1) → (1,0) → (1,1)), at least 100 µs must elapse after the setting of the ADS0 bit was 1 before it is again set to 1.

Note: For details of register settings, refer to the RL78/I1D User's Manual: Hardware.

Setting A/D conversion end interrupt

- Interrupt request flag register (IF1H)
  Clear interrupt request flags.
- Interrupt mask flag register (MK1H)
  Disable interrupt processing.

Symbol: IF1H

7	6	5	4	3	2	1	0
0	DOCIF	CMPIF1	CMPIF0	KRIF	TMKAIF	RTCIF	ADIF
0	x	x	x	x	x	x	**0**

Bit 0

ADIF	Interrupt request flag
0	**No interrupt request signal is generated**
1	Interrupt request is generated, interrupt request status

Symbol: MK1H

7	6	5	4	3	2	1	0
0	DOCMK	CMPMK1	CMPMK0	KRMK	TMKAMK	RTCMK	ADMK
x	x	x	x	x	x	x	**1**

Bit 0

ADMK	Interrupt servicing control
0	Interrupt servicing enabled
1	**Interrupt servicing disabled**

Note: For details of register settings, refer to the RL78/I1D User's Manual: Hardware.

5.7.6 Setting Timer Array Unit

Figure 5.7 shows the flowchart for setting the timer array unit.

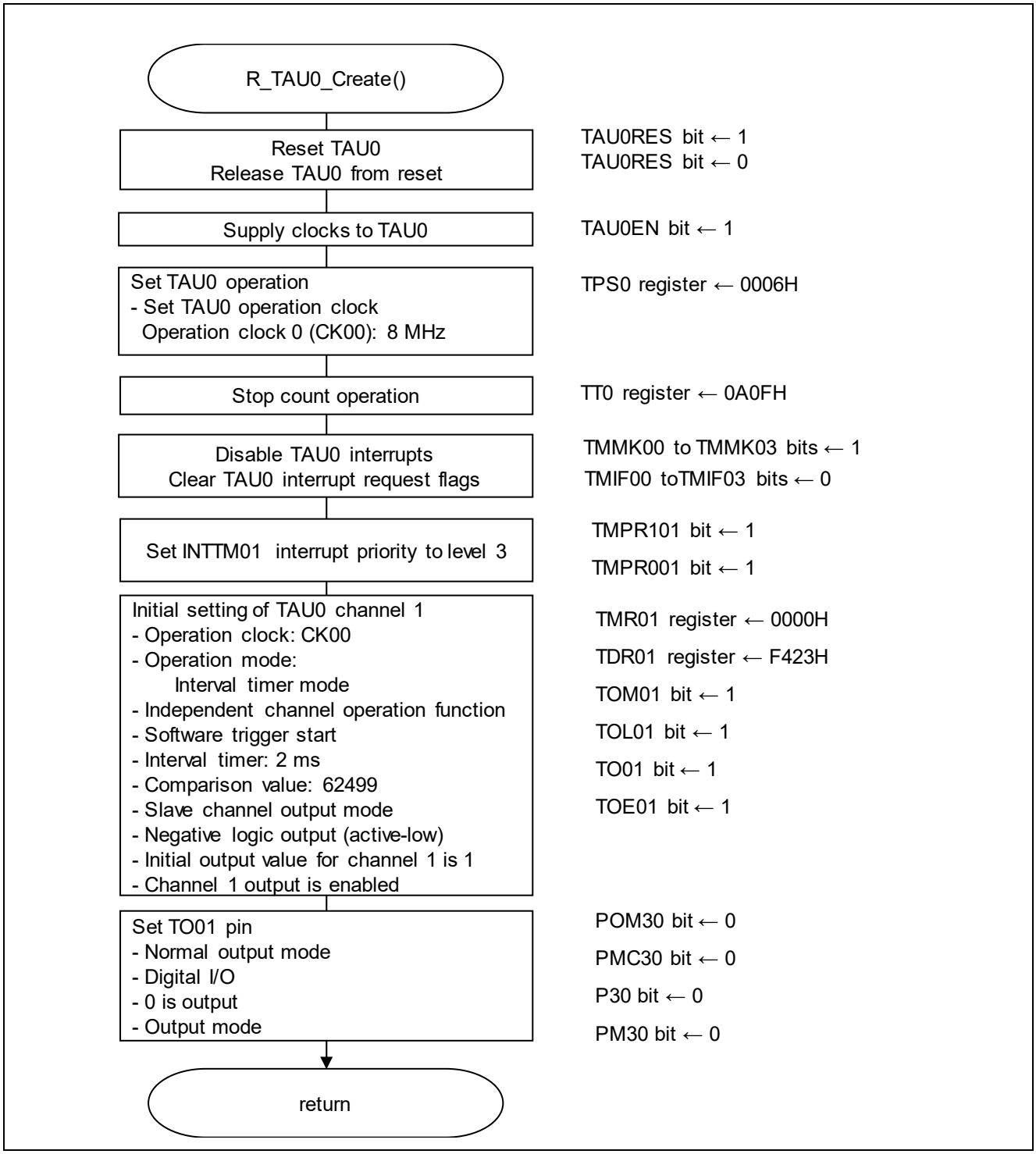

Figure 5.7 Setting Timer Array Unit

Controlling reset of timer array unit 0

- Peripheral reset control register 0 (PRR0)

Control reset of the timer array unit 0.

Symbol: PRR0

7	6	5	4	3	2	1	0
0	0	ADCRES	0	0	SAU0RES	0	TAU0RES
0	0	x	0	0	x	0	**1/0**

Bit 0

TAU0RES	Reset control of timer array unit 0
0	**Timer array unit reset release**
1	**Timer array unit reset state**

Starting clock supply to timer array unit 0

- Peripheral enable register 0 (PER0)

Start clock supply to timer array unit 0.

Symbol: PER0

7	6	5	4	3	2	1	0
RTCEN	0	ADCEN	0	0	SAU0EN	0	TAU0EN
x	0	x	0	0	x	0	**1**

Bit 0

TAU0EN	Control of timer array unit 0 input clock supply
0	Stops input clock supply.
1	**Enables input clock supply.**

Note: For details of register settings, refer to the RL78/I1D User's Manual: Hardware.

Setting timer clock frequency

- Timer clock select register 0 (TPS0)

Select the operation clock for timer array unit 0.

Symbol: TPS0

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	PRS031	PRS030	0	0	PRS021	PRS020	PRS013	PRS012	PRS011	PRS010	PRS003	PRS002	PRS001	PRS000
x	x	x	x	x	x	x	x	x	x	x	x	**0**	**1**	**1**	**0**

Bits 3 to 0

PRS003	PRS002	PRS001	PRS000		Selection of operation clock (CK00)				
					f_{CLK}= 2MHz	f_{CLK}= 5MHz	f_{CLK}= 10MHz	f_{CLK}= 20MHz	f_{CLK}= 24MHz
0	0	0	0	f_{CLK}	2 MHz	5 MHz	10 MHz	20 MHz	24 MHz
0	0	0	1	$f_{CLK}/2$	1 MHz	2.5 MHz	5 MHz	10 MHz	12 MHz
0	0	1	0	$f_{CLK}/2^2$	500 kHz	1.25 MHz	2.5 MHz	5 MHz	6 MHz
0	0	1	1	$f_{CLK}/2^3$	250 kHz	625 kHz	1.25 MHz	2.5 MHz	3 MHz
0	1	0	0	$f_{CLK}/2^4$	125 kHz	312.5 kHz	625 kHz	1.25 MHz	1.5 MHz
0	1	0	1	$f_{CLK}/2^5$	62.5 kHz	156.2 kHz	313kHz	625 kHz	750 kHz
0	**1**	**1**	**0**	$f_{CLK}/2^6$	31.25 kHz	78.1 kHz	**156 kHz**	313 kHz	375 kHz
0	1	1	1	$f_{CLK}/2^7$	15.62 kHz	39.1 kHz	78.1 kHz	156 kHz	187.5 kHz
1	0	0	0	$f_{CLK}/2^8$	7.81 kHz	19.5 kHz	39.1 kHz	78.1 kHz	93.8 kHz
1	0	0	1	$f_{CLK}/2^9$	3.91 kHz	9.76 kHz	19.5 kHz	39.1 kHz	46.9 kHz
1	0	1	0	$f_{CLK}/2^{10}$	1.95 kHz	4.88 kHz	9.77 kHz	19.5 kHz	23.4 kHz
1	0	1	1	$f_{CLK}/2^{11}$	976 Hz	2.44 kHz	4.88 kHz	9.77 kHz	11.7 kHz
1	1	0	0	$f_{CLK}/2^{12}$	488 Hz	1.22 kHz	2.44 kHz	4.88 kHz	5.86 kHz
1	1	0	1	$f_{CLK}/2^{13}$	244 Hz	610 Hz	1.22 kHz	2.44 kHz	2.93 kHz
1	1	1	0	$f_{CLK}/2^{14}$	122 Hz	305 Hz	610 Hz	1.22 kHz	1.46 kHz
1	1	1	1	$f_{CLK}/2^{15}$	61 Hz	153 Hz	305 Hz	610 Hz	732 Hz

Note: For details of register settings, refer to the RL78/I1D User's Manual: Hardware.

Setting channel 0 operation mode

- Timer mode register 01 (TMR01)
  Select the operation clock (f_{MCK}).
  Select the count clock.
  Set the software trigger start.
  Select the operation mode.

Symbol: TMR01

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CKS011	CKS010	0	CCS01	0	STS012	STS011	STS010	CIS011	CIS010	0	0	MD013	MD012	MD011	MD010
0	**0**	0	**0**	0	**0**	**0**	**0**	**0**	**0**	0	0	**0**	**0**	**0**	**0**

Bits 15 and 14

CKS011	CKS010	Selection of operation clock (f_{MCK}) of channel 0
0	**0**	**Operation clock CK00 set by timer clock select register 0 (TPS0)**
0	1	Operation clock CK02 set by timer clock select register 0 (TPS0)
1	0	Operation clock CK01 set by timer clock select register 0 (TPS0)
1	1	Operation clock CK03 set by timer clock select register 0 (TPS0)

Bit 12

CCS01	Selection of count clock (f_{TCLK}) of channel 0
0	**Operation clock (f_{MCK}) specified by the CKS010 and CKS011 bits**
1	Valid edge of input signal from the TI01 pin

Bit 11

SPLIT01	Selection of 8 or 16-bit timer operation for channel 1
0	**Operates as 16-bit timer. (Operates in independent channel operation function or as slave channel in simultaneous channel operation function)**
1	Operates as 8-bit timer.

Note: For details of register settings, refer to the RL78/I1D User's Manual: Hardware.

Symbol: TMR01

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CKS 011	CKS 010	0	CCS 01	0	STS 012	STS 011	STS 010	CIS 011	CIS 010	0	0	MD 013	MD 012	MD 011	MD 010
0	**0**	0	**0**	0	**0**	**0**	**0**	**0**	**0**	0	0	**0**	**0**	**0**	**0**

Bits 10 to 8

STS012	STS011	STS010	Setting of start trigger or capture trigger of channel 1
0	**0**	**0**	**Only software trigger start is valid (other trigger sources are unselected).**
0	0	1	Valid edge of the TI01 pin input is used as both the start trigger and capture trigger.
0	1	0	Both the edges of the TI01 pin input are used as a start trigger and a capture trigger.
1	0	0	Interrupt signal of the master channel is used (when the channel is used as a slave channel with the simultaneous channel operation function).
Other than above			Setting prohibited

Bits 7 and 6

CIS011	CIS010	Selection of TI01 pin input valid edge
0	**0**	**Falling edge**
0	1	Rising edge
1	0	Both edges (when low-level width is measured) Start trigger: Falling edge, Capture trigger: Rising edge
1	1	Both edges (when high-level width is measured) Start trigger: Rising edge, Capture trigger: Falling edge

Note: For details of register settings, refer to the RL78/I1D User's Manual: Hardware.

Symbol: TMR01

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CKS 011	CKS 010	0	CCS 01	0	STS 012	STS 011	STS 010	CIS 011	CIS 010	0	0	MD 013	MD 012	MD 011	MD 010
0	**0**	0	**0**	0	**0**	**0**	**0**	**0**	**0**	0	0	**0**	**0**	**0**	**0**

Bits 3 to 0

MD 013	MD 012	MD 011	MD 010	Operation mode of channel 1	Corresponding function	Count operation of TCR
0	**0**	**0**	1/**0**	**Interval timer mode**	**Interval timer/square wave output/divider function/PWM output (master)**	**Counting down**
0	1	0	1/0	Capture mode	Input pulse interval measurement	Counting up
0	1	1	0	Event counter mode	External event counter	Counting down
1	0	0	1/0	One-count mode	Delay counter/One-shot pulse output/PWM output (slave)	Counting down
1	1	0	0	Capture & one-count mode	Measurement of high-/low-level width of input signal	Counting up
Other than above				Setting prohibited		

MD010 bit operation differs depending on the operation mode. (See the table below.)

Operation mode (Value set by the MD003 to MD001 bits (see table above))	MD010	TCR counting operation
- Interval timer mode (0, 0, 0) **- Capture mode (0, 1, 0)**	**0**	**Timer interrupt is not generated when counting is started (timer output does not change, either).**
	1	Timer interrupt is generated when counting is started (timer output also changes).
- Event counter mode (0, 1, 1)	0	Timer interrupt is not generated when counting is started (timer output does not change, either).
- One-count mode (1, 0, 0)	0	Start trigger is invalid during counting operation. At that time, interrupt is not generated.
	1	Start trigger is valid during counting operation. At that time, interrupt is generated.
- Capture & one-count mode (1, 1, 0)	0	Timer interrupt is not generated when counting is started (timer output does not change, either). Start trigger is invalid during counting operation. At that time, interrupt is not generated.
Other than above		Setting prohibited

Note: For details of register settings, refer to the RL78/I1D User's Manual: Hardware.

Setting interval timer frequency

- Timer data register 01 (TDR01)
  Set the interval timer comparison value.

Symbol: TDR01

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Timer interrupt (INTTM01) generation = (TDR01 setting value + 1) x counting clock frequency

Setting timer output mode

- Timer output mode register 0 (TOM0)
  Set master/slave.

Symbol: TOM0

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	TOM03	TOM02	TOM01	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0

Bit 1

TOM01	Control of timer output mode of channel 1
0	Master channel output mode
1	**Slave channel output mode**

Setting timer output level

- Timer output level register 0 (TOL0)
  Set the timer output level.

Symbol: TOL0

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	TOL03	TOL02	TOL01	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0

Bit 1

TOL01	Control of timer output level of channel 1
0	Positive logic output (active-high)
1	**Negative logic output (active-low)**

Note: For details of register settings, refer to the RL78/I1D User's Manual: Hardware.

Setting timer output

- Timer output register 0 (TO0)
  Enable/disable timer output for each channel.

Symbol: TO0

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	TO03	TO02	TO01	TO00
0	0	0	0	0	0	0	0	0	0	0	0	0	0	**1**	0

Bit 1

TO01	Timer output of channel 1
0	Timer output value is 0.
1	**Timer output value is 1.**

Enabling timer output

- Timer output enable register 0 (TOE0)
  Enable/disable timer output of each channel.

Symbol: TOE0

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	0	TOE02	TOE01	TOE00
0	0	0	0	0	0	0	0	0	0	0	0	0	0	**1**	0

Bit 1

TOE01	Timer output enable/disable of channel 0
0	Timer output is disabled. Timer operation is not applied to the TM01 bit and the output is fixed. Writing to the TO01 bit is enabled and the level set in the TO01 bit is output from the TO01 pin.
1	**Timer output is enabled.** **Timer operation is applied to the TO01 bit and an output waveform is generated.** **Writing to TO01 bit is ignored.**

Note: For details of register settings, refer to the RL78/I1D User's Manual: Hardware.

Setting pins

- Port output mode register (POM3)
  Select the pin output mode.
- Port mode control register (PMC3)
  Select digital I/O or analog input for the pin.
- Port register (P3)
  Set the pin output latch value.
- Port mode register (PM3)
  Select input or output mode for the pin.

Symbol: POM3

7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	POM30
0	0	0	0	0	0	0	**0**

Bit 0

POM30	P30 pin output mode selection
0	**Normal output mode**
1	N-ch open drain output mode

Symbol: PMC3

7	6	5	4	3	2	1	0
0	0	0	0	0	0	PMC31	PMC30
0	0	0	0	0	0	x	**0**

Bit 0

PMC30	P30 pin digital I/O/analog input selection
0	**Digital I/O (alternate function other than analog input)**
1	Analog input

Symbol: P3

7	6	5	4	3	2	1	0
0	0	0	0	P33	P32	P31	P30
0	0	0	0	0	0	0	**0**

Bit 0

P30	P30 pin output data control
0	**Output 0.**
1	Output 1.

Note: For details of register settings, refer to the RL78/I1D User's Manual: Hardware.

Symbol: PM3

7	6	5	4	3	2	1	0
0	0	0	0	PM33	PM32	PM31	PM30
0	0	0	0	0	0	0	**0**

Bit 0

PM30	P30 pin I/O mode selection
0	**Output mode**
1	Input mode

Note: For details of register settings, refer to the RL78/I1D User's Manual: Hardware.

5.7.7 Setting 12-Bit Interval Timer

Figure 5.8 shows the flowchart for setting the 12-bit interval timer.

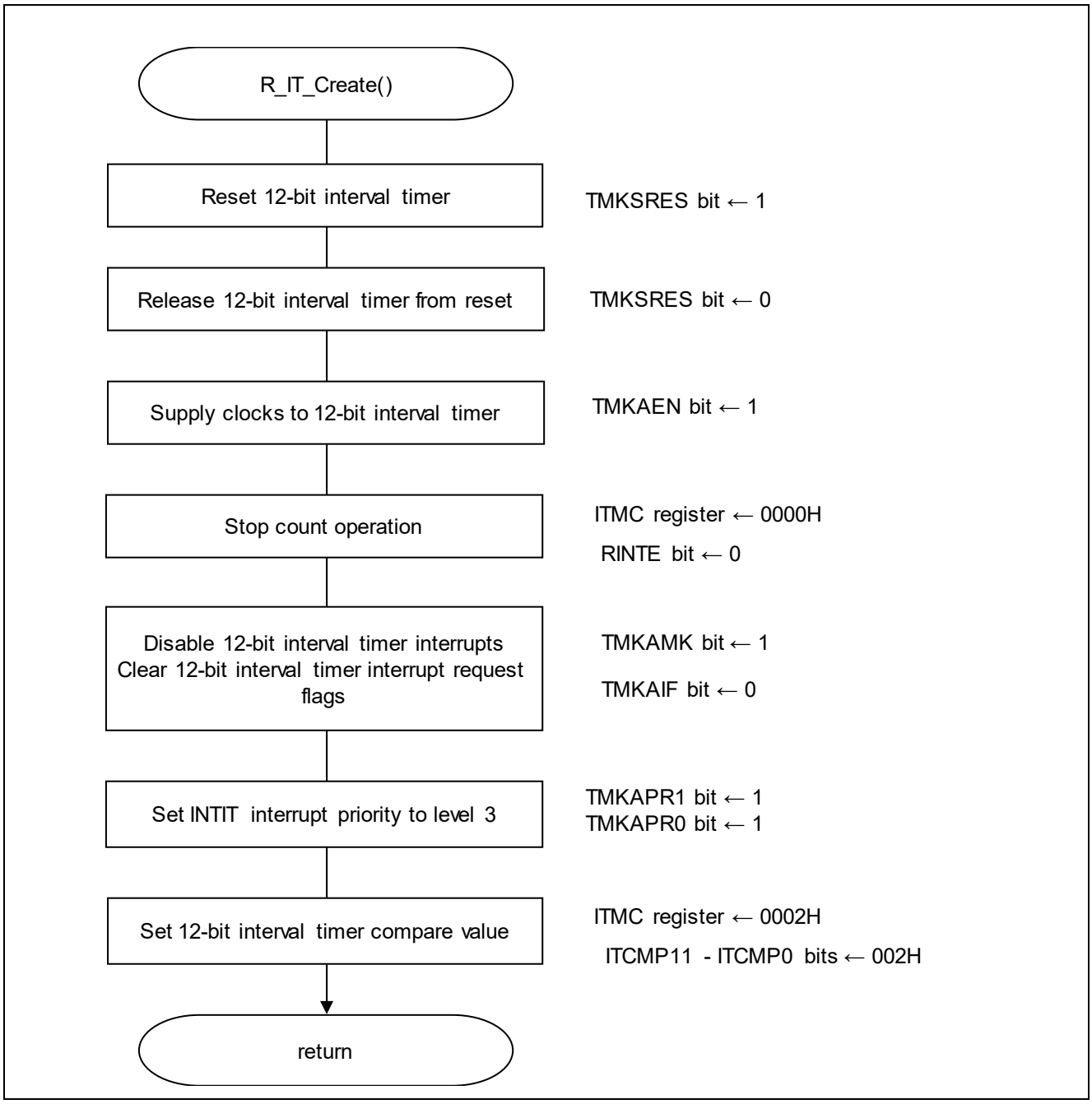

Figure 5.8 Setting 12-Bit Interval Timer

Controlling reset of 12-bit interval timer

- Peripheral reset control register 2 (PRR2)

Control reset of the 12-bit interval timer.

Symbol: PRR2

7	6	5	4	3	2	1	0
TMKARES	0	DOCRES	0	0	0	0	0
1/0	0	x	0	0	0	0	0

Bit 7

TMKARES	Reset control of 12-bit interval timer
0	**12-bit interval timer reset release**
1	**12-bit interval timer reset state**

Starting clock supply to 12-bit interval timer

- Peripheral enable register 2 (PER2)

Start clock supply to the 12-bit interval timer.

Symbol: PER2

7	6	5	4	3	2	1	0
TMKAEN	FMCEN	DOCEN	0	0	0	0	0
1	x	x	0	0	0	0	0

Bit 7

TMKAEN	Control of 12-bit interval timer input clock supply
0	Stops input clock supply.
1	**Enables input clock supply.**

Note: For details of register settings, refer to the RL78/I1D User's Manual: Hardware.

Setting 12-bit interval timer operation

- 12-bit interval timer control register (ITMC)
  Start or stop the 12-bit interval timer operation.
  Set the 12-bit interval timer compare value.

Symbol: ITMC

15	14	13	12	11-0
RINTE	0	0	0	ITCMP11-ITCMP0
0	0	0	0	**002H**

Bit 15

RINTE	12-bit interval timer operation control
0	**Count operation stopped**
1	Count operation started

Bits 11 to 0

ITCMP11 to ITCMP0	Specification of 12-bit interval timer compare value
001H	**These bits generate a fixed-cycle interrupt (counter clock cycles x (ITCMP setting + 1)).**
002H	
.	
.	
FFFH	
000H	Setting prohibited
Example interrupt cycles when 001H or FFFH is specified for ITCMP11 to ITCMP0 - ITCMP11 to ITCMP0 = 001H, count clock: when f_{SUB} = 32.768 kHz 1/32.768 [kHz] x (1 + 1) = 0.06103515625 [ms] ≅ 61.03 [µs] - ITCMP11 to ITCMP0 = FFFH, count clock: when f_{SUB} = 32.768 kHz 1/32.768 [kHz] x (4095 + 1) = 125 [ms]	

Note: For details of register settings, refer to the RL78/I1D User's Manual: Hardware.

Setting interrupts

- Interrupt request flag register (IF1H)
  Clear interrupt request flags.
- Interrupt mask flag register (MK1H)
  Cancel interrupt mask.

Symbol: IF1H

7	6	5	4	3	2	1	0
0	DOCIF	CMPIF1	CMPIF0	KRIF	TMKAIF	RTCIF	ADIF
0	x	x	x	x	0	x	x

Bit 2

TMKAIF	Interrupt request flag
0	**No interrupt request signal is generated**
1	Interrupt request is generated, interrupt request status

Symbol: MK1H

7	6	5	4	3	2	1	0
0	DOCMK	CMPMK1	CMPMK0	KRMK	TMKAMK	RTCMK	ADMK
0	x	x	x	x	0	x	x

Bit 2

TMKAMK	Interrupt servicing control
0	**Interrupt servicing enabled**
1	Interrupt servicing disabled

Note: For details of register settings, refer to the RL78/I1D User's Manual: Hardware.

5.7.8 Main Functions

Figures 5.9 and 5.10 show the flowcharts of the main functions.

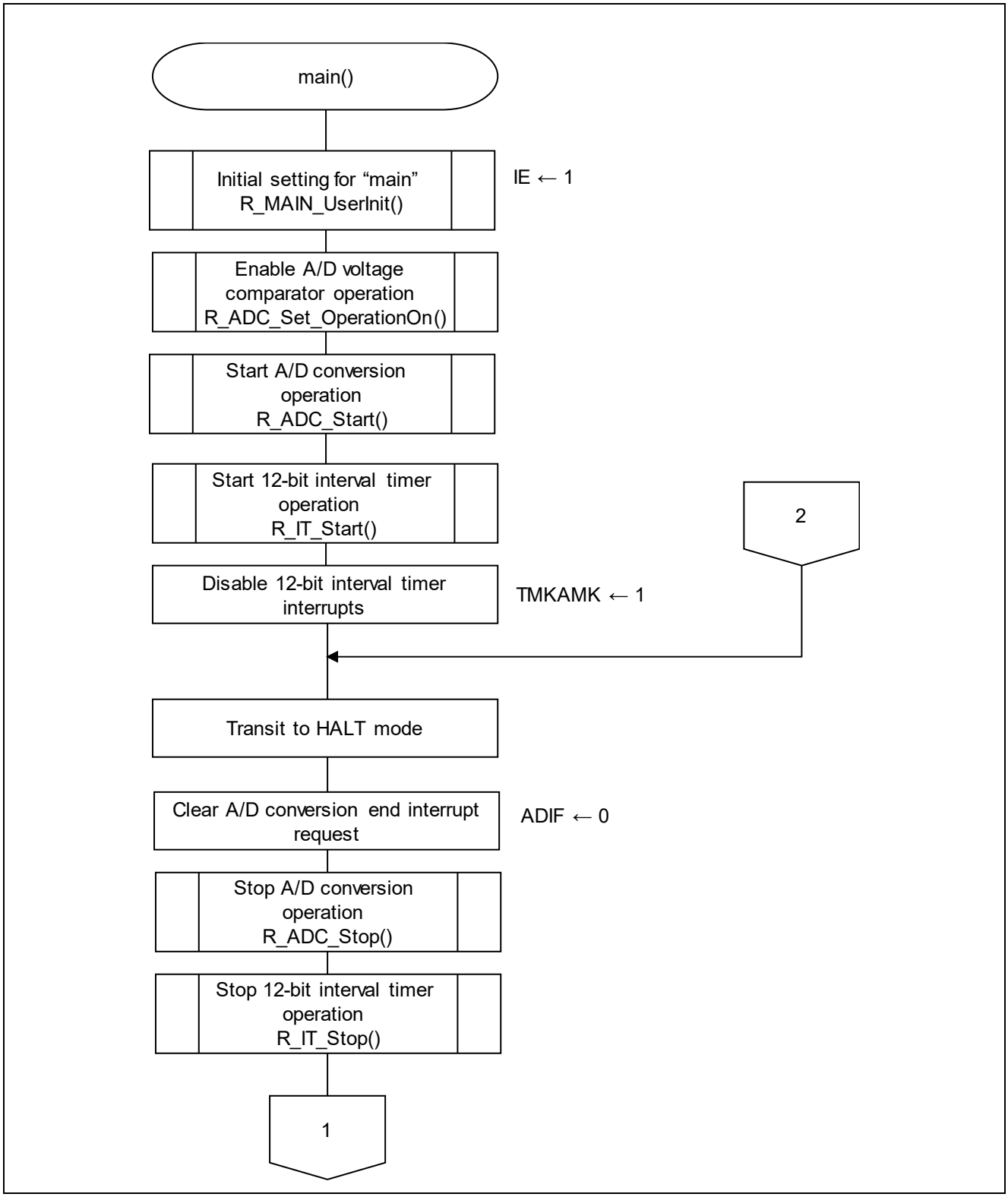

Figure 5.9 Main Functions (1/2)

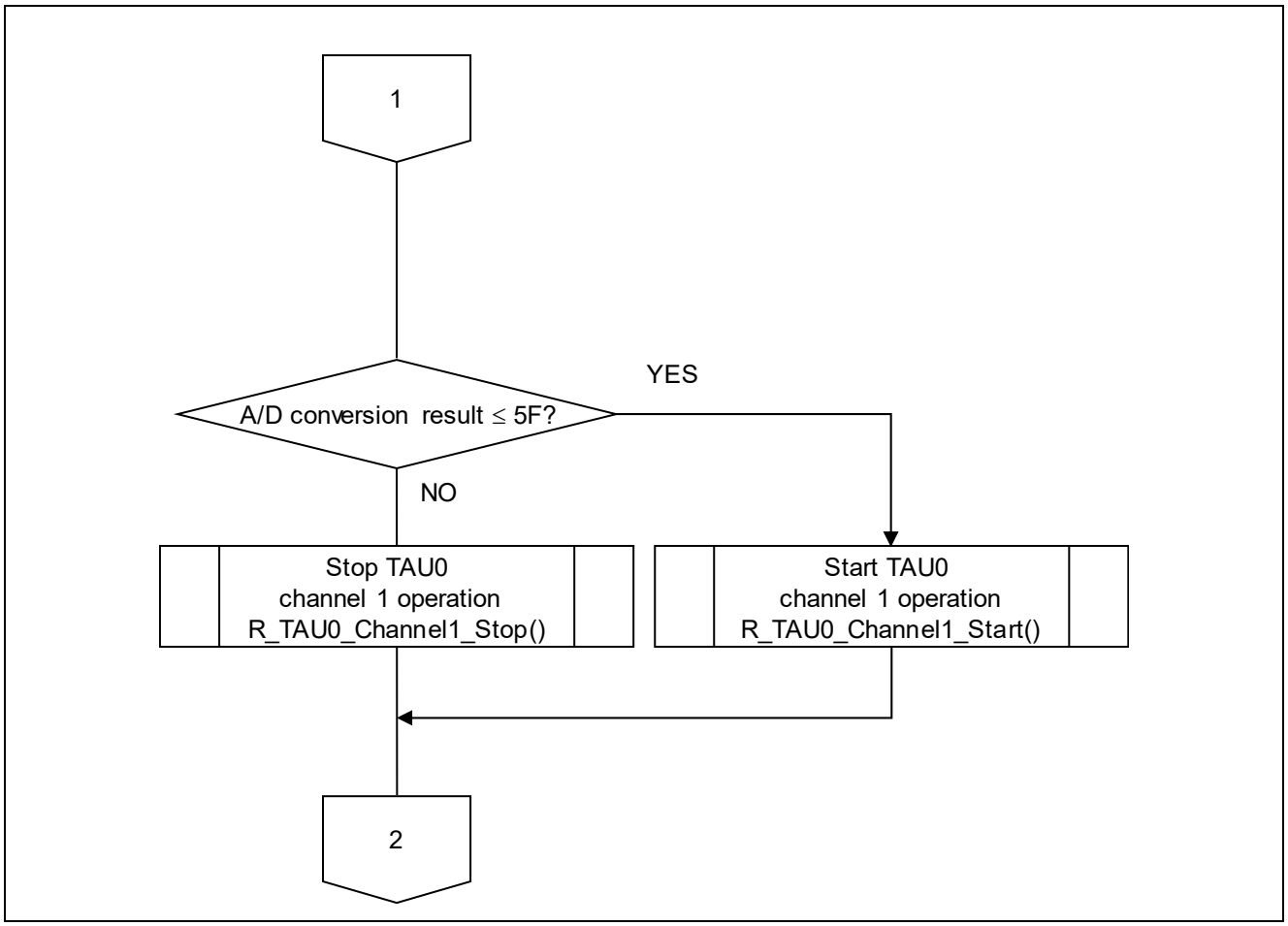

Figure 5.10 Main Functions (2/2)

5.7.9 Initial Setting for “main”

Figure 5.11 shows the flowchart of the initial setting for “main”.

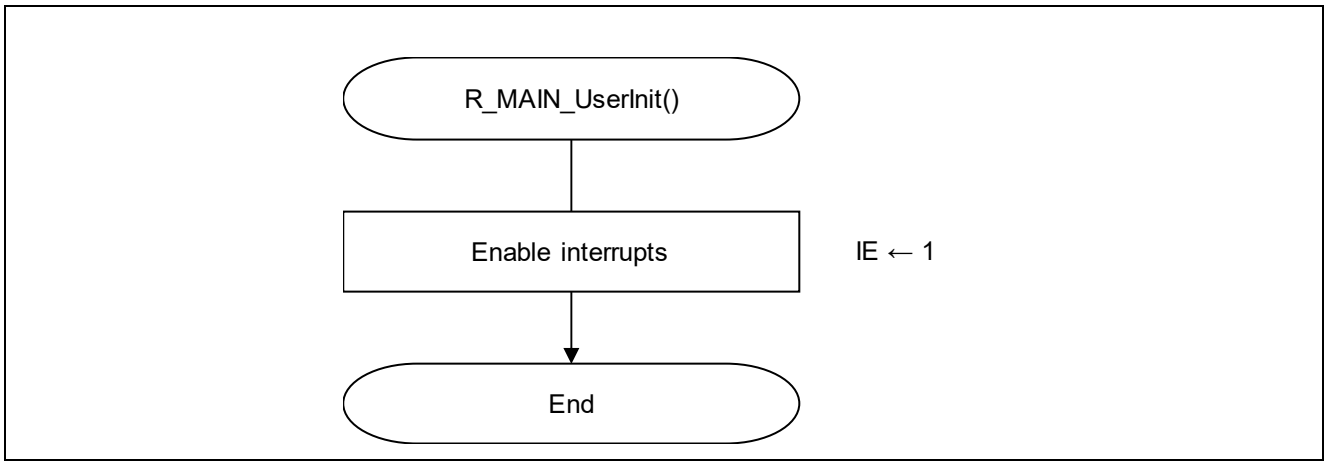

Figure 5.11 Initial Setting for “main”

5.7.10 A/D Voltage Comparator Operation Enable Function

Figure 5.12 shows the flowchart of the A/D voltage comparator operation enable function.

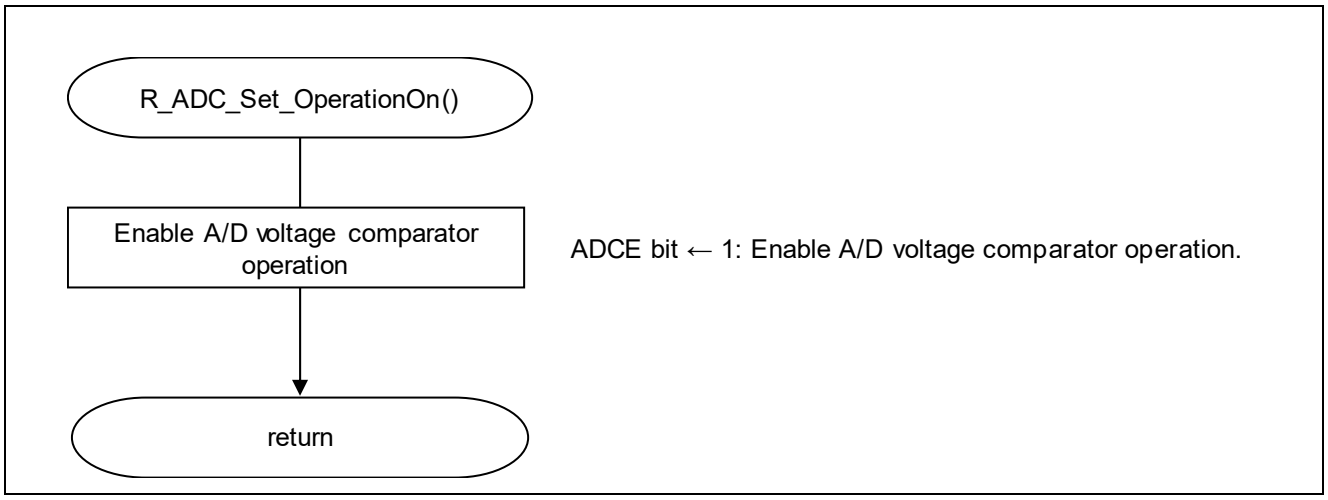

Figure 5.12 A/D Voltage Comparator Operation Enable Function

5.7.11 A/D Conversion Start Function

Figure 5.13 shows the flowchart of the A/D conversion start function.

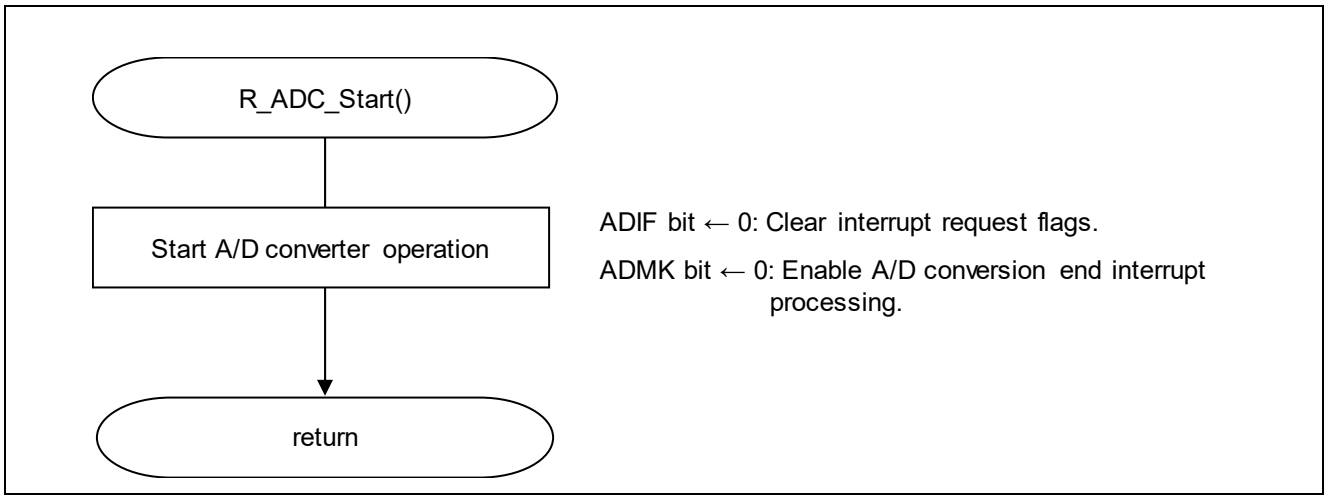

Figure 5.13 A/D Conversion Start Function

5.7.12 A/D Conversion Stop Function

Figure 5.14 shows the flowchart of the A/D conversion stop function.

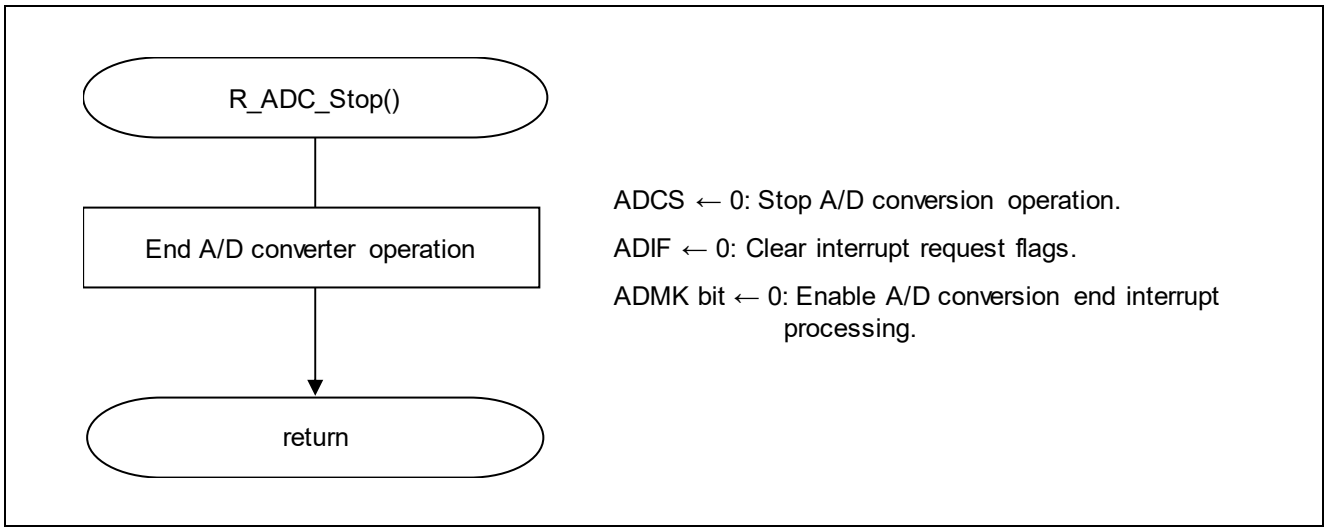

Figure 5.14 A/D Conversion Stop Function

5.7.13 A/D Conversion End Interrupt Processing

Figure 5.15 shows the flowchart of the A/D conversion end interrupt processing function.

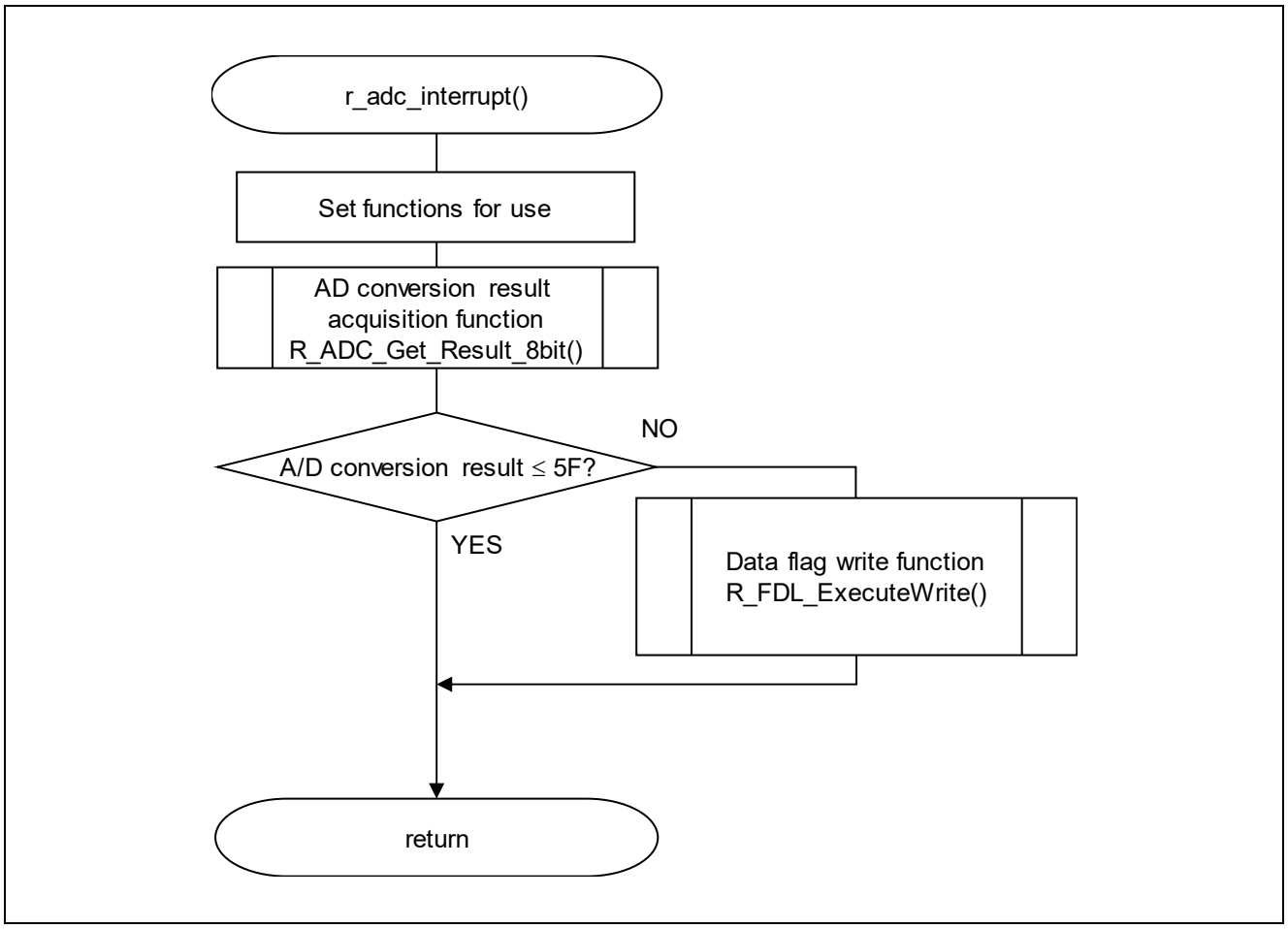

Figure 5.15 A/D Conversion End Interrupt Processing Function

5.7.14 12-Bit Interval Timer Start Function

Figure 5.16 shows the flowchart of the 12-bit interval timer start function.

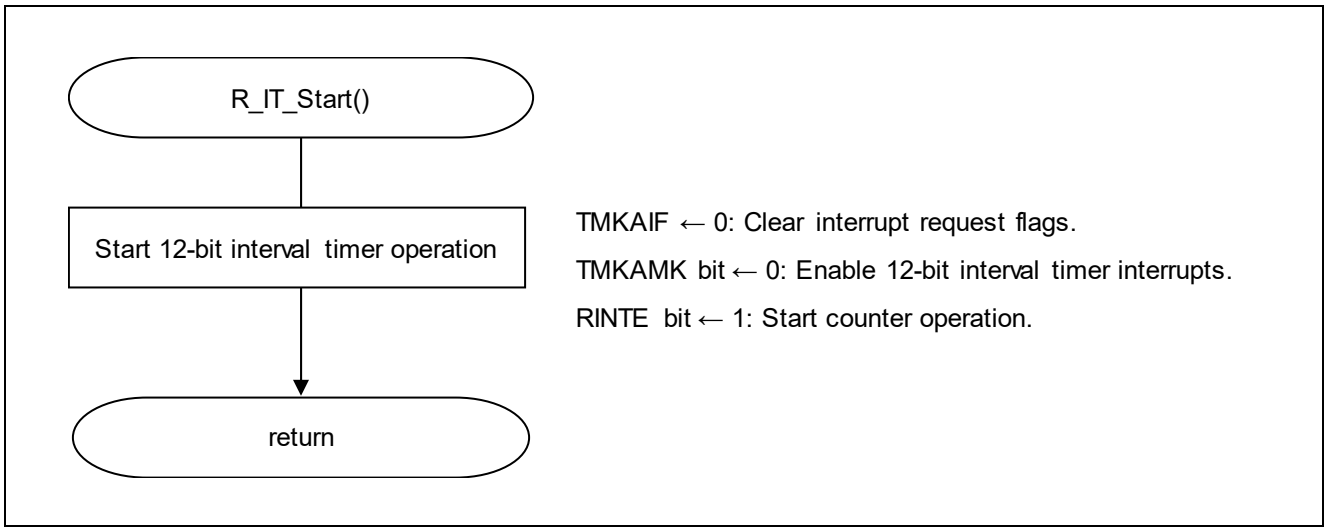

Figure 5.16 12-Bit Interval Timer Start Function

5.7.15 12-Bit Interval Timer Stop Function

Figure 5.17 shows the flowchart of the 12-bit interval timer stop function.

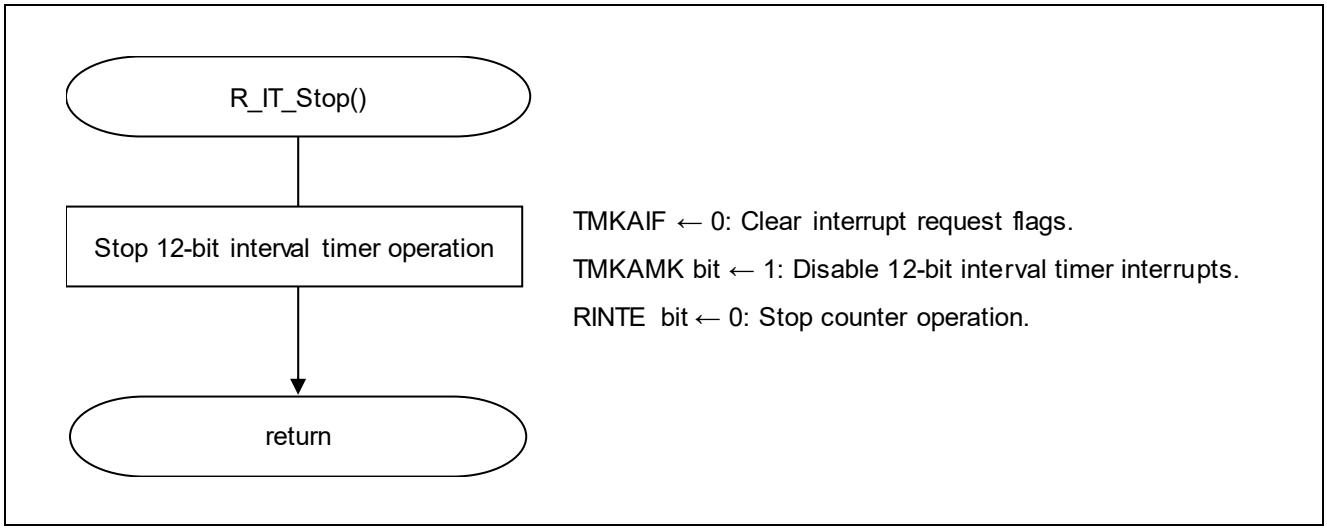

Figure 5.17 12-Bit Interval Timer Stop Function

5.7.16 TAU0 Channel 1 Operation Start Function

Figure 5.18 shows the flowchart of the TAU0 channel 1 operation start function.

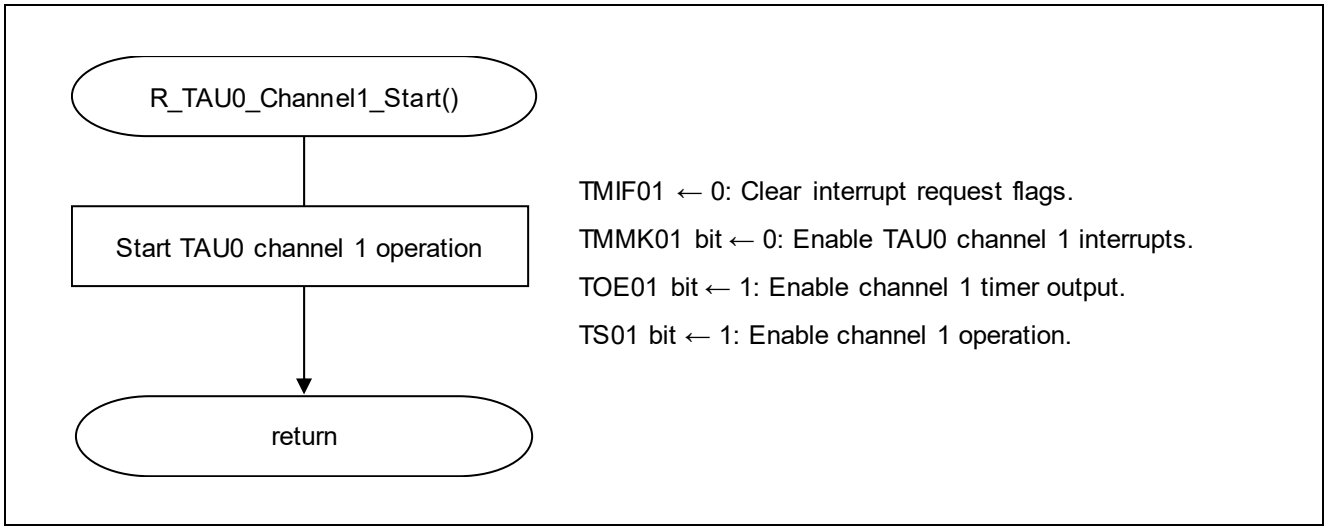

Figure 5.18 TAU0 Channel 1 Operation Start Function

5.7.17 TAU0 Channel 1 Operation Stop Function

Figure 5.19 shows the flowchart of the TAU0 channel 1 operation stop function.

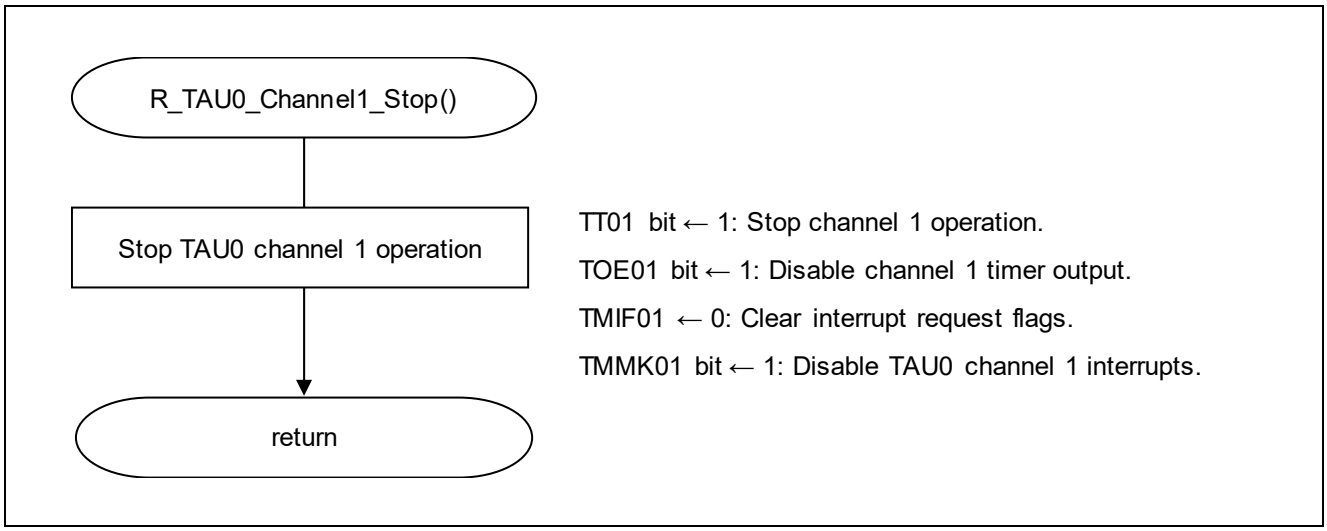

Figure 5.19 TAU0 Channel 1 Operation Stop Function

6. Sample Code

The user can get the sample code from the Renesas Electronics website.

7. Reference Documents

RL78/I1D User's Manual: Hardware (R01UH0474E)

RL78 Family User's Manual: Software (R01US0015E)

(Get the latest version from the Renesas Electronics website.)

Technical Updates/Technical News

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Revision History	RL78/I1D Power Supply Voltage Monitoring CC-RL

Rev.	Date	Revision Contents	
		Page	Description
1.00	Jan. 31, 2017	—	Newly created.

General Precautions in the Handling of Microprocessing Unit and Microcontroller Unit Products

The following usage notes are applicable to all Microprocessing unit and Microcontroller unit products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Handling of Unused Pins

   Handle unused pins in accordance with the directions given under Handling of Unused Pins in the manual.

   ¾ The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible. Unused pins should be handled as described under Handling of Unused Pins in the manual.

2. Processing at Power-on

   The state of the product is undefined at the moment when power is supplied.

   ¾ The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the moment when power is supplied.
   In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the moment when power is supplied until the reset process is completed.
   In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the moment when power is supplied until the power reaches the level at which resetting has been specified.

3. Prohibition of Access to Reserved Addresses

   Access to reserved addresses is prohibited.

   ¾ The reserved addresses are provided for the possible future expansion of functions. Do not access these addresses; the correct operation of LSI is not guaranteed if they are accessed.

4. Clock Signals

   After applying a reset, only release the reset line after the operating clock signal has become stable. When switching the clock signal during program execution, wait until the target clock signal has stabilized.

   ¾ When the clock signal is generated with an external resonator (or from an external oscillator) during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Moreover, when switching to a clock signal produced with an external resonator (or by an external oscillator) while program execution is in progress, wait until the target clock signal is stable.

5. Differences between Products

   Before changing from one product to another, i.e. to a product with a different part number, confirm that the change will not lead to problems.

   ¾ The characteristics of Microprocessing unit or Microcontroller unit products in the same group but having a different part number may differ in terms of the internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

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(Rev.3.0-1 November 2016)

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