RL78/I1D

Operation State Switching CC-RL

R01AN3095EJ0100
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Summary

The application note shows the register setting sequence for the switch of RL78/I1D operation state, using the Operation State Control. After reset, it operates in the LV mode. The flash operation mode is switched one by one by the button pressing (LV mode → LS mode → HS mode → LS mode → LP mode → LS mode →LV mode, repetition at the following). The power-supply voltage VDD should be confirmed with the A/D converter when switching to the HS mode, and if the voltage is out of specified range, the transition should be avoided.

Object device

RL78/I1D

When applying the application note to other microcomputers please change it according to the specification and evaluate it enough.

Contents

1. Specification

When the button is pressed (the INTP0 interrupt is generated), the flash operation mode is changed. After all the RL78/I1D supported operation state transitions are executed, it returns back to the state same as after reset.

Table 1.1 shows peripheral function and usage and Figure 1.1 shows the operation state transition sequence order.

Table 1.1 Peripheral function and usage

Peripheral function	Usage
A/D converter	Measurement of VDD voltage
12-bit interval timer	LED lighting control

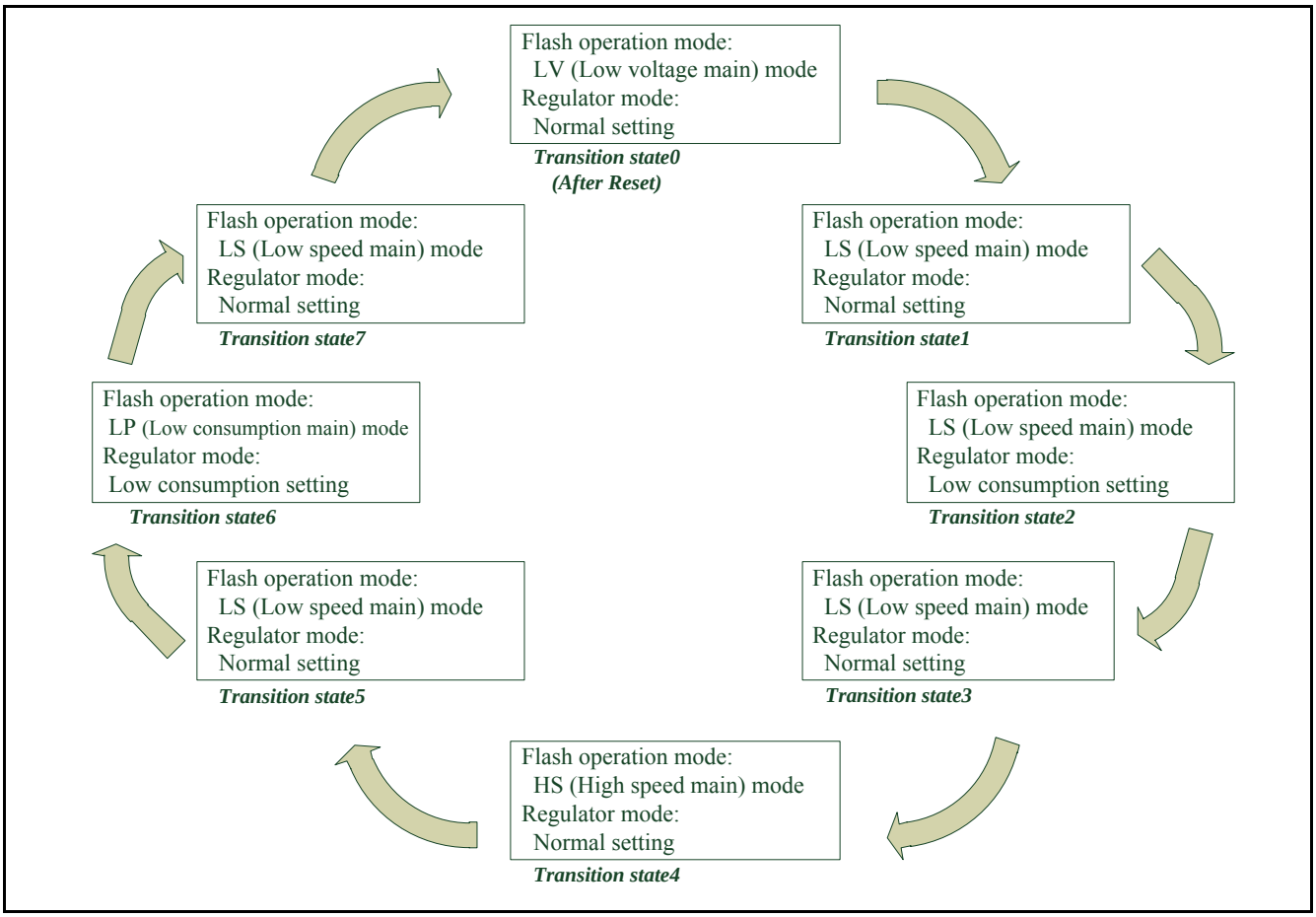

Figure 1.1 Operation state transition sequence order

2. Operation condition confirmation

The sample code of this application note confirms operation at the conditions stated below.

Table 2.1 Operation condition confirmation

Item	Content
MCU	RL78/I1D (R5F117GC)
Operating frequency	・High-speed on-chip oscillator (HOCO) clock: 16 MHz, 8MHz, 4 MHz ・Middle-speed on-chip oscillator (MOCO) clock: 4MHz, 1MHz ・Low-speed on chip oscillator clock: 15KHz ・CPU/peripheral hardware clock: 16MHz, 8MHz, 4MHz, 1 MHz
Operation voltage	3.3 V (operable at 1.6V-3.6V). LVD operation (V_{LVD}): LVD off
Integrated development environment(CS+)	CS+ for CC V3.01.00 from Renesas Electronics Corp.
C compiler(CS+)	CC-RL V1.01.00 from Renesas Electronics Corp.
Integrated development environment(e^2studio)	e^2studio V4.1.0.018 from Renesas Electronics Corp.
C compiler(e^2studio)	CC-RL V1.01.00 from Renesas Electronics Corp.

3. Hardware explanation

3.1. Example of hardware structure

Figure 3.1 shows an example of the hard structure used in the application note

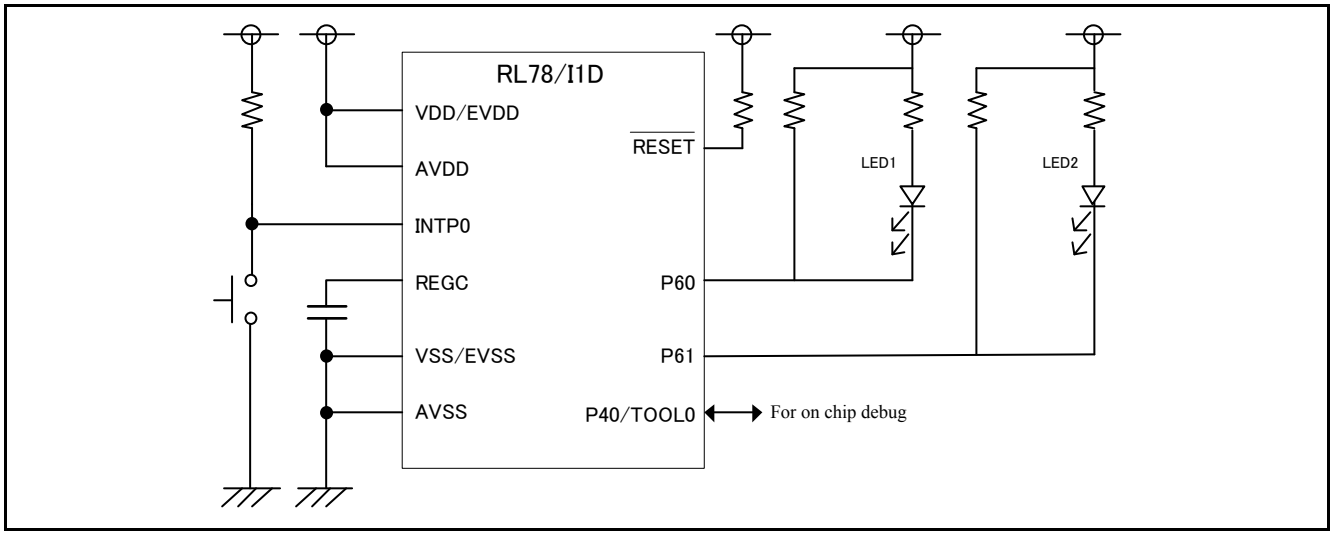

Figure 3.1 Hardware structure

Note: It is the circuit image and shows the simplified outline of the connection. Please design to do the pin processing etc. appropriately, and to meet with the electrical characteristics when the circuit is actually designed (Please connect the input only port to VDD or VSS through a resistor individually).

3.2. Used pin list

Table 3.1 shows the used pin and function.

Table 3.1 Used pin and function

Pin name	I/O	Content
P60	Output	LED1 turning on control
P61	Output	LED2 turning on control
P137/INTP0	Input	Operation state switching

4. Software explanation

4.1. Outline of operation

In this sample code, the operation state of RL78/I1D is switched by the button pressing (INTP0 interrupt generation). There are 8 kinds of operation states with combination of the flash operation mode and the regulator mode. After 8-time external interrupt INTO0 generations, it returns back to the state same as after reset. The operation state is displayed by the combination of turning on, turning off, and blinking LED. The fixed periodical interrupt processing triggered by the 12-bit interval timer updates the LED display. The transition to HS (high speed main) mode is executed when the VDD voltage is 2.4V or more. In the case of VDD below 2.4V, the transition to the HS mode is not executed. LED is blinked to inform the error.

Table 4.1 shows operation state detail and operation state transition.

Table 4.1 Operation state detail and operation state transition

Transition state	State	LED1	LED2	Operation clock	Range of operation voltage	Status of the next transition
0 (after reset)	LV mode	Turning off	Turning on	HOCO: 4MHz	1.6V~3.6V	1
1	LS mode (Normal setting)	Turning on	Turning off	HOCO: 8MHz	1.8V~3.6V	2
2	LS mode (low consumption setting)	High-speed blinking	Turning off	MOCO: 4MHz	1.8V~3.6V	3
3	LS mode (Normal setting)	Turning on	Turning off	HOCO: 8MHz	1.8V~3.6V	4 or 4-Error
4	HS mode	Turning on	Turning on	HOCO: 16MHz	2.4V~3.6V	5
4-Error	LS mode (Normal setting)	Super-high-speed blinking	Super-high-speed blinking	HOCO: 8MHz	1.8V~3.6V	5
5	LS mode (Normal setting)	Turning on	Turning off	HOCO: 8MHz	1.8V~3.6V	6
6	LP mode	Low-speed blinking	Turning off	MOCO: 1MHz	1.8V~3.6V	7
7	LS mode (Normal setting)	Turning on	Turning off	HOCO: 8MHz	1.8V~3.6V	0

4.2. Setting of option byte

Table 4.2 shows the setting of option byte. Please set the appropriate value to fit the different system.

Table 4.2 Optional byte setting

Address	Set value	Content
000C0H/010C0H	11101111B	Watch dog timer operation stop (count stop after reset)
000C1H/010C1H	11111111B	LVD off
000C2H/010C2H	00101011B	LV mode, High-speed on-chip oscillator : 4MHz
000C3H/010C3H	10000100B	On chip debug enable

4.3. List of Constants

Table 4.3 lists the constants that are used in the sample program.

Table 4.3 Constants for the Sample Program

Constant	Setting	Description
_00_TRANSITION_STATUS_0	00H	Transition status 0
_01_TRANSITION_STATUS_1	01H	Transition status 1
_02_TRANSITION_STATUS_2	02H	Transition status 2
_03_TRANSITION_STATUS_3	03H	Transition status 3
_04_TRANSITION_STATUS_4	04H	Transition status 4
_05_TRANSITION_STATUS_5	05H	Transition status 5
_06_TRANSITION_STATUS_6	06H	Transition status 6
_07_TRANSITION_STATUS_7	07H	Transition status 7
_00_FLASHMODE_LV	00H	LED control status (LV mode)
_01_FLASHMODE_LS_0	01H	LED control status (LS(normal) mode)
_02_FLASHMODE_LS_1	02H	LED control status (LS (low consumption) mode)
_04_FLASHMODE_HS	04H	LED control status (HS mode)
_08_FLASHMODE_LP	08H	LED control status (LP mode)
_10_FLASHMODE_HS_ERROR	10H	LED control status (HS error mode)

4.4. List of Variable

Table 4.4 lists the global variable that is used by this sample program.

Table 4.4 Global variable

Type	Variable identifier	Content	Use function
uint16_t	g_flash_mode	State variable of flash operation mode	r_it_interrupt, switch_flashmode_to_LV, switch_flashmode_to_LS_0, switch_flashmode_to_LS_1, switch_flashmode_to_HS, switch_flashmode_to_LP,
uint16_t	g_transition_status	Transition state variable	r_intc0_interrupt
uint16_t	g_ad_result	Value of A/D conversion result	switch_flashmode_to_HS, r_adc_interrupt
uint16_t	g_ad_busy	A/D conversion completion flag	r_adc_interrupt, switch_flashmode_to_HS

4.5. Function list

Table 4.5 shows the function list.

Table 4.5 Function

Function name	Outline
R_MAIN_UserInit	The main user initialization
R_INTC0_Start	INTP0 interrupt enable processing
R_IT_Start	12-bit interval timer start processing
R_PCLBUZ1_Start	Clock output start processing
R_ADC_Start	A/D conversion operation start processing
R_ADC_Stop	A/D converter stop processing
switch_flashmode_to_LV	The flash operation state is switched to the LV mode.
switch_flashmode_to_LS_0	The flash operation state is switched to the LS (normal) mode.
switch_flashmode_to_LS_1	The flash operation state is switched to the LS (low consumption) mode.
switch_flashmode_to_HS	The flash operation state is switched to the HS mode.
switch_flashmode_to_LP	The flash operation state is switched to the LP mode.
switch_flashmode_to_LV_M	The flash operation state is switched to the LV mode(MOCO).
r_adc_interrupt	A/D conversion complete interrupt processing
R_ADC_Result	A/D conversion result acquisition process
r_intc0_interrupt	External interrupt processing
r_it_interrupt	12-bit interval timer interrupt processing

4.6. Function specification

Below shows the function specification of the sample code.

R_MAIN_UserInit	
Outline	The main user initialization.
Header	r_cg_macrodriver.h, r_cg_userdefine.h, r_cg_intc.h, r_cg_it.h, r_cg_pclbuz.h
Declaration	void R_MAIN_UserInit(void)
Explanation	Performs initialization necessary to the operation of the application.
Parameter	None
Return value	None

R_INTC0_Start	
Outline	INTP0 interrupt enable processing.
Header	r_cg_macrodriver.h, r_cg_userdefine.h, r_cg_intc.h
Declaration	void R_INTC0_Start(void)
Explanation	After clearing the INTP0 interrupt request flag of, it will allow the interrupt.
Parameter	None
Return value	None

R_IT_Start	
Outline	12-bit interval timer start processing.
Header	r_cg_macrodriver.h, r_cg_userdefine.h, r_cg_it.h
Declaration	void R_IT_Start(void)
Explanation	Start the count operation of the 12-bit interval timer.
Parameter	None
Return value	None

R_PCLBUZ1_Start	
Outline	Clock output start processing.
Header	r_cg_macrodriver.h, r_cg_userdefine.h, r_cg_pclbuz.h
Declaration	void R_PCLBUZ1_Start(void)
Explanation	Start the clock count operation.
Parameter	None
Return value	None

R_ADC_Start	
Outline	A/D conversion operation start processing.
Header	r_cg_macrodriver.h, r_cg_userdefine.h, r_cg_adc.h
Declaration	void R_ADC_Start(void)
Explanation	Start the A/D conversion operation.
Parameter	None
Return value	None

R_ADC_Stop	
Outline	A/D converter stop processing.
Header	r_cg_macrodriver.h, r_cg_userdefine.h, r_cg_adc.h
Declaration	void R_ADC_Stop(void)
Explanation	Stop the A/D conver operation.
Parameter	None
Return value	None

switch_flashstatemode_to_LV	
Outline	The flash operation state is switched to the LV mode.
Header	r_cg_intc.h
Declaration	void switch_flashmode_to_LV(void)
Explanation	The flash operation state is switched to the LV mode.
Parameter	None
Return value	None

switch_flashmode_to_LS_0	
Outline	The flash operation state is switched to LS (normal) mode.
Header	r_cg_intc.h
Declaration	void switch_flashmode_to_LS_0(void)
Explanation	The flash operation state is switched to LS (normal) mode.
Parameter	None
Return value	None

switch_flashmode_to_LS_1	
Outline	The flash operation state is switched to LS (low consumption) mode.
Header	r_cg_intc.h
Declaration	void switch_flashmode_to_LS_1(void)
Explanation	The flash operation state is switched to LS (low consumption) mode.
Parameter	None
Return value	None

switch_flashmode_to_HS	
Outline	The flash operation state is switched to the HS mode.
Header	r_cg_intc.h
Declaration	void switch_flashmode_to_HS(void)
Explanation	The flash operation state is switched to the HS mode.
Parameter	None
Return value	None

switch_flashmode_to_LP	
Outline	The flash operation state is switched to the LP mode.
Header	r_cg_intc.h
Declaration	void switch_flashmode_to_LP(void)
Explanation	The flash operation state is switched to the LP mode.
Parameter	None
Return value	None

switch_flashstatemode_to_LV_M	
Outline	The flash operation state is switched to the LV mode(MOCO).
Header	r_cg_intc.h
Declaration	void switch_flashmode_to_LV_M(void)
Explanation	The flash operation state is switched to the LV mode. Set the CPU clock to the Middle-speed on-chip oscillator.
Parameter	None
Return value	None

r_adc_interrupt	
Outline	A/D conversion complete interrupt processing
Header	None
Declaration	None
Explanation	A/D function is stopped, and the result of A/D conversion is stored in RAM area.
Parameter	None
Return value	None

R_ADC_Result	
Outline	A/D conversion result acquisition process
Header	r_cg_macrodriver.h, r_cg_userdefine.h, r_cg_adc.h
Declaration	None
Explanation	Store the results of A/D conversion in the RAM area.
Parameter	None
Return value	None

r_intc0_interrupt	
Outline	External interrupt processing
Header	None
Declaration	None
Explanation	Pushing button calls this function where operation state switching is executed.
Parameter	None
Return value	None

r_it_interrupt	
Outline	12-bit interval timer interrupt processing
Header	None
Declaration	None
Explanation	LED state is updated according to the state of operation state.
Parameter	None
Return value	None

4.7. Flow chart

Figure 4.1 shows the whole flowchart.

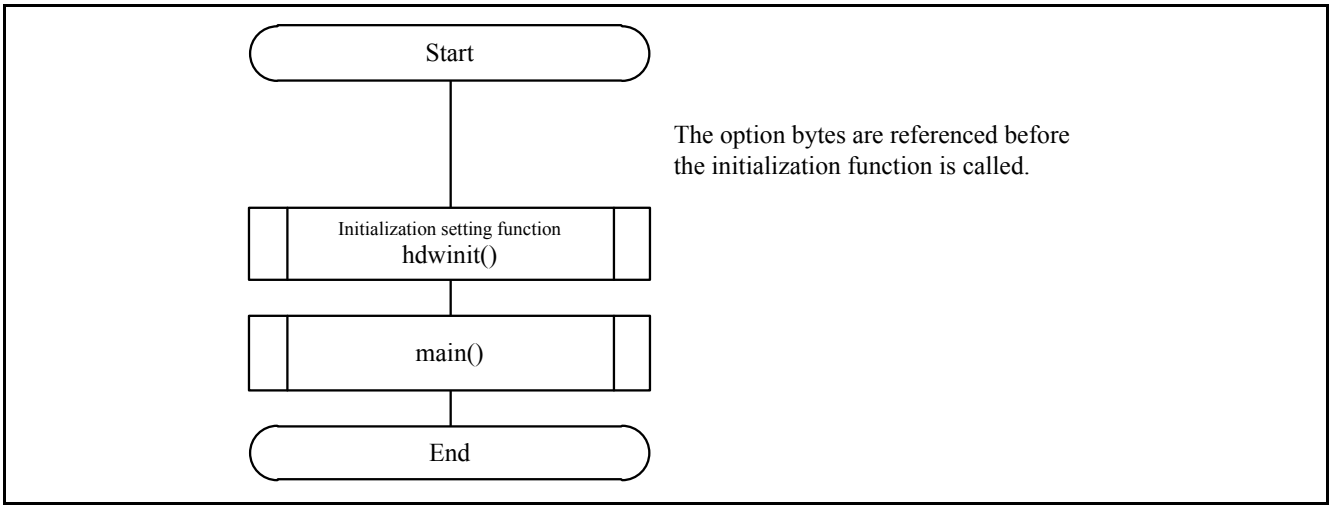

Figure 4.1 Overall Flow

4.7.1. Initialization

Figure 4.2 shows the flowchart of initialization flow chart.

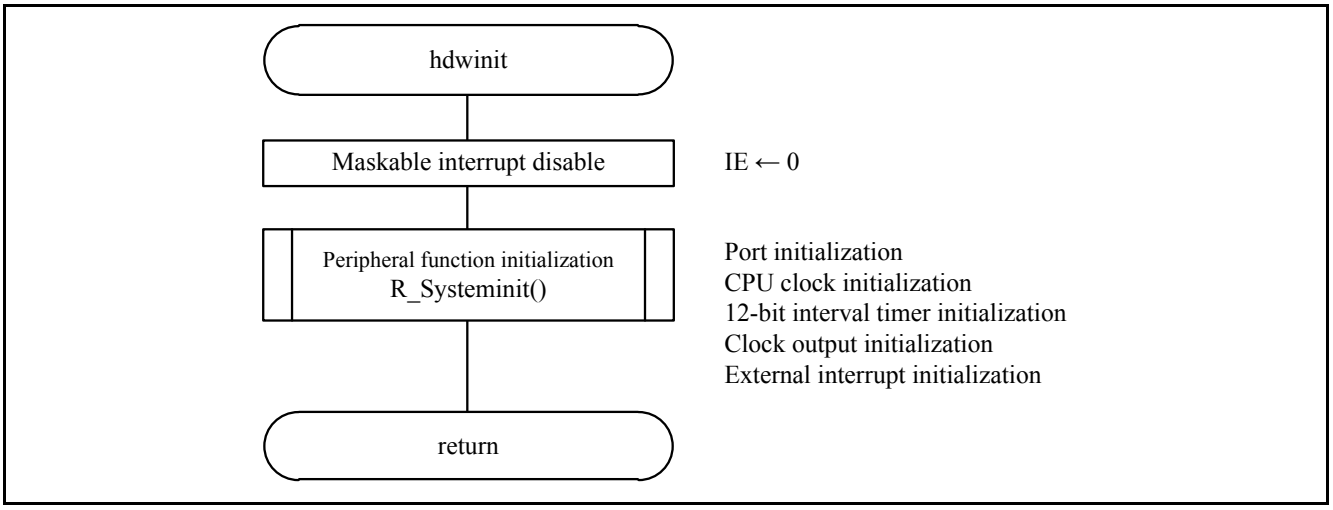

Figure 4.2 Initialization

4.7.2. Peripheral function Initialization

Figure 4.3 shows the flowchart of peripheral function initialization.

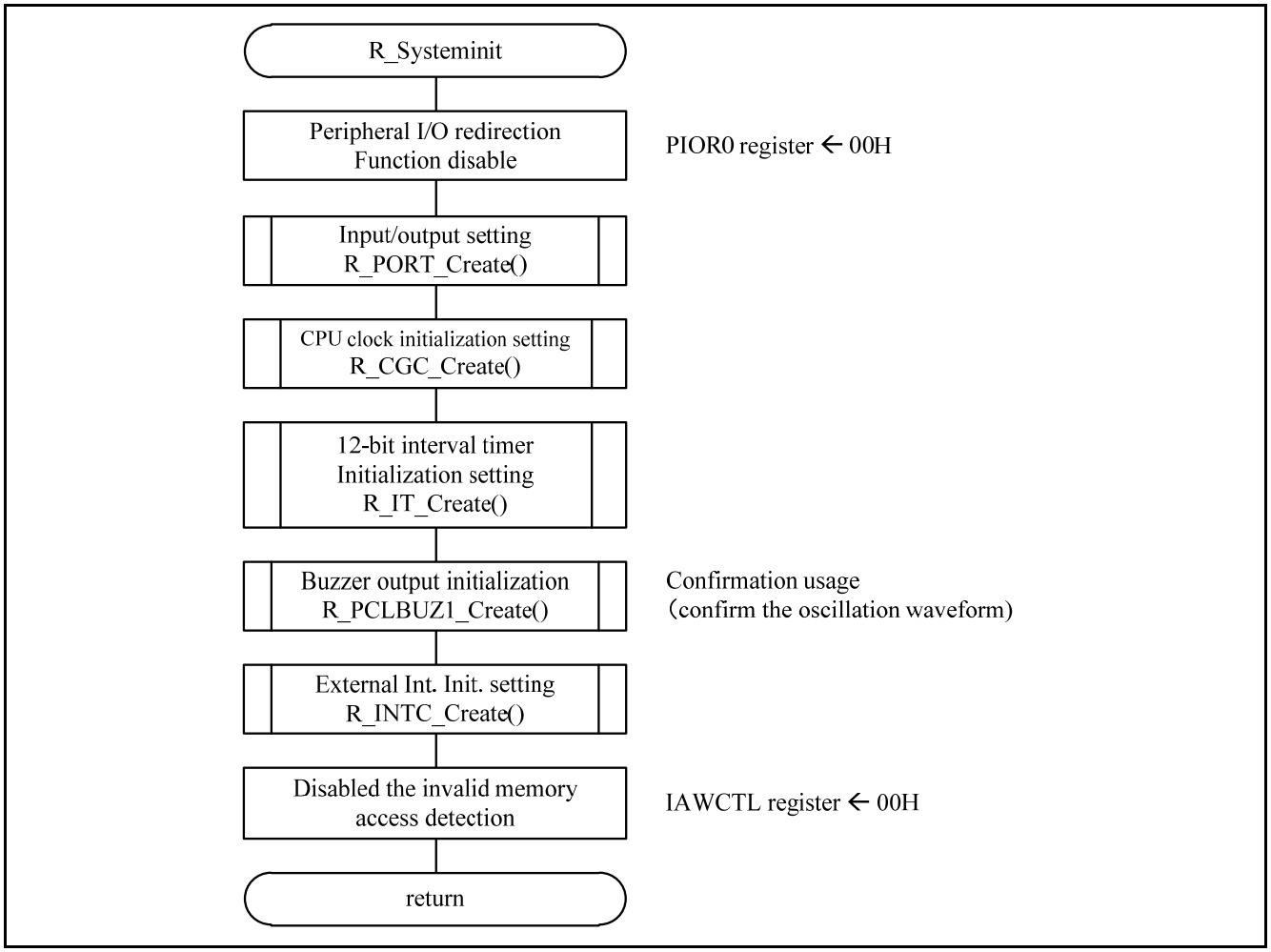

Figure 4.3 Peripheral function initialization

4.7.3. I/O Port Setup

Figure 4.4 shows the flowchart of I/O Port Setup.

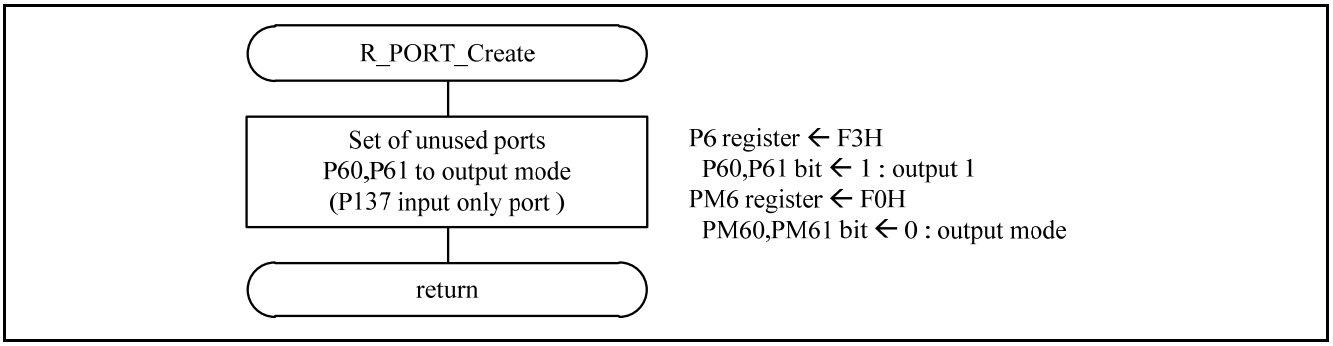

Figure 4.4 I/O Port Setup

Caution: Provide proper treatment for unused pins so that their electrical specifications are observed. Connect each of any unused input-only ports to V_{DD} or V_{SS} via a separate resistor.

Setting up the LED1-LED2 pin

- Port register (P6)
- Port mode register (PM6)

Select I/O mode and output level of each port for LED1,LED2

Symbol: PM6

7	6	5	4	3	2	1	0
0	0	0	0	P63	P62	P61	P60
0	**0**	**0**	**0**	**0**	**0**	**1**	**1**

Bit 1

P61	P61 I/O mode selection
0	Output 0
1	**Output 1**

Bit 0

P60	P60 I/O mode selection
0	Output 0
1	**Output 1**

Symbol: PM6

7	6	5	4	3	2	1	0
1	1	1	1	PM63	PM62	PM61	PM60
1	**1**	**1**	**1**	**0**	**0**	**0**	**0**

Bit 1

PM61	**PM61 I/O mode selection**
0	**Output mode (output buffer on)**
1	Input mode (output buffer off)

Bit 0

PM60	**PM60 I/O mode selection**
0	**Output mode (output buffer on)**
1	Input mode (output buffer off)

Caution: For details on the register setup procedures, refer to RL78/I1D User's Manual: Hardware.

4.7.4. CPU clock initialization

Figure 4.5 shows the flowchart of CPU clock initialization.

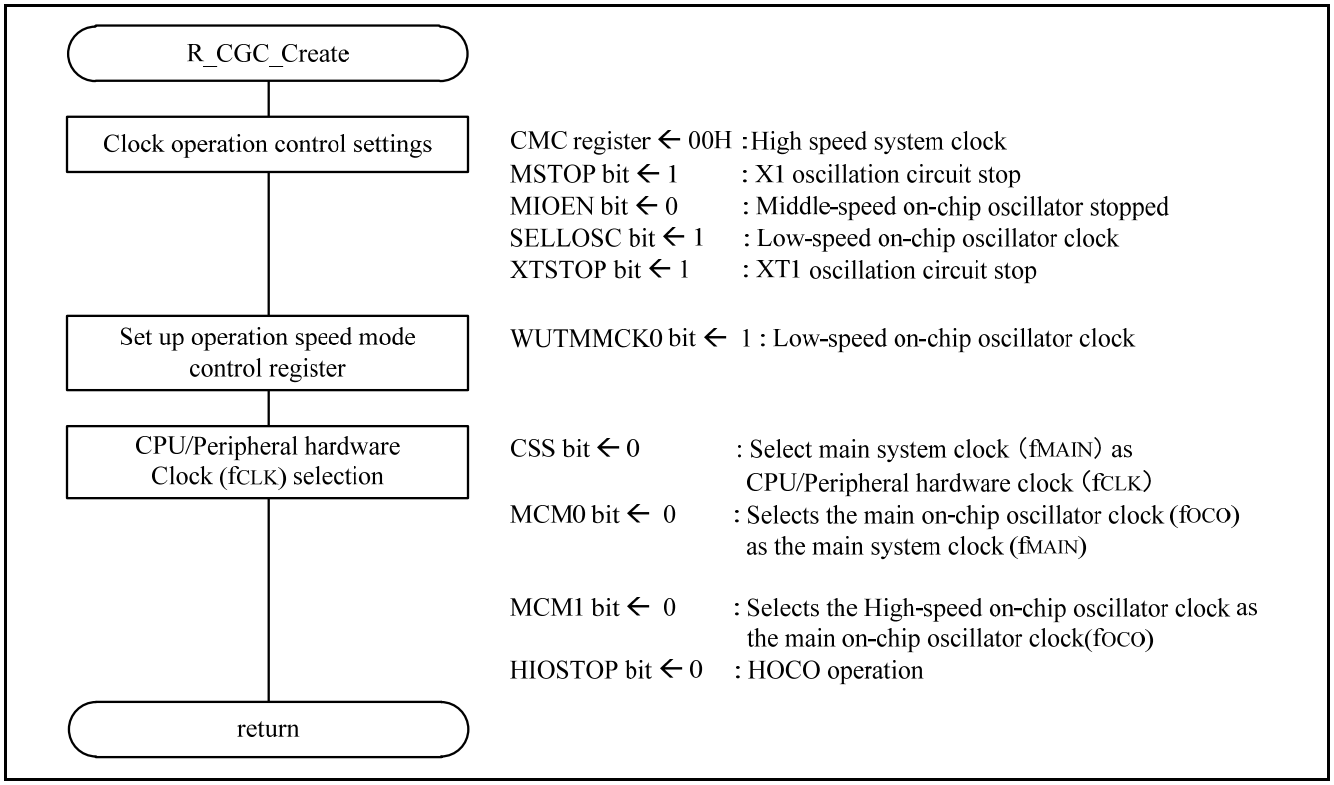

Figure 4.5 CPU clock initialization

Note: Refer to RL78/G13 (R01AN2575J) application note for CPU clock setting (R_CGC_Create()).

Setting up the clock operation mode

- Clock operation mode control register (CMC)
  High-speed system clock pin operation mode: Input port mode
  Subsystem clock pin operation mode: Input port mode

Symbol: CMC

7	6	5	4	3	2	1	0
EXCLK	OSCSEL	EXCLKS	OSCSELS	0	AMPHS1	AMPHS0	AMPH
0	**0**	**0**	**0**	0	**0**	**0**	0

Bits 7 and 6

EXCLK	OSCSEL	High-speed system clock pin operation mode	X1/P121 pin	X2/EXCLK/P122 pin
0	**0**	**Input port mode**	**Input port**	
0	1	X1 oscillation mode	Crystal/ceramic resonator connection	
1	0	Input port mode	Input port	
1	1	External clock input mode	Input port	External clock input

Bits 5 and 4

EXCLKS	OSCSELS	Subsystem clock pin operation mode	XT1/P123 pin	XT2/EXCLKS/P124 pin
0	**0**	**Input port mode**	**Input port**	
0	1	XT1 oscillation mode	Crystal resonator connection	
1	0	Input port mode	Input port	
1	1	External clock input mode	Input port	External clock input

Caution: For details on the register setup procedures, refer to RL78/I1D User's Manual: Hardware.

Controlling the operation of the clocks

- Clock operation status control register (CSC)
  High-speed system clock operation control: Stopped
  Subsystem clock operation control: Stopped
  High-speed on-chip oscillator clock operation control: Operating

Symbol: CSC

7	6	5	4	3	2	1	0
MSTOP	XTSTOP	0	0	0	0	MIOEN	HIOSTOP
1	**1**	0	0	0	0	0	**0**

Bit 7

MSTOP	**High-speed system clock operation control**		
	X1 oscillation mode	**External clock input mode**	**Input port mode**
0	X1 oscillator operating	External clock from EXCLK pin is valid	**Input port**
1	X1 oscillator stopped	External clock from EXCLK pin is invalid	

Bit 6

XTSTOP	**Subsystem clock operation control**		
	X1 oscillation mode	**External clock input mode**	**Input port mode**
0	X1 oscillator operating	External clock from EXCLKS pin is valid	Input port
1	**XT1 oscillator stopped**	External clock from EXCLKS pin is invalid	

Bit 1

MIOEN	**High-speed on-chip oscillator clock operation control**
0	**High-speed on-chip oscillator operating**
1	High-speed on-chip oscillator stopped

Bit 0

HIOSTOP	**High-speed on-chip oscillator clock operation control**
0	**High-speed on-chip oscillator operating**
1	High-speed on-chip oscillator stopped

Caution: For details on the register setup procedures, refer to RL78/I1D User's Manual: Hardware.

Subsystem clock select

- Subsystem clock select register (CKSEL)
  Select the sub clock or low-speed on-chip oscillator clock
  : low-speed on-chip oscillator clock

Symbol: CKSEL

7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	SELLOSC
0	0	0	0	0	0	0	**1**

Bit 0

SELLOSC	Selection of sub clock/low-speed on-chip oscillator clock
0	Sub clock
1	**Low-speed on-chip oscillator clock**

Controlling the operation speed mode

- Operation speed mode control register (OSMC)
  Setting in STOP mode or HALT mode while subsystem clock is selected as CPU clock
  : Enable supply of subsystem clock to peripheral functions.
  Operating clock for the real-time clock and 12-bit interval timer
  : Low-speed on-chip oscillator clock

Symbol: OSMC

7	6	5	4	3	2	1	0
RTCLPC	0	0	WUTMMCK0	0	0	0	0
0	0	0	**1**	0	0	0	0

Bit 7

RTCLPC	Setting in STOP mode or HALT mode while subsystem clock is selected as CPU clock
0	**Enables supply of subsystem clock to peripheral functions**
1	Stops supply of subsystem clock to peripheral functions other than real-time clock and 12-bit interval timer

Bit 4

WUTMMCK0	Selection of operation clock for real-time clock and 12-bit interval timer
0	**Subsystem clock**
1	**Low-speed on-chip oscillator clock**

Caution: The OSMC register is intended to be used to reduce power consumption by reducing the operating current of the device in the STOP and HALT modes while the subsystem clock is selected as CPU clock. For details on the register setup procedures, refer to RL78/I1D User's Manual: Hardware.

Setting up the CPU/peripheral hardware clock (f_{CLK})

- System clock control register (CKC)
  f_{CLK} initial value: High-speed on-chip oscillator clock (f_{IH})

Symbol: CKC

7	6	5	4	3	2	1	0
CLS	CSS	MCS	MCM0	0	0	MCS1	MCM1
0	**0**	0	**0**	0	0	0	**0**

Bit 6

CSS	Selection of CPU/peripheral hardware clock (f_{CLK})
0	**Main system clock (f_{MAIN})**
1	Subsystem clock (f_{SUB})

Bit 4

MCM0	Main system clock (f_{MAIN}) operation control
0	**Selects the high-speed on-chip oscillator clock (f_{IH}) as the main system clock (f_{MAIN})**
1	Selects the high-speed system clock (f_{MX}) as the main system clock (f_{MAIN}).

Bit 0

MCM1	Main system clock (f_{MAIN}) operation control
0	**High-speed on-chip oscillator clock**
1	Middle-speed on-chip oscillator clock

Caution: For details on the register setup procedures, refer to RL78/I1D User's Manual: Hardware.

4.7.5. 12-bit interval timer initialization

Figure 4.6 shows the flowchart of 12-bit interval timer initialization.

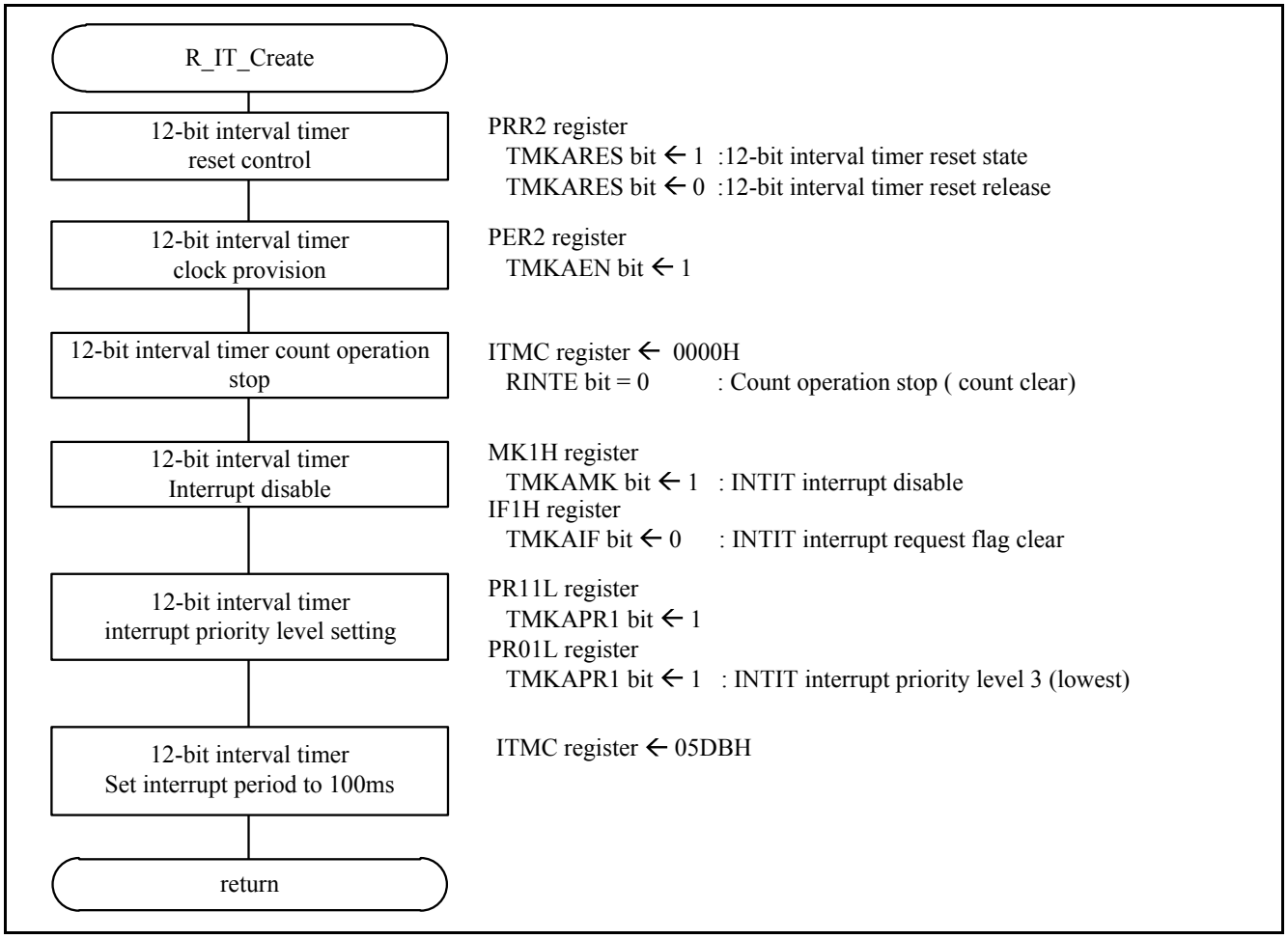

Figure 4.6 12-bit interval timer initialization

4.7.6. Clock output initialization

Figure 4.7 shows the flowchart of clock output initialization.

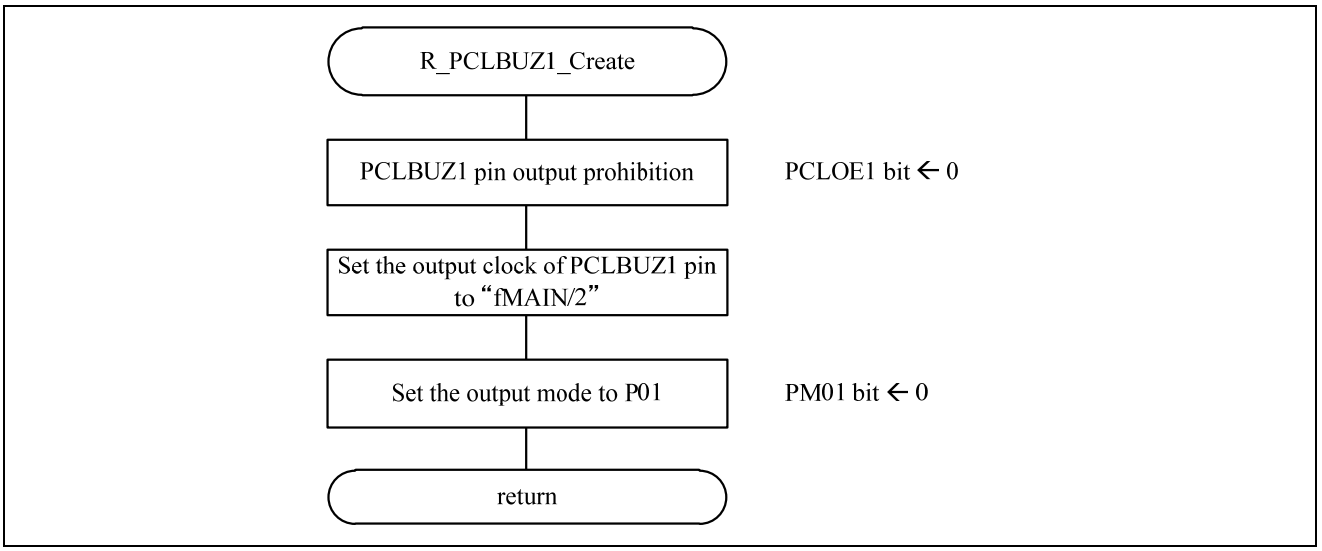

Figure 4.7 clock output initialization

4.7.7. INTP0 initialization

Figure 4.8 shows the flowchart of INTP0 initialization.

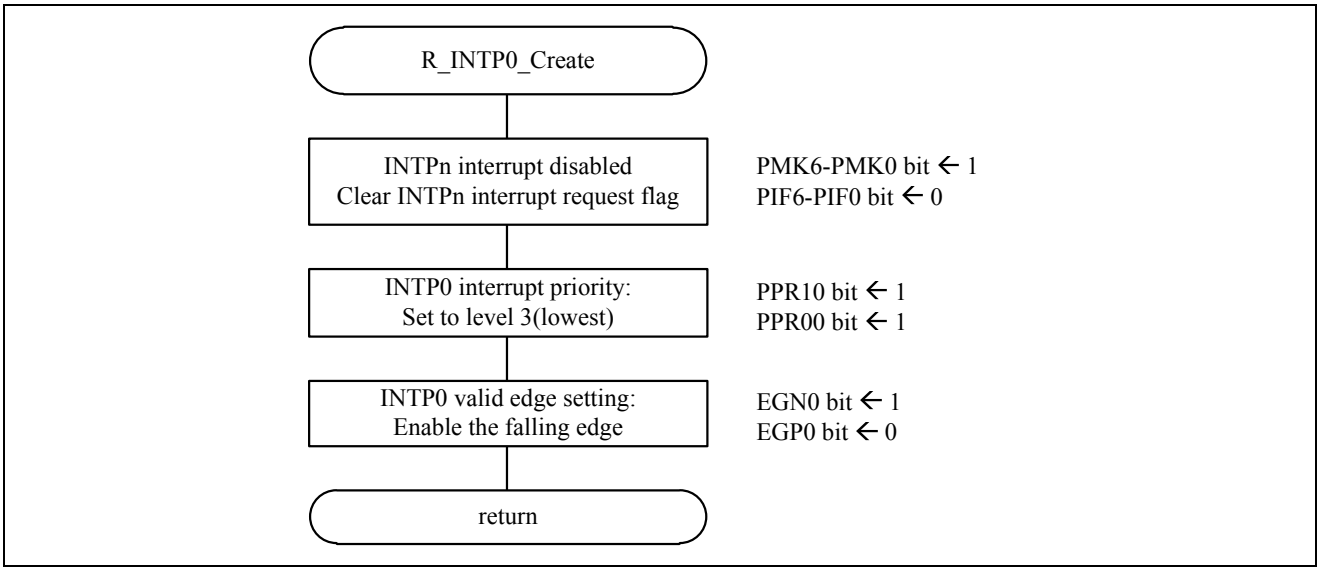

Figure 4.8 INTP0 initialization

4.7.8. The main processing

Figure 4.9 shows the flowchart of main processing.

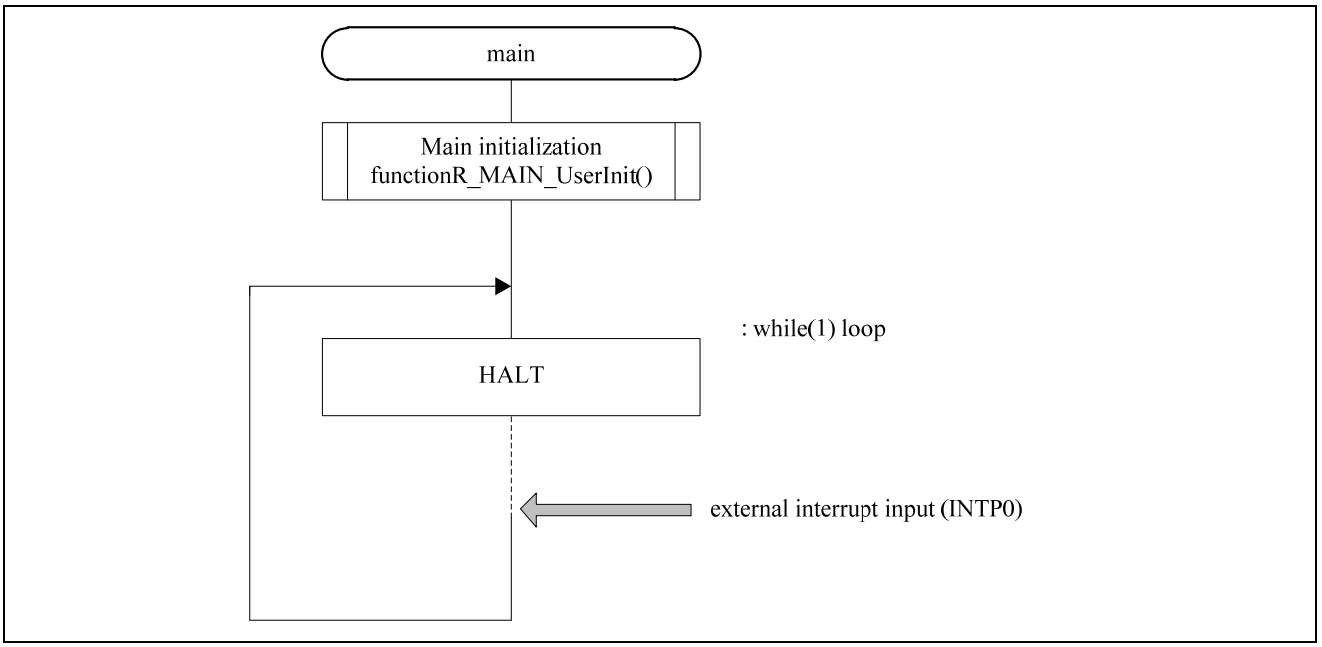

Figure 4.9 The main processing

4.7.9. The main user initialization

Figure 4.10 shows the flowchart of the main user initialization.

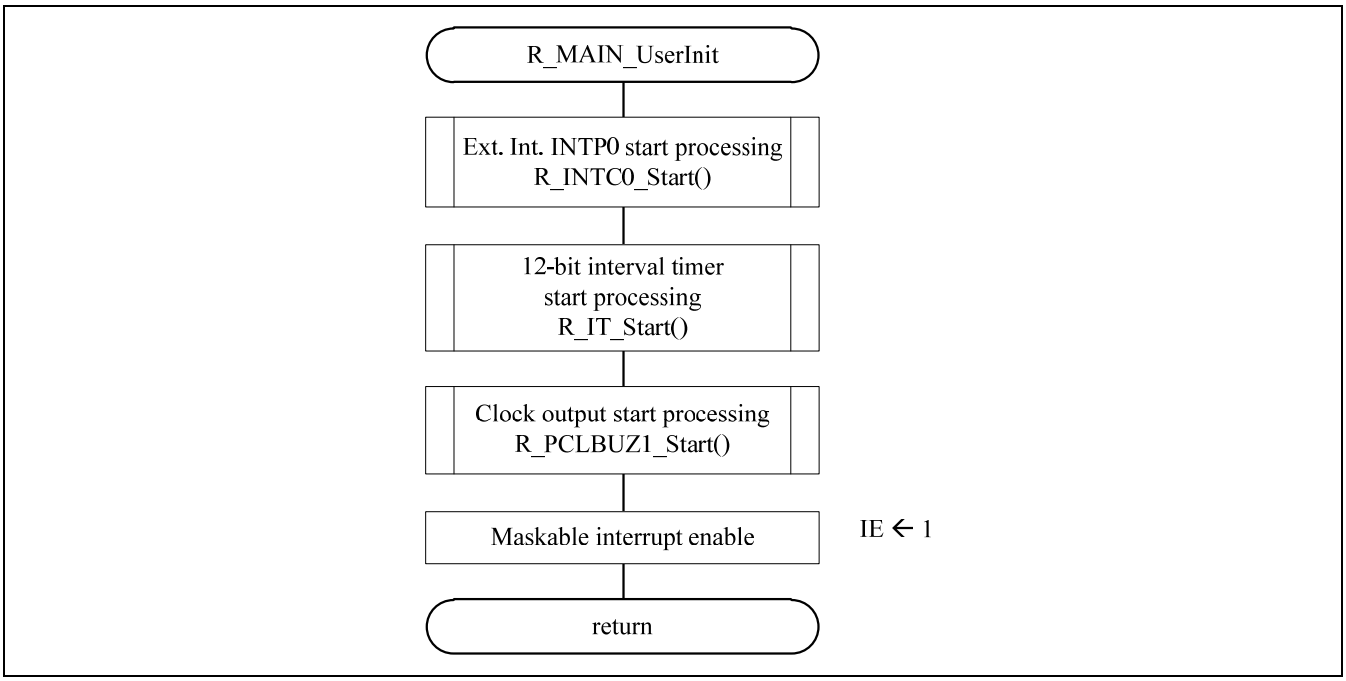

Figure 4.10 The main user initialization

4.7.10. INTP0 interrupt enable processing

Figure 4.11 shows the flowchart of INTP0 interrupt enable processing.

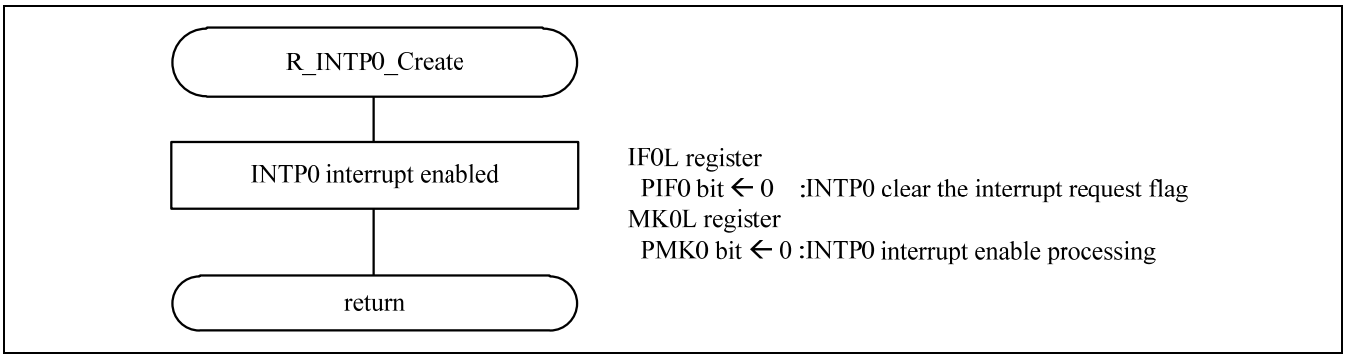

Figure 4.11 INTP0 interrupt enable processing

4.7.11. 12-bit interval timer start processing

Figure 4.12 shows the flowchart of 12-bit interval timer start processing.

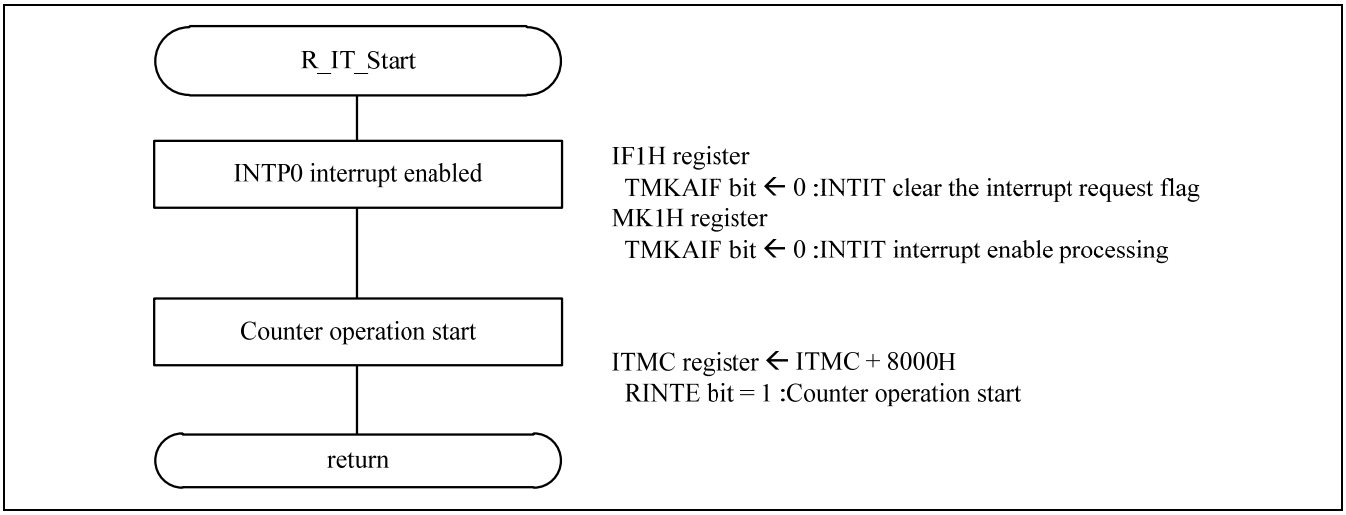

Figure 4.12 12-bit interval timer start processing

4.7.12. Clock output start processing

Figure 4.13 shows the flowchart of clock output start processing.

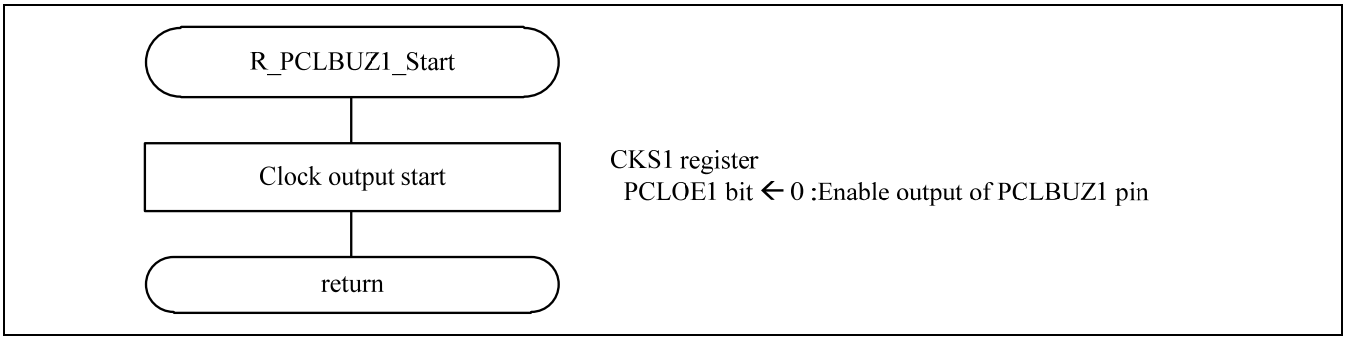

Figure 4.13 Clock output start processing

4.7.13. Flash operation mode switching (LV) processing

Figure 4.14 shows the flowchart of the flash operation mode switching (LV) processing.

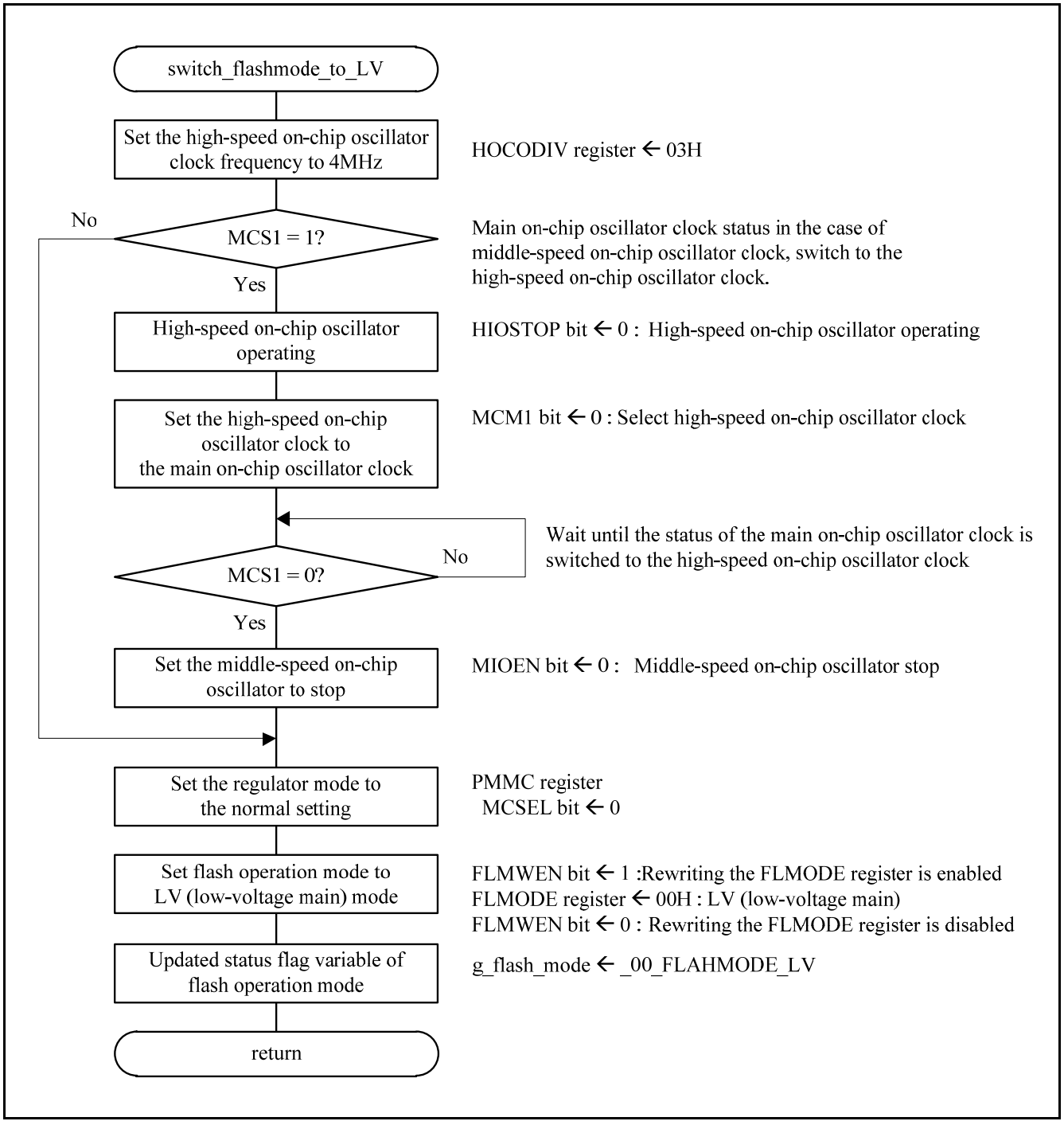

Figure 4.14 Flash operation switching (LV) processing

Regulator mode control

- Regulator mode control register (PMMC)
  Regulator mode control : Normal setting

Symbol: PMMC

7	6	5	4	3	2	1	0
0	MCSEL	0	0	0	0	0	0
0	**0**	**0**	**0**	0	**0**	**0**	0

Bit 6

MCSEL	Control of regulator mode
0	**Normal setting**
1	Low-power consumption setting

Access control to the flash operation mode select register

- Flash operating mode protect register (FLMWRP)
  Control of the flash operation mode select register
- : Rewriting the FLMODE register is enabled

Symbol: FLMWRP

7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	FLMWEN
0	**0**	**0**	**0**	0	**0**	**0**	1

Bit 0

FLMWEN	Control of regulator mode
0	Rewriting the FLMODE register is disabled
1	**Rewriting the FLMODE register is enabled**

Caution: For details on the register setup procedures, refer to RL78/I1D User's Manual: Hardware.

4.7.14. Flash operation mode switching (LS normal) processing

Figure 4.15, Figure 4.16 shows the flowchart of the flash operation mode switching (LS normal).

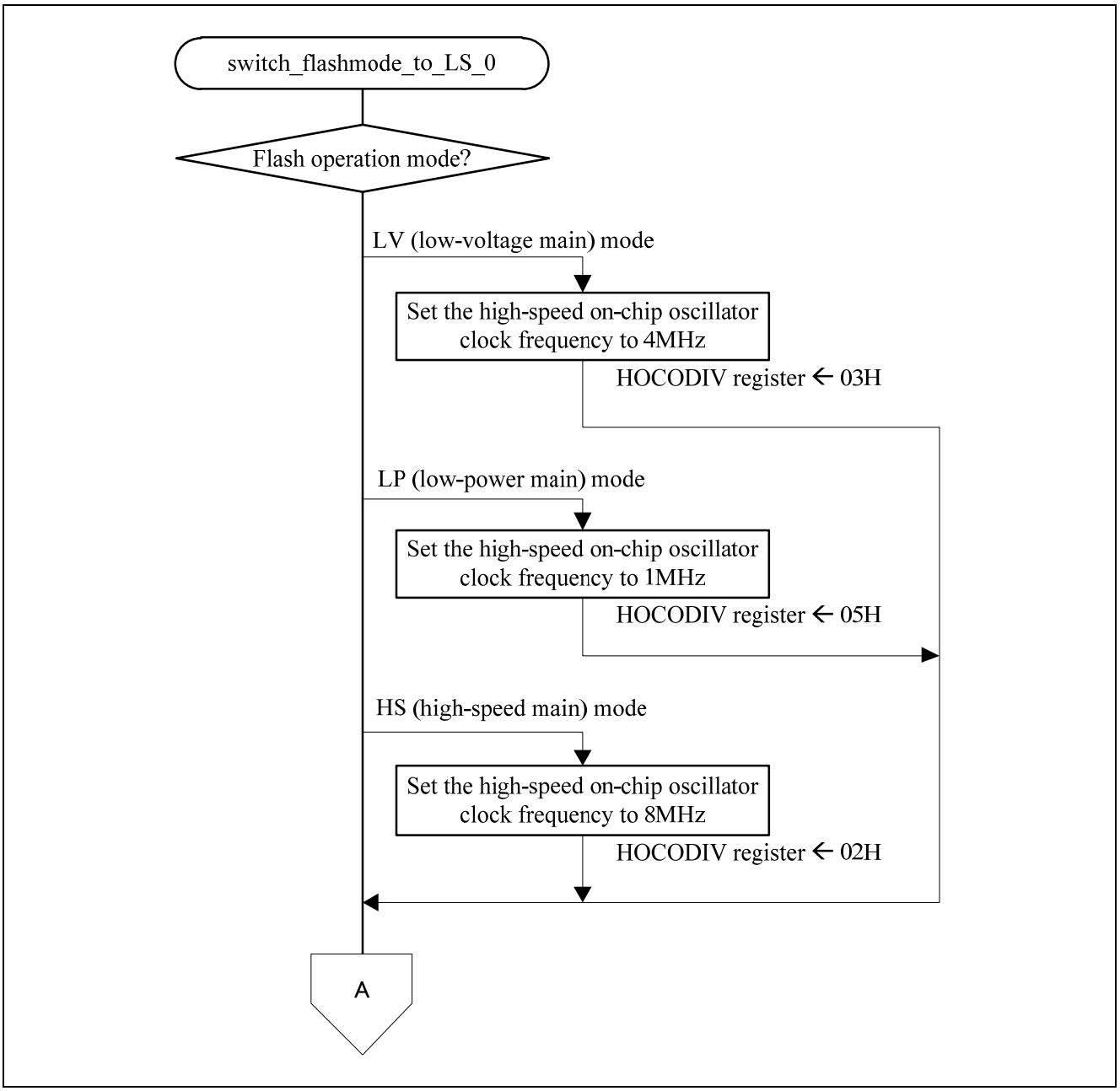

Figure 4.15 Flash operation mode switching (LS normal) processing(1/2)

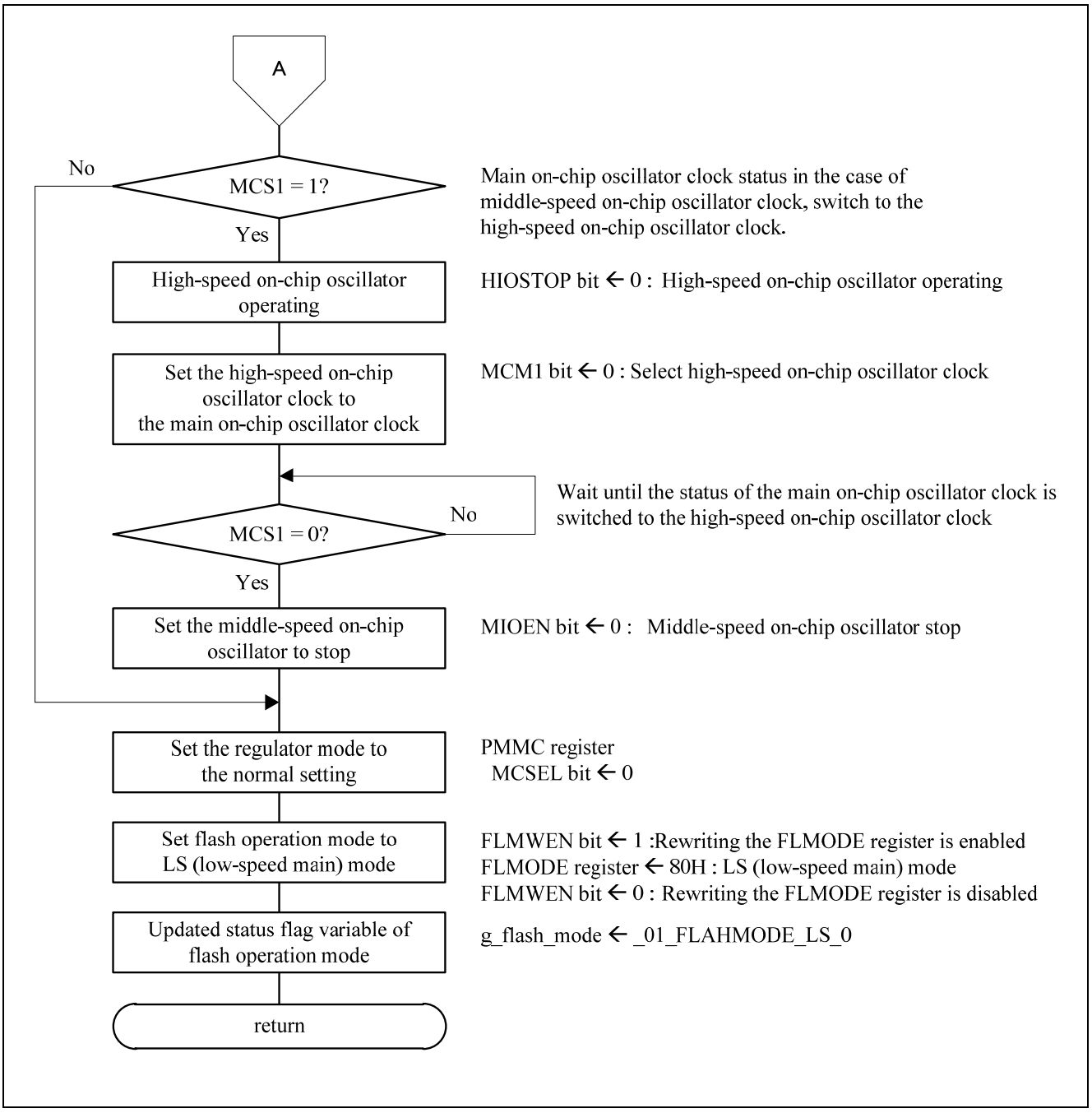

Figure 4.16 Flash operation mode switching (LS normal) processing(2/2)

4.7.15. Flash operation mode switching (LS low consumption) processing

Figure 4.17 shows the flowchart of the flash operation mode switching (LS low consumption) processing.

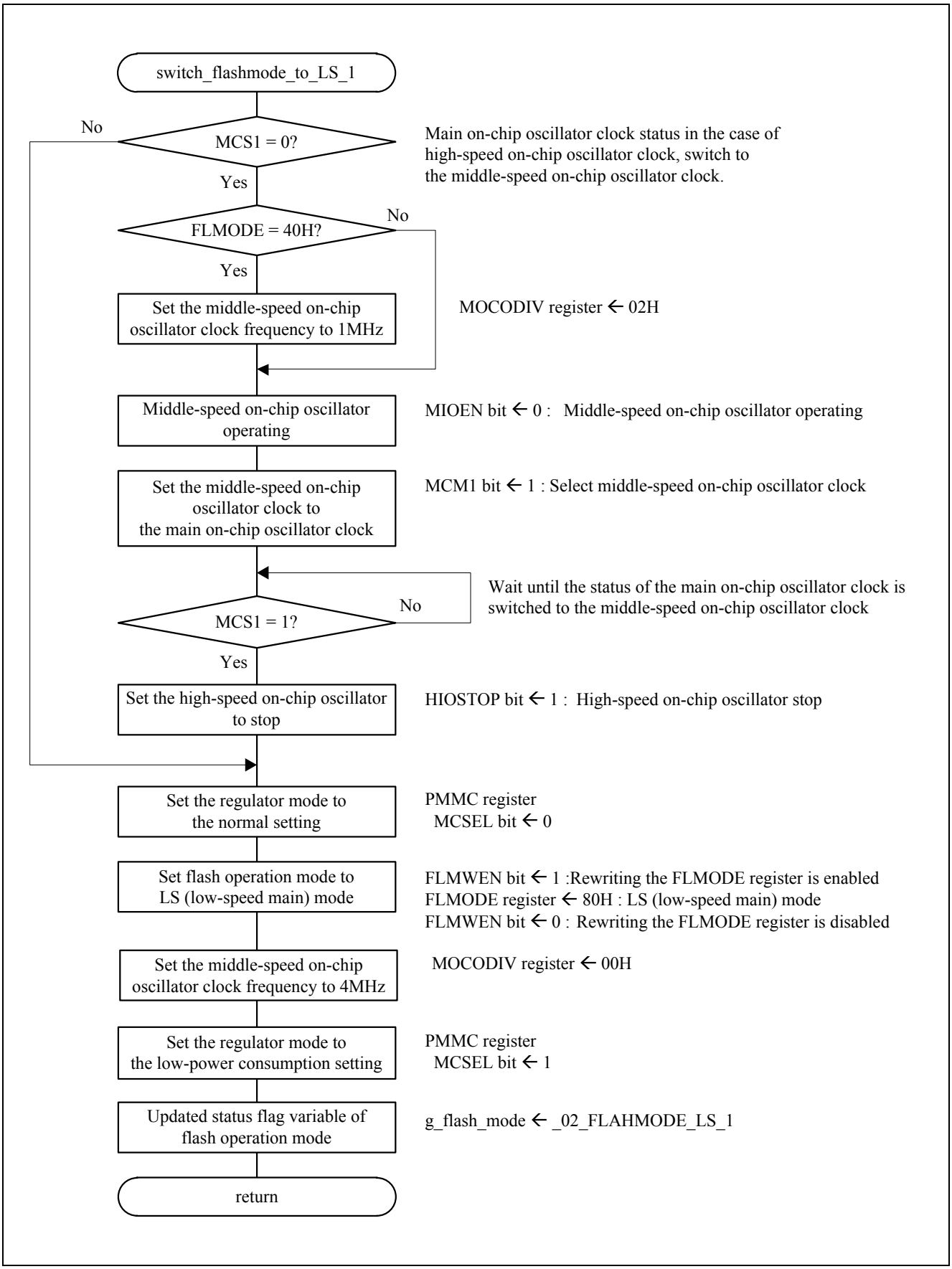

Figure 4.17 Flash operation mode switching (LS low consumption) processing

4.7.16. Flash operation mode switching (HS) processing

Figure 4.18, Figure 4.19 shows the flowchart of the flash operation mode switching (HS) processing.

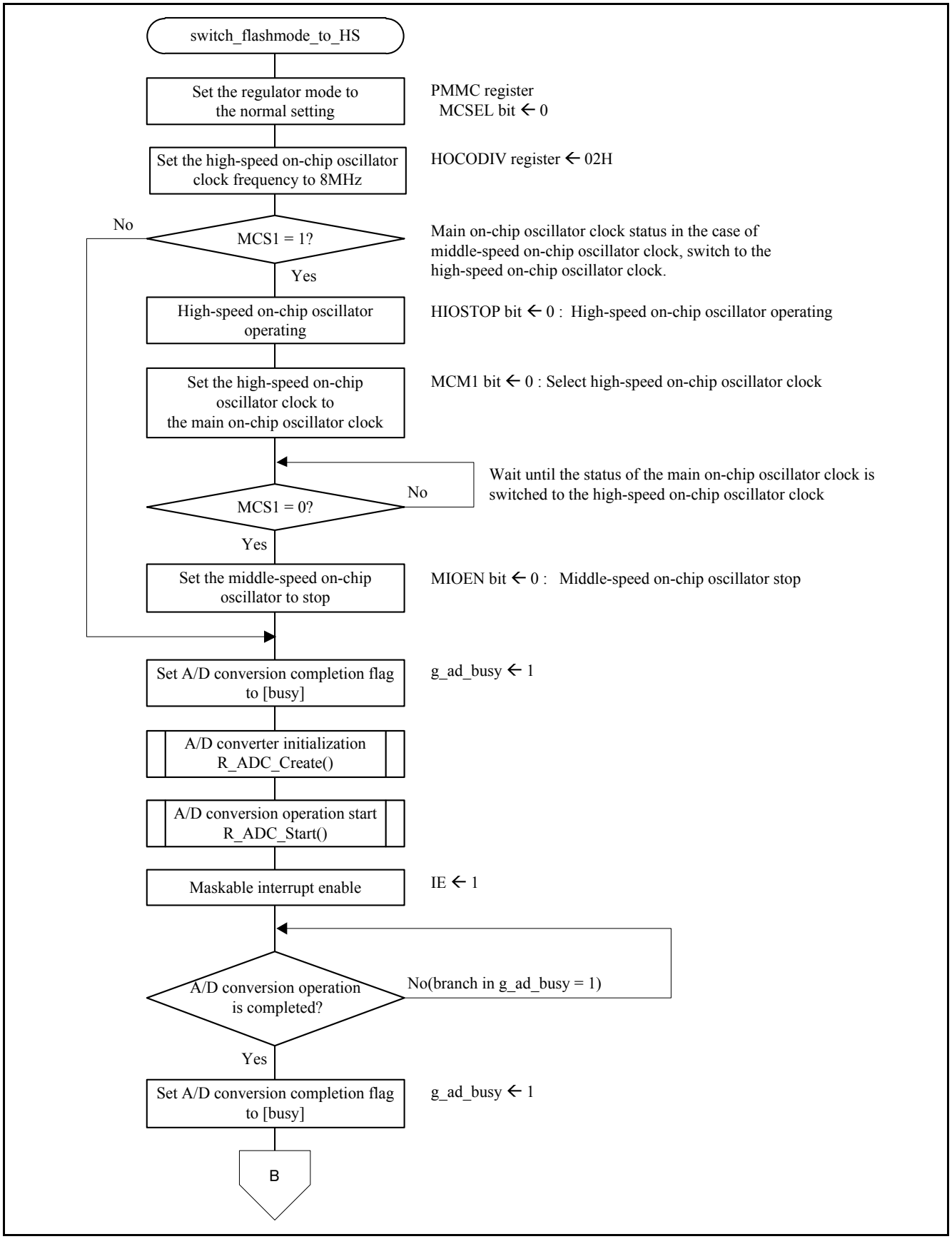

Figure 4.18 Flash operation mode switching (HS) processing(1/2)

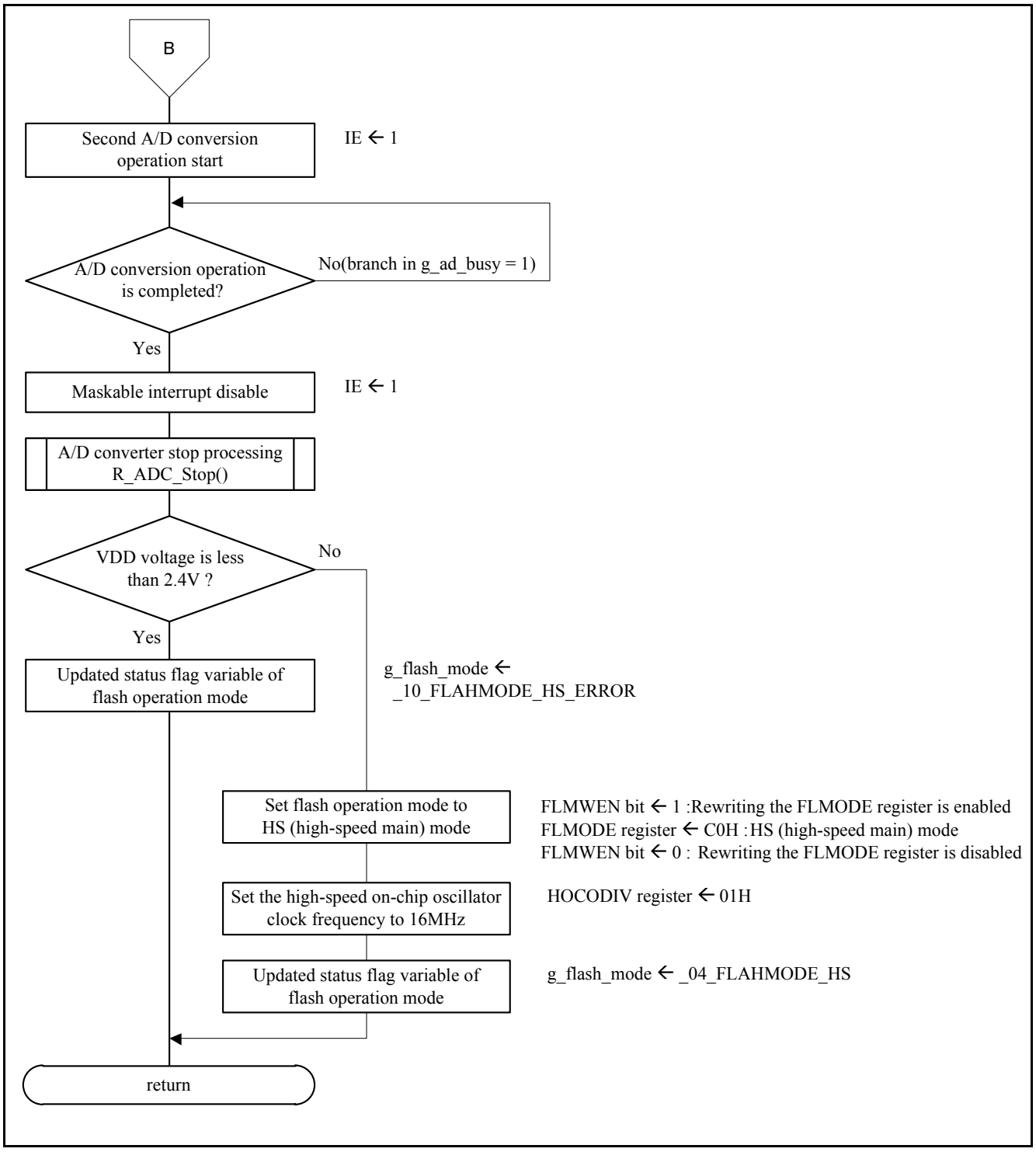

Figure 4.19 Flash operation mode switching (HS) processing(2/2)

4.7.17. A/D converter initialization

Figure 4.20 shows the flowchart of A/D converter initialization.

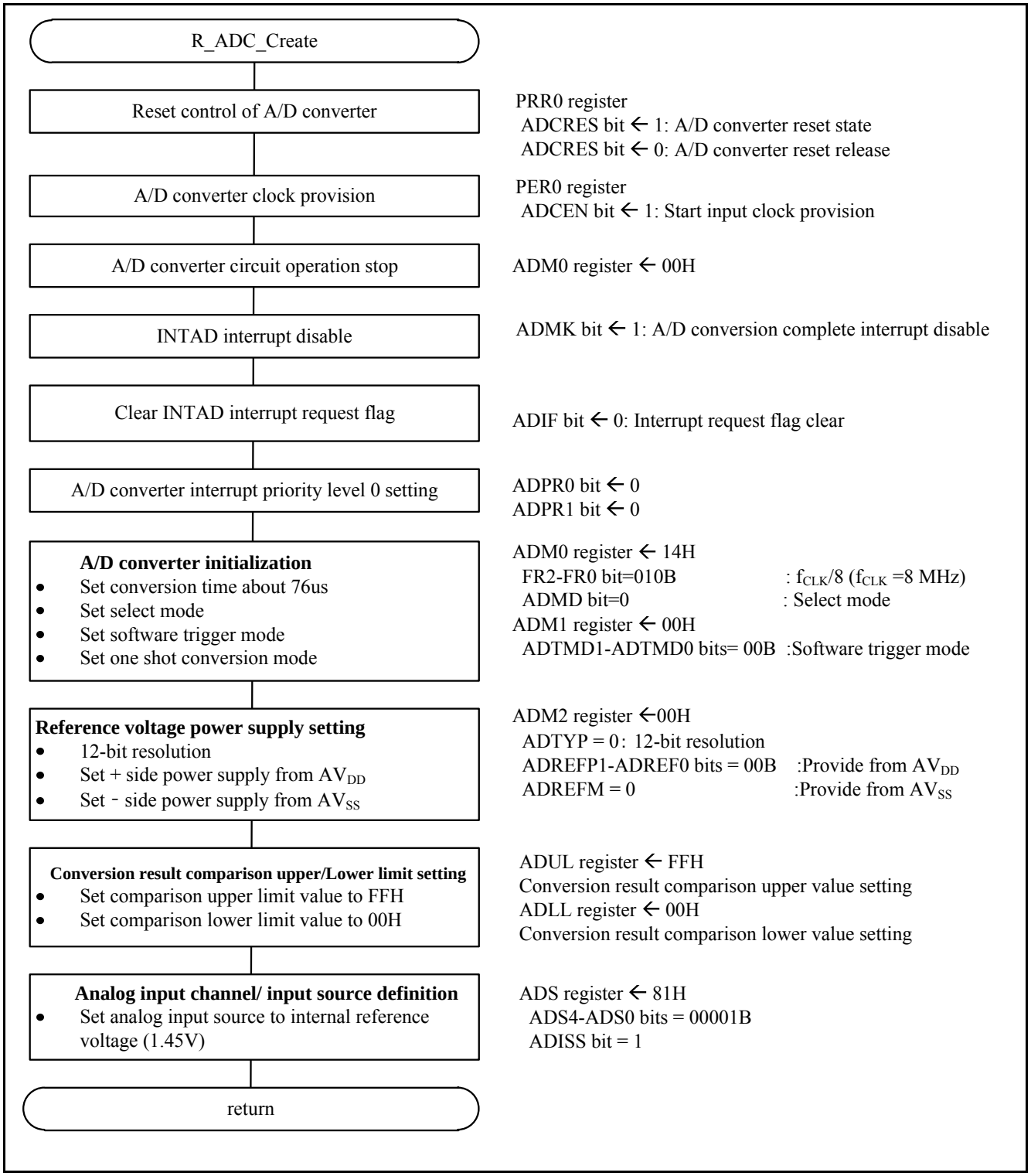

Figure 4.20 A/D converter initialization

4.7.18. A/D conversion operation start processing

Figure 4.21 shows the flowchart of A/D converter initialization.

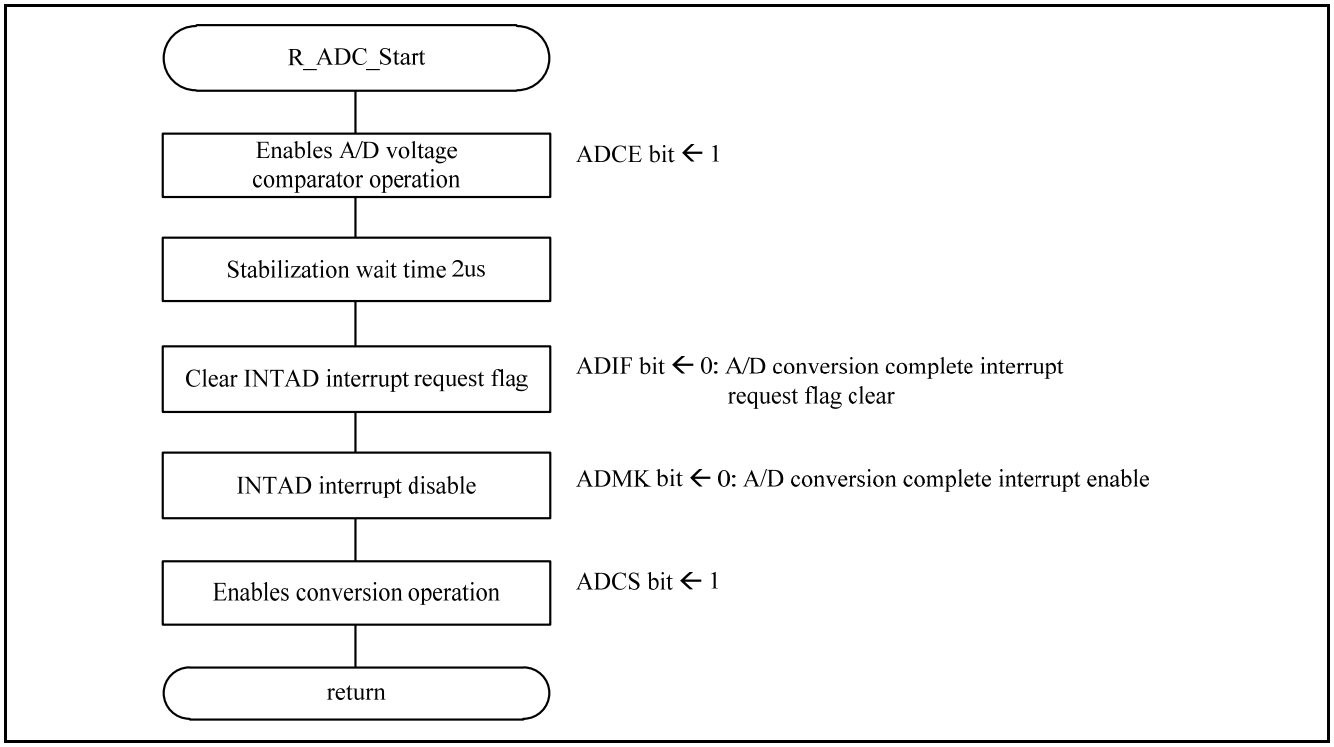

Figure 4.21 A/D conversion operation start processing

4.7.19. A/D converter stop processing

Figure 4.22 shows the flowchart of A/D converter initialization.

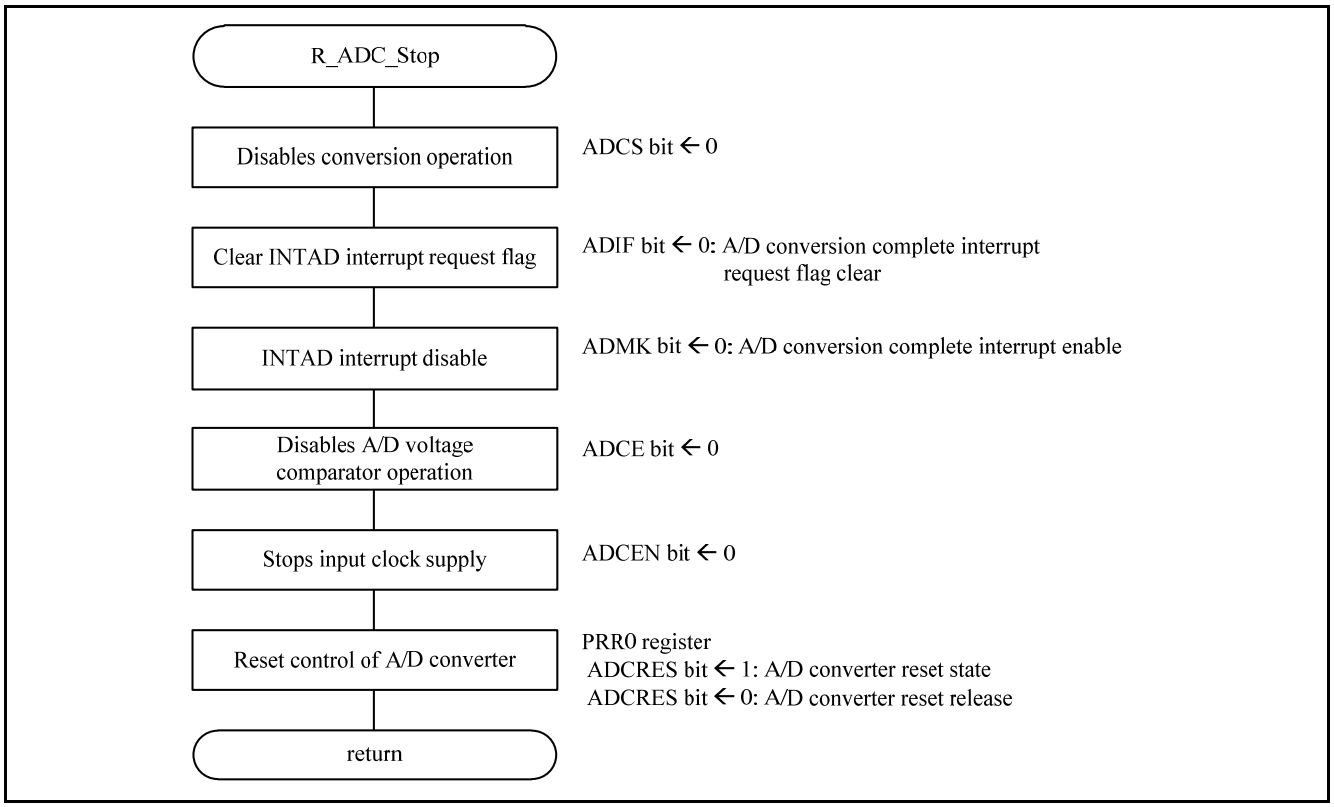

Figure 4.22 A/D converter stop processing

4.7.20. Flash operation mode switching (LP) processing

Figure 4.23 shows the flowchart of the flash operation mode switching (LP) processing.

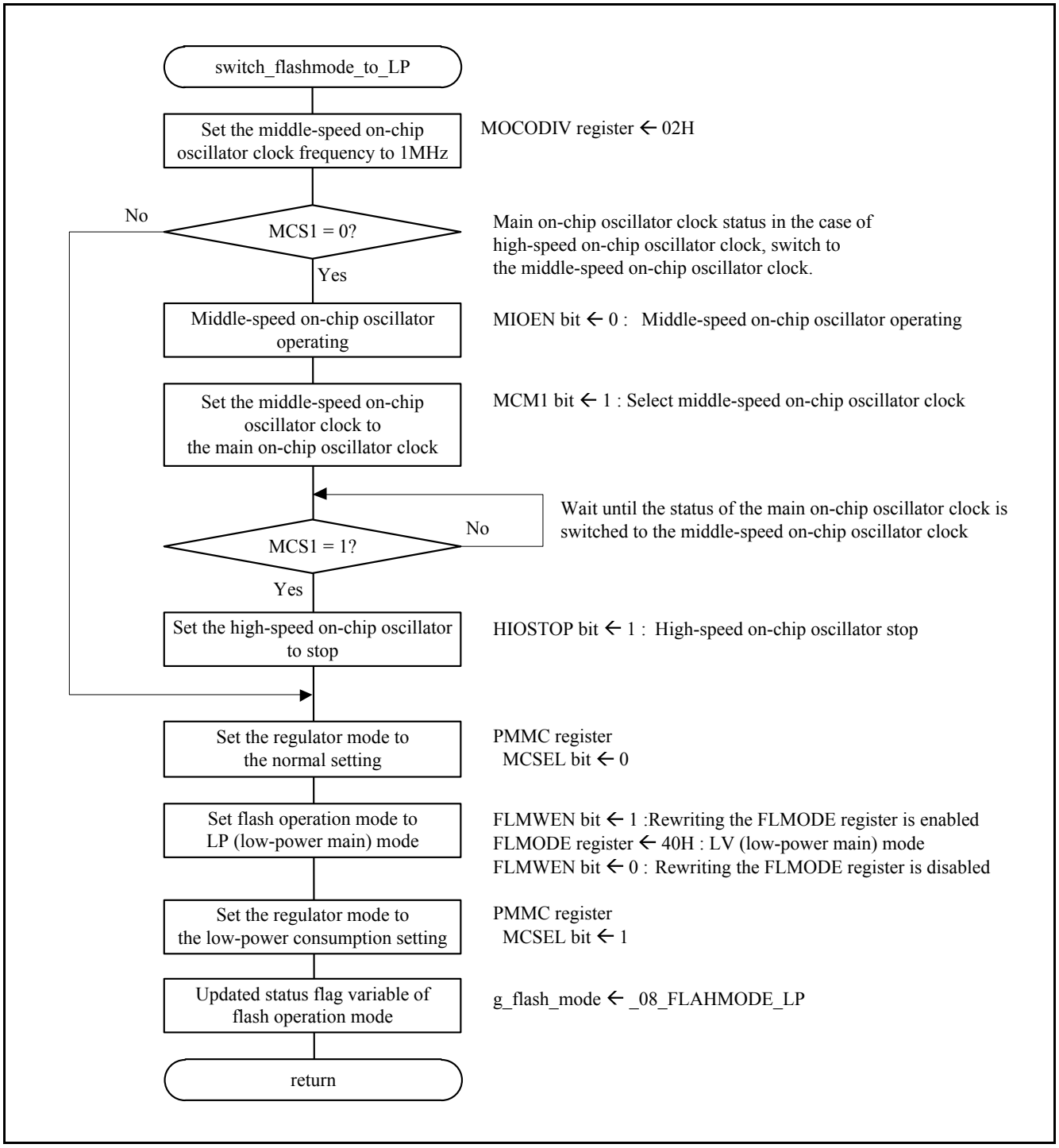

Figure 4.23 Flash operation mode switching (LP normal) processing

4.7.21. External interruption (INTP0) processing

Figure 4.24, Figure 4.25 shows the flowchart of the external interruption (INTP0) processing.

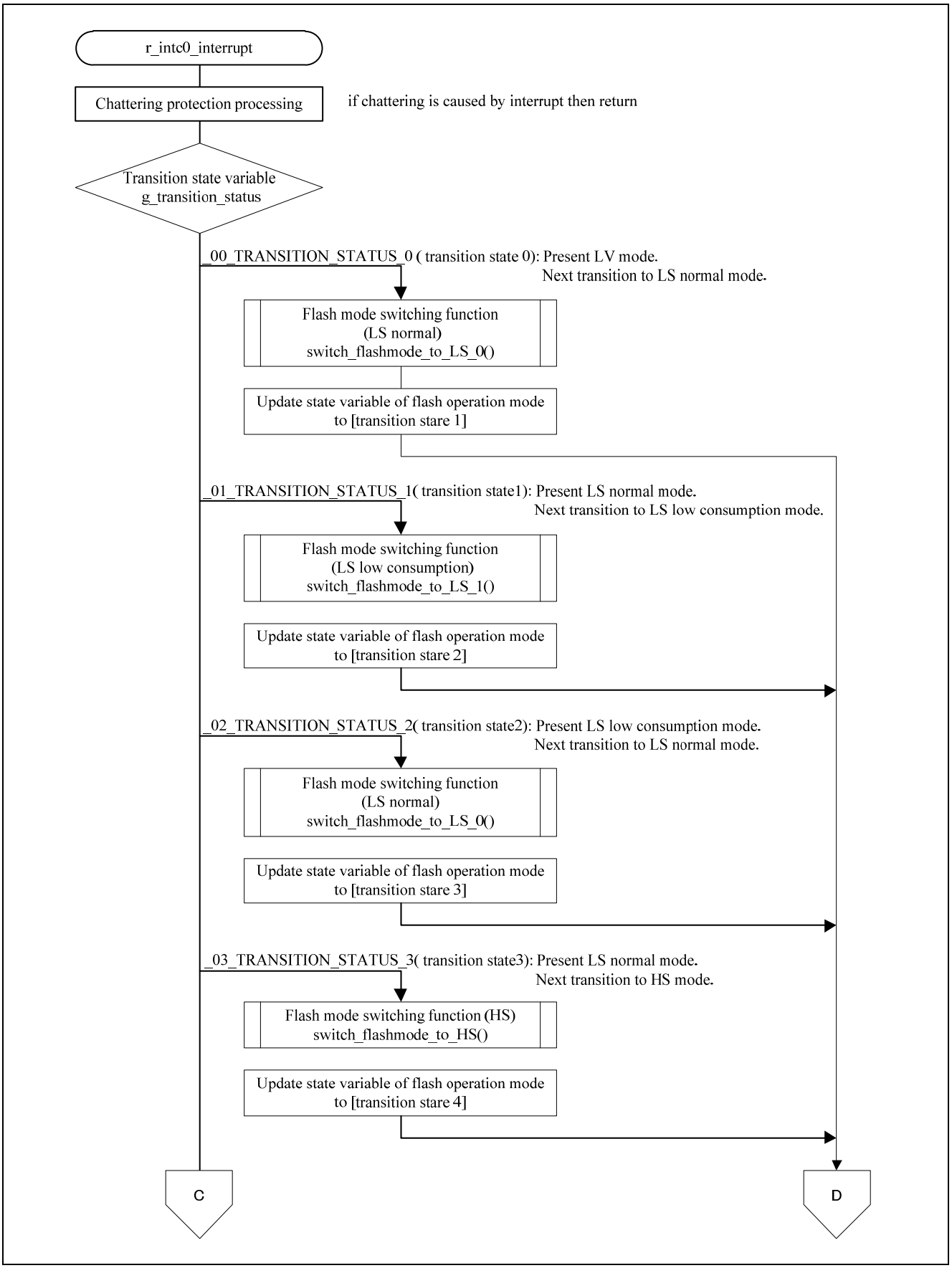

Figure 4.24 External interrupt (INTP0) processing(1/2)

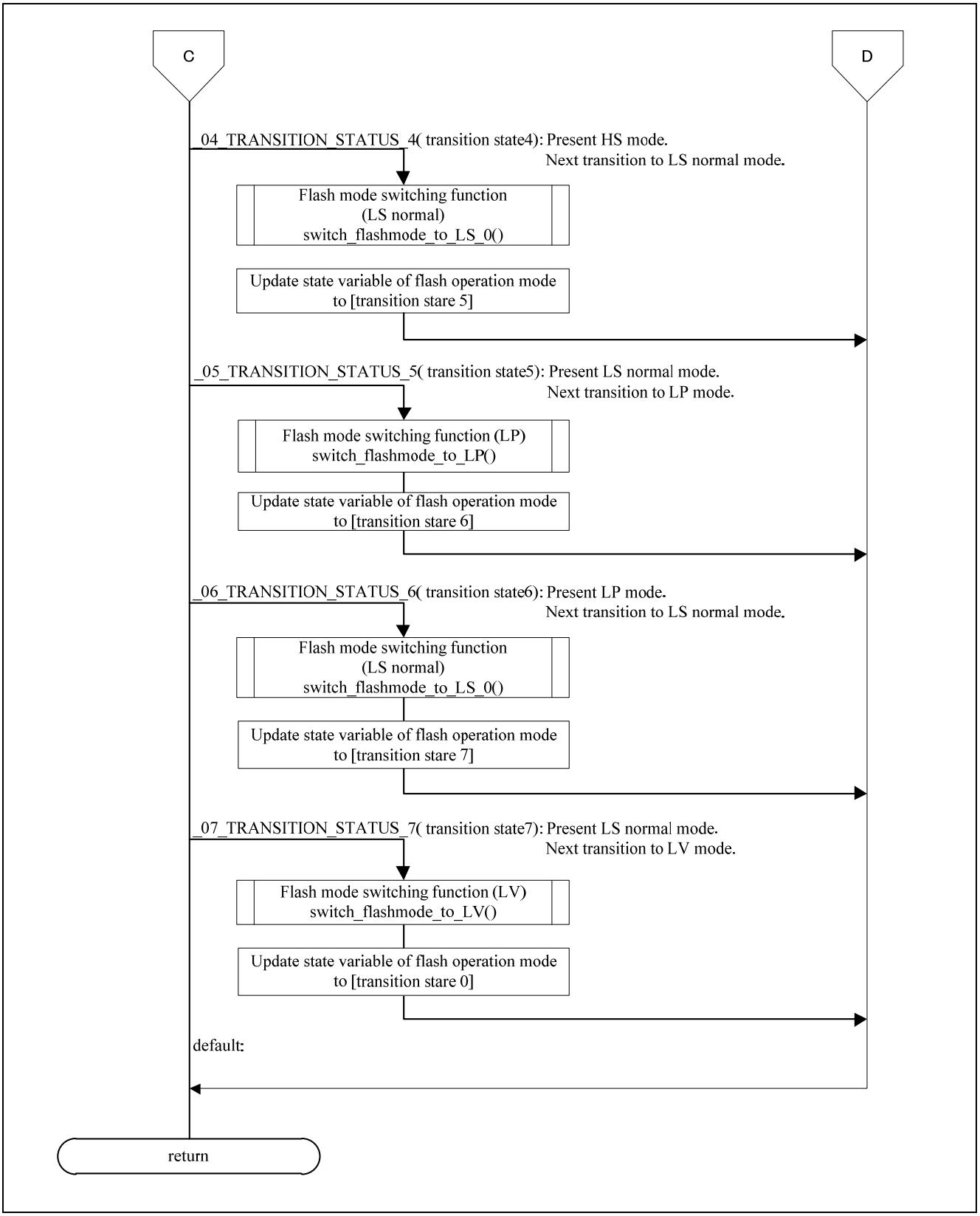

Figure 4.25 External interrupt (INTP0) processing(2/2)

4.7.22. 12-bit interval timer interrupt processing

Figure 4.26 shows the flowchart of the 12-bit interval timer interrupt processing.

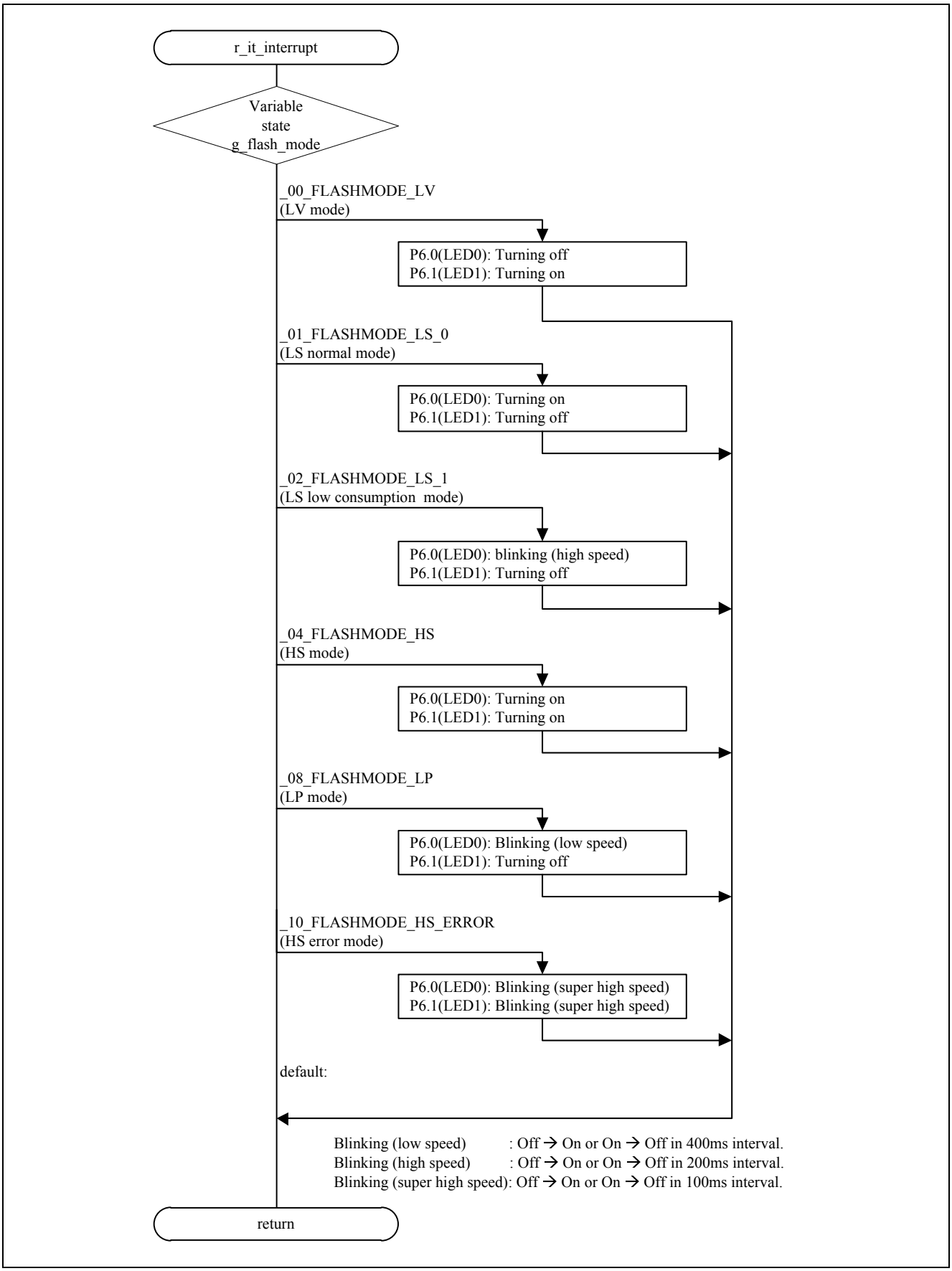

Figure 4.26 12-bit interval timer interrupt processing

4.7.23. A/D conversion complete interrupt processing

Figure 4.27 shows the flowchart of the A/D conversion complete interrupt processing.

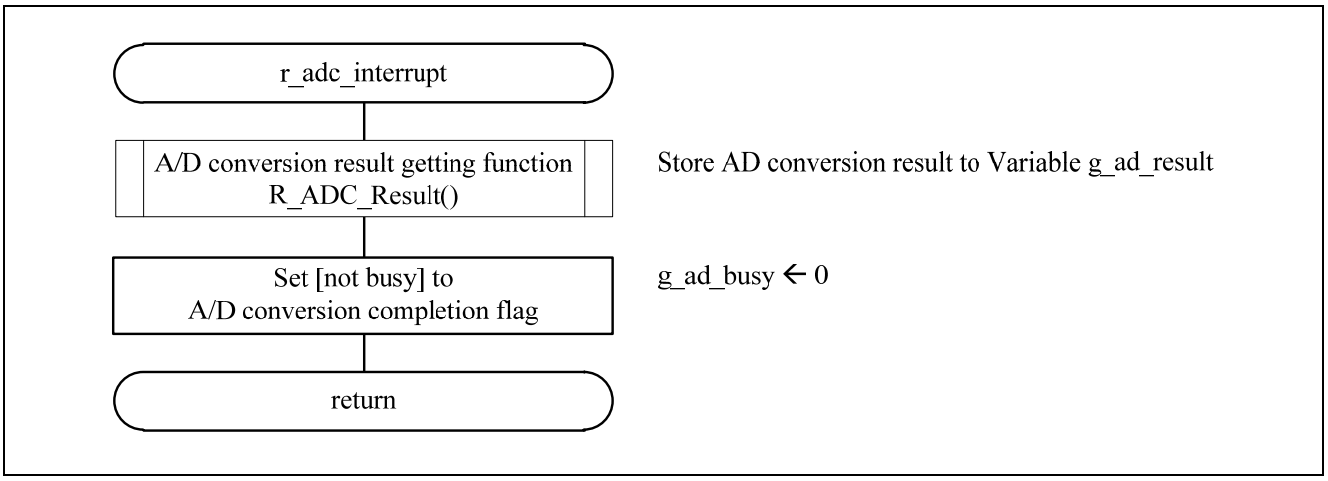

Figure 4.27 A/D conversion complete interrupt processing

4.7.24. A/D conversion result acquisition process

Figure 4.28 shows the flowchart of the A/D conversion result acquisition processing.

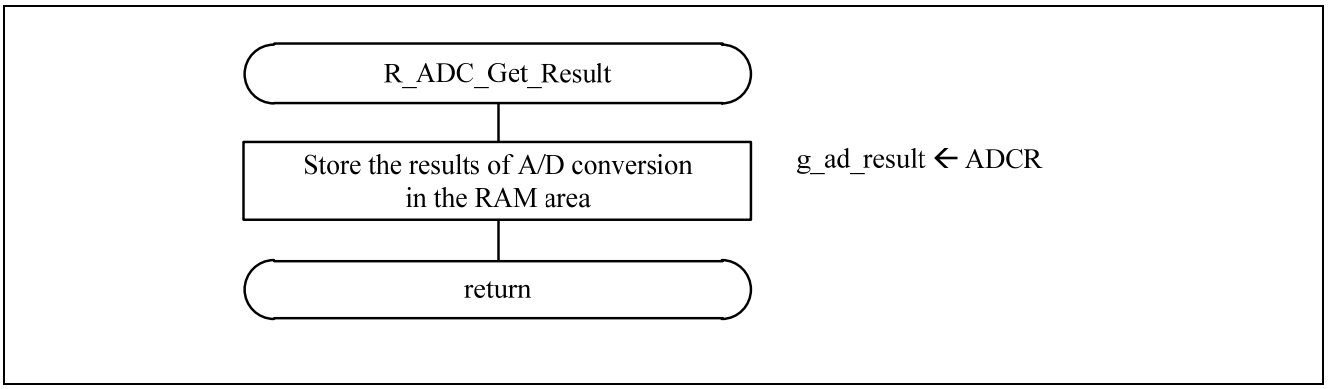

Figure 4.28 A/D conversion result acquisition processing

5. Power supply current measurement of the flash operating modes

The application note, there is a power supply current measurement mode. Please enable "#define _CURRENT_EVALUATION_MODE_" (r_cg_userdefine.h).

Power supply current measurement mode operates only the main system clock. All peripheral functions is stoped. Power supply current measurement mode can measure the HALT mode.

The operation of the power supply current measurement mode

RL78/I1D operation state is switched by a button is pressed (INTP0 interrupt generation).

Wait for the button press (INTP0 interrupt generation) in HALT mode.

All peripheral functions other than the main system clock is stopped.

Table 5.1 is describe the details and transition of power supply current measurement mode.

Table 5.1 Details and transition of power supply current measurement mode

Transition state	State	Operation clock	Range of operation voltage	Status of the next transition
0 (after reset)	LV mode	HOCO: 4MHz	1.6V~3.6V	1
1	LV mode	MOCO: 4MHz	1.8V~3.6V	2
2	LS mode (low consumption setting)	MOCO: 4MHz	1.8V~3.6V	3
3	LS mode (Normal setting)	HOCO: 8MHz	1.8V~3.6V	4 or 4-Error
4	HS mode	HOCO: 16MHz	2.4V~3.6V	5
4-Error	LS mode (Normal setting)	HOCO: 8MHz	1.8V~3.6V	5
5	LS mode (Normal setting)	HOCO: 8MHz	1.8V~3.6V	6
6	LP mode	MOCO: 1MHz	1.8V~3.6V	7
7	LS mode (Normal setting)	HOCO: 8MHz	1.8V~3.6V	0

Hardware configuration of the power supply current measurement mode

Power supply current measurement mode sets the digital input/output pin to the low-level output(P40/TOOL0 pin input setting). For this reason, please digital input/output pin is open.

If LED1 and LED2 are connected, because the current flows to the P60 pin and P61 pin, please check the power supply current by subtracting the amount of current.

6. Sample code

Please get the sample code from Renesas Electronics homepage.

7. Reference document

RL78/G14 User's Manual: Hardware (R01UH0474J)
RL78 family user's manual software (R01US0015J)
(Please get the latest version from Renesas Electronics homepage.)

Technical update
(Please acquire latest information from Renesas Electronics homepage.)

Website and support

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http://japan.renesas.com

Inquiries
http://japan.renesas.com/contact/

modification record	RL78/I1D Operation state switching CC-RL

Rev.	Date	Revision	
		Page	Summary
1.00	Feb. 12, 2016	—	First Edition

General Precautions in the Handling of Microprocessing Unit and Microcontroller Unit Products

The following usage notes are applicable to all Microprocessing unit and Microcontroller unit products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Handling of Unused Pins

   Handle unused pins in accordance with the directions given under Handling of Unused Pins in the manual.

   ¾ The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible. Unused pins should be handled as described under Handling of Unused Pins in the manual.

2. Processing at Power-on

   The state of the product is undefined at the moment when power is supplied.

   ¾ The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the moment when power is supplied.
   In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the moment when power is supplied until the reset process is completed.
   In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the moment when power is supplied until the power reaches the level at which resetting has been specified.

3. Prohibition of Access to Reserved Addresses

   Access to reserved addresses is prohibited.

   ¾ The reserved addresses are provided for the possible future expansion of functions. Do not access these addresses; the correct operation of LSI is not guaranteed if they are accessed.

4. Clock Signals

   After applying a reset, only release the reset line after the operating clock signal has become stable. When switching the clock signal during program execution, wait until the target clock signal has stabilized.

   ¾ When the clock signal is generated with an external resonator (or from an external oscillator) during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Moreover, when switching to a clock signal produced with an external resonator (or by an external oscillator) while program execution is in progress, wait until the target clock signal is stable.

5. Differences between Products

   Before changing from one product to another, i.e. to a product with a different part number, confirm that the change will not lead to problems.

   ¾ The characteristics of Microprocessing unit or Microcontroller unit products in the same group but having a different part number may differ in terms of the internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

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