RA Family

Guidelines for USB 2.0 Board Design

Introduction

This document describes the guidelines for USB 2.0 board design.

Target Device

The application explained in this document applies to the following .

- RA Family

Note: The contents in this document are provided as a reference example based on the USB specification, and the signal system quality is not guaranteed. When implementing this example into an existing system, the overall system should be thoroughly evaluated, and the user should integrate at their own discretion.

Contents

1. Introduction

This application note does not specify the USB terminal. For each terminal, refer to the RA series user's manual.

2. USB Transmission Line

The USB transmission line indicates the wiring pattern that connects the USB connector and the RA embedded USB transceiver.

USB 2.0 has three communication modes: High-Speed, Full-Speed, and Low-Speed modes. The High-Speed mode has a 480-Mbps communication speed. Therefore, the USB transmission lines must be designed as a high-frequency circuit.

- High-Speed: Impedance control is required for the USB transmission lines.
- Full-Speed, Low-Speed: Impedance control is recommended for the USB transmission lines.
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Notes on designing the wiring pattern of USB transmission lines are described below.

- The characteristic impedance required for the USB transmission lines is the differential impedance 90Ω ±15%.
- The pattern width and pattern pitch for impedance control vary depending on board thickness, material, and layer configuration. Contact the board manufacturer for more details.
- The wiring pattern length of USB transmission lines from the RA's USB pin to the USB connector must be designed not to exceed the maximum delay time which is regulated by the USB specification. Table 2 lists the recommended values for the wiring pattern length of USB transmission lines for host and Peripheral.

Table 1.   Recommended Value for the Wiring Pattern Length of USB Transmission Line

	Maximum Delay Time (USB Specification)	Wiring Length	D+ and D- Wiring Length Differential
Host Controller	3 ns	300 mm or less	2.5 mm or less
• Peripheral Controller	• 1 ns	• 100 mm or less	• 2.5 mm or less

- The USB transmission lines must be referenced to a ground plane. The ground plane must be at least 2 mm wider than the USB transmission lines. The power supply for the ground plane is GND
- Do not allocate other signal lines near the USB transmission lines. Particularly, lines of heavily fluctuating signals, such as clock and data bus lines must be allocated far from the USB transmission lines. Moreover, the USB transmission lines and other lines must not cross.
- The same layer (surface layer) as the USB transmission lines should be allocated 1 mm from the USB transmission lines and grounded with a guard ring.
- USB transmission lines should be allocated on the same layer without passing through a hole. In addition, the transmission lines should not branch off.
- The USB transmission lines should be wired with uniform spaces.
- The USB transmission lines should be allocated far from the oscillator, power supply circuit, and other I/O connectors.
- The USB transmission lines should be wired with straight lines. If they are bent, they should be bent gently in an arc or up to 135 degrees, and not bent at acute or right angles.

Figure 1 shows a design example of a Host controller USB transmission line pattern, and figure 2 shows a design example of a Peripheral controller USB transmission line pattern.
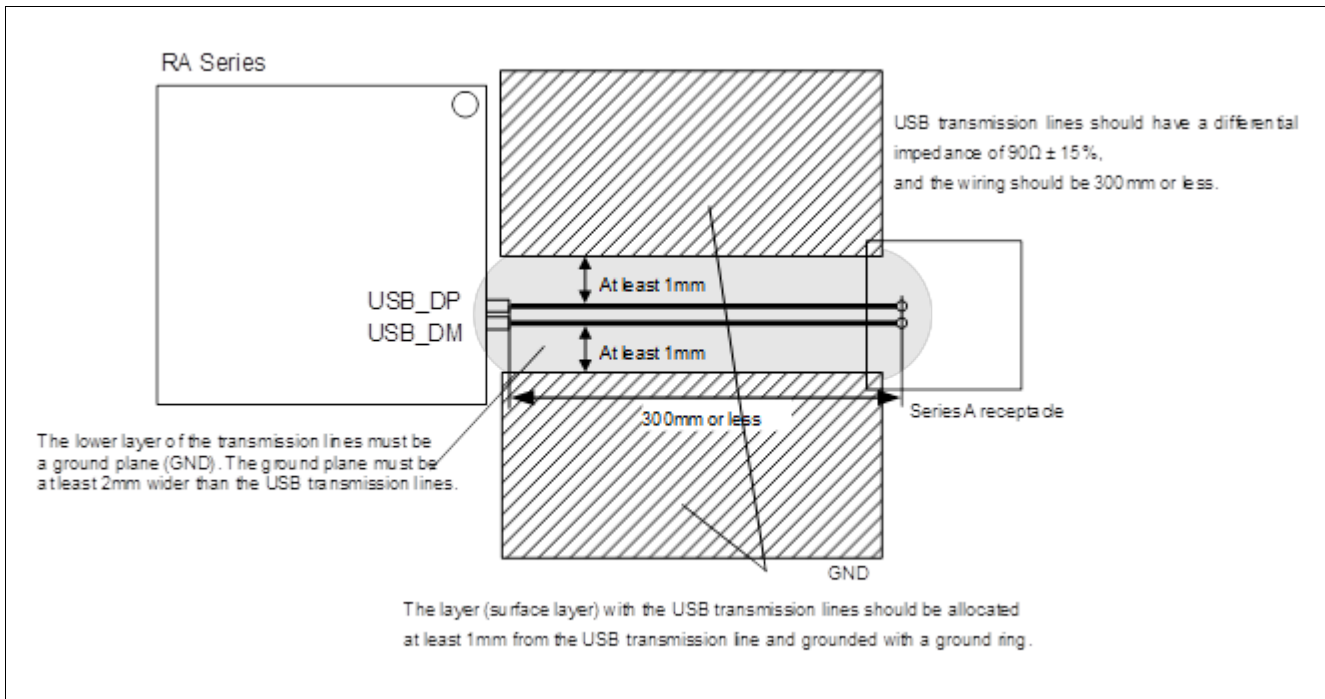
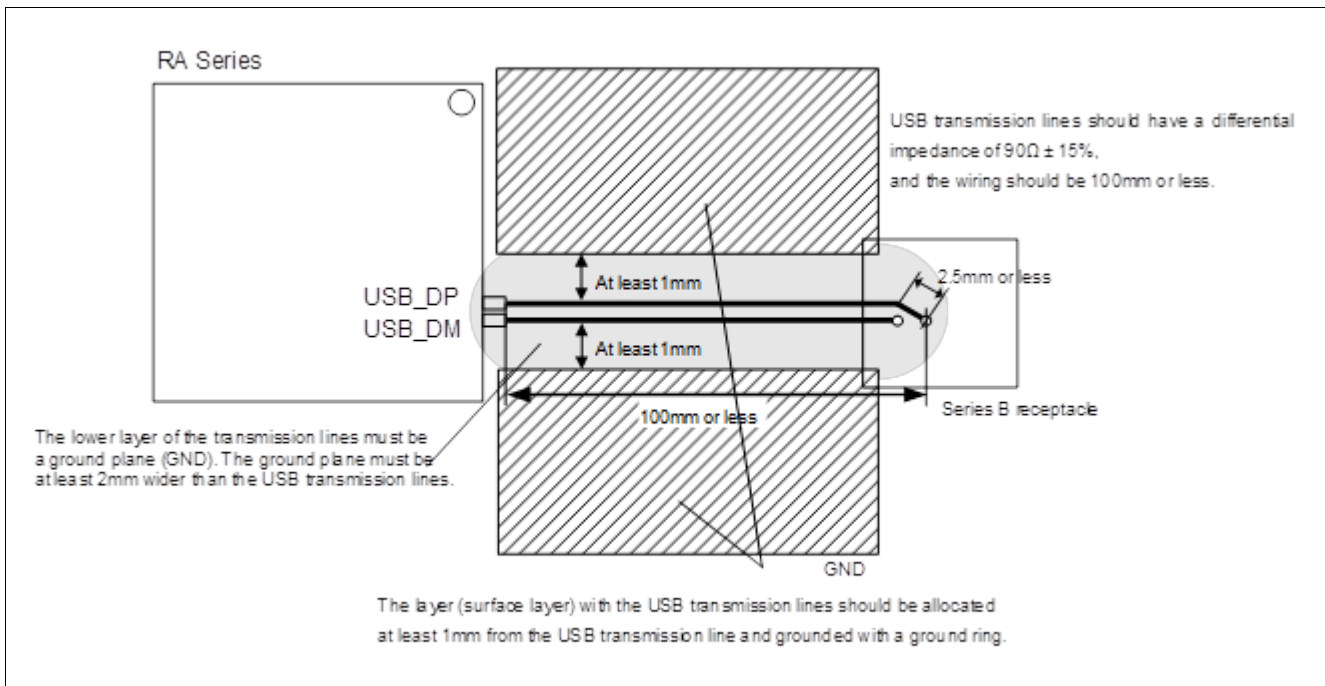**Figure 1.   Design Example of a Host Controller USB Transmission Line Pattern**

Figure 2   Design Example of a Peripheral Controller USB Transmission Line Pattern

3.   USBA_RREF Line

The RA High-speed driver's steady-state current and PLL bias current are generated by the reference voltage determined by the external resistor between USBHS_RREF and GND.

In other words, voltage fluctuation of the USBHS_RREF wiring causes fluctuations in the steady-state current and bias current, and affects the stability of the PLL and the transmission and reception waveform (jitter and amplitude of the transmission waveform).

Therefore, noise countermeasures are required.

The RA series Full-Speed drivers do not have this terminal.

- Place a 2.2-kΩ reference resistor (resistance accuracy ±1%) between USBHS_RREF and GND.
- Do not place a capacitor in parallel with the reference resistor.
- Avoid interference with other signals in the reference resistor.
- Design the parasitic resistance of the USBHS_RREF wiring to 0.5 Ω or less.
- Avoid interference with other signals, such as using the inner layer of the USBHS_RREF wiring, in order to prevent interference from noise sources.
- Wire so that other signal wiring does not cross USBHS_RREF wiring.
- Keep the USBHS_RREF wiring away from other signal wiring.

4.   Power Supply and Ground Pattern

4.1   USBHS Power Supply and Ground

The RA series High-Speed compatible products are high-frequency circuits, so the following power supply and GND processing is required.

1. Analog power supply
   Connect the AVCC_USBHS pin to the analog power supply plane.
   Keep the wiring impedance of the analog power supply as small as possible.
   Separate the analog power supply from the digital power supply via inductor and ferrite. In this case, please separate near the regulator of digital power supply. However, depending on the board, even if they are not separated, the PLL stability and transmit/receive waveform may not be affected. In the end, evaluate the board as a whole, and if there is no problem with the result, there is no problem in removing the inductor and ferrite.
   Place a decoupling capacitor between each power supply pin and GND to suppress voltage fluctuations. Place a 10000-pF ceramic capacitor near the chip.
   Wire so that no other signal wiring crosses the analog power plane.
   Keep the analog power supply plane away from other signal wiring.
2. Digital power supply
   Connect the VCC_USBHS terminal to the digital power supply plane.
   Make the wiring impedance of the digital power supply as small as possible.
   Place a decoupling capacitor between each power supply pin and GND to suppress voltage fluctuations. Place a 10000-pF ceramic capacitor near the chip and a 47-µF electrolytic capacitor. The 47-µ F capacitor can be placed away from the chip.
3. GND
   Connect the VSSx_USBHS/PVSS_USBHS/AVSS_USBHS pin to the USB GND plane.
   Make the GND wiring impedance as small as possible. Make sure that no other signal wiring crosses the USB GND plane. Keep the USB GND plane away from other signal wiring.

4.1.1   USBHS Connection Example

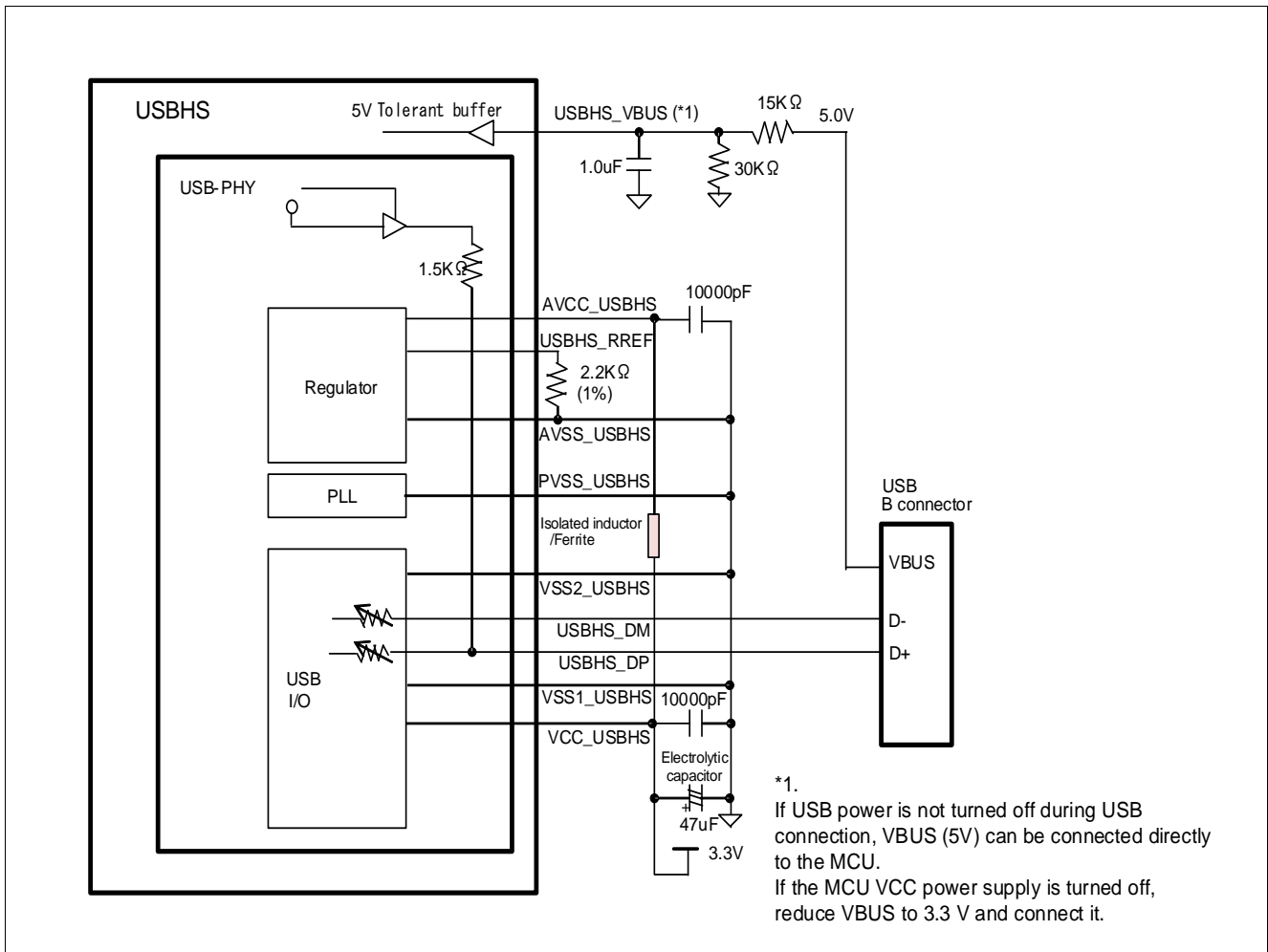The USBHS connection example is shown below.

Figure 2.   USBHS Self-Powered Function Connection Example

4.1.2   USBFS Power Supply and Ground

Notes on designing a power supply/ground pattern are described below.

- The patterns of power supplies and grounds should be designed with as wide a surface layer as possible.
- Ceramic capacitors with excellent high-frequency characteristics are recommended as power supply capacitors.
- Aluminum electrolytic capacitors affect the jitter value when measuring the EYE pattern. The capacitors should be thoroughly analyzed and tested before use.
- As the capacitance value of the decoupling capacitor, it is recommended that the capacitances for 0.1 µF and 10 µF are allocated closest to the USB power supply pin. Figure 3 shows an example of decoupling capacitor allocation.
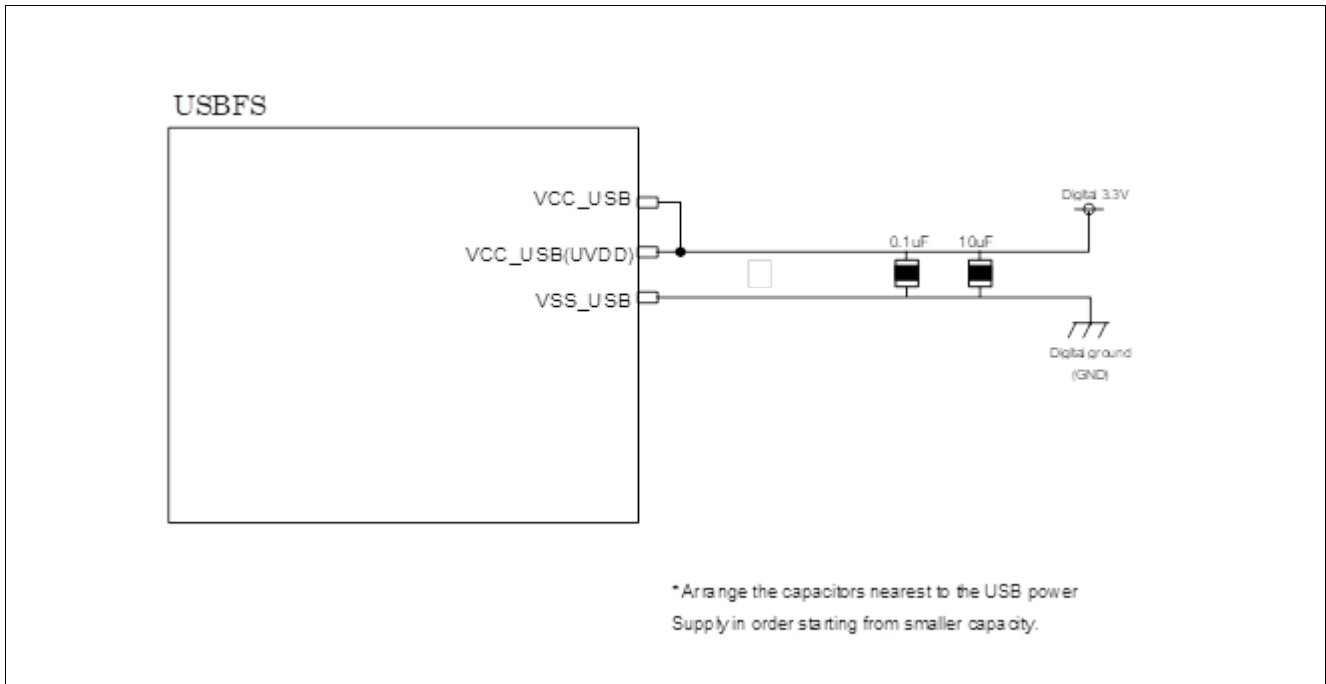
Figure 3.   USBFS Power/GND connection

5.   VBUS Power Supply Circuit

Notes on designing the VBUS power supply circuit are described below.

- When the RA MCU is used as a Host controller, the additional capacitance of the VBUS line should be designed to be 120 µF or more.
- When the RA MCU is used as a Peripheral controller, the additional capacitance of the VBUS line should be designed to be within 1.0 µF to 10 µF.
- The VBUS line should include a filter circuit because an overshoot may be caused by inconsistent impedance when the USB cable is connected. The 1.0-µF capacitor and 100-Ω to 1-kΩ resistor should be added as a filter circuit. The constant should be defined after confirming that an overshoot has not occurred on the board. Also, a resistor of more than 1 kΩ should not be added.
- When the RA MCU is used as a Host controller, the VBUS power should be supplied to the Peripheral devices. A power supply switch IC with over-current protection for the USB power bus (hereinafter called "USB power supply switch IC") is recommended for the VBUS power supply control. Make sure to consider the limitation value of the current of VBUS power supply line based on the current value used by the system power supply applied and the USB Peripheral devices communicated. In addition, refer to the USB power supply switch IC datasheet used for VBUS power supply control circuit.

Figure Figure 4 shows an example of the VBUS power supply circuit when it is used as a Host controller. Figure 5 and Figure 6 show an example of the VBUS power supply circuit when it is used as a Peripheral controller.
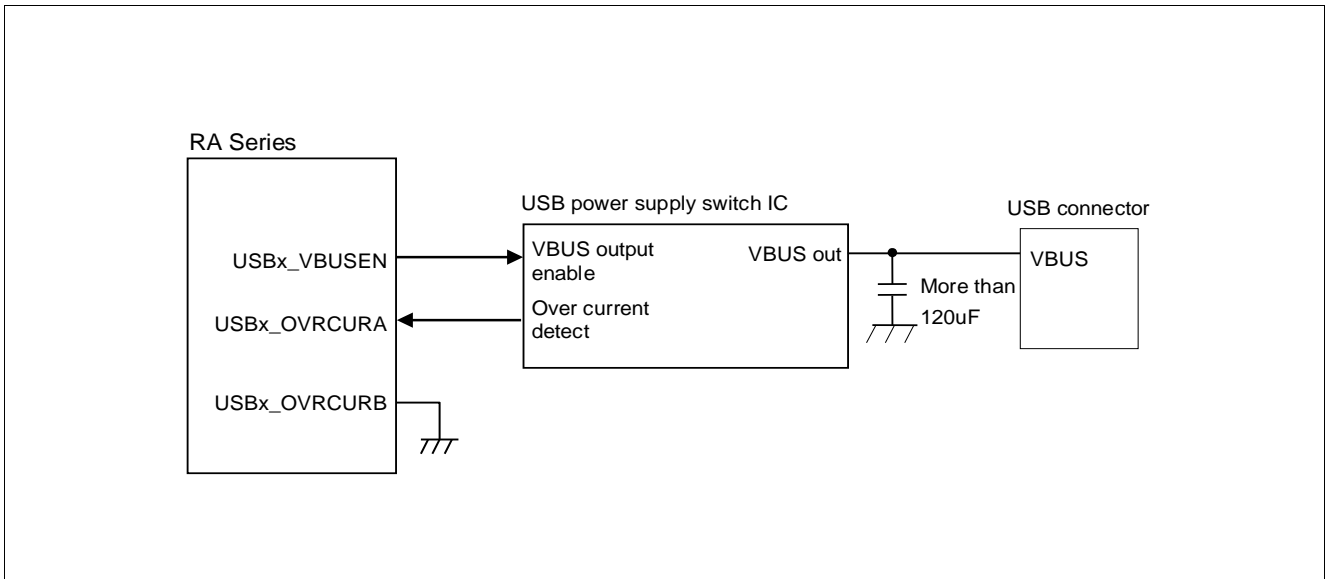
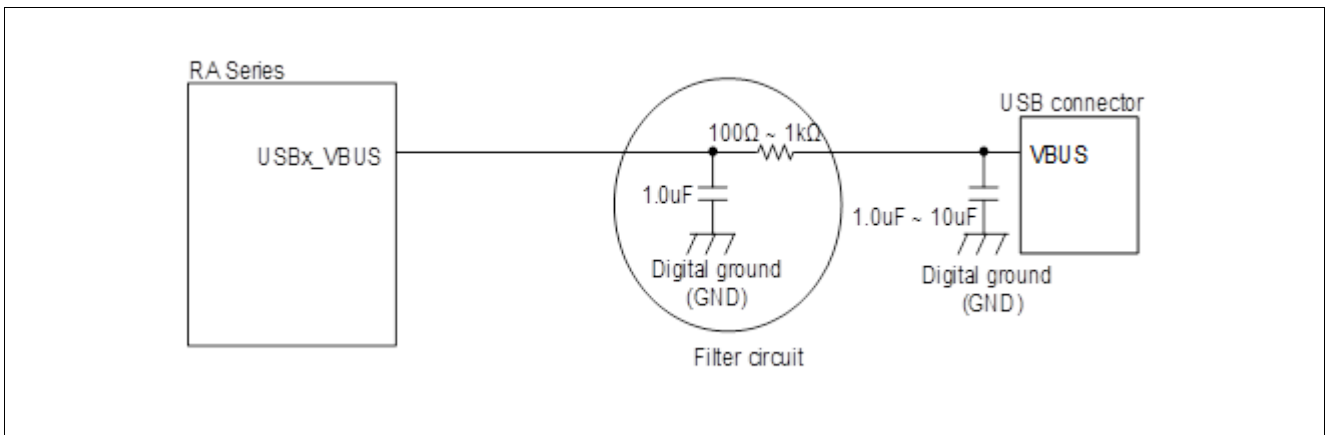**Figure 4.   Example of Host Controller VBUS Power Supply Circuit**

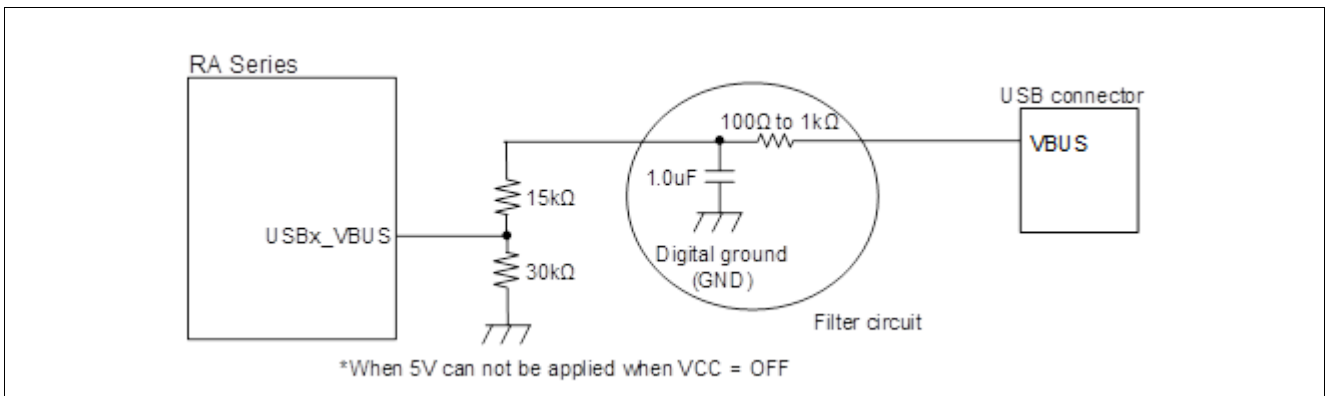**Figure 5.   Example of Peripheral Controller VBUS Power Supply Circuit 1**

Figure 6.   Example of Peripheral Controller VBUS Power Supply Circuit 2

6. EMI/ESD Workarounds

Notes on EMI/ESD workarounds are described below.

- When components for EMI/ESD workarounds such as coils and diodes are mounted on the USB transmission lines, they should be allocated near the USB transmission lines and the wiring should be as short as possible.
- The components for the EMI/ESD workarounds must be USB 2.0 compliant. Also, mounting EMI/ESD workaround components may cause an inconsistent impedance on the USB transmission lines, and the waveform may become distorted. Components for use should be selected after thorough evaluation.

Figure 7 shows the block diagram of a connection example when the components for EMI/ESD workarounds are used.
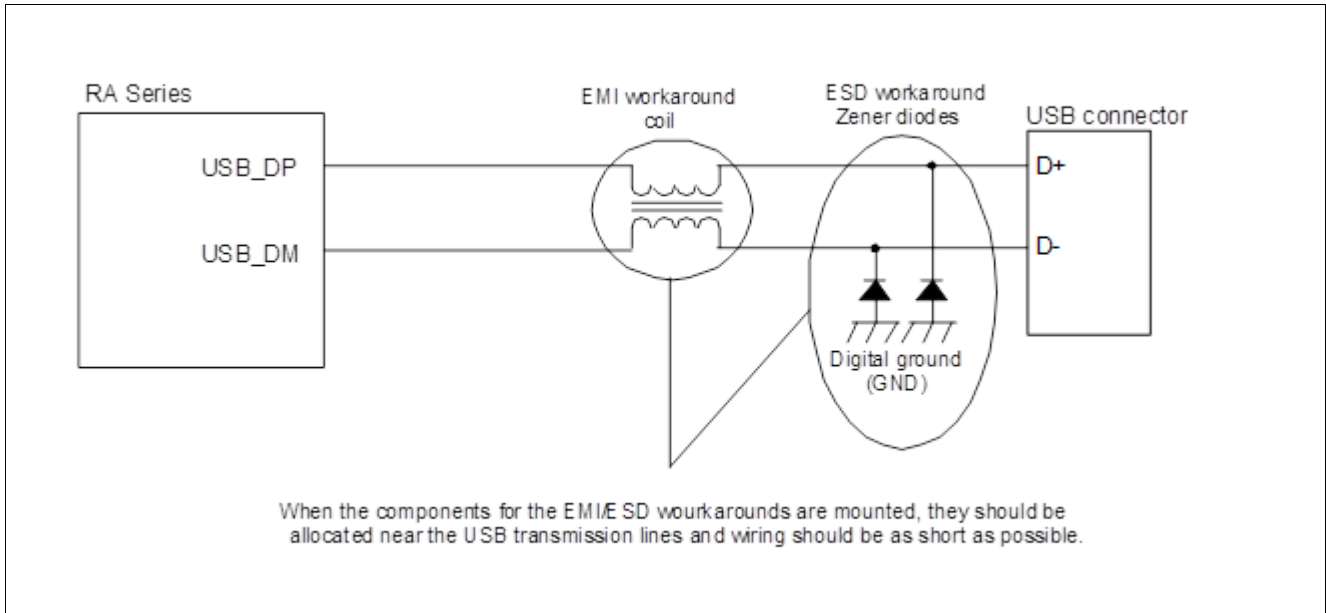
Figure 7.   Connection Example When Components for EMI/ESD Workarounds are Used

Website and Support

Visit the following vanity URLs to learn about key elements of the RA family, download components and related documentation, and get support.

RA Product Information   www.renesas.com/ra
RA Product Support Forum   www.renesas.com/ra/forum
RA Flexible Software Package   www.renesas.com/FSP

Renesas Support   www.renesas.com/support

Revision History

Rev.	Date	Description	
		Page	Summary
1.00	Feb 3, 2022	—	First edition issued

General Precautions in the Handling of Microprocessing Unit and Microcontroller Unit Products

The following usage notes are applicable to all Microprocessing unit and Microcontroller unit products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Precaution against Electrostatic Discharge (ESD)

    A strong electrical field, when exposed to a CMOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop the generation of static electricity as much as possible, and quickly dissipate it when it occurs. Environmental control must be adequate. When it is dry, a humidifier should be used. This is recommended to avoid using insulators that can easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors must be grounded. The operator must also be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions must be taken for printed circuit boards with mounted semiconductor devices.

2. Processing at power-on

    The state of the product is undefined at the time when power is supplied. The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the time when power is supplied. In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the time when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the time when power is supplied until the power reaches the level at which resetting is specified.

3. Input of signal during power-off state

    Do not input signals or an I/O pull-up power supply while the device is powered off. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Follow the guideline for input signal during power-off state as described in your product documentation.

4. Handling of unused pins

    Handle unused pins in accordance with the directions given under handling of unused pins in the manual. The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of the LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible.

5. Clock signals

    After applying a reset, only release the reset line after the operating clock signal becomes stable. When switching the clock signal during program execution, wait until the target clock signal is stabilized. When the clock signal is generated with an external resonator or from an external oscillator during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Additionally, when switching to a clock signal produced with an external resonator or by an external oscillator while program execution is in progress, wait until the target clock signal is stable.

6. Voltage application waveform at input pin

    Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between V_{IL} (Max.) and V_{IH} (Min.) due to noise, for example, the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between V_{IL} (Max.) and V_{IH} (Min.).

7. Prohibition of access to reserved addresses

    Access to reserved addresses is prohibited. The reserved addresses are provided for possible future expansion of functions. Do not access these addresses as the correct operation of the LSI is not guaranteed.

8. Differences between products

    Before changing from one product to another, for example to a product with a different part number, confirm that the change will not lead to problems. The characteristics of a microprocessing unit or microcontroller unit products in the same group but having a different part number might differ in terms of internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

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(Rev.5.0-1 October 2020)

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