

Low Latency High Bandwidth Memory

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Introduction

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1. Low Latency High Bandwidth Memory

Renesas' Low Latency High Bandwidth Memory consists of multiple Renesas' original low latency memory dies and realizes high random-access rate and small data granularity as well as high bandwidth. By populating the stack memory along with your accelerator or processor in the same package, you can differentiate your systems with its performance improvement by keeping effective bandwidth high even at non-sequential memory access. The stack memory accelerates datacenter application such as artificial intelligence (Deep Learning, Convolutional Neural Network, etc.), Graph Analytics, Database, Sparse Matrix. It also fits network applications such as table lookup with high search rate, packet buffer, control memory in routers, switches etc.



2. Features

2.1 Stacked memory

Low Latency High Bandwidth Memory stacks 4 or 8 low latency DRAM dies through TSV and base die on logic process and realize 2304 [Gbps] with thousands of IOs keeping low latency DRAM features, high random access and small granularity. The stack memory is utilized integrating with customer's ASIC, GPU, CPU, NPU, FPGA, AI accelerator on silicon interposer in the same package and realizes near memory computing.



2.2 High Random-Access Rate and Small Data Granularity

Figure.1 shows a trend of DRAM’s access rate and bandwidth. Standard DRAMs (DDR3, DDR4, GDDR6) have gradually been improving bandwidth, while the data granularity is getting bigger and bigger in figure.2. These trends would not be changed because standard DRAM has been focusing on bandwidth and density which are required from bigger volume applications in DRAM market. On the other side, there are some applications which are unable to achieve the performance with standard DRAM. It is because standard memory only allows sequential access to get maximum high bandwidth. To further improve performance of these applications, random access capability is getting critical. To meet the requirement from these applications, Renesas has been improving not only bandwidth but random access capability as well. Now, we achieved 16 billion random access per second and 16-Byte data granularity with stacking multiple low latency memory dies and realize high effective bandwidth regardless applications even sparse AI model, FFT, hash function for block chain in datacenter as well as packet classification of network.

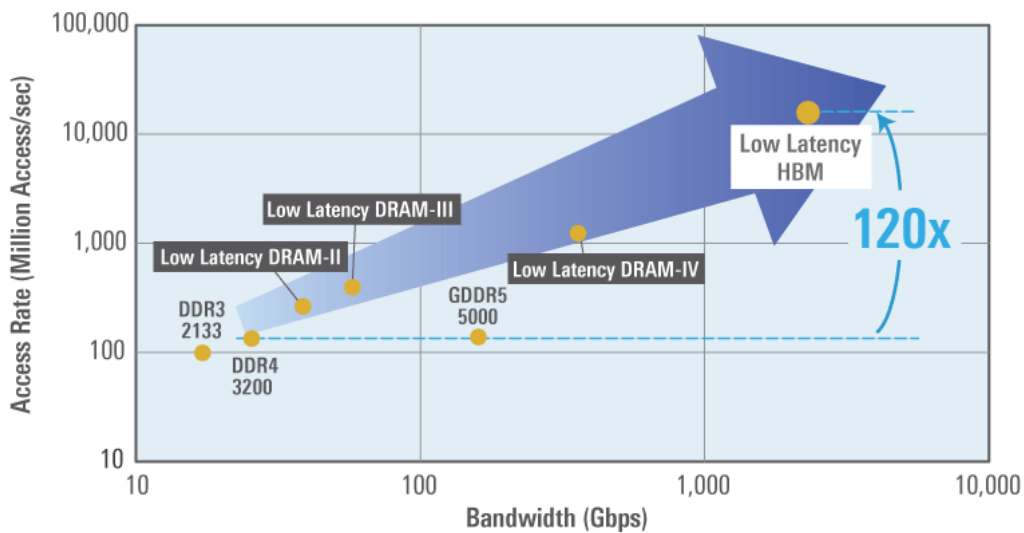


Figure.1

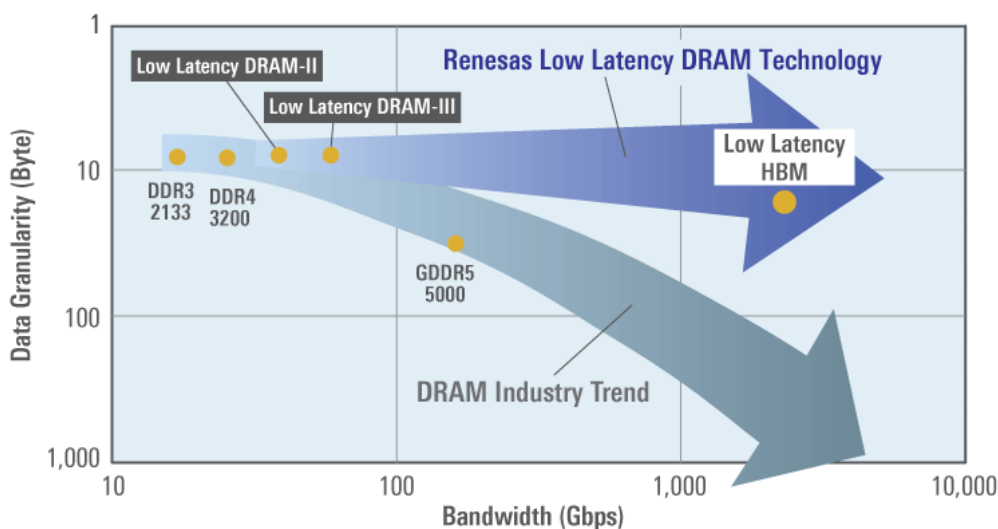
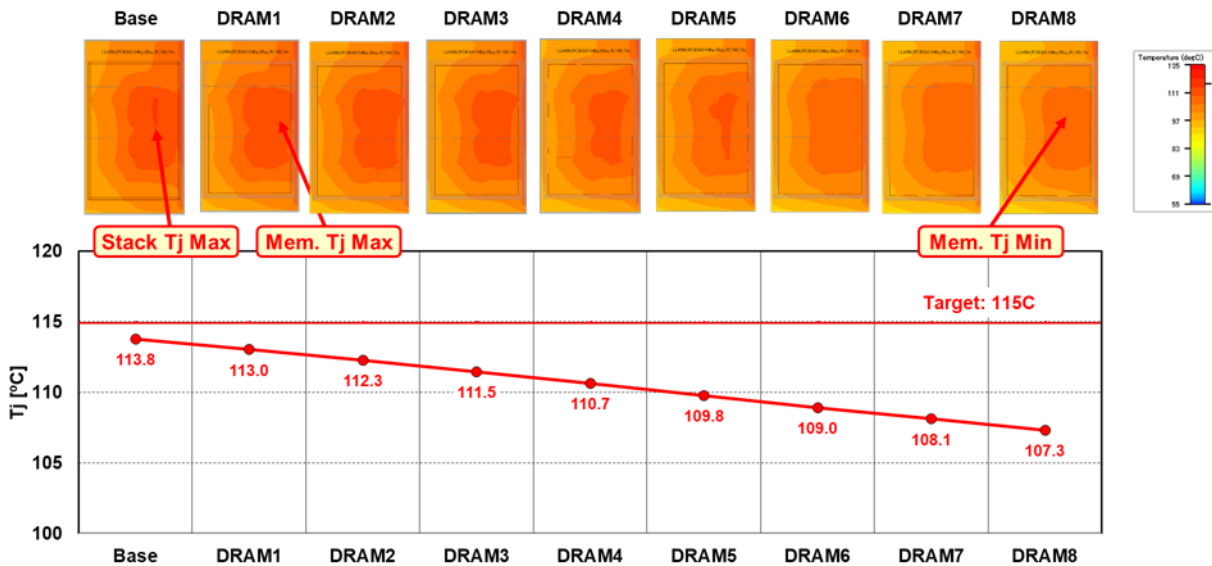


Figure.2

2.3 Guarantees Tjmax=115C

Renesas’ low latency DRAM products have long history to meet severe high maximum temperature requirement with long life from network industry customers. The new stack memory also guarantees Tjmax=115°C and delivers realistic solutions to your package thermal problem. To help the problem, Renesas can operate user custom thermal simulation adapted user’s environment such as power consumption of the processor, package size etc.



2.4 JEDEC Std. HBM-Like Interface

Low Latency HBM has two configurations. Config2 following JEDEC Std. HBM2 interface has the same number and location as that of HBM2 μBumps. Config 1 needs additional μBumps to achieve highest performance..

2.5 Ecosystem partner of PHY and Controller

Renesas has relationship with multiple PHY and Controller IP partners. Users can utilize their IP specialized Low Latency HBM for your ASIC, processor or accelerator. Even more partners are under discussing. For more information, please contact our representatives.

3. Line up

Density [Gb]	Config.	Burst Length	Clock Freq. [MHz]	Data Width	tRC [ns]	Access Rate [Maps]	Bandwidth [Gbps]	Data Granularity	VDDQ(I/O) [V]
9Gb/ 18Gb	1	2	1,000	x 1,152	12.0	16,000	2,304	16Byte	1.0
									1.2
	2	4	1,000	x 1,152	16.0	8,000	2,304	32Byte	1.0
									1.2

Website and Support

Renesas Electronics Website

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Revision History

Rev.	Date	Description	
		Page	Summary
0.01	Jan. 29, 2019	-	Preliminary Release

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