

**Introduction**

The ISL5217 Quad Programmable Up-converter (QPUC) efficiently filters and upconverts baseband data to intermediate bandpass data utilizing from 1 to 4 programmable channels. Four channels can be independently used for narrowband applications such as IS-136, GSM, and EDGE, while 2, 3, or 4 channels can be combined in wideband application such as IS-95, CDMA-2000-1x, CDMA2000-3x MC and CDMA-2000-3x DS, TD-SCDMA, and UMTS. The design of the ISL5217 allows one device to implement four narrowband channels, two midwidth channels, or one wideband channel.

This application note describes the device configuration examples for several air interface standards with the information formatted for use with the ISL5217EVAL1 evaluation board and windows software.

**For All Examples**

**Input Data Format**

The ISL5217EVAL1 evaluation board was designed to utilize the QPUC serial data inputs as the primary input path. The board contains a 128Kx32 RAM to support driving the input data into the ISL5217 via the SDA-SDD serial data inputs. Data samples are input into the device serially in order, with sample n, followed by n+1....etc. The channel bit rate is the device symbol rate ( $f_s$ ), which is the rate at which the I/Q samples are input into the device.

The I/Q sample pairs can be input in parallel through  $\mu P$  addressable registers or serially through 1 of 4 serial interfaces SDA-SDD, as shown in Figure 1. To provide increased flexibility for the user, many of the data input parameters are programmable, including word bit length, symbol rate, time slot values, and the data input flags. As only the device parameters required for the configurations in the examples are documented herein, please see the ISL5217 data sheet for complete device programming information.

The parallel mode allows the QPUC  $\mu P$  to write up to 16 bit I and Q samples directly into the FIFO holding registers through control words 0x1 and 0x0. The writing order is Q first, followed by I, with each channel having independent I and Q data control word locations. The  $\mu P$  can perform back-to-back write accesses, but must maintain four  $f_{CLK}$  periods between accesses to the same address. This limits the maximum  $\mu P$  write access rate for an I/ Q sample pair to  $CLK/4$  or a maximum of 26MHz.

The serial channels provide for transfer of the input data at reduced rates, as each bit of serial data input requires a CLK for latching. This effectively limits 16 bit I and 16 bit Q

samples to  $CLK/32$  or 3.25MHz maximum. Lesser bit width data, like 4 bit I and 4 bit Q can be input at  $CLK/8$ , or 13MHz maximum.

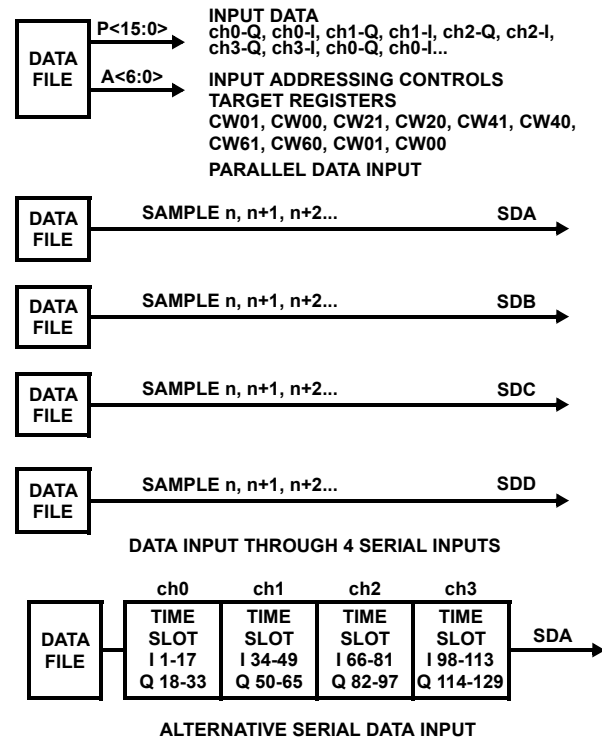


FIGURE 1. SINGLE CHANNEL INPUT DATA FORMAT

**Shaping Filter Requirements**

The required number of shaping filter coefficients is determined by the programmed Interpolation Phases (IP) and the Data Span (DS), where:

$$\# \text{ Coefficients} = (DS)(IP) \tag{EQ. 1}$$

The interpolation phase determines the rate to compute a polyphase output by selecting the appropriate timing from the Sample Rate NCO to drive the shaping filter at 4x, 8x, or 16x the input sample rate. The Data Span selects the number of samples to convolve. Each convolution requires DS reference clocks for each phase of the filter. An output is calculated (IP) times for each input sample. To ensure sufficient processing time for each output, the clock must be:

$$CLK > (DS)(IP)(f_s) \tag{EQ. 2}$$

Conversely, the input sample rate requires:

$$f_s < (CLK)/[(IP)(DS)] \tag{EQ. 3}$$

Although the serial and parallel inputs can accommodate 3.25-13MHz and 26MHz data throughput, the shaping Finite Impulse Response (FIR) is programmable to x4, x8, or x16



TABLE 1. GSM CONFIGURATION

|                             |              |
|-----------------------------|--------------|
| Clock Rate CLK =            | 80MHz        |
| Sample Frequency $f_s$ =    | 270.833kHz   |
| Configuration File:         | GSM_only.js  |
| Filter File:                | gs5t16x.imp  |
| Stimulus File:              | gmsknpnc.imp |
| Dynamic Configuration File: | N/A          |

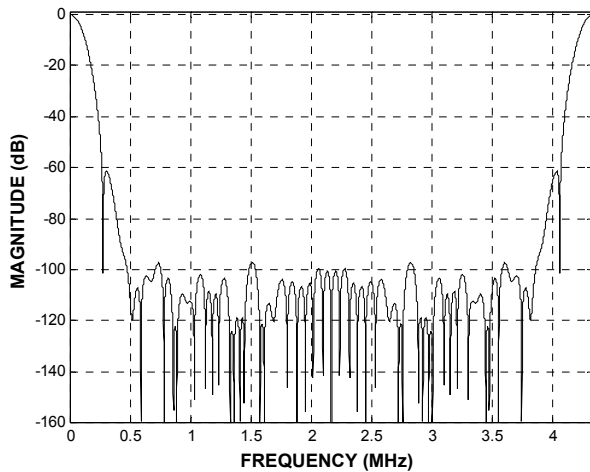


FIGURE 3. SHAPING FILTER FREQUENCY RESPONSE

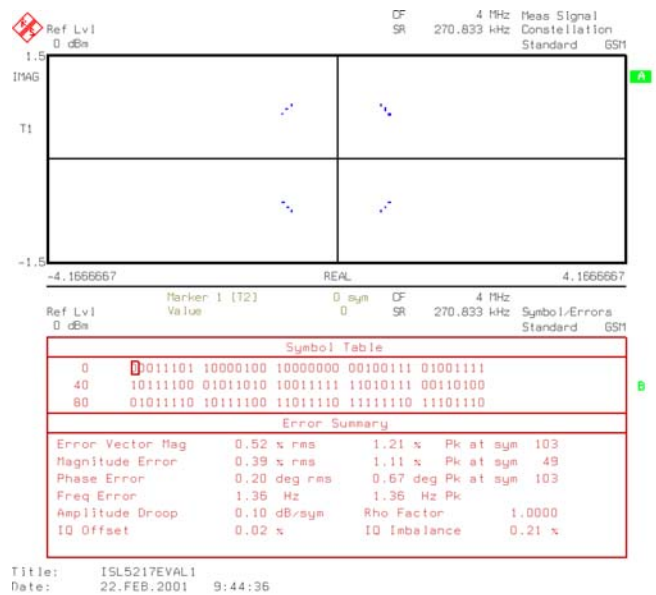


FIGURE 5. VECTOR ANALYZER OUTPUT

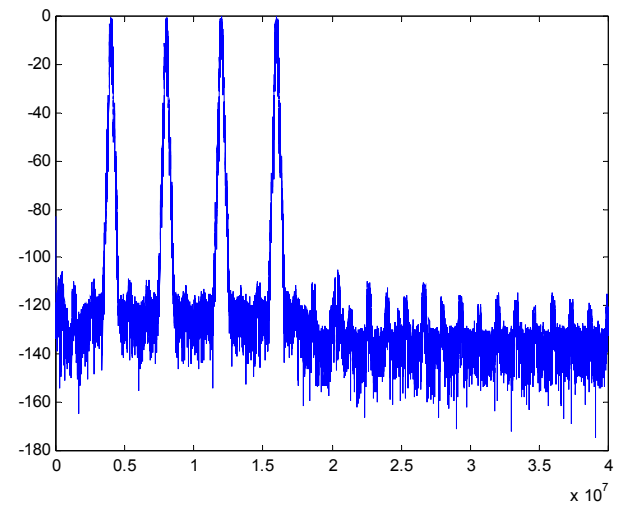


FIGURE 6. DIGITAL OUTPUT

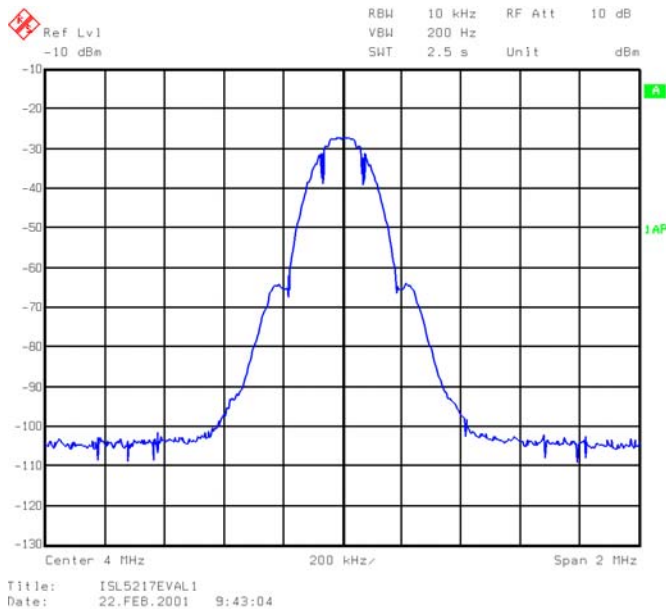


FIGURE 4. ANALOG SPECTRUM

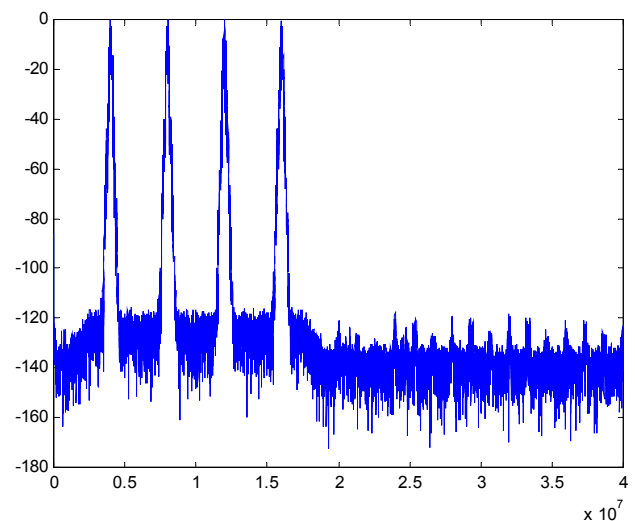


FIGURE 7. DIGITAL OUTPUT, HALFBAND ENABLED

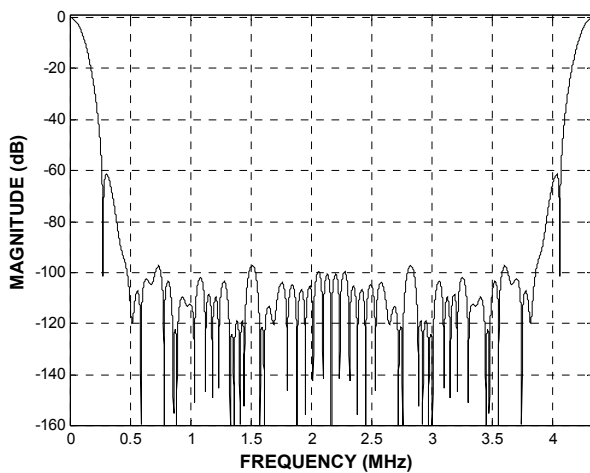
**GSM Burst Mode**

The device is configured for outputting one channel of GSM in burst mode. The 16-bit I and 16-bit Q data is input through the serial channel SDA input, and the fixed integer divider (FID) is enabled to provide an integer relationship of CLK/288 or  $f_S = 270.833\text{kHz}$  rate. The shaping FIR is programmed to interpolate by x16 with a dataspan of 6. The filter frequency response is shown in Figure 8. The half band filter is not enabled, the carrier phase is pre-loaded to zero degrees, and the carrier frequency is set to 4MHz. The output mode is Cascade, with reCASout output on IOOUT<19:0> and imCASout output on QOUT<19:0>. The analog performance of the device is shown in Figure 9, utilizing the on-board HI5828 dual DAC, and the vector analysis is shown in Figure 10. The stimulus file is 148 samples of pseudo random data with a synchronization pattern included.

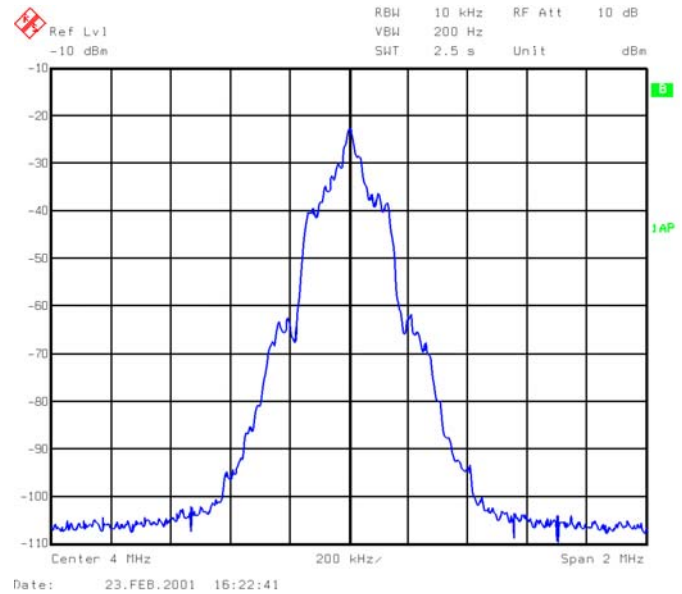
The dynamic configuration software mode is utilized with a programed value of TXEN on =148.5 bits or 42768 clocks on ( $148.5 * (1/270.833\text{e}3) / (1/78\text{e}6)$ ) and 8.25 bits or 2376 clocks off ( $8.25 * (1/270.833\text{e}3) / (1/78\text{e}6)$ ). These settings allow the device to transmit 148 bits in the required on normal burst period and to ramp up/down in the guard period. The gain profile is enabled in this example with 192 gain profile coefficients being utilized. The gain profile coefficients were derived from the EDGE transmit filter profile with trailing full scale bits added to extend the transmit on time.

**TABLE 2. GSM Burst Configuration**

|                             |                 |
|-----------------------------|-----------------|
| Clock Rate CLK =            | 78MHz           |
| Sample Frequency $f_S$ =    | 270.833kHz      |
| Configuration File:         | GSM_Only.js     |
| Filter File:                | gs5t16xTest.imp |
| Stimulus File:              | GSM_Only.imp    |
| Dynamic Configuration File: | GSM_Only.imp    |

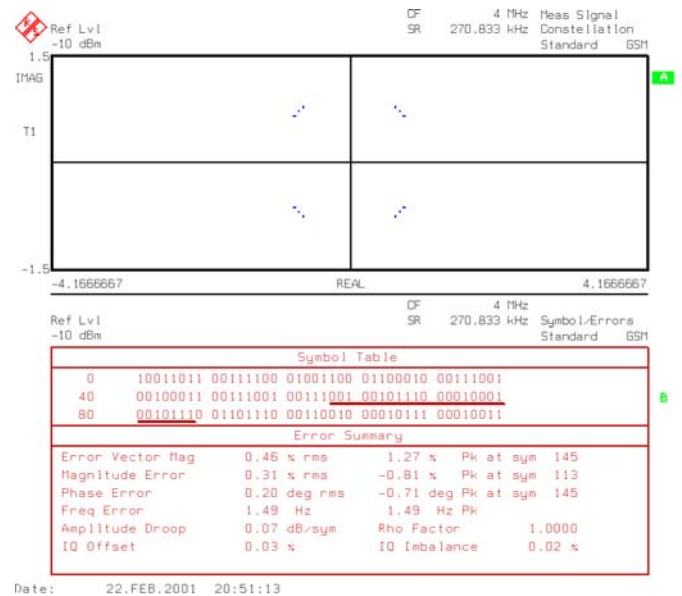


**FIGURE 8. SHAPING FILTER FREQ. RESPONSE**



**FIGURE 9. ANALOG SPECTRUM**

The peak shown in the analog spectrum is due to the pattern loaded, the data does not present a pn spectral outline.



**FIGURE 10. VECTOR ANALYZER OUTPUT**

The digital data was collected utilizing a 32K FFT with the results shown in Figure 11. Enabling the halfband, the digital performance is improved as shown in Figure 12.

TXEN timing latency in the offset binary mode is shown in Figure 13.

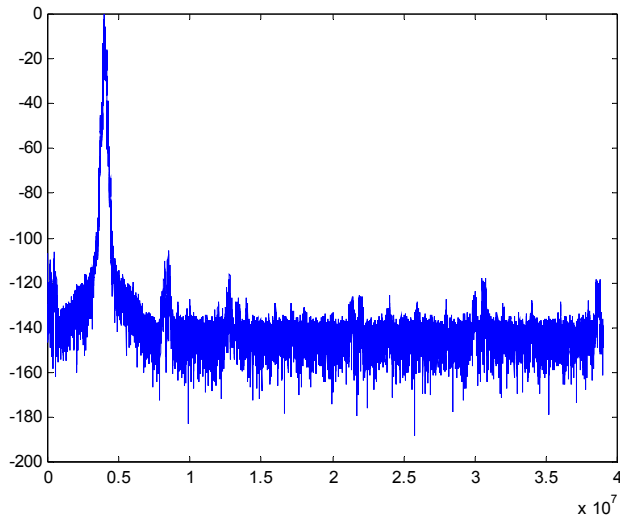


FIGURE 11. DIGITAL OUTPUT

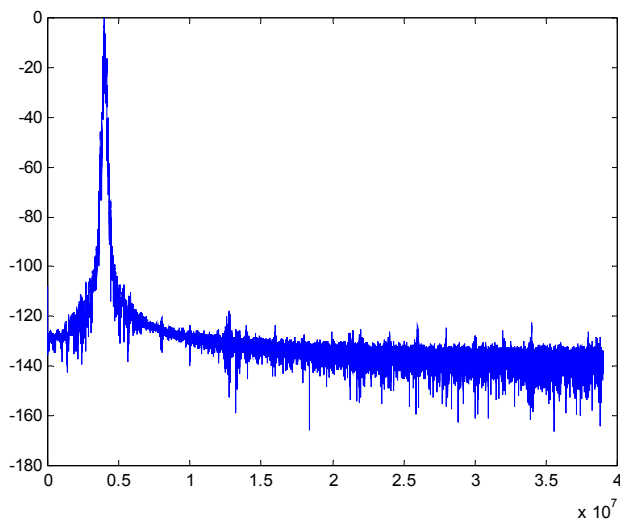


FIGURE 12. DIGITAL OUTPUT, HALFBAND ENABLED

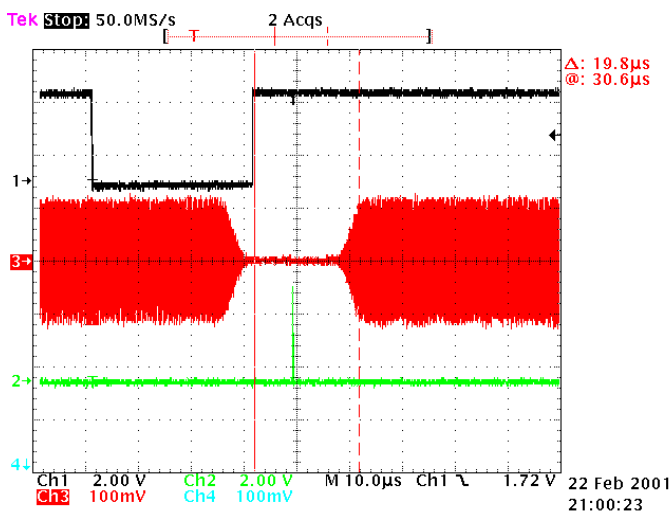


FIGURE 13. TXEN vs BURST TIMING (HALFBAND ON)

**EDGE**

The device is configured for QASK and outputting four channels of EDGE in continuous mode. The 16-bit I and 16-bit Q data is input through the serial channel SDA-SDD inputs, and the symbol NCO is programmed to provide a sample rate of  $f_S = 270.833\text{kHz}$ . The shaping FIR is programmed to interpolate by x16 with a dataspan of 5. The filter frequency response is shown in Figure 14. The half band filter is not enabled, the carrier phase is pre-loaded to zero degrees, and the carrier frequencies are set to 4, 8, 12, and 16MHz. The output mode is Cascade, with reCASout output on IOOUT<19:0> and imCASout output on QOUT<19:0>. The analog performance of the device is shown in Figure 15, utilizing the on-board HI5828 dual DAC, and the vector analysis is shown in Figure 16. The stimulus file is 1022 samples of pseudo random 3/8pi 8psk data.

TABLE 3. EDGE CONFIGURATION

|                             |              |
|-----------------------------|--------------|
| Clock Rate CLK =            | 80MHz        |
| Sample Frequency $f_S$ =    | 270.833kHz   |
| Configuration File:         | EDGE.js      |
| Filter File:                | edget16x.imp |
| Stimulus File:              | edgem6db.imp |
| Dynamic Configuration File: | N/A          |

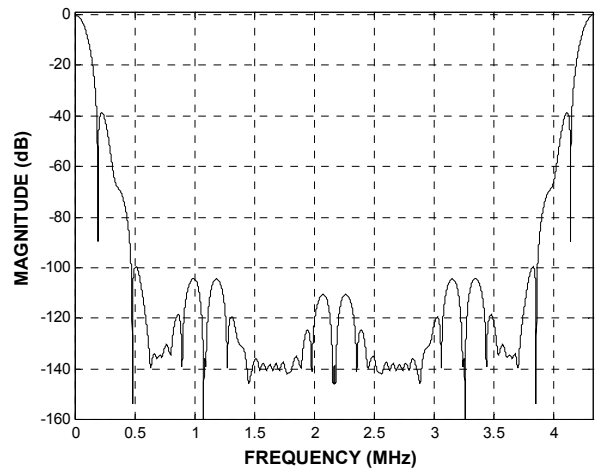


FIGURE 14. SHAPING FILTER FREQ. RESPONSE

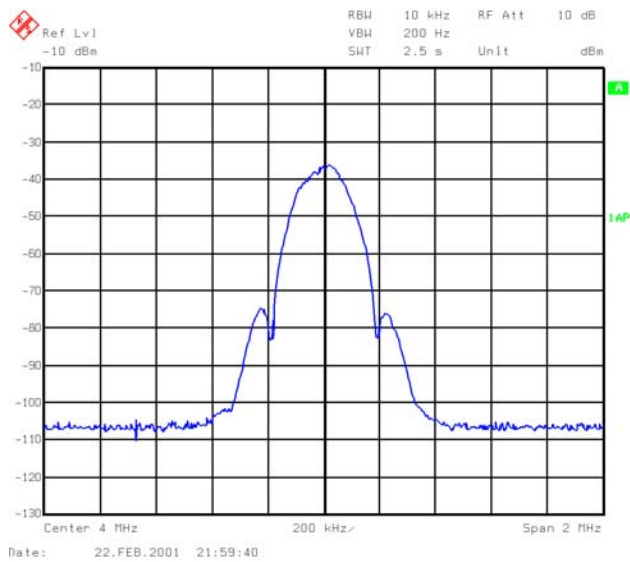


FIGURE 15. ANALOG SPECTRUM

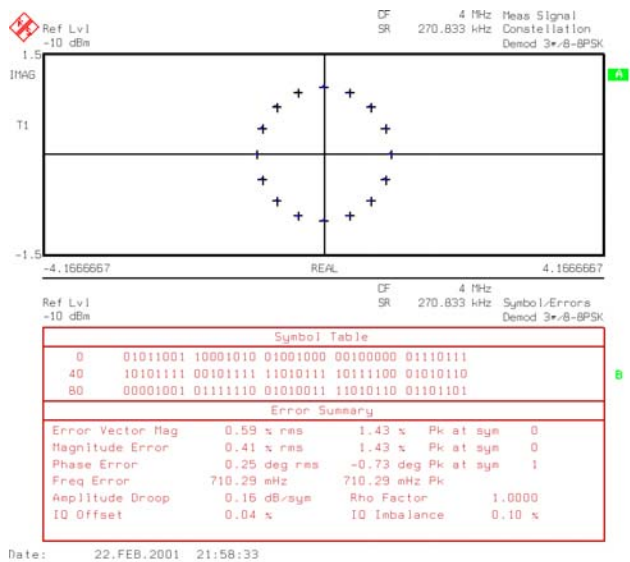


FIGURE 16. VECTOR ANALYZER OUTPUT

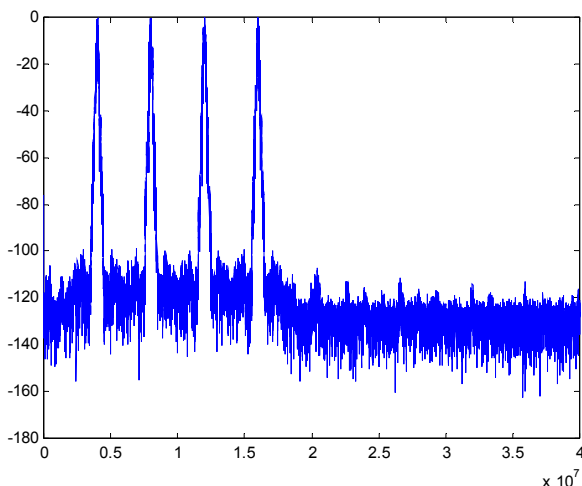


FIGURE 17. DIGITAL OUTPUT

The digital data was collected utilizing a 32K FFT with the results shown in Figure 17. Enabling the halfband, the digital performance is improved as shown in Figure 18.

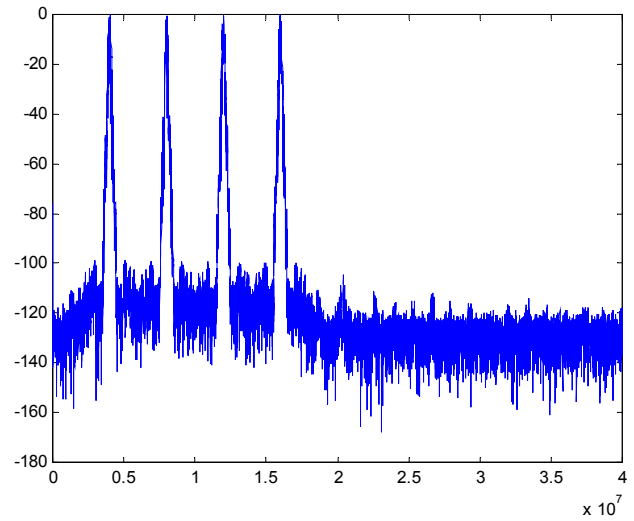


FIGURE 18. DIGITAL OUTPUT, HALFBAND ENABLED

### EDGE Burst Mode

The device is configured for outputting one channel of EDGE in burst mode. The 16-bit I and 16-bit Q data is input through the serial channel SDA input, and the fixed integer divider (FID) is enabled to provide an integer relationship of  $CLK/288$  or  $f_s = 270.833\text{kHz}$  rate. The shaping FIR is programmed to interpolate by x16 with a dataspan of 6. The filter frequency response is shown in Figure 19. The half band filter is not enabled, the carrier phase is pre-loaded to zero degrees, and the carrier frequency is set to 4MHz. The output mode is Cascade, with reCASout output on IOUT<19:0> and imCASout output on QOUT<19:0>. The analog performance of the device is shown in Figure 20, utilizing the on-board HI5828 dual DAC, and the vector analysis is shown in Figure 21. The stimulus file is 148 samples of pseudo random QPSK data.

The dynamic configuration software mode is utilized with a programmed value of TXEN on =148.5 bits  $(148.5 * (1/270.8333\text{e}3) / (1/78\text{e}6))$  or 42768 clocks on and 8.25 bits  $(8.25 * (1/270.8333\text{e}3) / (1/78\text{e}6))$  or 2376 clocks off. These settings allow the device to transmit 148 bits in the required on normal burst period and to ramp up/down in the guard period. The gain profile is not enabled, with the EDGE FIR coefficients providing the required pulse shaping.

TABLE 4. EDGE BURST CONFIGURATION

|                             |                  |
|-----------------------------|------------------|
| Clock Rate CLK =            | 78MHz            |
| Sample Frequency $f_s$ =    | 270.833kHz       |
| Configuration File:         | EDGE_Only.js     |
| Filter File:                | edget16xTest.imp |
| Stimulus File:              | EDGE_Only.imp    |
| Dynamic Configuration File: | EDGE_Only.imp    |

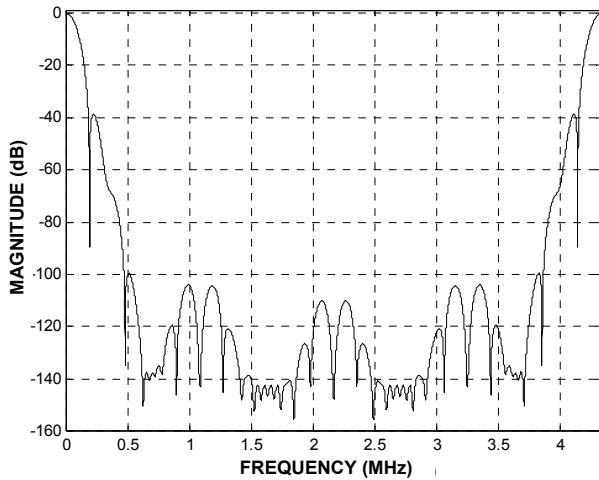


FIGURE 19. SHAPING FILTER FREQ. RESPONSE

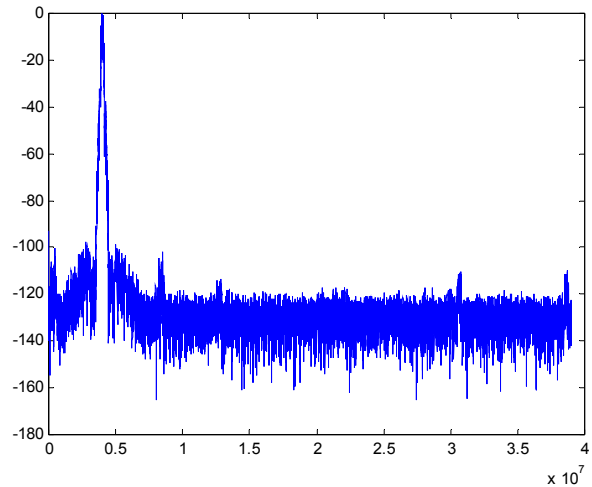


FIGURE 22. DIGITAL OUTPUT

The digital data was collected utilizing a 32K FFT with the results shown in Figure 22. Enabling the halfband, the digital performance is improved as shown in Figure 23.

TXEN timing latency in the offset binary mode is shown in Figure 13, while 2's complement timing is approximately 13.2μS.

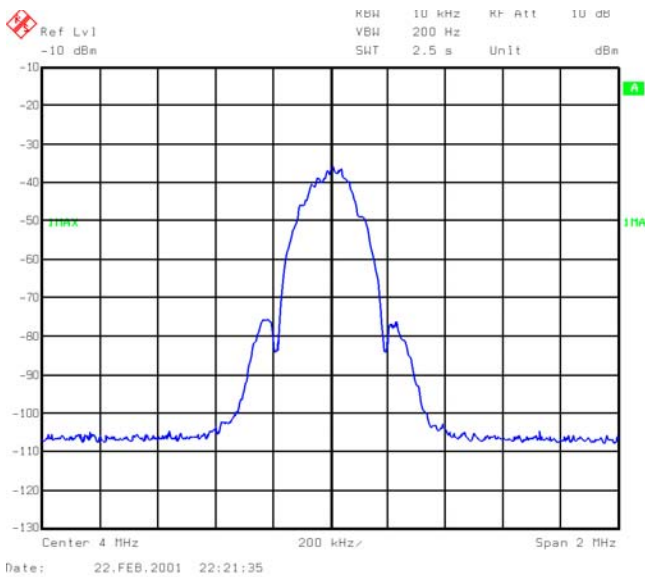


FIGURE 20. ANALOG SPECTRUM

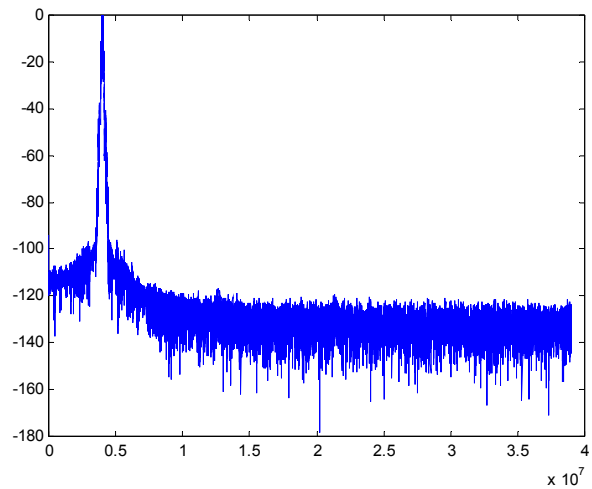


FIGURE 23. DIGITAL OUTPUT, HALFBAND ENABLED

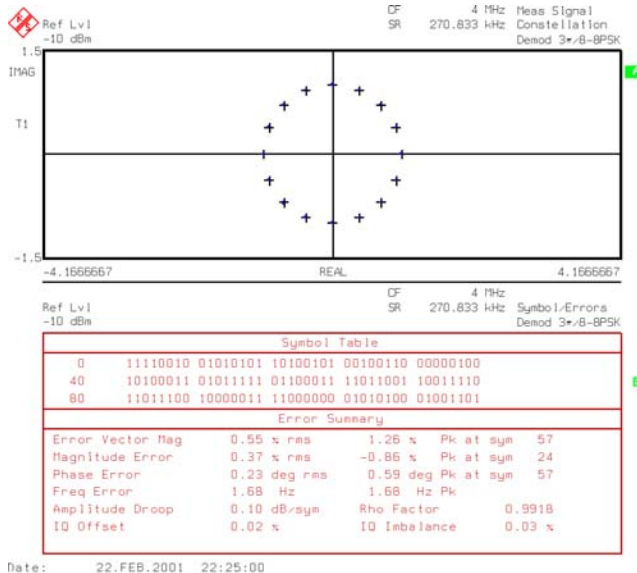


FIGURE 21. VECTOR ANALYZER OUTPUT

### GSM/EDGE Overlay

The device is configured for one normal burst of pre-filtered FM GSM followed by one normal burst of QASK EDGE with different filters. The 16-bit I and 16-bit Q data is input through the serial channel SDA input, and the fixed integer divider (FID) is enabled to provide an integer relationship of CLK/288 or  $f_s = 270.833\text{kHz}$  rate. The shaping FIR is programmed to interpolate by x16 with a dataspan of 6, with the GSM filter coefficients preloaded in memory bank one and the EDGE coefficients in bank two. The filters utilized are the same as for the GSM or EDGE burst mode. The half band filter is not enabled, the carrier phase is pre-loaded to zero degrees, and the carrier frequency is set to 4MHz. The output mode is Cascade, with reCASout output on IOUT<19:0> and imCASout

output on QOUT<19:0>. The analog performance of the device is shown in Figure 25, utilizing the on-board HI5828 dual DAC. Figures 26-34 show various timing depictions for the overlaid burst. The stimulus file is 148 samples of pseudo random GMSK data with a synchronization pattern included followed by 148 patterns of 3/8pi 8psk pn data.

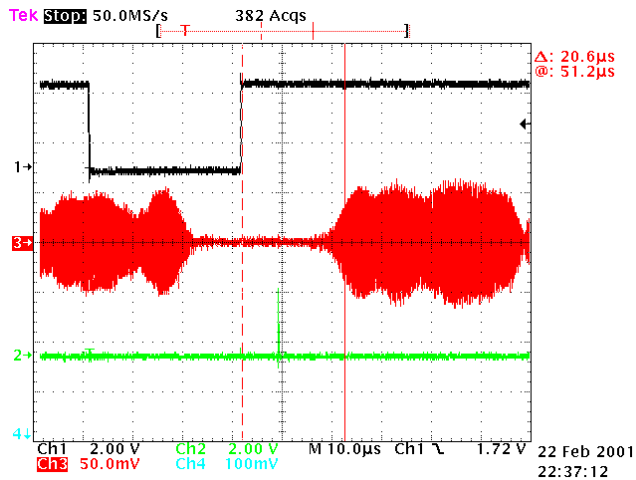


FIGURE 24. TXEN vs BURST TIMING (HALFBAND ON)

TABLE 5. GSM/EDGE OVERLAY CONFIGURATION

|                             |                                       |
|-----------------------------|---------------------------------------|
| Clock Rate CLK =            | 78MHz                                 |
| Sample Frequency $f_s$ =    | 270.833kHz                            |
| Configuration File:         | GSM_EDGE.js                           |
| Filter File:                | gs5t16xTest.imp, and edget16xTest.imp |
| Stimulus File:              | GSM_EDGE.imp                          |
| Dynamic Configuration File: | GSM_EDGE.cfg                          |

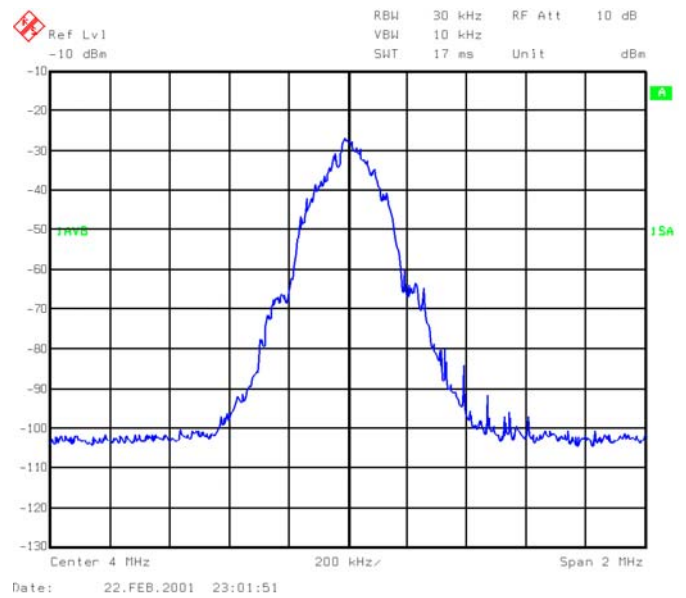


FIGURE 25. SPECTRUM GSM/EDGE

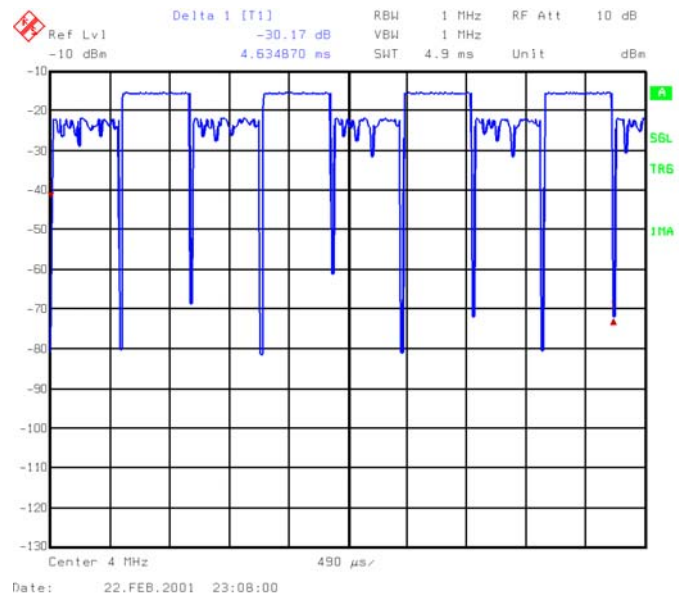


FIGURE 26. TDMA FRAME GSM/EDGE



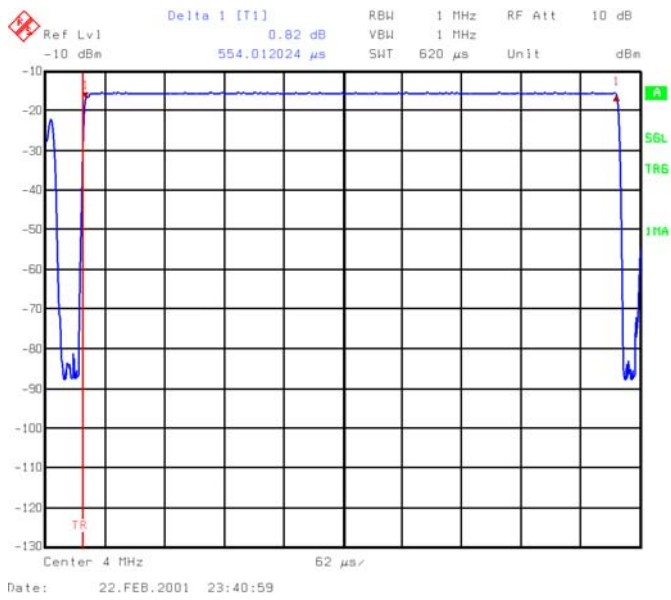


FIGURE 27. GSM FRAME TIMING

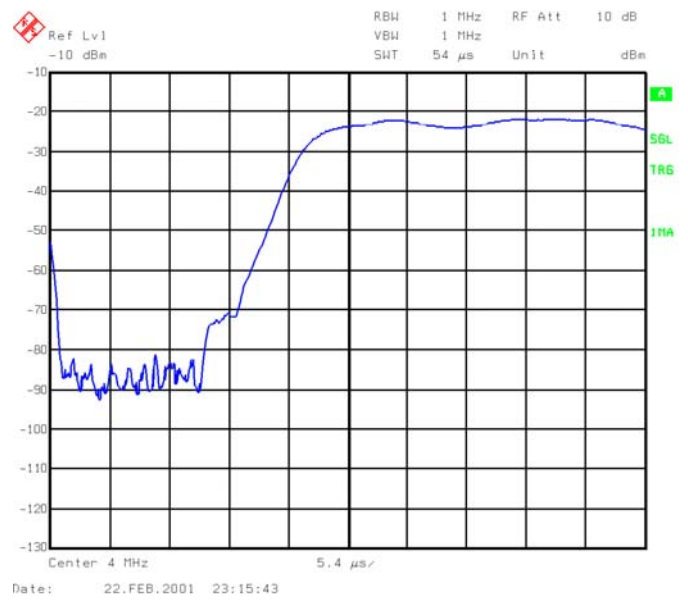


FIGURE 29. EDGE RAMP UP TIMING

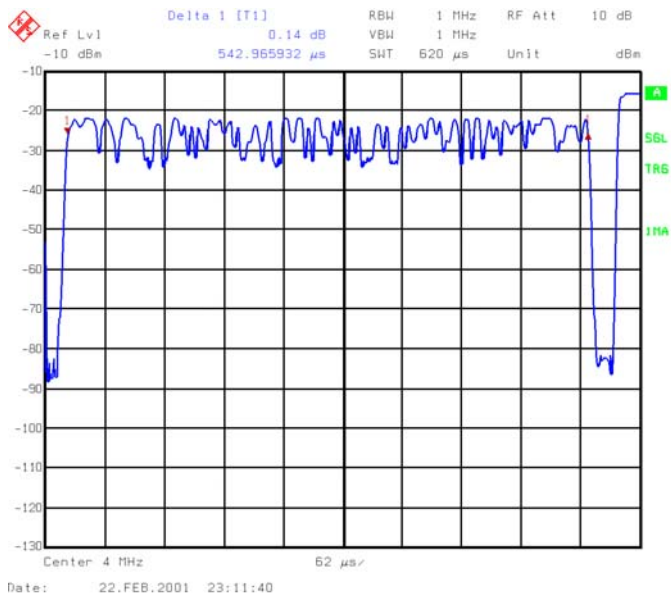


FIGURE 28. EDGE FRAME TIMING

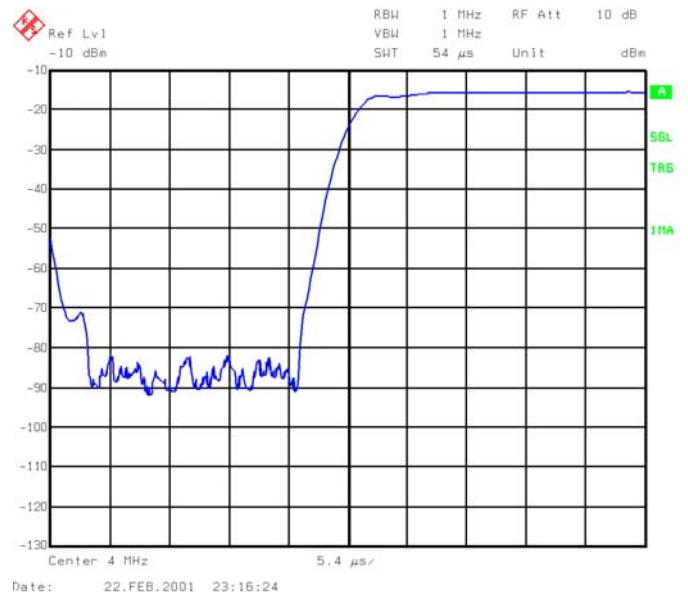


FIGURE 30. GSM RAMP UP TIMING

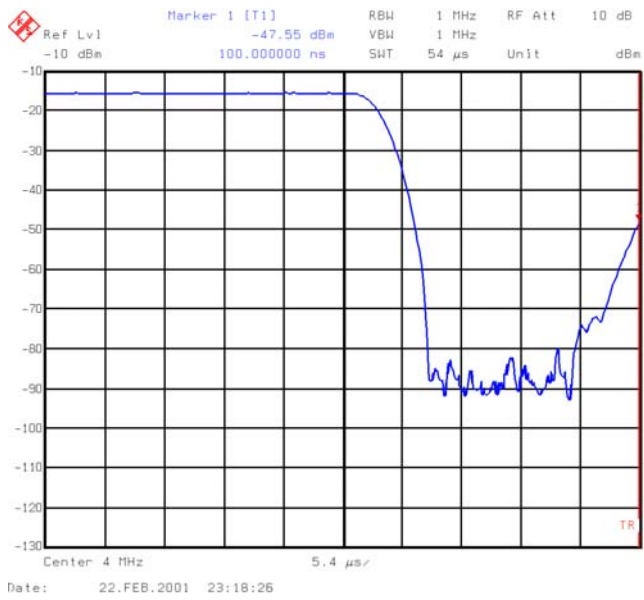


FIGURE 31. GSM QUENCH TIMING

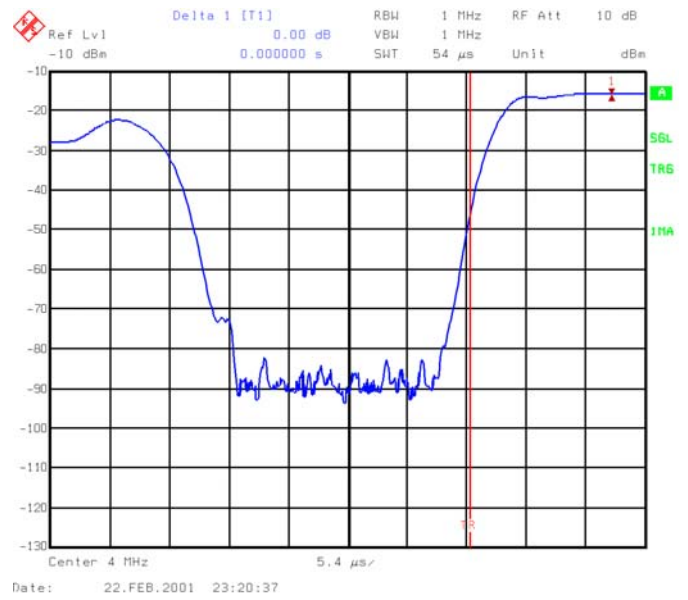


FIGURE 33. EDGE TO GSM GUARD TIMING

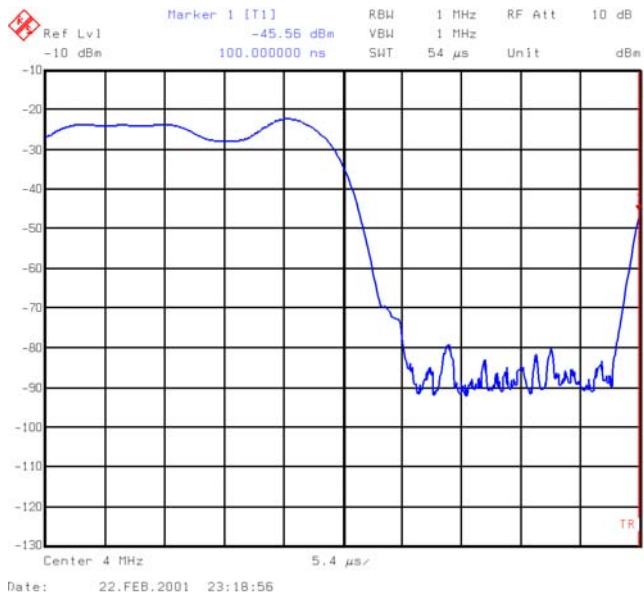


FIGURE 32. EDGE QUENCH TIMING

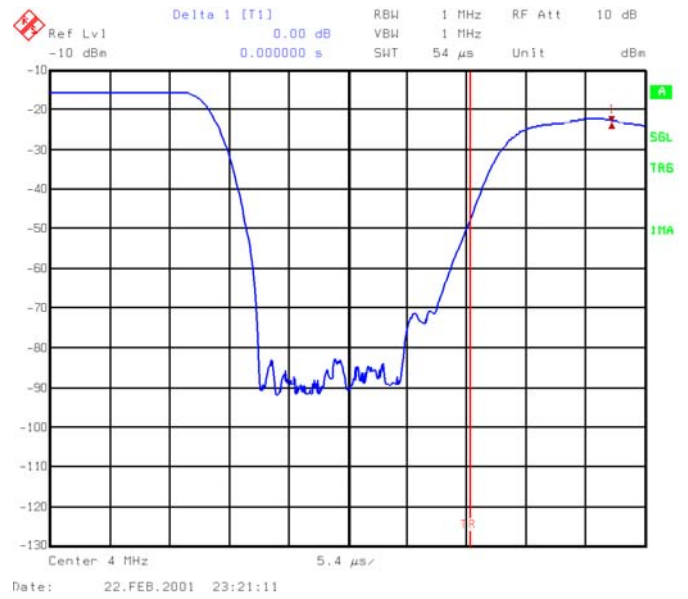


FIGURE 34. GSM TO EDGE GUARD TIMING

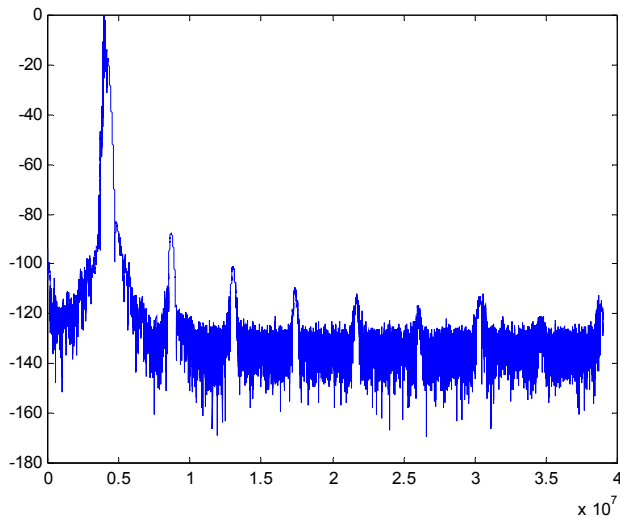


FIGURE 35. DIGITAL OUTPUT

The digital data was collected utilizing a 32K FFT with the results shown in Figure 35. Enabling the halfband, the digital performance is improved as shown in Figure 36.

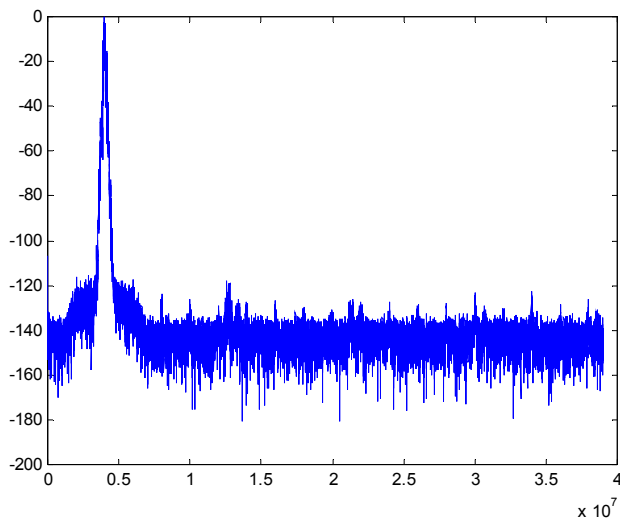


FIGURE 36. DIGITAL OUTPUT WITH HALFBAND

**CDMA2000-1x**

The device is configured for QASK and outputting four channels of CDMA in continuous mode with no phase equalization. The 16-bit I and 16-bit Q data is input through the serial channel SDA-SDD inputs, and the symbol NCO is programmed to provide a sample rate of  $f_s = 1.2288\text{kHz}$ . The shaping FIR is programmed to interpolate by x4 with a dataspan of 12. The filter frequency response is shown in Figure 37. The half band filter is not enabled, the carrier phase is pre-loaded to zero degrees, and the carrier frequencies are set to 4, 8, 12, and 16MHz. The output mode is Cascade, with reCASout output on IOOUT<19:0> and imCASout output on QOUT<19:0>. The analog performance of the device is shown in Figure 38, utilizing the on-board HI5828 dual DAC. The stimulus file is 511 samples of pseudo random QPSK data.

TABLE 6. CDMA2000-1X CONFIGURATION

|                             |                    |
|-----------------------------|--------------------|
| Clock Rate CLK =            | 80MHz              |
| Sample Frequency $f_s$ =    | 1.2288MHz          |
| Configuration File:         | CDMA2000_1x.js     |
| Filter File:                | IS95CoefScaled.imp |
| Stimulus File:              | qpskpn.imp         |
| Dynamic Configuration File: | N/A                |

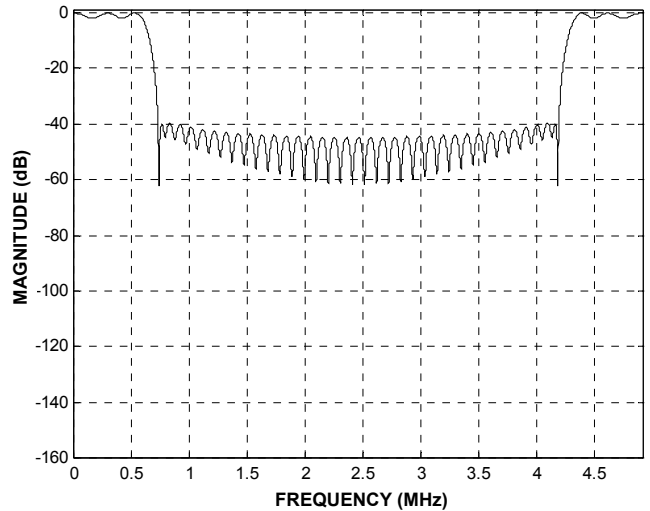


FIGURE 37. SHAPING FILTER FREQ. RESPONSE

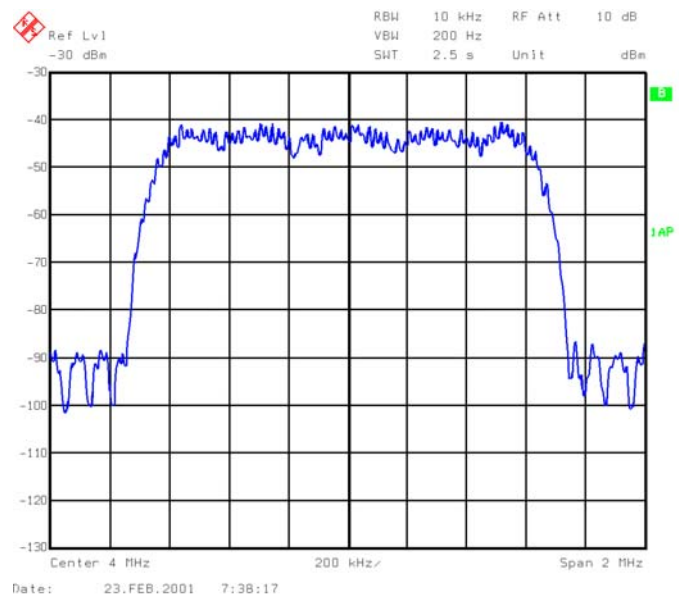


FIGURE 38. ANALOG SPECTRUM

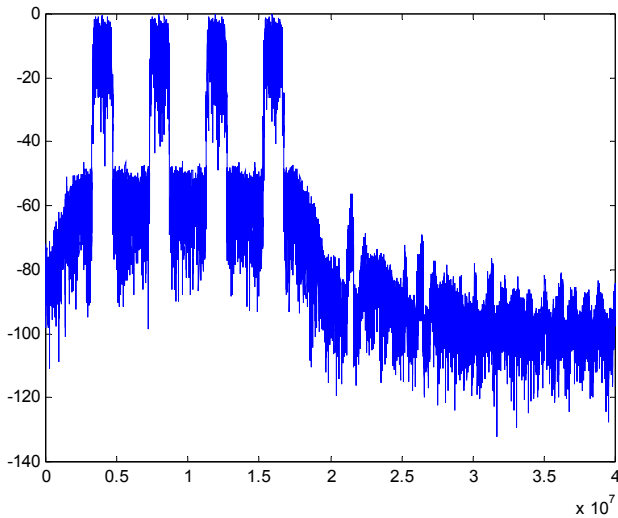


FIGURE 39. DIGITAL OUTPUT

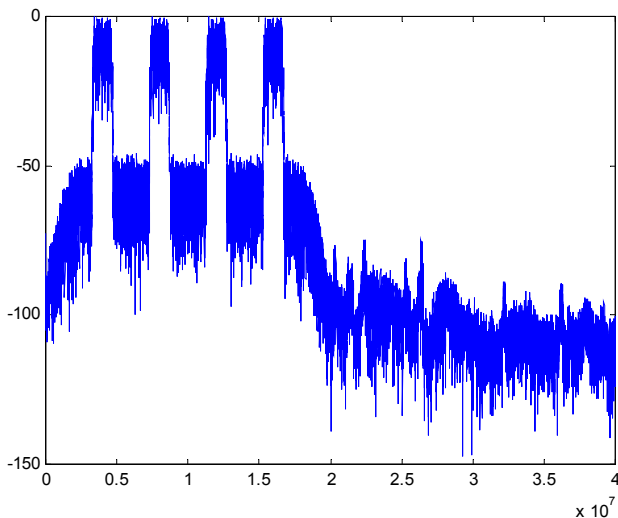


FIGURE 40. DIGITAL OUTPUT, HALFBAND ENABLED

The digital data was collected utilizing a 32K FFT with the results shown in Figure 39. Enabling the halfband, the digital performance is improved as shown in Figure 40.

TABLE 7. CDMA2000-3X MC CONFIGURATION

|                             |                    |
|-----------------------------|--------------------|
| Clock Rate CLK =            | 61.44MHz           |
| Sample Frequency $f_s$ =    | 1.2288MHz          |
| Configuration File:         | CDMA2000_3x_MC.js  |
| Filter File:                | IS95CoefScaled.imp |
| Stimulus File:              | qpskpn.imp         |
| Dynamic Configuration File: | N/A                |

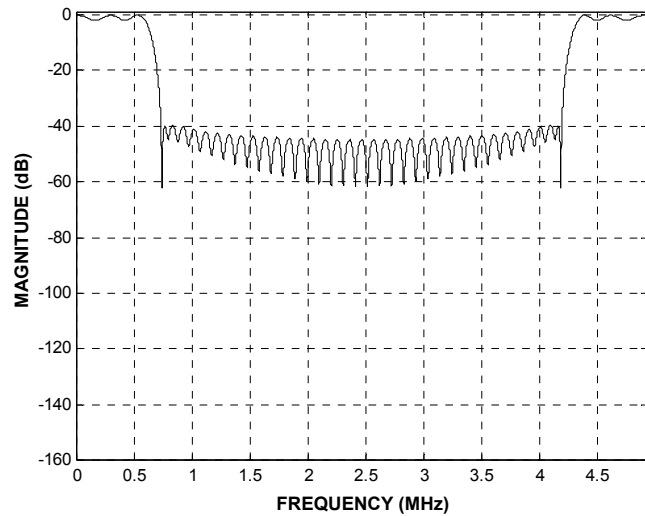


FIGURE 41. SHAPING FILTER FREQUENCY RESPONSE

**CDMA2000-3x MC**

The device is configured for outputting three channels of CDMA in continuous mode. The 16-bit I and 16-bit Q data is input through the serial channel SDA-SDC inputs, and the symbol NCO is programmed to provide a sample rate of  $f_s = 1.2288\text{kHz}$ . The shaping FIR is programmed to interpolate by x4 with a dataspan of 12. The filter frequency response is shown in Figure 41. The half band filter is not enabled, the carrier phase is pre-loaded to zero degrees, and the carrier frequencies are set to 4, 5.25, and 6.5MHz. The output mode is Cascade, with reCASout output on IOUT<19:0> and imCASout output on QOUT<19:0>. The analog performance of the device is shown in Figure 42, utilizing the on-board HI5828 dual DAC, and the vector analysis is shown in Figure 43. The stimulus file is 511 samples of pseudo random QPSK data.

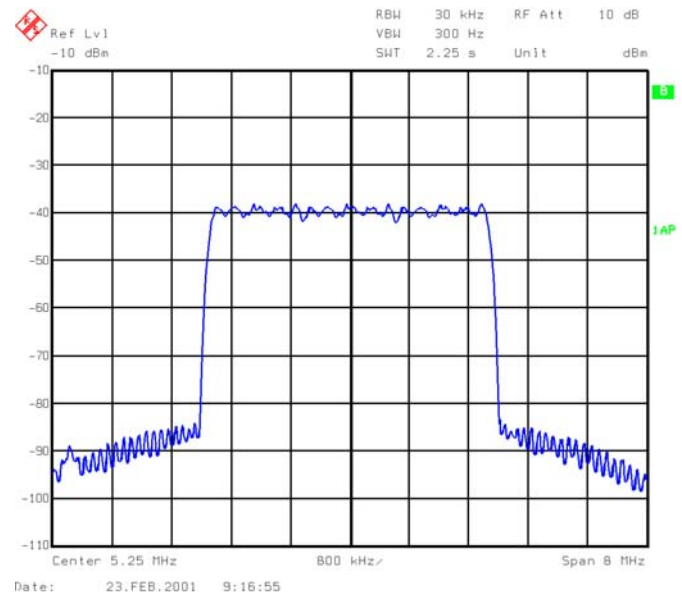


FIGURE 42. ANALOG SPECTRUM

The digital data was collected utilizing a 32K FFT with the results shown in Figure 43. Enabling the halfband, the digital performance is improved as shown in Figure 44.

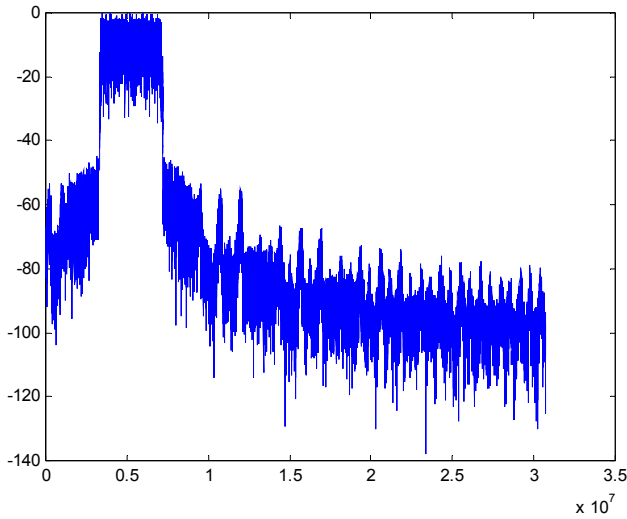


FIGURE 43. DIGITAL OUTPUT

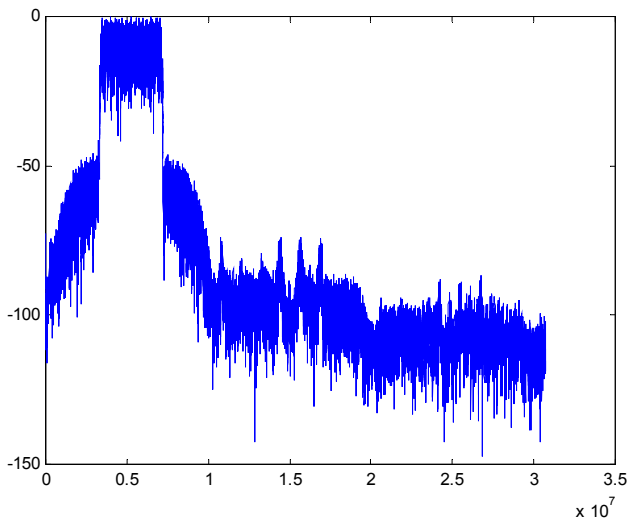


FIGURE 44. DIGITAL OUTPUT, HALFBAND ENABLED

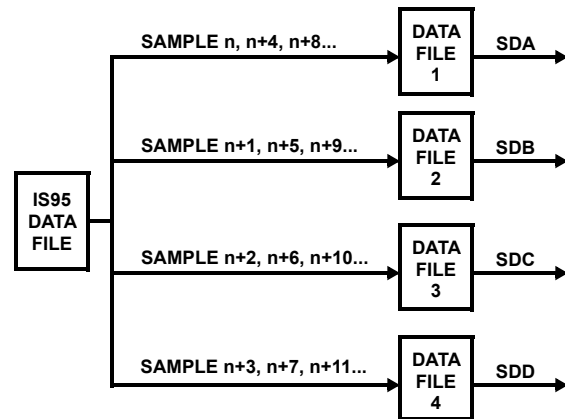
**CDMA-2000-3x DS**

The device is configured for outputting one channel of CDMA in continuous mode. The 16-bit I and 16-bit Q data is input through the serial channel SDA-SDD inputs, and the symbol NCO is programmed to provide a sample rate of  $f_s = 960\text{kHz}$ . All four channels of the device are utilized in polyphase mode to create this wideband channel. The serial input samples are parsed into four inputs, with each channel receiving every fourth input, as shown in Figure 45. The shaping FIR is programmed to interpolate by x16 with a dataspan of 4, with the filters loaded in a time shifted configuration as shown in Figure 46. The coefficient location shift in the filters allows for the polyphased outputs from each channel to be re-combined in the summer to effectively produce a single wideband

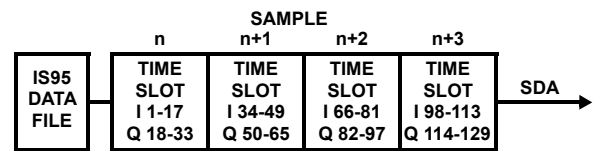
channel. The filter frequency response is shown in Figure 47. The half band filter is not enabled, the carrier phase is pre-loaded to zero degrees, and the carrier frequencies are set to 8MHz. The output mode is Cascade, with reCASout output on IOUT<19:0> and imCASout output on QOUT<19:0>. The analog performance of the device is shown in Figure 48, utilizing the on-board HI5828 dual DAC. The stimulus file is 511 samples of pseudo random QPSK data.

TABLE 8. CDMA2000-3X DS CONFIGURATION

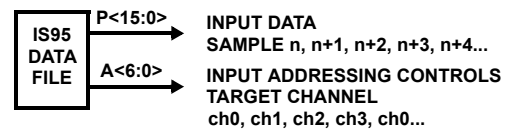
|                             |                          |
|-----------------------------|--------------------------|
| Clock Rate CLK =            | 80MHz                    |
| Sample Frequency $f_s$ =    | 0.960MHz overall 3.84MHz |
| Configuration File:         | CDMA2000_3x_DS.js        |
| Filter File:                | IS95CoefScaled0-3.imp    |
| Stimulus File:              | parsedqpskpn0-3.imp      |
| Dynamic Configuration File: | N/A                      |



DATA RE-FORMATTED INTO 4 SERIAL DATA INPUTS



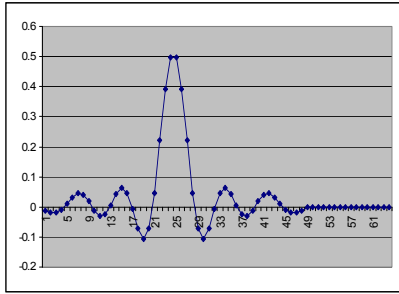
ALTERNATIVE SERIAL SINGLE DATA INPUT CHANNEL



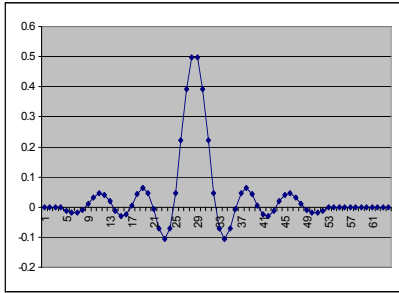
ALTERNATIVE PARALLEL DATA INPUT CHANNEL

FIGURE 45. MULTIPLE CHANNEL INPUT DATA FORMAT

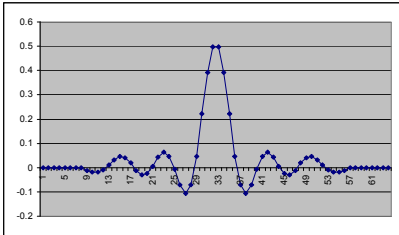
CHANNEL 0  
(NO SHIFT)



CHANNEL 1  
(SHIFTED 4)



CHANNEL 2  
(SHIFTED 8)



CHANNEL 3  
(SHIFTED 12)

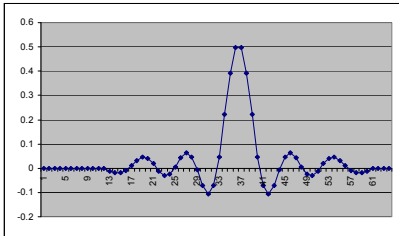


FIGURE 46. FILTER ALIGNMENT

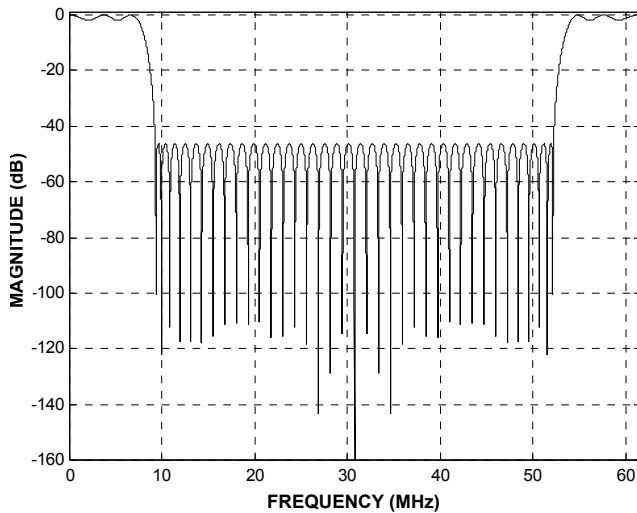


FIGURE 47. SHAPING FILTER FREQ. RESPONSE

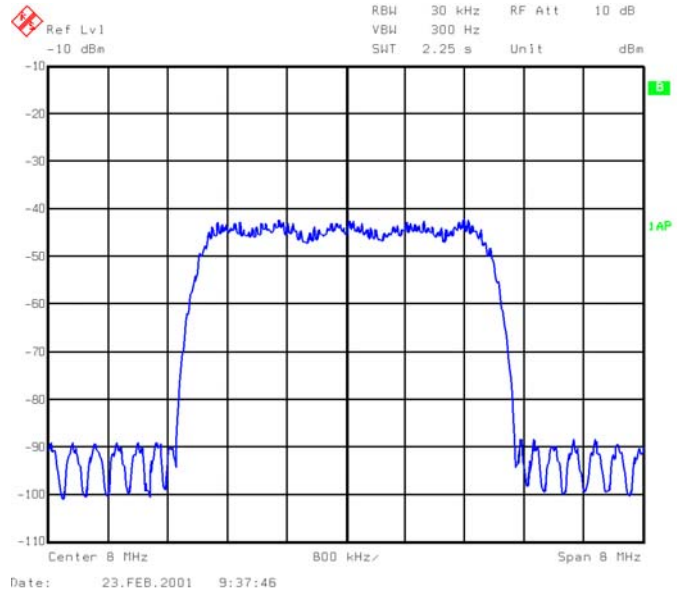


FIGURE 48. ANALOG SPECTRUM

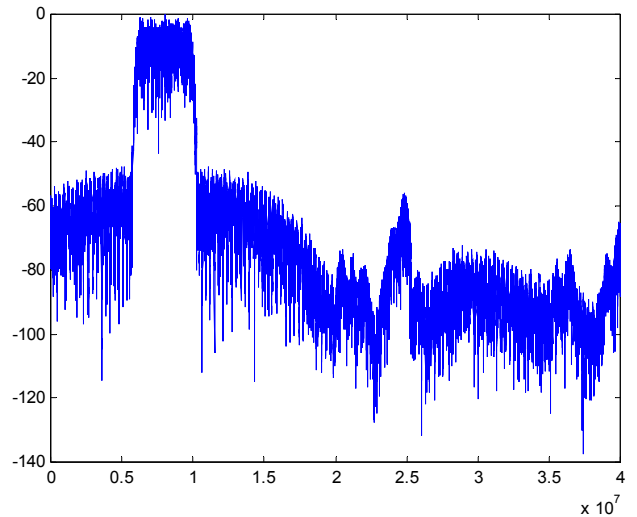


FIGURE 49. DIGITAL OUTPUT

The digital data was collected utilizing a 32K FFT with the results shown in Figure 49. Enabling the halfband, the digital performance is improved as shown in Figure 50.

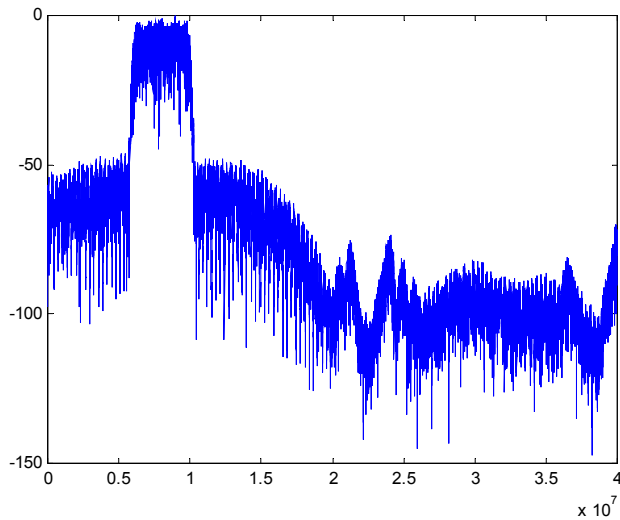


FIGURE 50. DIGITAL OUTPUT, HALFBAND ENABLED

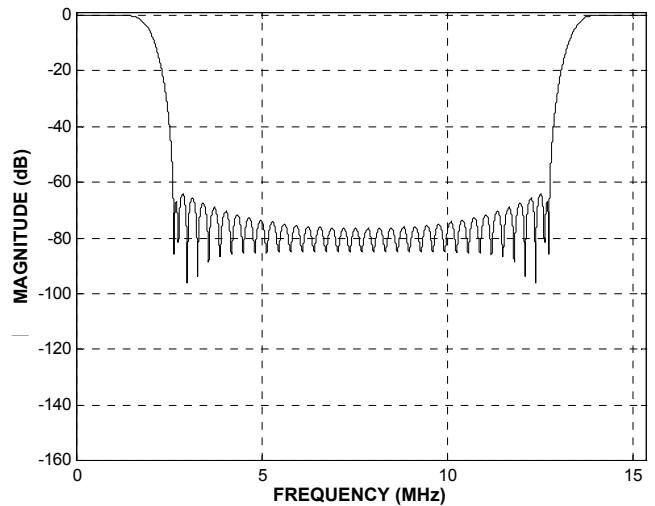


FIGURE 51. SHAPING FILTER FREQ. RESPONSE

### UMTS

The device is configured for outputting one channel of UMTS in continuous mode. The 12-bit I and 12-bit Q data is input through the serial channel SDA-SDD inputs, and the symbol NCO is programmed to provide a sample rate of  $f_S = 960\text{kHz}$ . All four channels of the device are utilized in polyphase mode to create this wideband channel. The serial input samples are parsed into four inputs, with each channel receiving every fourth input, as shown in Figure 51. The shaping FIR is programmed to interpolate by x16 with a dataspan of 4, with the filters loaded in a time shifted configuration as shown in Figure 52. The coefficient location shift in the filters allows for the polyphased outputs from each channel to be re-combined in the summer to effectively produce a single wideband channel. The filter frequency response is shown in Figure 53. The half band filter is not enabled, the carrier phase is pre-loaded to zero degrees, and the carrier frequencies are set to 7.3424MHz. The output mode is Cascade, with reCASout output on IOOUT<19:0> and imCASout output on QOUT<19:0>. The analog performance of the device is shown in Figure 54, utilizing the on-board HI5828 dual DAC. The stimulus file is 511 samples of pseudo random QPSK data..

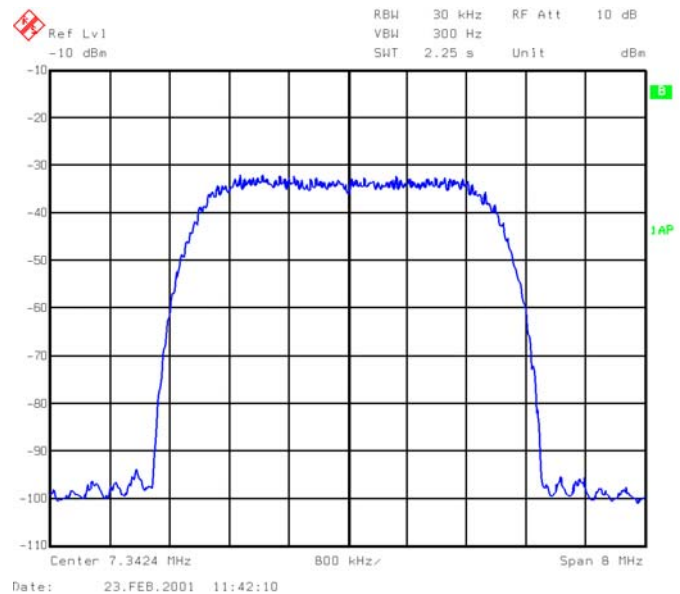


FIGURE 52. ANALOG SPECTRUM

TABLE 9. UMTS CONFIGURATION

|                             |                          |
|-----------------------------|--------------------------|
| Clock Rate CLK =            | 61.44MHz                 |
| Sample Frequency $f_S$ =    | 0.960MHz overall 3.84MHz |
| Configuration File:         | UMTS.js                  |
| Filter File:                | UMTS0-3.imp              |
| Stimulus File:              | parsedqpskpn0-3.imp      |
| Dynamic Configuration File: | N/A                      |

The digital data was collected utilizing a 32K FFT with the results shown in Figure 51. Enabling the halfband, the digital performance is improved as shown in Figure 51.

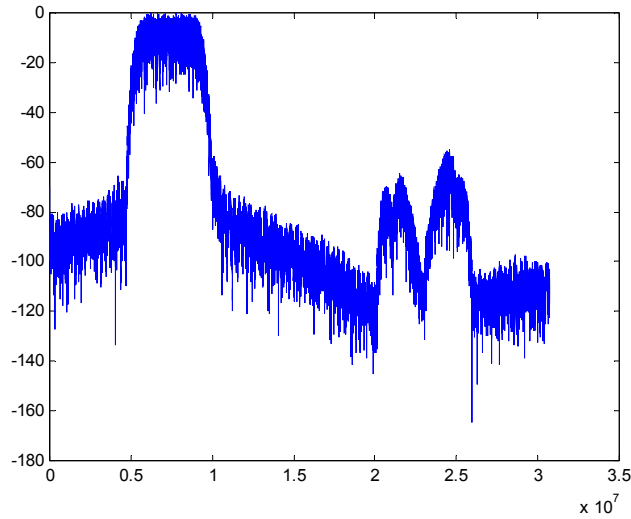


FIGURE 53. DIGITAL OUTPUT

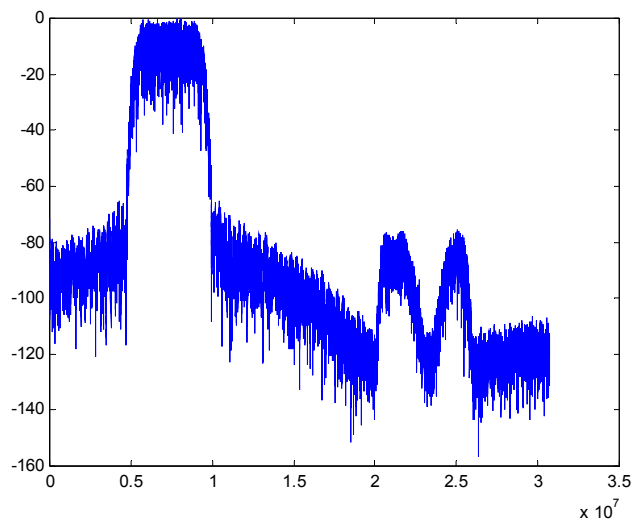


FIGURE 54. DIGITAL OUTPUT, HALFBAND ENABLED

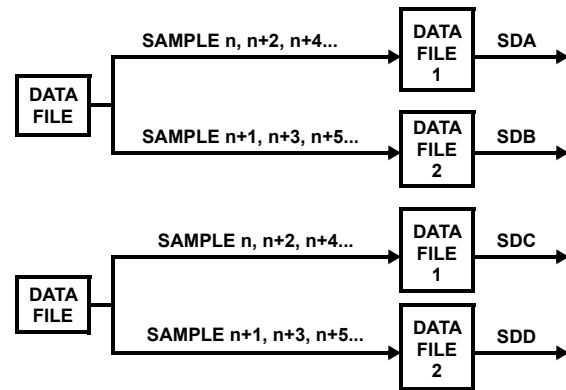
**UMTS-Two Channels**

The device is configured for outputting two channel of UMTS in continuous mode. The 12-bit I and 12-bit Q data is input through the serial channel SDA-SDD inputs, and the symbol NCO is programmed to provide a sample rate of  $f_S = 1.92\text{MHz}$ . All four channels of the device are utilized by combining 2 channels in polyphase mode to create each of the two wideband channels. The serial input samples are parsed into two inputs, with each channel receiving every second input, as shown in Figure 55. The shaping FIR is programmed to interpolate by x8 with a dataspan of 6, with the filters loaded in a time shifted configuration as shown in Figure 56. The coefficient location shift in the filters allows for the polyphased outputs from each channel to be recombined in the summer to effectively produce a wideband channel. The filter frequency response is shown in Figure 57. The half band filter is not

enabled, the carrier phase is pre-loaded to zero degrees, and the carrier frequencies are set to 5 and 12MHz. The output mode is Cascade, with reCASout output on IOUT<19:0> and imCASout output on QOUT<19:0>. The analog performance of the device is shown in Figure 58, utilizing the on-board HI5828 dual DAC. The stimulus file is 511 samples of pseudo random QPSK data..

TABLE 10. UMTS CONFIGURATION

|                             |                         |
|-----------------------------|-------------------------|
| Clock Rate CLK =            | 92.16MHz                |
| Sample Frequency $f_S$ =    | 1.92MHz overall 3.84MHz |
| Configuration File:         | UMTS2.js                |
| Filter File:                | UMTS_44t0-1.imp         |
| Stimulus File:              | 2parsedqpskpn0-1.imp    |
| Dynamic Configuration File: | N/A                     |



DATA RE-FORMATTED INTO 4 SERIAL DATA INPUTS

FIGURE 55. MULTIPLE CHANNEL INPUT DATA FORMAT

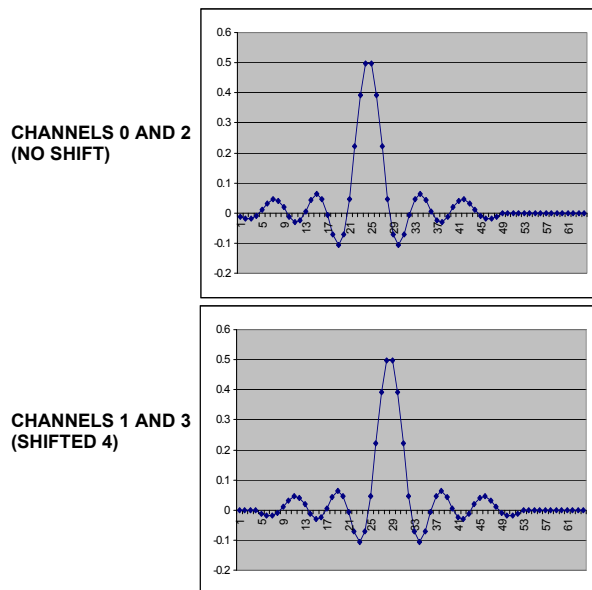


FIGURE 56. FILTER ALIGNMENT



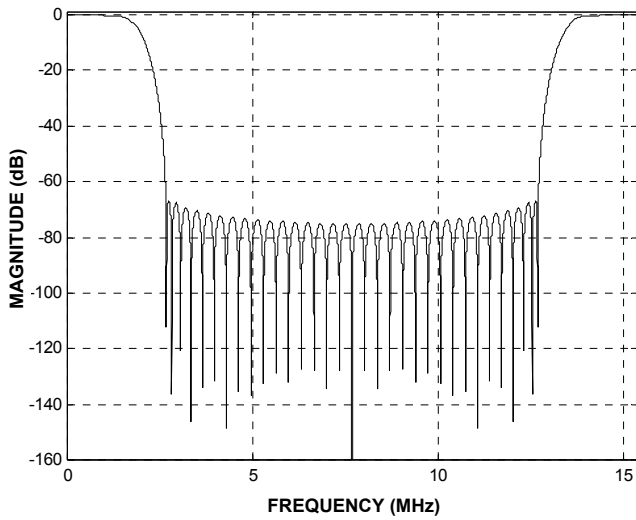


FIGURE 57. SHAPING FILTER FREQ. RESPONSE

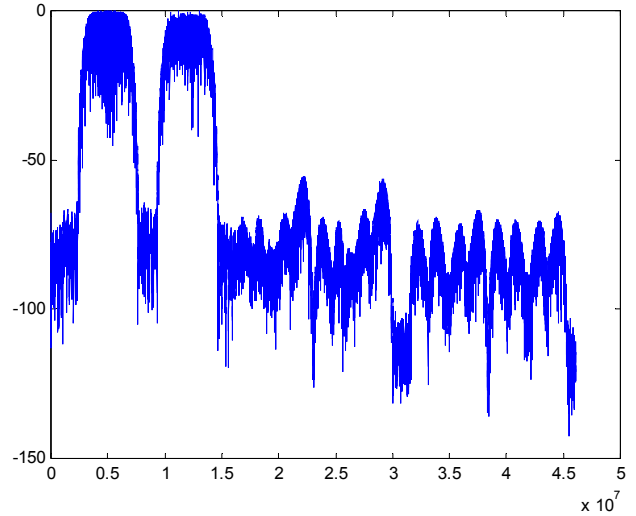


FIGURE 59. DIGITAL OUTPUT

The digital data was collected utilizing a 32K FFT with the results shown in Figure 58. Enabling the halfband, the digital performance is improved as shown in Figure 59.

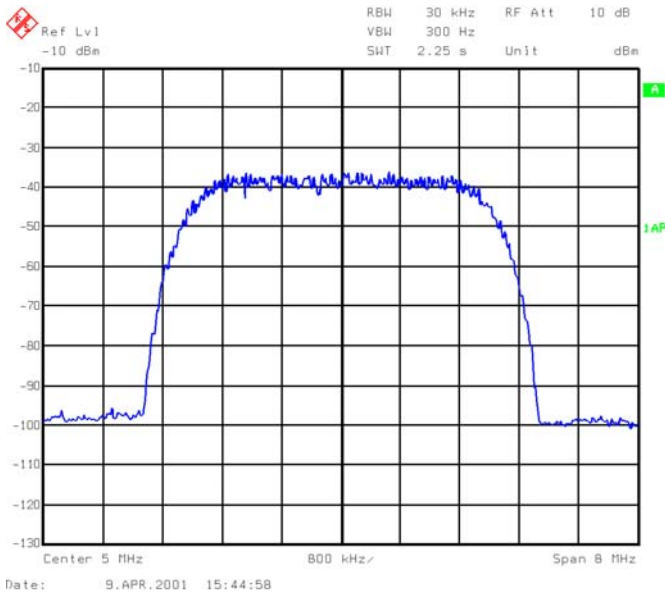


FIGURE 58. ANALOG SPECTRUM

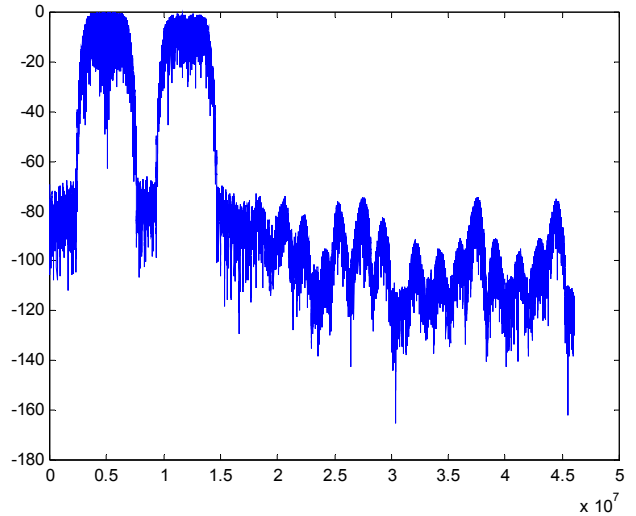


FIGURE 60. DIGITAL OUTPUT, HALFBAND ENABLED

## Notice

1. Descriptions of circuits, software and other related information in this document are provided only to illustrate the operation of semiconductor products and application examples. You are fully responsible for the incorporation or any other use of the circuits, software, and information in the design of your product or system. Renesas Electronics disclaims any and all liability for any losses and damages incurred by you or third parties arising from the use of these circuits, software, or information.
2. Renesas Electronics hereby expressly disclaims any warranties against and liability for infringement or any other claims involving patents, copyrights, or other intellectual property rights of third parties, by or arising from the use of Renesas Electronics products or technical information described in this document, including but not limited to, the product data, drawings, charts, programs, algorithms, and application examples.
3. No license, express, implied or otherwise, is granted hereby under any patents, copyrights or other intellectual property rights of Renesas Electronics or others.
4. You shall not alter, modify, copy, or reverse engineer any Renesas Electronics product, whether in whole or in part. Renesas Electronics disclaims any and all liability for any losses or damages incurred by you or third parties arising from such alteration, modification, copying or reverse engineering.
5. Renesas Electronics products are classified according to the following two quality grades: "Standard" and "High Quality". The intended applications for each Renesas Electronics product depends on the product's quality grade, as indicated below.  
"Standard": Computers; office equipment; communications equipment; test and measurement equipment; audio and visual equipment; home electronic appliances; machine tools; personal electronic equipment; industrial robots; etc.  
"High Quality": Transportation equipment (automobiles, trains, ships, etc.); traffic control (traffic lights); large-scale communication equipment; key financial terminal systems; safety control equipment; etc.  
Unless expressly designated as a high reliability product or a product for harsh environments in a Renesas Electronics data sheet or other Renesas Electronics document, Renesas Electronics products are not intended or authorized for use in products or systems that may pose a direct threat to human life or bodily injury (artificial life support devices or systems; surgical implantations; etc.), or may cause serious property damage (space system; undersea repeaters; nuclear power control systems; aircraft control systems; key plant systems; military equipment; etc.). Renesas Electronics disclaims any and all liability for any damages or losses incurred by you or any third parties arising from the use of any Renesas Electronics product that is inconsistent with any Renesas Electronics data sheet, user's manual or other Renesas Electronics document.
6. When using Renesas Electronics products, refer to the latest product information (data sheets, user's manuals, application notes, "General Notes for Handling and Using Semiconductor Devices" in the reliability handbook, etc.), and ensure that usage conditions are within the ranges specified by Renesas Electronics with respect to maximum ratings, operating power supply voltage range, heat dissipation characteristics, installation, etc. Renesas Electronics disclaims any and all liability for any malfunctions, failure or accident arising out of the use of Renesas Electronics products outside of such specified ranges.
7. Although Renesas Electronics endeavors to improve the quality and reliability of Renesas Electronics products, semiconductor products have specific characteristics, such as the occurrence of failure at a certain rate and malfunctions under certain use conditions. Unless designated as a high reliability product or a product for harsh environments in a Renesas Electronics data sheet or other Renesas Electronics document, Renesas Electronics products are not subject to radiation resistance design. You are responsible for implementing safety measures to guard against the possibility of bodily injury, injury or damage caused by fire, and/or danger to the public in the event of a failure or malfunction of Renesas Electronics products, such as safety design for hardware and software, including but not limited to redundancy, fire control and malfunction prevention, appropriate treatment for aging degradation or any other appropriate measures. Because the evaluation of microcomputer software alone is very difficult and impractical, you are responsible for evaluating the safety of the final products or systems manufactured by you.
8. Please contact a Renesas Electronics sales office for details as to environmental matters such as the environmental compatibility of each Renesas Electronics product. You are responsible for carefully and sufficiently investigating applicable laws and regulations that regulate the inclusion or use of controlled substances, including without limitation, the EU RoHS Directive, and using Renesas Electronics products in compliance with all these applicable laws and regulations. Renesas Electronics disclaims any and all liability for damages or losses occurring as a result of your noncompliance with applicable laws and regulations.
9. Renesas Electronics products and technologies shall not be used for or incorporated into any products or systems whose manufacture, use, or sale is prohibited under any applicable domestic or foreign laws or regulations. You shall comply with any applicable export control laws and regulations promulgated and administered by the governments of any countries asserting jurisdiction over the parties or transactions.
10. It is the responsibility of the buyer or distributor of Renesas Electronics products, or any other party who distributes, disposes of, or otherwise sells or transfers the product to a third party, to notify such third party in advance of the contents and conditions set forth in this document.
11. This document shall not be reprinted, reproduced or duplicated in any form, in whole or in part, without prior written consent of Renesas Electronics.
12. Please contact a Renesas Electronics sales office if you have any questions regarding the information contained in this document or Renesas Electronics products.  
(Note 1) "Renesas Electronics" as used in this document means Renesas Electronics Corporation and also includes its directly or indirectly controlled subsidiaries.  
(Note 2) "Renesas Electronics product(s)" means any product developed or manufactured by or for Renesas Electronics.

(Rev.4.0-1 November 2017)



### SALES OFFICES

Renesas Electronics Corporation

<http://www.renesas.com>

Refer to "<http://www.renesas.com/>" for the latest and detailed information.

**Renesas Electronics America Inc.**  
1001 Murphy Ranch Road, Milpitas, CA 95035, U.S.A.  
Tel: +1-408-432-8888, Fax: +1-408-434-5351

**Renesas Electronics Canada Limited**  
9251 Yonge Street, Suite 8309 Richmond Hill, Ontario Canada L4C 9T3  
Tel: +1-905-237-2004

**Renesas Electronics Europe Limited**  
Dukes Meadow, Millboard Road, Bourne End, Buckinghamshire, SL8 5FH, U.K  
Tel: +44-1628-651-700, Fax: +44-1628-651-804

**Renesas Electronics Europe GmbH**  
Arcadiastrasse 10, 40472 Düsseldorf, Germany  
Tel: +49-211-6503-0, Fax: +49-211-6503-1327

**Renesas Electronics (China) Co., Ltd.**  
Room 1709 Quantum Plaza, No.27 ZhichunLu, Haidian District, Beijing, 100191 P. R. China  
Tel: +86-10-8235-1155, Fax: +86-10-8235-7679

**Renesas Electronics (Shanghai) Co., Ltd.**  
Unit 301, Tower A, Central Towers, 555 Langao Road, Putuo District, Shanghai, 200333 P. R. China  
Tel: +86-21-2226-0888, Fax: +86-21-2226-0999

**Renesas Electronics Hong Kong Limited**  
Unit 1601-1611, 16/F., Tower 2, Grand Century Place, 193 Prince Edward Road West, Mongkok, Kowloon, Hong Kong  
Tel: +852-2265-6688, Fax: +852-2886-9022

**Renesas Electronics Taiwan Co., Ltd.**  
13F, No. 363, Fu Shing North Road, Taipei 10543, Taiwan  
Tel: +886-2-8175-9600, Fax: +886-2-8175-9670

**Renesas Electronics Singapore Pte. Ltd.**  
80 Bendemeer Road, Unit #06-02 Hyflux Innovation Centre, Singapore 339949  
Tel: +65-6213-0200, Fax: +65-6213-0300

**Renesas Electronics Malaysia Sdn.Bhd.**  
Unit 1207, Block B, Menara Amcorp, Amcorp Trade Centre, No. 18, Jln Persiaran Barat, 46050 Petaling Jaya, Selangor Darul Ehsan, Malaysia  
Tel: +60-3-7955-9390, Fax: +60-3-7955-9510

**Renesas Electronics India Pvt. Ltd.**  
No.777C, 100 Feet Road, HAL 2nd Stage, Indiranagar, Bangalore 560 038, India  
Tel: +91-80-67208700, Fax: +91-80-67208777

**Renesas Electronics Korea Co., Ltd.**  
17F, KAMCO Yangjae Tower, 262, Gangnam-daero, Gangnam-gu, Seoul, 06265 Korea  
Tel: +82-2-558-3737, Fax: +82-2-558-5338