Four-level voltage comparison with single comparator in GreenPAK

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Introduction

The SLG46120V is a versatile, programmable, configurable, small and low cost device. To minimize cost and size, the SLG46120V does not include an ADC. For applications that only require a few levels of comparison, we can make a 2-bit ADC, or 4 level comparator using just some of the resources of Dialog's 1.6 x 1.6mm SLG46120V GreenPAK.

Application

An example application is a battery monitor with a state of charge indicator as shown in Figure 1. The 2-bit ADC will determine battery level and light a series of output LEDs. Four lit LEDs indicate a fully charged battery and zero lit LEDs indicate a discharged battery.

A 4.2V battery is interfaced by a PMIC, which creates a linear representation of the battery voltage from 0V to 1V. 1V means the battery is fully charged and 0V means the battery is fully discharged.

This linearized voltage is then fed into the 2-bit ADC, comprised of a 2-bit DAC and the GreenPAK analog comparator. If the 2-bit DAC is greater, the output of the analog comparator is HIGH. After checking all four DAC levels, the GreenPAK will drive the LEDs which indicate battery voltage.

The PMIC, GreenPAK and DAC are powered by an LDO. The LDO is needed to make sure the 2-bit DAC reference voltages are stable.

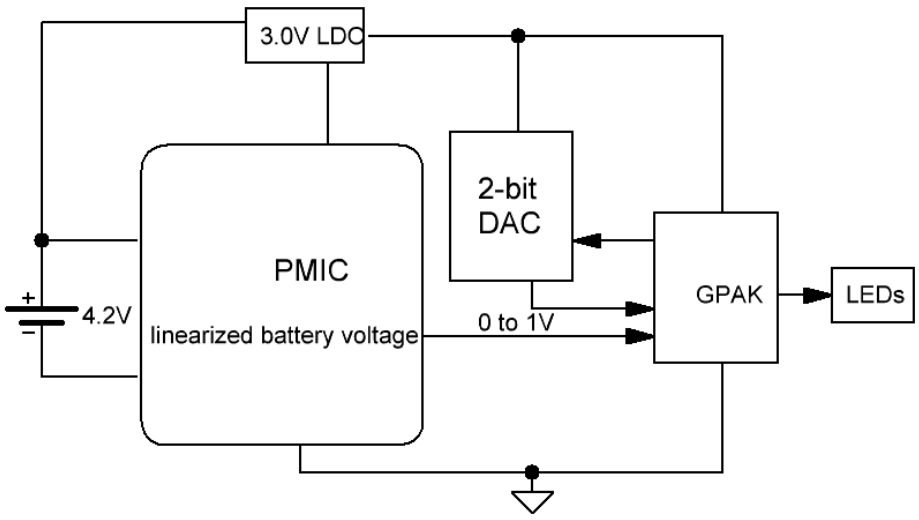

Figure 1. System Level View

GreenPAK Design

An ADC compares a target voltage (linearized battery voltage) to a reference voltage generated by a DAC. In this application, we will use an Analog Comparator to compare the external DAC with the target voltage.

The DAC is a 2-bit resistor network where the resistors are pulled up or down in different combinations to divide the LDO into different voltages. These voltages enter the Analog Comparator on IN+ as the reference voltage.

The pull up and pull down state of the resistors are set by two binary signals: PIN#5 (MSB) and PIN#8 (LSB). The signals are generated by the OSC as shown in Figure 2. The sample rate is OSC/48.

The ACMP output is connected to four DFFs (DFF0, 1, 2, and 3) which latch and hold the ACMP output.

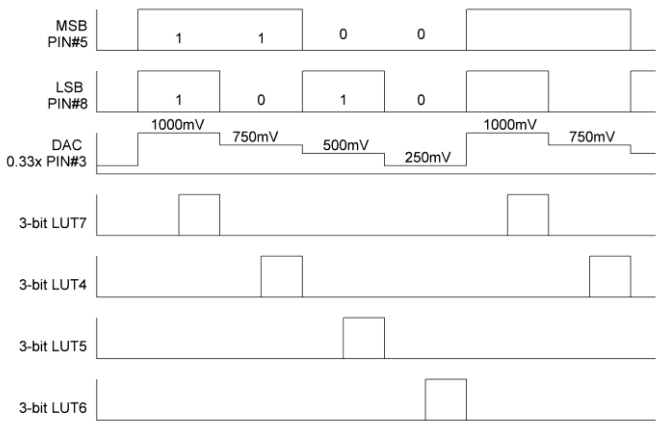

Figure 2. Timing Diagram

The DFFs are clocked one after the other by a time multiplexed signal. This signal is generated by the combinational logic of the MSB, LSB and OSC/12. We use OSC/12 to make sure the ACMP output has stabilized before the DFFs are clocked. Figure 2 shows the time multiplexed clock signals generated by the 3-bit LUTs 4, 5, 6 and 7.

Each DFF drives an LED on PINs 12, 11, 10 and 9. As the battery voltage increases, the number of LEDs lit will also increase.

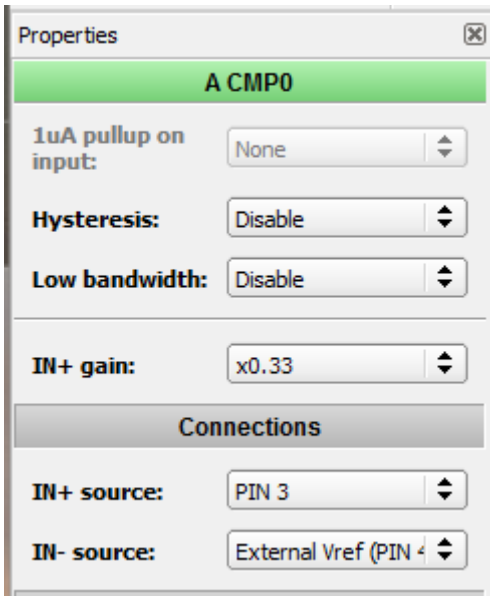

Figure 3. ACMP0 Properties

Analog Comparator Settings

The Analog Comparator IN+ is the DAC reference voltage. An optional IN+ gain can be used to divide the reference down to 1V if it is not already.

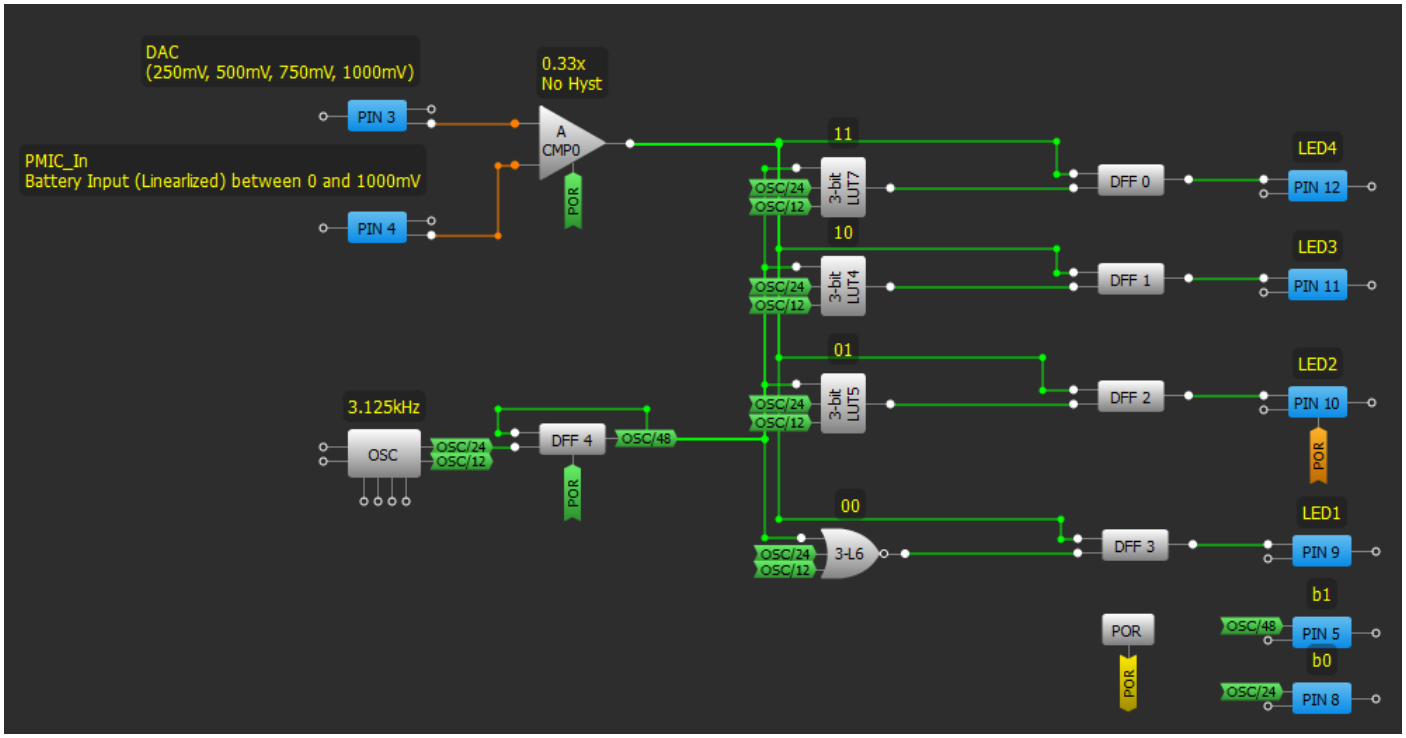

Figure 4. GP Design

The IN- source comes from the PMIC through PIN#4. It is important to note that PIN#4 should not exceed 1.2V. Refer to the datasheet section 5.0 for limits at different VDDs.

Resistor Network Scheme #1

The first resistor network uses a R/2R resistor ladder and pulls two resistors up or down to get four different combinations. If the resistors are selected in accordance to the formulas below, all thresholds will be evenly spaced, and the input impedance is set by R. Since the GPIOs can only drive to GND or VDD, you will need another divider stage to scale the reference to 1V.

In our application where VDD is 3.0V, we are able to use the 0.33x input gain stage of the ACMP to divide 3.0V by three. Otherwise, external voltage dividers must be used.

R1 = 2*R

R2 = 2*R

R3 = R

R4 = 2*R

Input impedance is a parallel combination of R and the gain stage. Refer to datasheet section 13.0. The 0.33x gain has input impedance of 0.75MΩ.

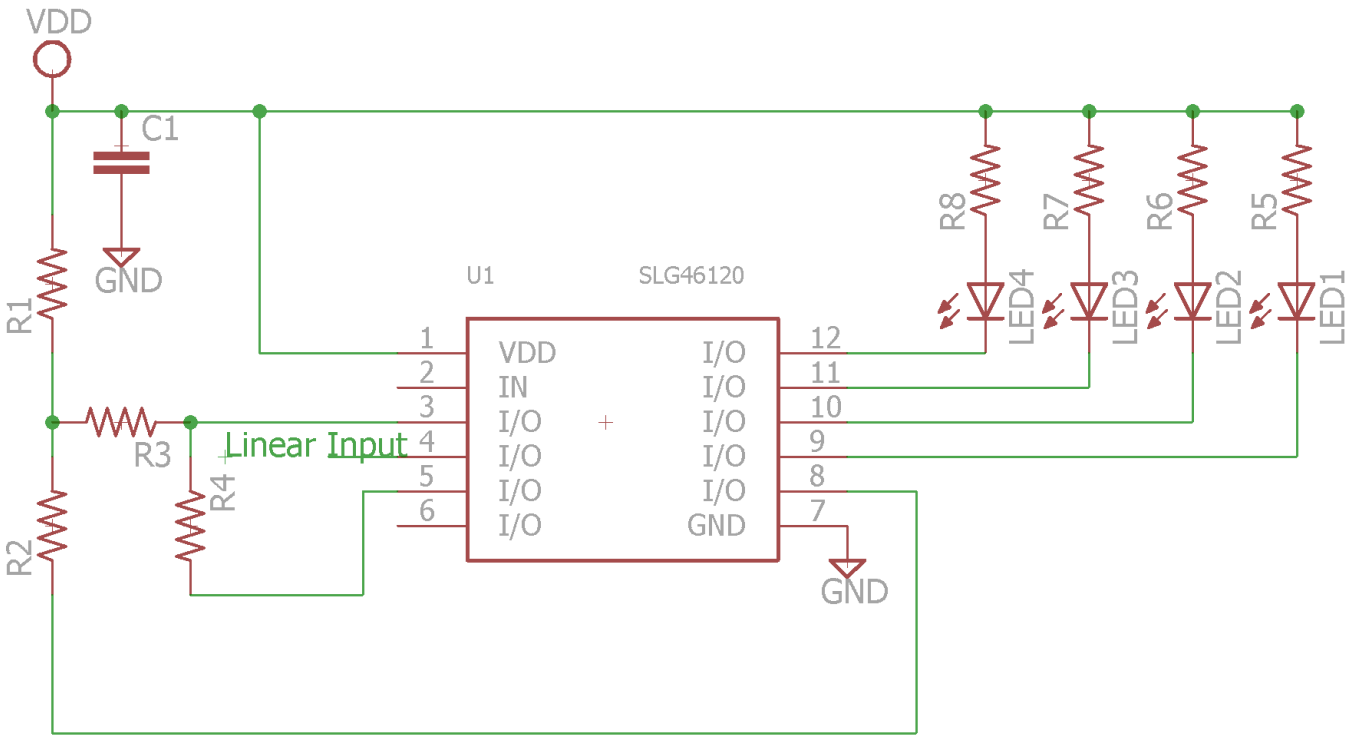

Figure 5. Resistor Network Schematic #1

In Figure 5, the bottom side of resistors R2 and R4 are controlled by PIN#5 (MSB) and PIN#8 (LSB). These two pins represent the binary bits b1 and b0 as described in Table 1. Table 1 lists the expected DAC reference voltage at the PIN#3 input if VDD is 3000mV.

PIN#5 (b1)	PIN#8 (b0)	PIN#3
0	0	750mV
0	1	1500mV
1	0	2250mV
1	1	3000mV

Table 1. b1 and b0 to DAC voltage

If we use the 0.33x internal gain divider of the ACMP, the expected IN+ voltage is listed in Table 2.

PIN#3	0.33x
750mV	250mV
1500mV	500mV
2250mV	750mV
3000mV	1000mV

Table 2. ACMP IN+ voltage

Resistor Network Scheme #2

A second resistor network that can be used is a resistor pull down-only layout. Unlike the previous design, this one only pulls down instead of pulling resistors both up and down. Outputs PIN#5 and PIN#8 are ODNMOS. This automatically keeps the voltages under 1V, eliminating need for a second divider stage. However, due to lack of flexibility, the resulting thresholds are non-linear. See Table 3 and Figure 6 below.

R1 = 10000

R2 = 4348

R3 = 6559

R4 = 2249

The percent error for this set of resistors, if the expected values are 250, 500, 750 and 1000mV, is 14.511%.

See Appendix A for an octave script which finds the resistor values that result in the least percent error from the expected values and desired input impedance. It also includes a weight parameter to add weight to certain values if desired. For this example, all variables hold equal weight. The output of the octave code is shown below where xx, yy and zz are the DAC voltages in volts, entered into Table 3.

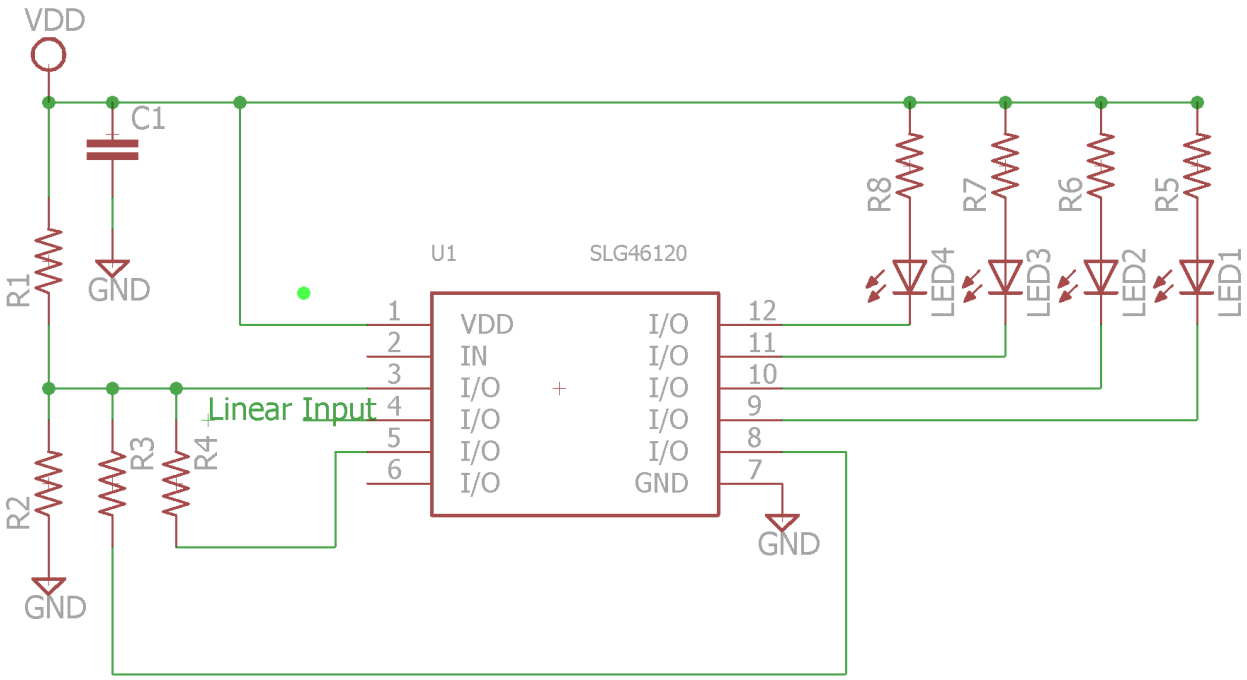

Figure 6. Resistor Network Schematic #2

```
>> adc2bit
xx =  0.68400
yy =  0.42600
zz =  0.35595
R1 =  10000
R2 =  4347.8
R3_val =  6559.3
R4_val =  2249.0
Error_percent =  14.511
input_impedance =  1216.4
```

PIN#5 (b1)	PIN#8 (b0)	PIN#3
0	0	356mV
0	1	426mV
1	0	680mV
1	1	1000mV

Table 3. b1 and b0 to DAC Voltage

Functionality Waveforms

D0 – PIN#12 (LED4)

D1 – PIN#11 (LED3)

D2 – PIN#10 (LED2)

D3 – PIN#9 (LED1)

Channel 1 (yellow) – PIN#3 (DAC)

Channel 3 (magenta) – PIN#4 (PMIC_In)

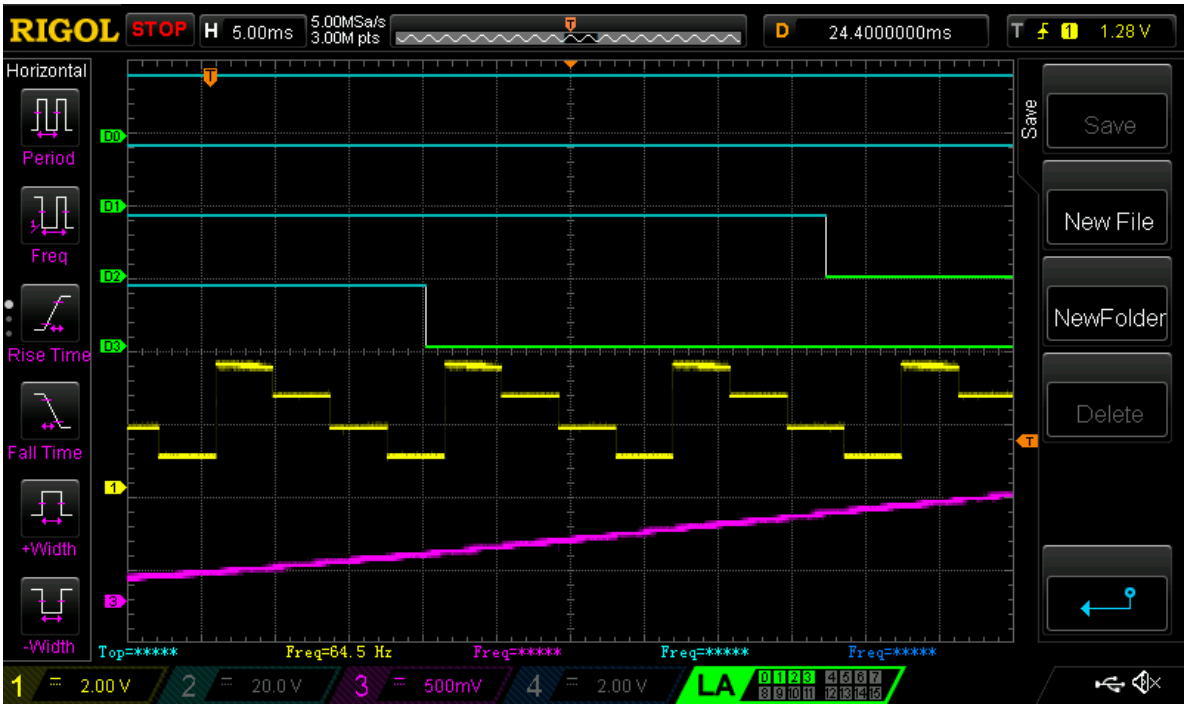

Figure 7. Device Functionality (ZOOM) for Resistor Network Schematic #1

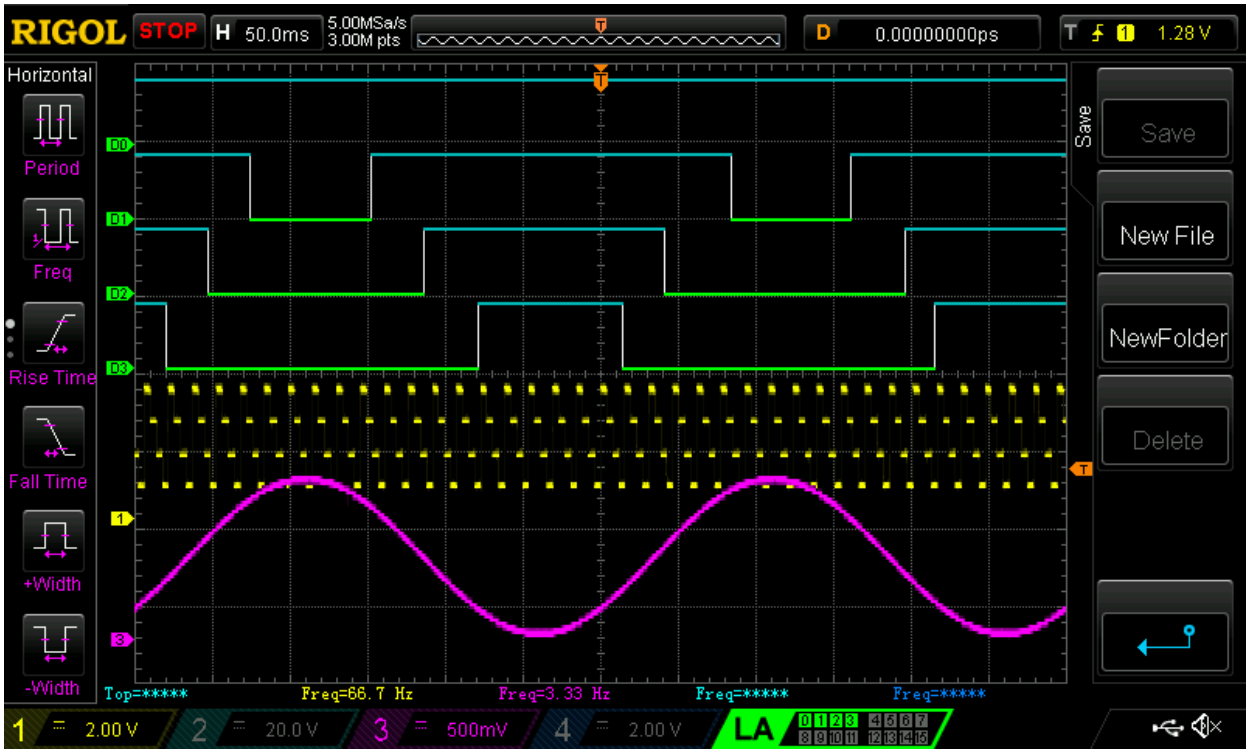

Figure 8. Device Functionality for Resistor Network Schematic #1

Conclusion

The 2-bit ADC, or four level Analog Comparator, works for applications that only need a coarse set of thresholds. With a few external resistors and some control logic, the SLG46120V can do just that. Select the best resistor network that suits the system. If the concern is cost and the internal gain dividers do not suffice, the first resistor schematic leaves you with six external resistor components. In this case, the second resistor schematic may be more cost efficient, requiring only four external resistors but the threshold accuracy decreases.

More than four levels would require another output pin to control the next most significant bit in the binary selection, but there aren't enough outputs to control 8 LEDs. A 3-bit ADC could be implemented in a SLG46721V, which has more GPIO and also does not have a built-in ADC.

Appendix A. Resistor Calculation (Octave)

```
function res_calculator
VDD = 3.3;
%desired input impedance
R = 1000;

%assume
R1 = 10000; %set the top side
resistor
R2 = R1/(VDD-1);
x = 0.5:0.001:0.9;
y = 0.35:0.001:0.65;
col_x = columns(x);
col_y = columns(y);

%weight
a = 0.25;
b = 0.25;
c = 0.25;
d = 1-a-b-c;

for i = 1:col_x
  for j = 1:col_y
    R3(i) = R1*R2./(R2*(VDD./x(i)-
1)-R1);
    R4(j) = R1*R2./(R2*(VDD./y(j)-
1)-R1);
    inputimpedance(i,j) =
par(par(par(R1, R2), R3), R4);

    R234 = par(R2,
par(R3(i),R4(j)));
    z(i,j) = VDD * R234/(R1+R234);

    weighted_error(i,j) =
sqrt(a*(x(i)-0.75).^2 + b*(y(j)-
0.5).^2 + c*(z(i,j)-0.25).^2 +
d*((inputimpedance(i,j)-R)/R).^2);
  end
end

[row,col]= find(weighted_error ==
min(min(weighted_error(:))));

xx = x(row)
yy = y(col)
zz = z(row,col)
R1
R2
R3_val = R3(row)
R4_val = R4(col)
Error_percent = sqrt((x(row)-
0.75).^2+(y(col)-
0.5).^2+(z(row,col)-0.25).^2)*100
input_impedance =
inputimpedance(row,col)

end

function retval = par (R1, R2)
  retval = R1*R2/(R1+R2);
end
```

Output

```
>> adc2bit
xx =  0.68400
yy =  0.42600
zz =  0.35595
R1 =  10000
R2 =  4347.8
R3_val =  6559.3
R4_val =  2249.0
Error_percent =  14.511
input_impedance =  1216.4
```

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