GreenPAK Macro Circuit Design: Adding nSET/ nRESET to DFF's

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Introduction

A D Flip-Flop (DFF) with nRESET or nSET captures the value of the D-input, usually at the rising edge of the clock (CK) input. That captured value becomes the Q output. At other times, the output Q does not change. The nRESET or nSET input is used for resetting the device to its initial state. Both nRESET / nSET input types are active LOW, but nRESET initializes Q output to LOW, while nSET initializes Q HIGH. If a DFF cell had no nRESET / nSET inputs available, this design example shows how to add them.

D Flip-Flop with nRESET circuit design

As shown in Figure 1, DFF nRESET function is implemented using 2-bit LUT4 (AND gate), 3-bit LUT8 and 2-bit LUT5. DFF_INPUT (PIN2) is connected to IN1 of 2-bit LUT4, DFF_CLK (PIN3) to IN1 of 2-bit LUT5 and DFF_nRESET_INPUT (PIN4) to IN2 of 3-bit LUT8.

Also DFF4 has a feedback from its output to IN2 of 3-bit LUT8.

D Flip-Flop with nRESET circuit analysis

Only when DFF_INPUT (PIN2) and DFF_nRESET_INPUT (PIN4) are HIGH, 2-bit LUT4 (AND gate) produces a HIGH signal on its output connected to data input of DFF4 cell. After DFF_CLK (PIN3) goes HIGH, 2-bit LUT5 (XOR gate) will produce a HIGH level signal and switch DFF4 output to a HIGH state.

When DFF_nRESET _INPUT (PIN4) goes LOW, output of 2-bit LUT4 (AND gate) also will go LOW. Meanwhile, 3-bit LUT8, due to feedback from its output to IN0 will form an oscillator. It will send pulses to IN0 of 2-bit LUT5 which in turn will clock the CK input of DFF4 until its output goes LOW. See truth table of 3-bit LUT8 in Figure 3.

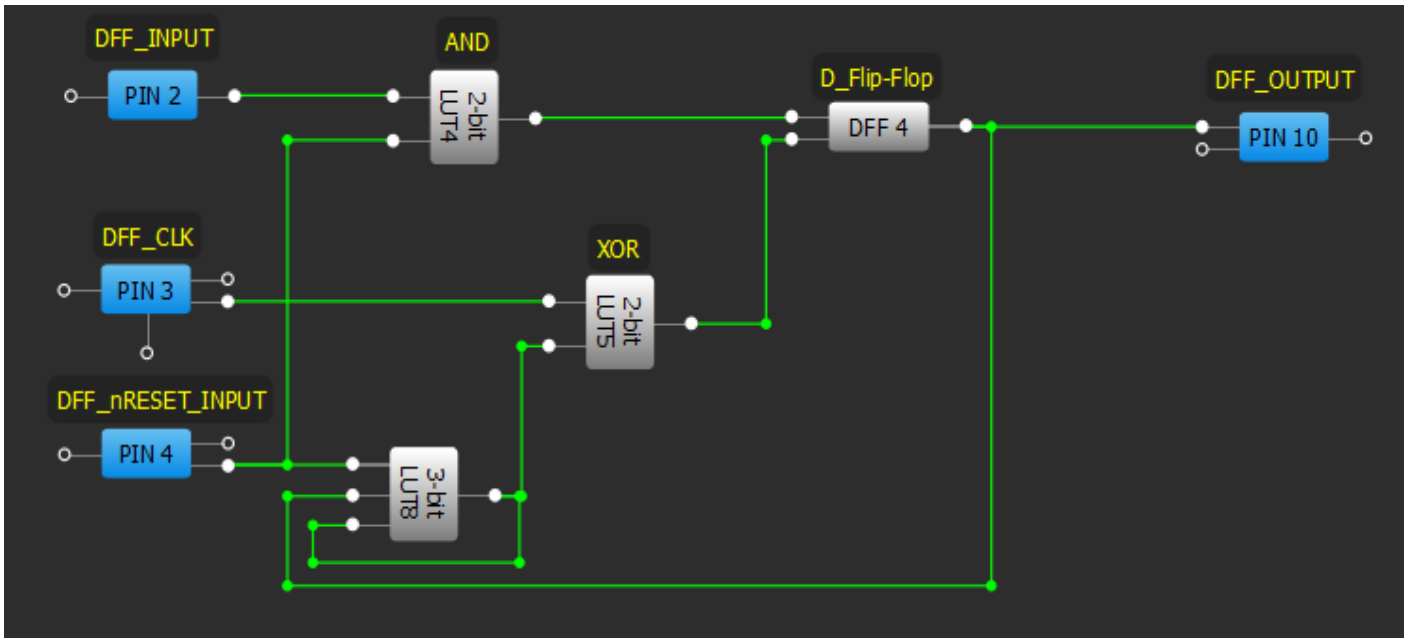


Figure 1. DFF with nRESET circuit design

The nRESET DFF circuit can be simplified if 2-bit LUT5 and 3-bit LUT8 are replaced with their logic equivalent using 4-bit LUT0. See Figure 4. The only difference is that the truth table of 4-bit LUT0 will combine both 2-bit LUT5 and 3-bit LUT8 truth tables. See 4-bit LUT0 truth table in Figure 5.

Functionality waveforms of this nRESET DFF circuit created in GreenPAK3 Designer software are shown in Figure 6.

Channel 1 (yellow/top line) – PIN2 (DFF_INPUT), Channel 2 (light blue/2nd line) – PIN3 (DFF_CLK), Channel 3 (magenta/3rd line) – PIN4 (DFF_nRESET_INPUT)

Channel 4 (blue/4th line) – PIN10 (DFF_OUTPUT).

To create an nSET operation a simple change is needed, see Figure 7.

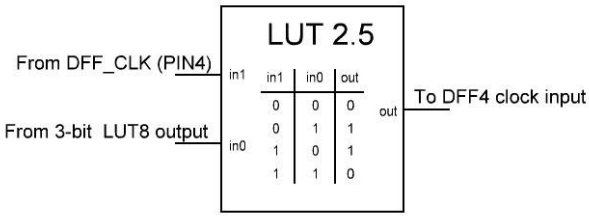


Figure 2. 2-bit LUT5 truth table

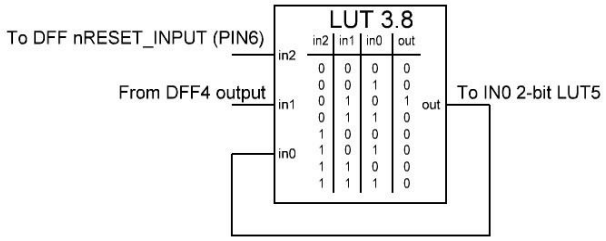


Figure 3. 3-bit LUT8 truth table

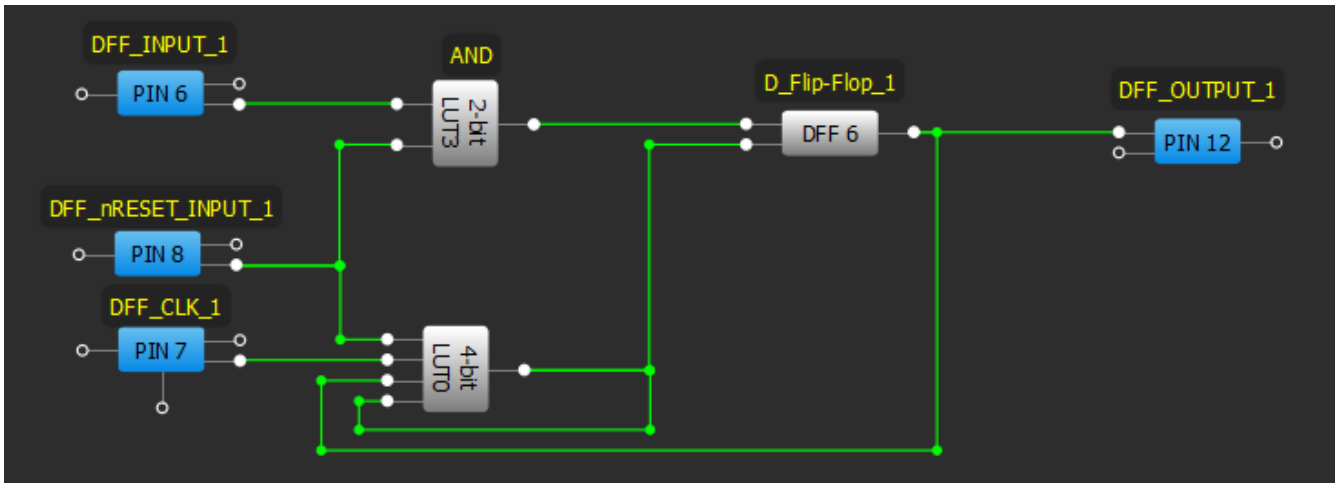
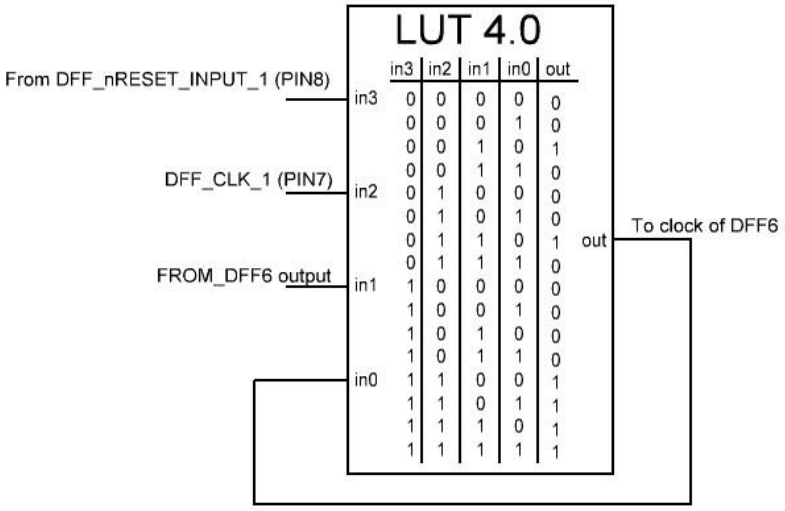


Figure 4. Digital nRESET DFF trigger circuit design simplified



in3	in2	in1	in0	out
0	0	0	0	0
0	0	0	1	0
0	0	1	0	1
0	0	1	1	0
0	1	0	0	0
0	1	0	1	0
0	1	1	0	1
0	1	1	1	0
1	0	0	0	0
1	0	0	1	0
1	0	1	0	0
1	0	1	1	0
1	1	0	0	1
1	1	0	1	1
1	1	1	0	1
1	1	1	1	1

Figure 5. 4-bit LUT0 truth table

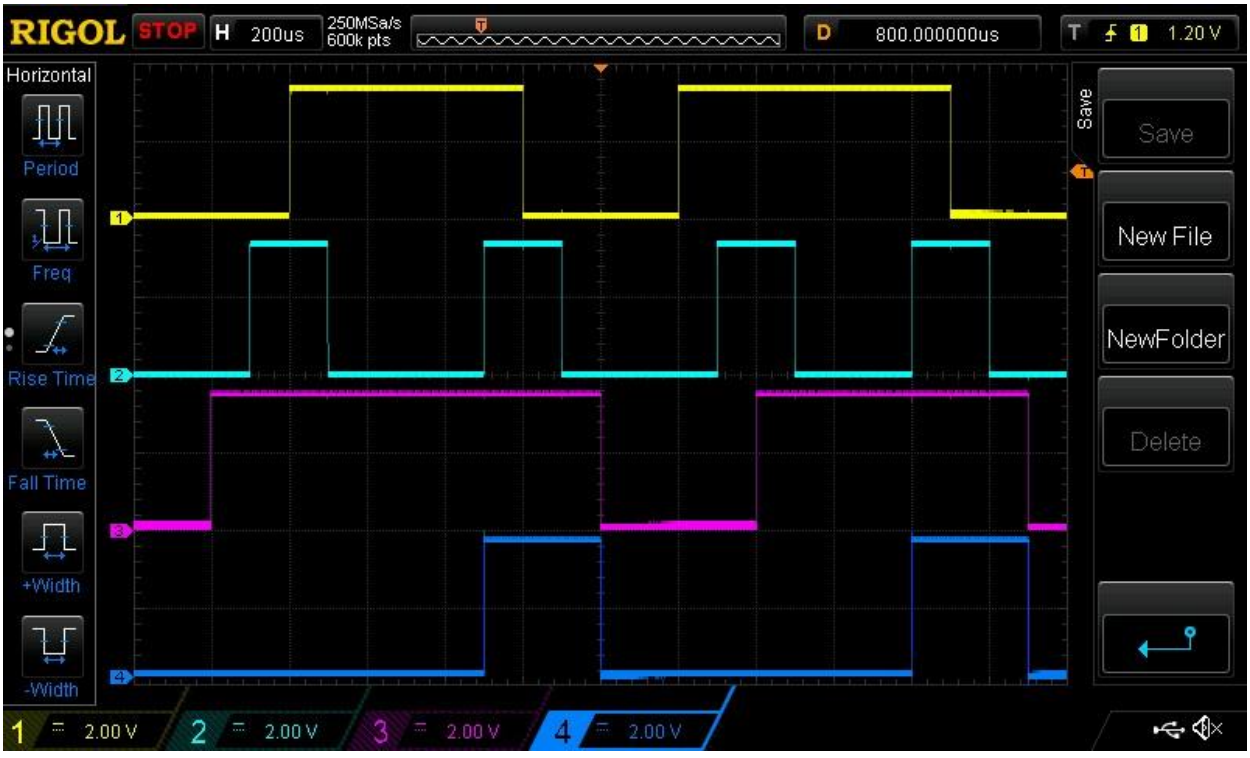


Figure 6. D Flip-Flop with nRESET Function Timing Diagrams

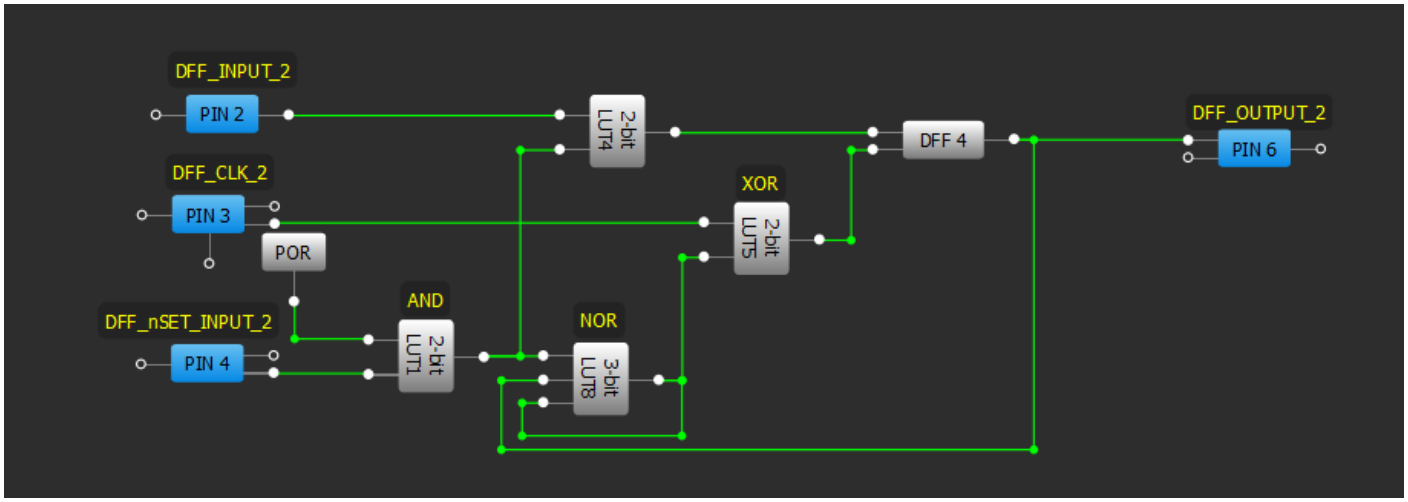
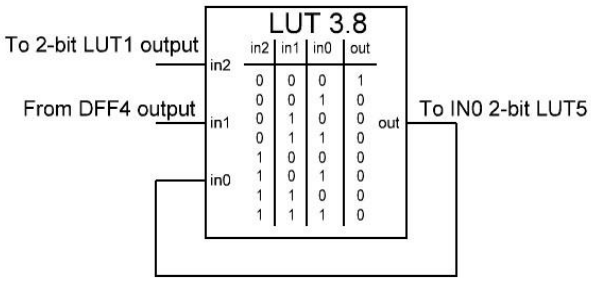


Figure 7. D Flip-Flop with nSET Function Circuit Design

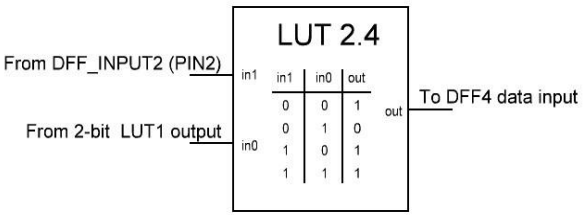
As shown in Figure 7, a 2-bit LUT1 (AND gate) is added. On chip power up, before POR output goes HIGH, 2-bit LUT1 output will be LOW. This initiates an oscillator from 3-bit LUT8 (truth table in Figure 8) which will run until the DFF4 output goes HIGH.

Also, a LOW state from 2-bit LUT1 will propagate to IN0 of 2-bit LUT4 and set its output HIGH (truth table in Figure 9). Thus, the DFF with nSET will initialize HIGH.



in2	in1	in0	out
0	0	0	1
0	0	1	0
0	1	0	0
0	1	1	0
1	0	0	0
1	0	1	0
1	1	0	0
1	1	1	0

Figure 8. 3-bit LUT8 truth table



in1	in0	out
0	0	1
0	1	0
1	0	1
1	1	1

Figure 9. 2-bit LUT4 truth table

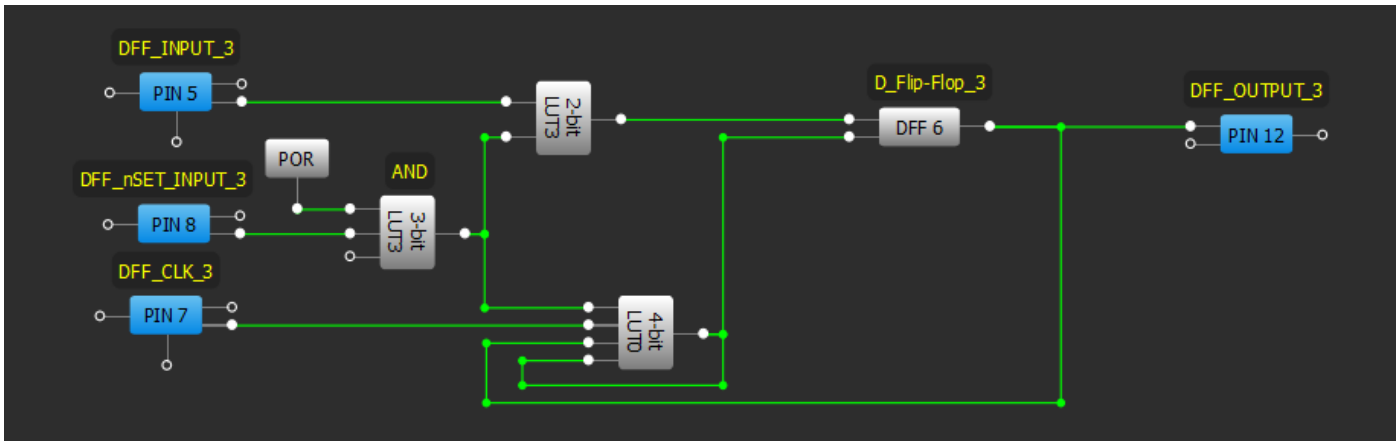


Figure 10. Digital nSET D Flip-Flop Trigger circuit design simplified

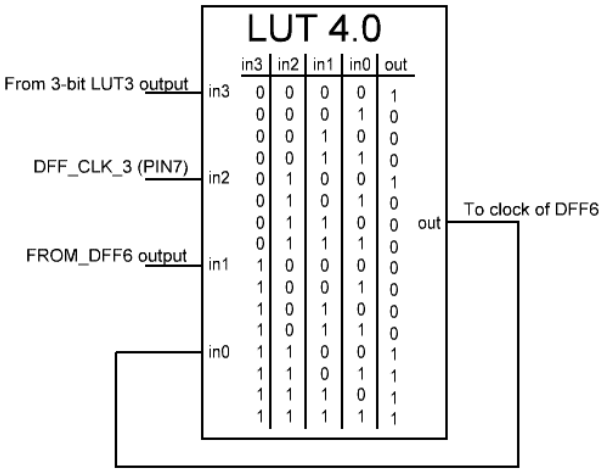
As in the nRESET circuit, this design also could be simplified by replacing 2-bit and 3-bit LUTs with 4-bit LUT0. See Figure 10.

In the simplified version of the design, NOR and XOR functions are combined in 4-bit LUT0. See Figure 7 and truth table in Figure 11.

Functionality waveforms of DFF with nSET is shown in Figure 12. Where:

Channel 1 (yellow/top line) – PIN2 (DFF_INPUT_2), Channel 2 (light blue/2nd line) – PIN3 (DFF_CLK_2), Channel 3 (magenta/3rd line) – PIN4 (DFF_nSET_INPUT_2) and

Channel4 (blue/4th line) – PIN10 (DFF_OUTPUT_2).



in3	in2	in1	in0	out
0	0	0	0	1
0	0	0	1	0
0	0	1	0	0
0	0	1	1	0
0	1	0	0	1
0	1	0	1	0
0	1	1	0	0
0	1	1	1	0
1	0	0	0	0
1	0	0	1	0
1	0	1	0	0
1	0	1	1	0
1	1	0	0	1
1	1	0	1	1
1	1	1	0	1
1	1	1	1	1

Figure 11. 4-bit LUT0 truth table

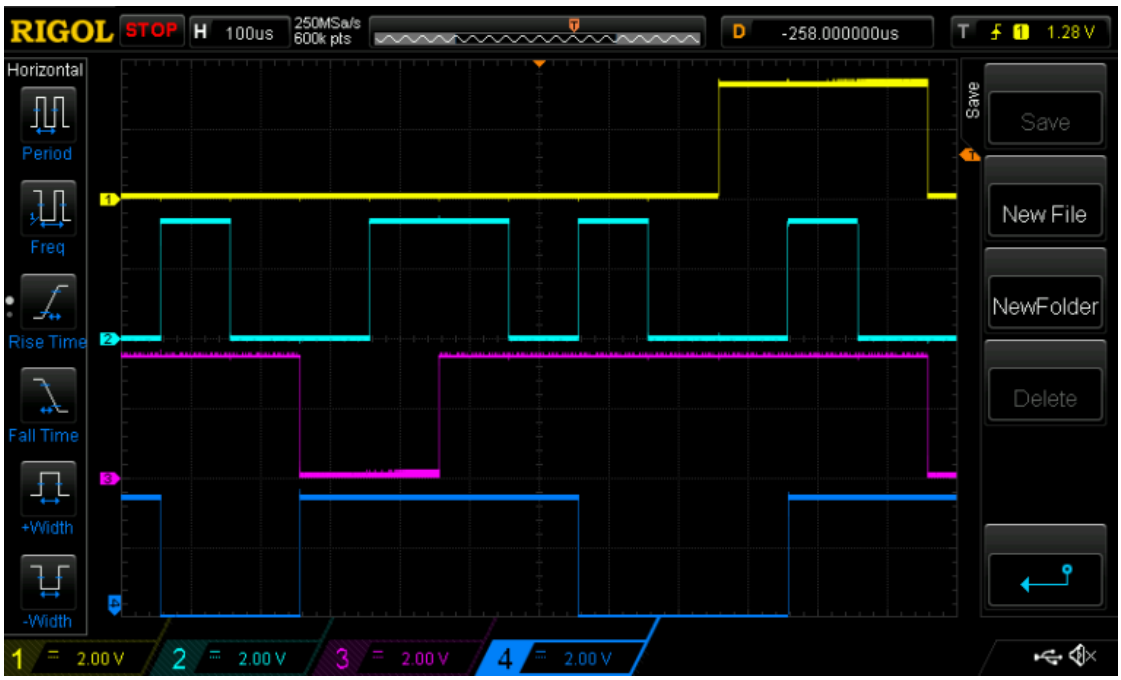


Figure 12. D Flip-Flop with nSET Functionality Waveform

Conclusion

nRESET / nSET DFF function can be very useful in the design of data processing and latching systems. The absence of the nSET/nRESET function of a DFF can be resolved by adding some combinatorial logic cells to the circuit as was shown.

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