RENESAS Tool News

The Simulator Debuggers for the SuperH RISC engine Family and the H8SX, H8S, and H8 Families of MCUs Revised

We have revised the simulator debuggers for the SuperH RISC engine family and the H8SX, H8S, and H8 families* as follows:

- The simulator debugger for the SuperH RISC engine family V.9.07.00
- The simulator debugger for the H8SX, H8S, and H8 families V.5.06.00

*These simulator debuggers are included in the C/C++ compiler packages for the SuperH RISC engine family and the H8SX, H8S, and H8 families.
When you install either of these compiler packages, the simulator debugger included in it is automatically installed in the development environment using High-performance Embedded Workshop.

1. Descriptions of Revision
1.1 Capabilities Improved in Both Simulator Debuggers
  (1) Capability of simulating peripheral functions
     In the peripheral function simulation module, the vector numbers and
     the bit positions of the interrupt priority register have been
     made variable.
  (2) Tracing capability
     The maximum recordable capacity of tracing has been extended
     from 32K records to 256K records.
  (3) Event capabilities
    - To the break conditions, the following two have been added:
     Sign inversion: Met if the sign of a value in memory is
       inverted before and after the value is rewritten.
     Differential: Met if the differential between a value
       in memory before it is rewritten and the one after
       rewritten exceeds the specified limit.
    - Information on break conditions have been added to the

information messages dispatched when the program is halted at a break point.

1.2 Capabilities Introduced and Improved in the Simulator Debugger for the the SuperH RISC engine Family

(1) The execution mode has been introduced: If an interrupt is requested, whether simulation is continued or discontinued is selectable when the SH2A-FPU, SH-4A, or SH4AL-DSP simulator is operating.

(2) Two commands have been introduced: These commands set and display the address of the bank control register when the SH2A-FPU simulator is operating.

(3) The method of setting the number of access states has been improved: The number of states for reading to and writing from ROM and RAM can be changed using the Set Memory Map dialog box when SH2A-FPU simulator is operating.

1.3 Problems Fixed

The following two problems have been fixed:

(1) Problem that if the 16-bit Timer Pulse unit (TPU) is made valid, incorrect addresses may be referenced when the H8SX or H8S simulators is operating.

(2) Problem that even if the CCR.UI bit is used as a user bit, it is set to 1 after the TRAPA instruction is executed when the H8SX or H8S simulators is operating.

2. How to Update Your Simulator Debuggers

Free-of-charge online update is available. Update yours using AutoUpdate Utility (available on and after September 7) or download the updater program you want from the corresponding Web site shown below and execute it (these sites will be opened from September 5 on).

(1) The simulator debugger for the SuperH RISC engine family V.9.07.00
   http://www.renesas.com/sh_sim_download

(2) The simulator debugger for the H8SX, H8S, and H8 families V.5.06.00
   http://www.renesas.com/h8_sim_download

3. Notice

If you have not already installed High-performance Embedded Workshop V.4.03.00, you cannot update your simulator debugger to the one described in (1) or (2) above.

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