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# RENESAS TECHNICAL UPDATE

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| Product Category | MPU/MCU | | Document No. | TN-RZ*-A0088A/E | Rev. | 1.00 |
|---|---|---|---|---|---|---|
| Title | RZ/G2H, G2M V1.3, V3.0, G2N and G2E Additional Descriptions for DU | | Information Category | Technical Notification | | |
| Applicable Product | RZ/G Series, 2nd Generation<br>RZ/G2H<br>RZ/G2M V1.3, V3.0<br>RZ/G2N<br>RZ/G2E | Lot No.<br>All lots | Reference Document | RZ/G Series, 2nd Generation<br>User's Manual: Hardware Rev.1.10<br>(R01UH0808EJ0110) | | |

This technical update describes document correction of RZ/G Series, 2nd Generation product.

[Summary]

Additional Descriptions for “RZ/G Series, 2nd Generation User's Manual: Hardware Rev.1.10”.

[Priority level]

Importance: “Normal”

Urgency: “Normal”

[Products]

RZ/G2H.

RZ/G2M V1.3, V3.0

RZ/G2N,

RZ/G2E

[Section number and title]

Section 36. Display Unit (DU)

“This is empty adjustment page to compare next Current (from) and Correction (to) on facing page. “

(By using two pages view of PDF readers this enables previously and prospectively view on odd and even pages.)

[Correction]

1. Section 36. DU, Page 36-22, 36.1.4 Register Description, (d) Display Plane Register Configuration, Alpha blending related registers are added.

Current (from):

**(d) Display Plane Register Configuration**

**Table 36.14 Display Plane Register Configuration (1)**

Base address: DU0/DU1: H'FEB0_0000 (suffix 0) [DU1 is for RZ/G2H, RZ/G2M V1.3, RZ/G2M V3.0, RZ/G2N, RZ/G2E]
DU2/DU3: H'FEB4_0000 (suffix 2) [DU2 is for RZ/G2M V1.3, RZ/G2M V3.0, DU3 is only for RZ/G2H, RZ/G2N]

| Register Name | Abbr. | R/W | Offset Address | Access Size | Bit with Internal Update Function* | Second Generation RZ/G Series Products | | | |
|---|---|---|---|---|---|---|---|---|---|
| | | | | | | RZ/G2H | RZ/G2M V1.3 RZ/G2M V3.0 | RZ/G2N | RZ/G2E |
| Plane 1 mode register m | P1MRm | R/W | H'0100 | 32 | All bits | √ | √ | √ | √ |
| Plane 1 display size X register m | P1DSXRm | R/W | H'0110 | 32 | All bits | √ | √ | √ | √ |
| Plane 1 display size Y register m | P1DSYRm | R/W | H'0114 | 32 | All bits | √ | √ | √ | √ |
| Plane 1 display position X register m | P1DPXRm | R/W | H'0118 | 32 | All bits | √ | √ | √ | √ |
| Plane 1 display position Y register m | P1DPYRm | R/W | H'011C | 32 | All bits | √ | √ | √ | √ |
| Plane 1 display data control 4 register m | P1DDC4Rm | R/W | H'0190 | 32 | All bits | √ | √ | √ | √ |
| Plane 3 mode register m | P3MR0 | R/W | H'0300 | 32 | All bits | √ | √ | √ | √ |
| | P3MR2 | | | | | √ | — | √ | — |
| Plane 3 display size X register m | P3DSXR0 | R/W | H'0310 | 32 | All bits | √ | √ | √ | √ |
| | P3DSXR2 | | | | | √ | — | √ | — |
| Plane 3 display size Y register m | P3DSYR0 | R/W | H'0314 | 32 | All bits | √ | √ | √ | √ |
| | P3DSYR2 | | | | | √ | — | √ | — |
| Plane 3 display position X register m | P3DPXR0 | R/W | H'0318 | 32 | All bits | √ | √ | √ | √ |
| | P3DPXR2 | | | | | √ | — | √ | — |
| Plane 3 display position Y register m | P3DPYR0 | R/W | H'031C | 32 | All bits | √ | √ | √ | √ |
| | P3DPYR2 | | | | | √ | — | √ | — |
| Plane 3 display data control 4 register m | P3DDC4R0 | R/W | H'0390 | 32 | All bits | √ | √ | √ | √ |
| | P3DDC4R2 | | | | | √ | — | √ | — |

Note: * The register available code is excluded. There is no internal update function for the register available code.

Correction (to):

### (d) Display Plane Register Configuration

**Table 36.14 Display Plane Register Configuration (1)**

Base address: DU0/DU1: H'FEB0_0000 (suffix 0) [DU1 is for RZ/G2H, RZ/G2M V1.3, RZ/G2M V3.0, RZ/G2N, RZ/G2E]
DU2/DU3: H'FEB4_0000 (suffix 2) [DU2 is for RZ/G2M V1.3, RZ/G2M V3.0, DU3 is only for RZ/G2H, RZ/G2N]

| | | | | | | Second Generation RZ/G Series Products | | | |
|---|---|---|---|---|---|---|---|---|---|
| **Register Name** | **Abbr.** | **R/W** | **Offset Address** | **Access Size** | **Bit with Internal Update Function*** | **RZ/G2H** | **RZ/G2M V1.3 RZ/G2M V3.0** | **RZ/G2N** | **RZ/G2E** |
| Plane 1 mode register m | P1MRm | R/W | H'0100 | 32 | All bits | √ | √ | √ | √ |
| Plane 1 display size X register m | P1DSXRm | R/W | H'0110 | 32 | All bits | √ | √ | √ | √ |
| Plane 1 display size Y register m | P1DSYRm | R/W | H'0114 | 32 | All bits | √ | √ | √ | √ |
| Plane 1 display position X register m | P1DPXRm | R/W | H'0118 | 32 | All bits | √ | √ | √ | √ |
| Plane 1 display position Y register m | P1DPYRm | R/W | H'011C | 32 | All bits | √ | √ | √ | √ |
| Plane 1 display data control 4 register m | P1DDC4Rm | R/W | H'0190 | 32 | All bits | √ | √ | √ | √ |
| Plane 1 blending ratio register m | P1ALPHAR0 | RW | H'0108 | 32 | All bits | √ | √ | √ | √ |
| Plane 3 mode register m | P3MR0 | R/W | H'0300 | 32 | All bits | √ | √ | √ | √ |
| | P3MR2 | | | | | √ | — | √ | — |
| Plane 3 display size X register m | P3DSXR0 | R/W | H'0310 | 32 | All bits | √ | √ | √ | √ |
| | P3DSXR2 | | | | | √ | — | √ | — |
| Plane 3 display size Y register m | P3DSYR0 | R/W | H'0314 | 32 | All bits | √ | √ | √ | √ |
| | P3DSYR2 | | | | | √ | — | √ | — |
| Plane 3 display position X register m | P3DPXR0 | R/W | H'0318 | 32 | All bits | √ | √ | √ | √ |
| | P3DPXR2 | | | | | √ | — | √ | — |
| Plane 3 display position Y register m | P3DPYR0 | R/W | H'031C | 32 | All bits | √ | √ | √ | √ |
| | P3DPYR2 | | | | | √ | — | √ | — |
| Plane 3 display data control 4 register m | P3DDC4R0 | R/W | H'0390 | 32 | All bits | √ | √ | √ | √ |
| | P3DDC4R2 | | | | | √ | — | √ | — |
| Plane 3 blending ratio register m | P3ALPHAR0 | RW | H'0308 | 32 | All bits | √ | √ | √ | √ |

Note: * The register available code is excluded. There is no internal update function for the register available code.

[Description]

Two of alpha blending related registers are added.

[Reason for Correction]

If enable α blending on the DU, the value of non-disclosed register that is not initialized by reset may refer to the other Plane as α value and unexpected image is output. Disclosed the above registers for using with software workaround.

[Correction]

2. Section 36. DU, Page 36-23, 36.1.4 Register Description, (d) Display Plane Register Configuration, Alpha blending related registers are added.

Current (from):

**Display Plane Register Configuration (2)**

| Register Name | Abbr. | Power-on Reset | Second Generation RZ/G Series Products | | | |
|---|---|---|---|---|---|---|
| | | | RZ/G2H | RZ/G2M V1.3 RZ/G2M V3.0 | RZ/G2N | RZ/G2E |
| Plane 1 mode register m | P1MRm | H'****_**** | √ | √ | √ | √ |
| Plane 1 display size X register m | P1DSXRm | H'****_**** | √ | √ | √ | √ |
| Plane 1 display size Y register m | P1DSYRm | H'****_**** | √ | √ | √ | √ |
| Plane 1 display position X register m | P1DPXRm | H'****_**** | √ | √ | √ | √ |
| Plane 1 display position Y register m | P1DPYRm | H'****_**** | √ | √ | √ | √ |
| Plane 1 display data control 4 register m | P1DDC4Rm | H'****_**** | √ | √ | √ | √ |
| Plane 3 mode register m | P3MR0 | H'****_**** | √ | √ | √ | √ |
| | P3MR2 | | √ | — | √ | — |
| Plane 3 display size X register m | P3DSXR0 | H'****_**** | √ | √ | √ | √ |
| | P3DSXR2 | | √ | — | √ | — |
| Plane 3 display size Y register m | P3DSYR0 | H'****_**** | √ | √ | √ | √ |
| | P3DSYR2 | | √ | — | √ | — |
| Plane 3 display position X register m | P3DPXR0 | H'****_**** | √ | √ | √ | √ |
| | P3DPXR2 | | √ | — | √ | — |
| Plane 3 display position Y register m | P3DPYR0 | H'****_**** | √ | √ | √ | √ |
| | P3DPYR2 | | √ | — | √ | — |
| Plane 3 display data control 4 register m | P3DDC4R0 | H'****_**** | √ | √ | √ | √ |
| | P3DDC4R2 | | √ | — | √ | — |

Correction (to):

**Display Plane Register Configuration (2)**

| Register Name | Abbr. | Power-on Reset | Second Generation RZ/G Series Products | | | |
|---|---|---|---|---|---|---|
| | | | RZ/G2H | RZ/G2M V1.3 RZ/G2M V3.0 | RZ/G2N | RZ/G2E |
| Plane 1 mode register m | P1MRm | H'****_**** | √ | √ | √ | √ |
| Plane 1 display size X register m | P1DSXRm | H'****_**** | √ | √ | √ | √ |
| Plane 1 display size Y register m | P1DSYRm | H'****_**** | √ | √ | √ | √ |
| Plane 1 display position X register m | P1DPXRm | H'****_**** | √ | √ | √ | √ |
| Plane 1 display position Y register m | P1DPYRm | H'****_**** | √ | √ | √ | √ |
| Plane 1 display data control 4 register m | P1DDC4Rm | H'****_**** | √ | √ | √ | √ |
| Plane 1 blending ratio register | P1ALPHAR0 | H'****_**** | √ | √ | √ | √ |
| Plane 3 mode register m | P3MR0 | H'****_**** | √ | √ | √ | √ |
| | P3MR2 | | √ | — | √ | — |
| Plane 3 display size X register m | P3DSXR0 | H'****_**** | √ | √ | √ | √ |
| | P3DSXR2 | | √ | — | √ | — |
| Plane 3 display size Y register m | P3DSYR0 | H'****_**** | √ | √ | √ | √ |
| | P3DSYR2 | | √ | — | √ | — |
| Plane 3 display position X register m | P3DPXR0 | H'****_**** | √ | √ | √ | √ |
| | P3DPXR2 | | √ | — | √ | — |
| Plane 3 display position Y register m | P3DPYR0 | H'****_**** | √ | √ | √ | √ |
| | P3DPYR2 | | √ | — | √ | — |
| Plane 3 display data control 4 register m | P3DDC4R0 | H'****_**** | √ | √ | √ | √ |
| | P3DDC4R2 | | √ | — | √ | — |
| Plane 3 blending ratio register m | P3ALPHAR0 | H'****_**** | √ | √ | √ | √ |

[Description]

Two of alpha blending related registers are added.

[Reason for Correction]

If enable α blending on the DU, the value of non-disclosed register that is not initialized by reset may refer to the other Plane as α value and unexpected image is output. Disclosed the above registers for using with software workaround.

[Correction]

3. Section 36. DU, Page 36-99, 36.2.4 Display Plane Registers, (1) Plane p Mode Register m (PpMRm). Concerning alpha blending setting description added.

Current (from):

| Bit | Bit Name | Initial Value | R/W | Internal Update | Description |
|---|---|---|---|---|---|
| 14 to 12 | PpSPIM | B'000 | R/W | Available | Plane p Super Impose Mode [(DU0/DU1)]<br>B'000: Setting prohibited.<br>B'001: Setting prohibited.<br>B'010: Setting prohibited.<br>B'011: Setting prohibited.<br>B'100: Transparent color processing is not performed for plane p.<br>Plane p is displayed.<br>B'101: α blending of plane p and the lower plane is performed.<br>The transparent color specification for plane p is ignored, and α blending is performed between all the pixels of plane p and the lower plane.<br>B'110: An EOR operation is performed on plane p and the lower plane.<br>The transparent color specification for plane p is ignored, and EOR operation is performed on all the pixels of plane p and the lower plane.<br>B'111: Setting prohibited |
| | | | | | Plane 1 Super Impose Mode [RZ/G2M V1.3, RZ/G2M V3.0(DU2)]<br>B'000: Setting prohibited.<br>B'001: Setting prohibited.<br>B'010: Setting prohibited.<br>B'011: Setting prohibited.<br>B'100: Transparent color processing is not performed for plane 1.<br>Plane 1 is displayed.<br>B'101: Setting prohibited.<br>B'110: Setting prohibited.<br>B'111: Setting prohibited |
| | | | | | Plane 3 Super Impose Mode [RZ/G2H, RZ/G2N(DU3)]<br>B'000: Setting prohibited.<br>B'001: Setting prohibited.<br>B'010: Setting prohibited.<br>B'011: Setting prohibited.<br>B'100: Transparent color processing is not performed for plane 3.<br>Plane 3 is displayed.<br>B'101: Setting prohibited.<br>B'110: Setting prohibited.<br>B'111: Setting prohibited |
| 11 to 2 | — | — | R | — | Reserved<br>The read value is undefined. The write value should always be 0. |

Correction (to):

| Bit | Bit Name | Initial Value | R/W | Internal Update | Description |
|---|---|---|---|---|---|
| 14 to 12 | PpSPIM | B’000 | R/W | Available | Plane p Super Impose Mode [(DU0/DU1)]<br>B’000: Setting prohibited.<br>B’001: Setting prohibited.<br>B’010: Setting prohibited.<br>B’011: Setting prohibited.<br>B’100: Transparent color processing is not performed for plane p.<br>Plane p is displayed.<br>B’101: α blending of plane p and the lower plane is performed.<br>The transparent color specification for plane p is ignored, and α blending is performed between all the pixels of plane p and the lower plane.<br>This setting is prohibited if α blending is not used. When α blending has been set, set the PpBRSL in PpALPHARm to B’00.<br>B’110: An EOR operation is performed on plane p and the lower plane.<br>The transparent color specification for plane p is ignored, and EOR operation is performed on all the pixels of plane p and the lower plane.<br>B’111: Setting prohibited |
| | | | | | Plane 1 Super Impose Mode [RZ/G2M V1.3, RZ/G2M V3.0(DU2)]<br>B’000: Setting prohibited.<br>B’001: Setting prohibited.<br>B’010: Setting prohibited.<br>B’011: Setting prohibited.<br>B’100: Transparent color processing is not performed for plane 1.<br>Plane 1 is displayed.<br>B’101: Setting prohibited.<br>B’110: Setting prohibited.<br>B’111: Setting prohibited |
| | | | | | Plane 3 Super Impose Mode [RZ/G2H, RZ/G2N(DU3)]<br>B’000: Setting prohibited.<br>B’001: Setting prohibited.<br>B’010: Setting prohibited.<br>B’011: Setting prohibited.<br>B’100: Transparent color processing is not performed for plane 3.<br>Plane 3 is displayed.<br>B’101: Setting prohibited.<br>B’110: Setting prohibited.<br>B’111: Setting prohibited |
| 11 to 2 | — | — | R | — | Reserved<br>The read value is undefined. The write value should always be 0. |

[Description]

Add precautions when using alpha blending

[Reason for Correction]

If enable α blending on the DU, the value of non-disclosed register that is not initialized by reset may refer to the other Plane as α value and unexpected image is output. Disclosed the above registers for using with software workaround.

[Correction]

4. Section 36. DU, Page 36-106, 36.2.4 Display Plane Registers, (7) Plane p Blending Ratio Register m (PpALPHARm) register is disclosed.

Current (from):

— (none)

Correction (to):

### (7) Plane p Blending Ratio Register m (PpALPHARm)

| RZ/G2H | RZ/G2M V1.3, RZ/G2M V3.0 | RZ/G2N | RZ/G2E |
|---|---|---|---|
| √ | √ | √ | √ |

Address: DU0/DU1: H 'FEB00#08, DU2/DU3: H'FEB40#08

| Bit: | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — |
| Initial value: | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — |
| R/W: | R | R | R | R | R | R | R | R | R | R | R | R | R | R | R | R |

| Bit: | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | — | — | — | — | — | — | PpBRSL | | — | | | | — | | | |
| Initial value: | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — |
| R/W: | R | R | R | R | R | R | R/W | R/W | R | R | R | R | R | R | R | R |

| Bit | Bit Name | Initial Value | R/W | Internal Update | Description |
|---|---|---|---|---|---|
| 31 to 10 | — | — | R | — | Reserved<br>The read value is undefined. The write value should always be 0. |
| 9, 8 | PpBRSL | — | R/W | Available | Plane p Blending Ratio Select<br>When the PpSPIM bits in PpMRm are set to B'101, set the PpBRSL to B'00<br>00: Bits 31 to 24 of data supplied from VSP is taken to be the alpha ratio.<br>Others: Setting prohibited |
| 7 to 0 | — | — | R | — | Reserved<br>The read value is undefined. The write value should always be 0. |

[Description]

Alpha blending related register description is added.

[Reason for Correction]

If enable α blending on the DU, the value of non-disclosed register that is not initialized by reset may refer to the other Plane as α value and unexpected image is output. Disclosed the above registers for using with software workaround.

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