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RENESAS TECHNICAL UPDATE

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Product Category	MPU/MCU		Document No.	TN-RX*-A0236B/E	Rev.	2.00
Title	RX600 Series, RX700 Series Errata to User's Manual: Hardware Regarding the Realtime Clock (RTC)		Information Category	Technical Notification		
Applicable Product	RX64M Group, RX65N Group, RX651 Group, RX66N Group, RX71M Group, RX72M Group , RX72N Group	Lot No. All	Reference Document	User's Manual: Hardware for applicable products (see the table at the last page)		

This document describes corrections to the "Realtime Clock (RTC)" chapter in User's Manual: Hardware for the applicable products.
Page and section numbers are based on the manual for the RX64M Group. Refer to the table on the last page for the corresponding page and section numbers in the other groups.

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A note is added to the START and CNTMD bits in the table for section 32.2.18, RTC Control Register 2 (RCR2) as follows.

Before correction

32.2.18 RTC Control Register 2 (RCR2)

Address(es): RTC.RCR2 0008 C424h

	b7	b6	b5	b4	b3	b2	b1	b0
	CNTMD	HR24	AADJP	AADJE	RTCOE	ADJ30	RESET	START
Value after reset:	x	x	x	x	0	0	0	x

x: Undefined

Bit	Symbol	Bit Name	Description	R/W
b0	START	Start	0: Prescaler and counter are stopped. 1: Prescaler and counter operate normally.	R/W
b1	RESET	RTC Software Reset	• In writing 0: Writing is invalid. 1: The prescaler and the target registers for RTC software reset*1 are initialized • In reading 0: In normal time operation, or an RTC software reset has completed. 1: During an RTC software reset	R/W
b2	ADJ30	30-Second Adjustment*2	• In writing 0: Writing is invalid. 1: 30-second adjustment is executed. • In reading 0: In normal time operation, or 30-second adjustment has completed. 1: During 30-second adjustment	R/W
b3	RTCOE	RTCOUT Output Enable	0: RTCOUT output disabled. 1: RTCOUT output enabled.	R/W
b4	AADJE	Automatic Adjustment Enable *3, *4	0: Automatic adjustment is disabled. 1: Automatic adjustment is enabled.	R/W
b5	AADJP	Automatic Adjustment Period Select*3, *4	0: The RADJ.ADJ[5:0] setting value is adjusted from the count value of the prescaler every minute (every 32 seconds in binary counter mode). 1: The RADJ.ADJ[5:0] setting value is adjusted from the count value of the prescaler every 10 seconds (every 8 seconds in binary counter mode).	R/W
b6	HR24	Hours Mode*2, *4	0: The RTC operates in 12-hour mode. 1: The RTC operates in 24-hour mode.	R/W
b7	CNTMD	Count Mode Select	0: The calendar count mode. 1: The binary count mode.	R/W

Note 1. R64CNT, RSECAR/BCNT0AR, RMINAR/BCNT1AR, RHRAR/BCNT2AR, RWKAR/BCNT3AR, RDAYAR/BCNT0AER, RMONAR/BCNT1AER, RYRAR/BCNT2AER, RYRAREN/BCNT3AER, RADJ, RTCCRy, RSECCPy/BCNT0CPy, RMINCPy/BCNT1CPy, RHRCPy/BCNT2CPy, RDAYCPy/BCNT3CPy, RMONCPy, RCR2.ADJ30, RCR2.AADJE, RCR2.AADJP

Note 2. This bit is reserved in binary counter mode. The write value should be 0.

Note 3. When the main clock is selected, the setting of this bit is disabled.

Note 4. After writing to this bit, confirm that its value has actually changed before proceeding with further processing.
Refer to section 32.6.5, Notes When Writing to and Reading from Registers for notes on accessing registers.

After correction

32.2.18 RTC Control Register 2 (RCR2)

Address(es): RTC.RCR2 0008 C424h

	b7	b6	b5	b4	b3	b2	b1	b0
	CNTMD	HR24	AADJP	AADJE	RTCOE	ADJ30	RESET	START
Value after reset:	x	x	x	x	0	0	0	x

x: Undefined

Bit	Symbol	Bit Name	Description	R/W
b0	START	Start*4	0: Prescaler and counter are stopped. 1: Prescaler and counter operate normally.	R/W
b1	RESET	RTC Software Reset	• In writing 0: Writing is invalid. 1: The prescaler and the target registers for RTC software reset*1 are initialized. • In reading 0: In normal time operation, or an RTC software reset has completed. 1: During an RTC software reset	R/W
b2	ADJ30	30-Second Adjustment*2	• In writing 0: Writing is invalid. 1: 30-second adjustment is executed. • In reading 0: In normal time operation, or 30-second adjustment has completed. 1: During 30-second adjustment	R/W
b3	RTCOE	RTCOUT Output Enable	0: RTCOUT output disabled. 1: RTCOUT output enabled.	R/W
b4	AADJE	Automatic Adjustment Enable *3, *4	0: Automatic adjustment is disabled. 1: Automatic adjustment is enabled.	R/W
b5	AADJP	Automatic Adjustment Period Select*3, *4	0: The RADJ.ADJ[5:0] setting value is adjusted from the count value of the prescaler every minute (every 32 seconds in binary counter mode). 1: The RADJ.ADJ[5:0] setting value is adjusted from the count value of the prescaler every 10 seconds (every 8 seconds in binary counter mode).	R/W
b6	HR24	Hours Mode*2, *4	0: The RTC operates in 12-hour mode. 1: The RTC operates in 24-hour mode.	R/W
b7	CNTMD	Count Mode Select*4	0: The calendar count mode. 1: The binary count mode.	R/W

Note 1. R64CNT, RSECAR/BCNT0AR, RMINAR/BCNT1AR, RHRAR/BCNT2AR, RWKAR/BCNT3AR, RDAYAR/BCNT0AER, RMONAR/BCNT1AER, RYRAR/BCNT2AER, RYRAREN/BCNT3AER, RADJ, RTCCRy, RSECCPy/BCNT0CPy, RMINCPy/BCNT1CPy, RHRCPy/BCNT2CPy, RDAYCPy/BCNT3CPy, RMONCPy, RCR2.ADJ30, RCR2.AADJE, RCR2.AADJP

Note 2. This bit is reserved in binary counter mode. The write value should be 0.

Note 3. When the main clock is selected, the setting of this bit is disabled.

Note 4. After writing to this bit, confirm that its value has actually changed before proceeding with further processing.
Refer to section 32.6.5, Notes on Writing to and Reading from Registers, regarding changes to the values of the AADJE, AADJP, and HR24 bits.

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Description of the CNTMD bit in section 32.2.18, RTC Control Register 2 (RCR2) is corrected as follows.

Before correction

CNTMD Bit (Count Mode Select)

This bit specifies whether the RTC count mode is operated in calendar count mode or in binary count mode.
When setting the count mode, execute an RTC software reset and start again from the initial settings.
This bit is updated synchronously with the count source, and its value is fixed before the RTC software reset is completed.
For details on initial settings, refer to section 32.3.1, Outline of Initial Settings of Registers after Power On.

After correction

CNTMD Bit (Count Mode Select)

This bit specifies whether the RTC count mode is operated in calendar count mode or in binary count mode.
After setting the count mode, execute an RTC software reset and start again from the initial settings.
The CNTMD bit is updated in synchronization with the count source, so when the value of the CNTMD bit has been changed, check that the value of the bit has actually been updated before applying the RTC software reset. The count mode changes to that which was specified beforehand in the CNTMD bit after the RTC software reset is applied.
For details on initial settings, refer to section 32.3.1, Outline of Initial Settings of Registers after Power On.

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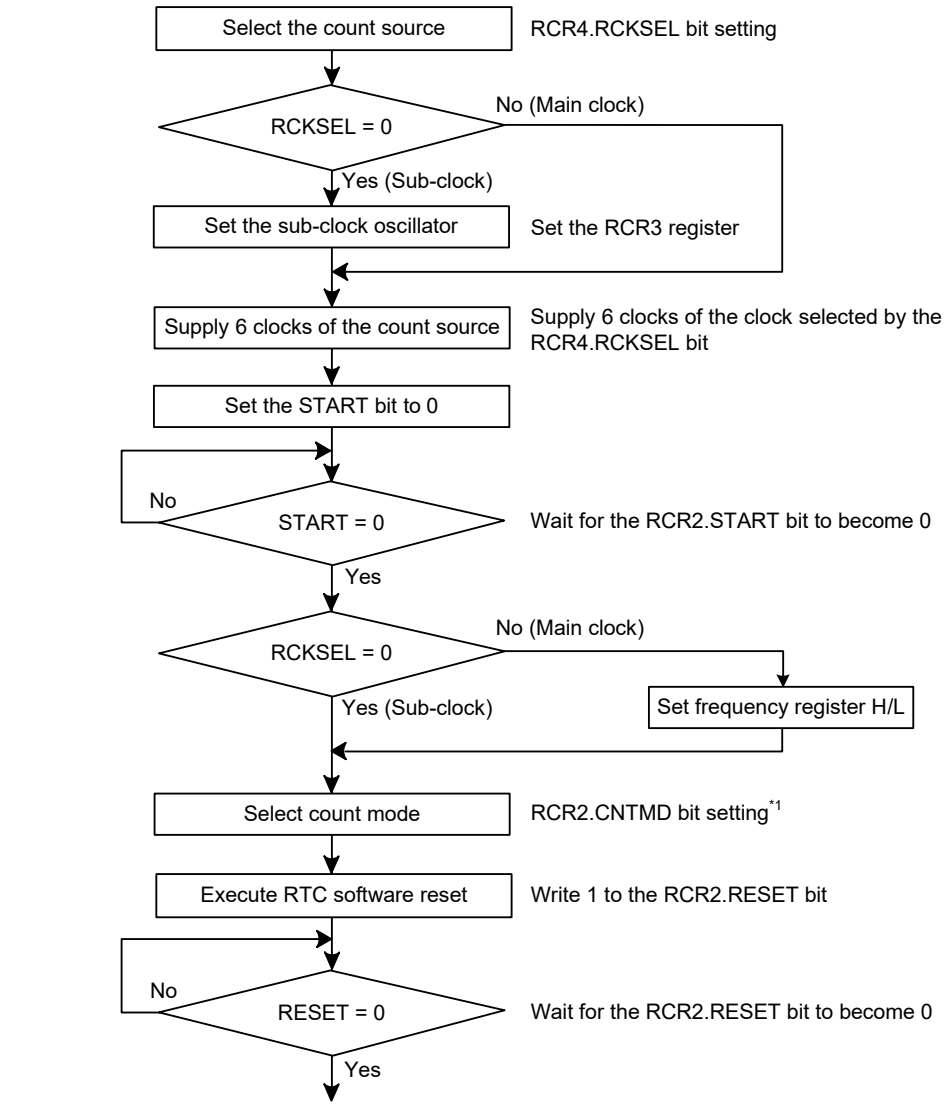
The setting procedure described in Figure 32.3, Clock and Count Mode Setting Procedure is corrected as follows.

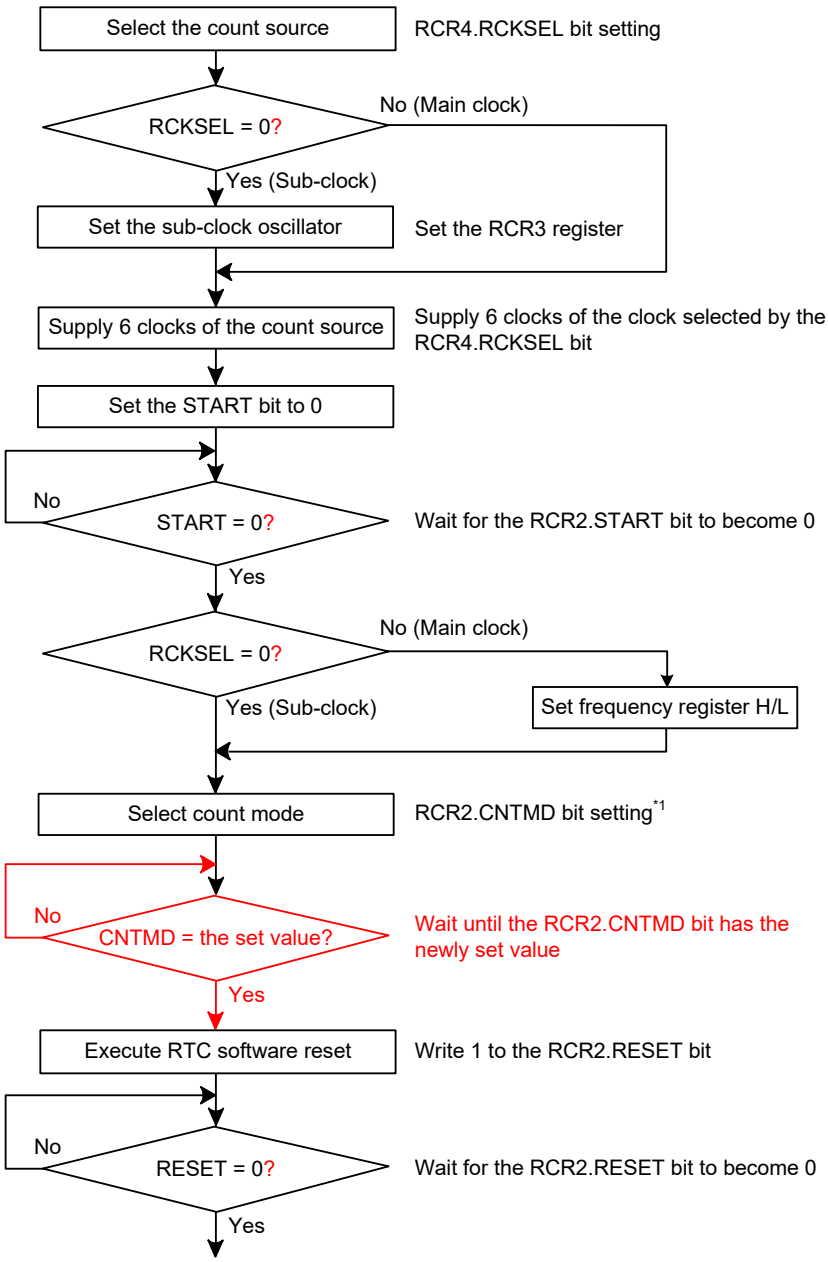
Before correction



Note 1. This step is not necessary if the count mode has been set concurrently with setting the START bit to 0. A value corresponding to the count mode setting must be written to the RCR2.CNTMD bit.

Figure 32.3 Clock and Count Mode Setting Procedure

After correction



Note 1. This step is not necessary if the count mode has been set concurrently with setting the START bit to 0. A value corresponding to the count mode setting must be written to the RCR2.CNTMD bit.

Figure 32.3 Clock and Count Mode Setting Procedure

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The initialization procedure described in Figure 32.14 of section 32.6.7 Initialization Procedure When the Realtime Clock is Not to be Used is corrected as follows.

Before correction

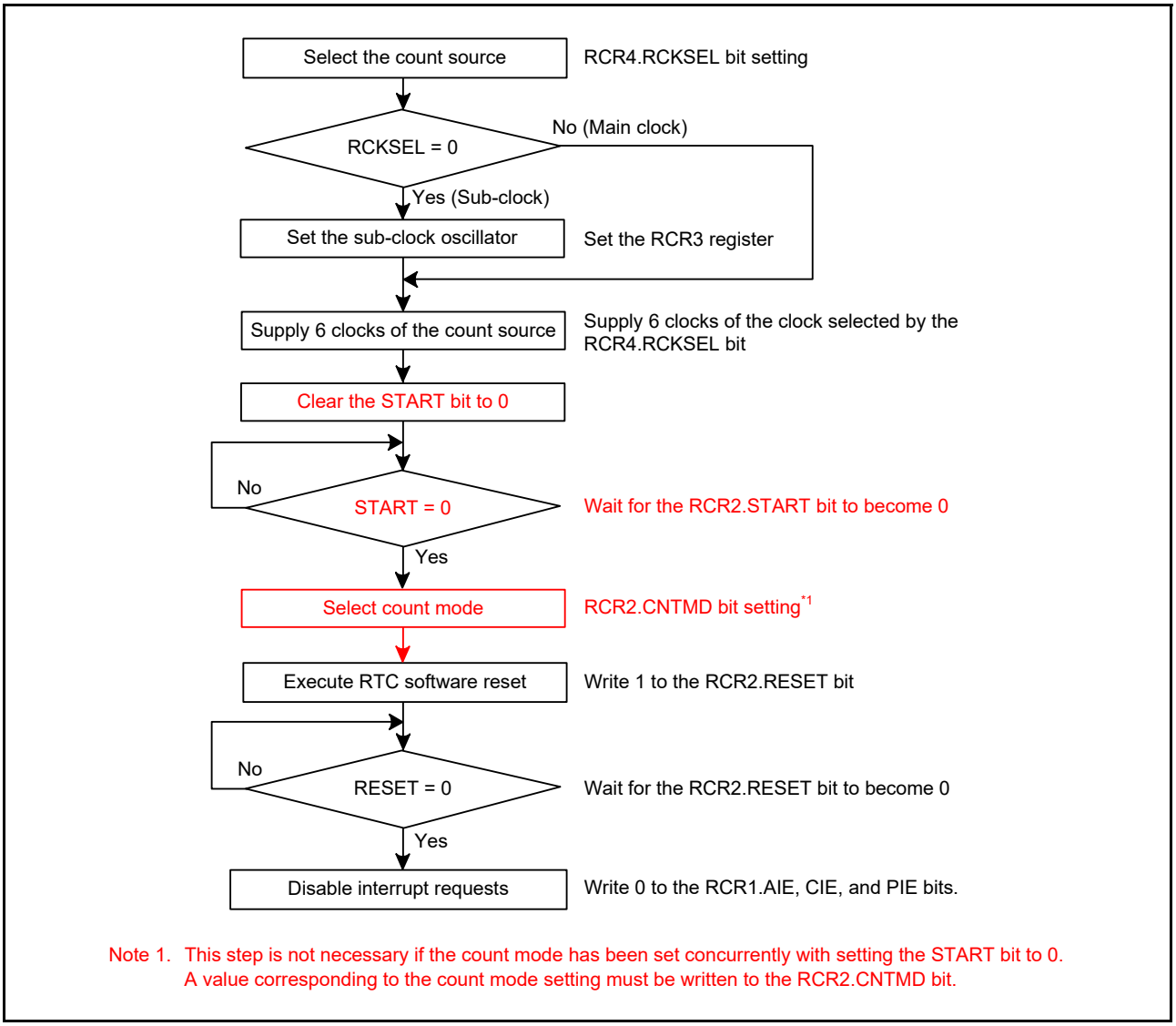

Figure 32.14 Initialization Procedure

After correction

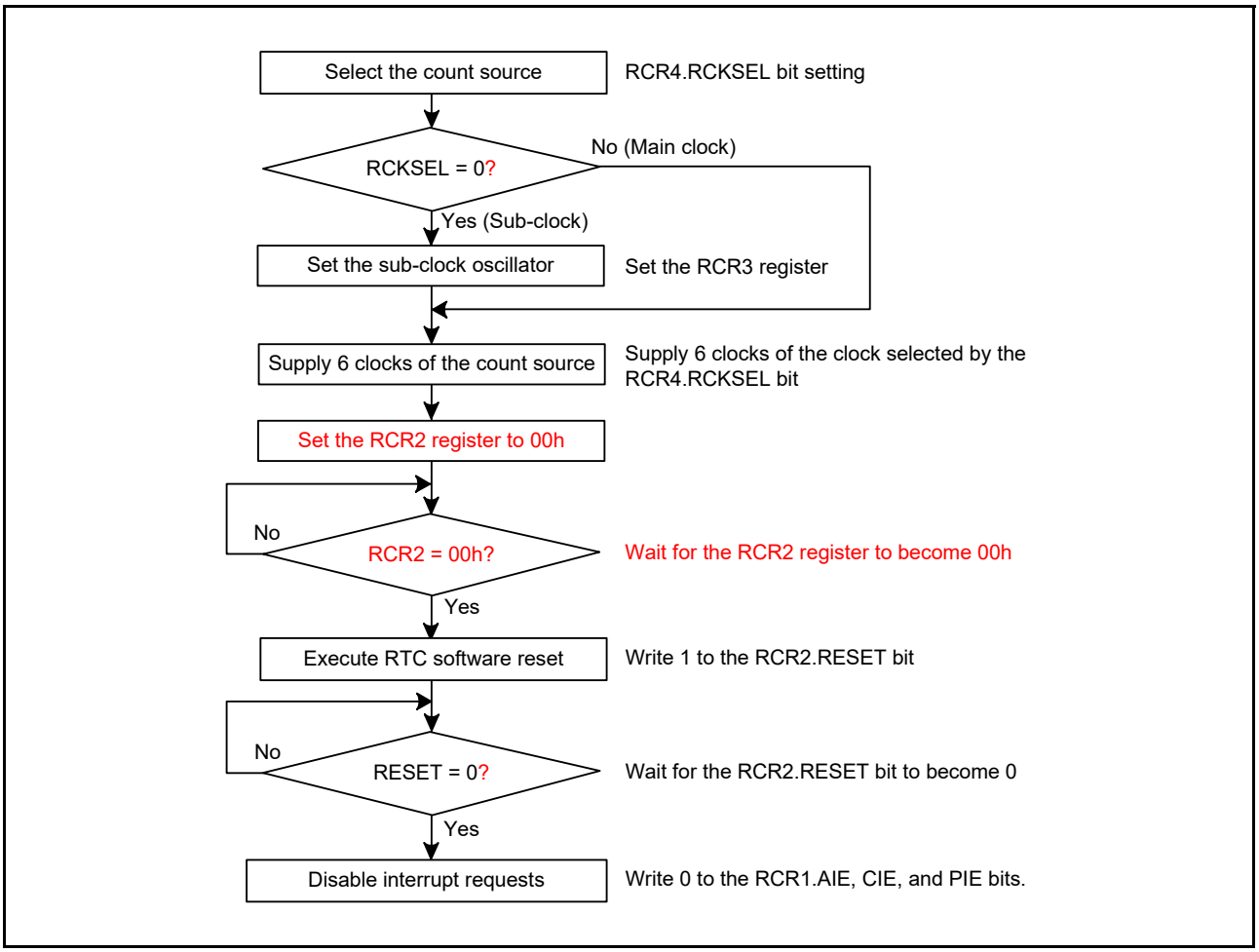

Figure 32.14 Initialization Procedure

Reference Documents

Applicable Products	Manual Title (Document Number)
RX71M Group	RX71M Group User's Manual: Hardware Rev.1.10 (R01UH0493EJ0110)
RX72M Group	RX72M Group User's Manual: Hardware Rev1.00 (R01UH0804EJ0100)
RX72N Group	RX72N Group User's Manual: Hardware Rev1.00 (R01UH0824EJ0100)
RX64M Group	RX64M Group User's Manual: Hardware Rev.1.10 (R01UH0377EJ0110)
RX65N Group, RX651 Group	RX65N Group, RX651 Group User's Manual: Hardware Rev.2.30 (R01UH0590EJ0230)
RX66N Group	RX66N Group User's Manual: Hardware Rev1.00 (R01UH0825EJ0100)

Page Number, Section/Figure/Table Number

Item	Page Number, Section/Figure/Table Number					
	RX71M Group	RX72M Group	RX72N Group	RX64M Group	RX65N Group, RX651 Group	RX66N Group
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Descriptions of the CNTMD bit	Page 1463 32.2.18	Page 1627 33.2.18	Page 1636 33.2.18	Page 1457 32.2.18	Page 1363 31.2.18	Page 1616 33.2.18
Figure of the clock and count mode setting procedure	Page 1477 Figure 32.3	Page 1641 Figure 33.3	Page 1650 Figure 33.3	Page 1471 Figure 32.3	Page 1377 Figure 31.3	Page 1630 Figure 33.3
Figure of the initialization procedure when the realtime clock is not to be used	Page 1491 Figure 32.14	Page 1655 Figure 33.14	Page 1664 Figure 33.14	Page 1485 Figure 32.14	Page 1391 Figure 31.14	Page 1644 Figure 33.14