Date: Apr. 3, 2018

RENESAS TECHNICAL UPDATE

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Product Category	MPU/MCU		Document No.	TN-RL*-A086A/E	Rev.	1.00
Title	Restriction regarding Watchdog timer interrupt		Information Category	Technical Notification		
Applicable Products	RL78/G11, RL78/G12, RL78/G13, RL78/G14, RL78/G1A, RL78/G1C, RL78/G1D, RL78/G1E, RL78/G1F, RL78/G1G, RL78/G1H, RL78/L12, RL78/L13, RL78/L1A, RL78/L1C, RL78/I1A, RL78/I1B, RL78/I1C, RL78/I1D	Lot No. All lot	Reference Document	Latest user's Manual of applicable products		

The restriction below applies to the watchdog timer in the above mentioned Applicable Products.

1. Restriction

Condition:

The restriction on applies to the following settings:

- The overflow time of the watchdog timer is set to $2^{13}/f_{IL}$, $2^{14}/f_{IL}$, or $2^{16}/f_{IL}$
- The watchdog timer interval interrupt is used.
- When “ACH” is written to the WDTE register (FFFABH) under conditions of greater than or equal to 75% of the overflow time.
- User option byte (000C0H) is following settings

7	6	5	4	3	2	1	0
WDTINIT	WINDOW1	WINDOW0	WDTON	WDCS2	WDCS1	WDCS0	WDSTBYON

WDTINIT	Use of interval interrupt of watchdog timer
1	Interval interrupt is generated when 75% + 1/2 f_{IL} of the overflow time is reached.

WDTON	Operation control of watchdog timer counter
1	Counter operation enabled (counting started after reset)

WDCS2	WDCS1	WDCS0	Watchdog timer overflow time
1	0	1	$2^{13}/f_{IL}$ (474.89 ms)
1	1	0	$2^{14}/f_{IL}$ (949.79 ms)
1	1	1	$2^{16}/f_{IL}$ (3799.18 ms)

Settings other than the above do not apply to the restriction.

Description:

After clearing the watchdog timer, the watchdog timer interval interrupt (INTWDTI) may be unintentionally generated after one clock of the watchdog timer elapses.

2. Workaround

Perform the procedure below to reset the watchdog timer counter.

(1) Set the WDTIMK bit in interrupt mask flag register 0 (MK0L) to 1 before clearing the counter of the watchdog timer.
(2) Clear the counter of the watchdog timer.
(3) Wait at least 80 µs.
(4) Clear the WDTIIF bit in interrupt request flag register 0 (IF0L) to 0.
(5) Clear the WDTIMK bit in interrupt mask flag register 0 (MK0L) to 0.

3. Modification plan

We are handling this countermeasure as a restriction on usage.

We will add a precautionary note to the next revision of the user's manual.

4. Applicable product name

Table 1 shows product group and part numbers of applicable product.

Table 1. Product group and part numbers of applicable product

Product group	Part numbers
RL78/G11	R5F105xxx
RL78/G12	R5F102xxx, R5F103xxx
RL78/G13	R5F100xxx, R5F101xxx
RL78/G14	R5F104xxx
RL78/G1A	R5F10Exxx
RL78/G1C	R5F10Jxxx, R5F10Kxxx
RL78/G1D	R5F11Axxx
RL78/G1E	R5F10Fxxx
RL78/G1F	R5F11Bxxx
RL78/G1G	R5F11Exxx
RL78/G1H	R5F11Fxxx
RL78/L12	R5F10Rxxx
RL78/L13	R5F10Wxxx
RL78/L1A	R5F11Mxxx
RL78/L1C	R5F110xxx, R5F111xxx
RL78/I1A	R5F107xxx
RL78/I1B	R5F10Mxxx
RL78/I1C	R5F10Nxxx
RL78/I1D	R5F117xxx

End