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RENESAS TECHNICAL UPDATE

TOYOSU FORESIA, 3-2-24, Toyosu, Koto-ku, Tokyo 135-0061, Japan
Renesas Electronics Corporation

Product Category	MPU/MCU		Document No.	TN-RX*-A0256A/E	Rev.	1.00
Title	Point to Note regarding the Initial Settings of the Sub-Clock		Information Category	Technical Notification		
Applicable Product	RX64M Group, RX71M Group	Lot No. All	Reference Document	RX64M Group User's Manual: Hardware Rev.1.10 (R01UH0377EJ0110) RX71M Group User's Manual: Hardware Rev.1.10 (R01UH0493EJ0110)		

This document describes a point to note regarding the procedure of stopping oscillation by the sub-clock oscillator while its initial setting is being made following the power being turned on.

1. Point to Note

The CPU may hang so that execution of the subsequent programs does not proceed when the sub-clock oscillator is in use. The condition for this is 1 being written to the SOSCCR.SOSTP bit after the counter of the oscillation stabilization wait circuit has overflowed, which takes approximately two seconds, since release from the reset state following the power being turned on.

2. Cause of this Effect

The load capacitance (CL) of the crystal does not match the drive capacity of the sub-clock oscillator, so oscillation by the sub-clock becomes unstable. This prevents updating of the internal state of the sub-clock oscillator.
An effect of this is that the cycle of writing to the SOSCCR register is not completed. Since the address range where the SOSCCR register is located does not lead to a bus error in the case of a timeout, the CPU hangs.

3. Conditions for this Effect

The CPU will hang when all of the following conditions are met.

(1) The drive capacity (specified in the RCR3.RTCDV[2:0] bits) of the sub-clock oscillator on release from the reset state is not sufficient for the crystal's CL.

(2) The sub-clock is oscillating after release from the reset state, but the oscillation stops before the counter of the oscillation stabilization wait circuit overflows, that is, before the OSCOVFSR.SOOVF flag becomes 1.

(3) The SOSCCR.SOSTP bit is set to 1 after the counter of the oscillation stabilization wait circuit has overflowed.

4. Workaround

You can work around this problem by taking either measure A or B below.

A. Set the SOSCCR.SOSTP bit to 1 before the OSCOVFSR.SOOVF flag becomes 1.

B. Set the SOSCCR.SOSTP bit to 1 after having rewritten the RCR3.RTCDV[2:0] bits according to the following procedure.

(1) Set the RCR4.RCKSEL bit to 0 to select the sub-clock oscillator.

(2) Set the RCR3.RTCEN bit to 0 to stop the sub-clock oscillator and set the RCR3.RTCDV[2:0] bits.

(3) Confirm that the RCR3.RTCEN bit is 0 and the RCR3.RTCDV[2:0] bits have changed to the set value.

5. Time until the SOSCCR.SOSTP Bit is Set to 1 by Using Our Libraries

We have confirmed that using our libraries for the RX64M group products ensures that 1 is written to the SOSCCR.SOSTP bit within two seconds following release from the reset state. The following table shows the times from release from the reset state until the SOSCCR.SOSTP bit is set to 1 when using the libraries prepared for the RX64M group products.

Library	Time until the SOSTP bit is set to 1	Order of Clock Setting	Reference Document
Initial settings example	2.6 ms*1	Oscillation is started in the order sub-clock, main clock, and then HOCO.	R01AN1918EJ (https://www.renesas.com/document/apn/rx64m-group-initial-settings-example)
BSP FIT module	12.9 ms*1	Oscillation is started in the order HOCO, main clock, and then sub-clock.	R01AN1685EJ (https://www.renesas.com/document/apn/rx-family-board-support-package-module-using-firmware-integration-technology)

Note 1. Add 4.6 ms to this value when the power-on reset function (POR) is in use.