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RENESAS TECHNICAL UPDATE

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Product Category	MPU/MCU		Document No.	TN-RX*-A124A/E	Rev.	1.00
Title	Notes on using the 12-Bit A/D Converter (S12ADC)		Information Category	Technical Notification		
Applicable Product	RX64M Group	Lot No. All lots	Reference Document	RX64M Group User's Manual: Hardware Rev.1.00 (R01UH0377EJ0100)		

We have identified some restrictions on usage of 12-Bit A/D Converter (S12ADC) in group scan mode when group A is given priority and extended operation in double trigger mode. The following describes the usage limitations and the corrections in the manual.

■Usage Limitations

1) Group scan mode when group A is given priority

At the time of the "ADGSPCR.GBRSCN = 1", please make peripheral Module Clock B (PCLKB) and A/D conversion clock ADCLK (Unit0：PCLKC、Unit1：PCLKD) the same frequency.

When the limitation mentioned above does not keep, the following problems may occur.

Though A/D conversion movement of Group B completes it and produces S12GBADI interrupt request when there is trigger input of Group A in a timing of the A/D conversion movement end of Group B, A/D conversion of Group B may work at the time of the A/D conversion end of Group A again.

If a group-A trigger is input during A/D conversion for group B, though A/D conversion movement of Group B is completed and produces S12GBADI interrupt request, A/D conversion of Group B may work at the time of the A/D conversion end of Group A again.

2) A/D Conversion in Extended Double Trigger Mode

Using A/D Conversion in Extended Double Trigger Mode, when A/D conversion is stopped by ADCSR.ADST bit set to 0, S12ADI interrupt is occurred, but data may not be stored away by A/D Data Duplication Register A and A/D Data Duplication Register B (ADDBLDRA,ADDBLDRB).

When A/D conversion is stopped by ADCSR.ADST bit set to 0, please do in the following procedures.

1) To disable trigger inputs, set the ADSTRGR register to 3F3Fh.
2) Set the ADCSR.ADIE bit to 0, and the ADCSR.GBADIE bit to 0 to disable A/D conversion end interrupt. When the A/D conversion end event in ELC is used, set the event link setting register (ELSR) using the scan end event to 0.
3) Set the ADCSR.ADST bit to 0 to perform software clear operation. Stop A/D conversion.

■Corrections in the Manual

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The description of the A/D Group Scan Priority Control Register (ADGSPCR) has been changed as follows.

Bit	Symbol	Bit Name	Description	R/W
b0	PGS	Group-A Priority Control Setting*1	0: Operation is without group A priority control 1: Operation is with group A priority control	R/W
b1	GBRSCN	Group B Restart Setting*2	(Enabled only when PGS = 1. Reserved when PGS = 0.) 0: Scanning for group B is not restarted after having been discontinued due to group A priority control. 1: Scanning for group B is restarted after having been discontinued due to group A priority control.	R/W
b14 to b2	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b15	GBRP	Group B Single Scan Continuous Start*3	(Enabled only when PGS = 1. Reserved when PGS = 0.) 0: Single scan for group B is not continuously activated. 1: Single scan for group B is continuously activated	R/W

Note 1. When the PGS bit is to be set to 1, the ADCSR.ADCS[1:0] bits must be set to 01b (group scan mode). If the bits are set to any other values, proper operation is not guaranteed.

Note 2. When the GBRSCN bit has been set to 1, the frequency division ratio of peripheral module clock PCLKB to A/D conversion clock ADCLK should be set to 1:1.

Note 3. When the GBRP bit has been set to 1, single scan is performed continuously for group B regardless of the setting of the GBRSCN bit.

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The description of Figure 57.41 Procedures for Clear Operation by Software through the ADCSR.ADST Bit has been changed as follows.