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RENESAS TECHNICAL UPDATE

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Product Category	MPU/MCU		Document No.	TN-RL*-A057A/E	Rev.	1.00
Title	The limitation regarding “Clocked communication function with SPI function” in Serial Array Unit (SAU)		Information Category	Technical Notification		
Applicable Product	RL78/F13, F14 series	Lot No. -	Reference Document	Latest user’s manual of applicable product		

Precaution described below is added to the following products in the User’s Manual.
These contents will be reflected at the next time of the user’s manual revision for each applicable products.

1. Details

As for SAU use, when the slave transmission/reception function is used in “Clocked communication function that uses three lines (SCK, SI, SO) with SPI function” mode, the transmission/reception for 1 bit behave illegally before the shift clock is supplied from SCKp pin depending on asset timing of SSImn (slave select) pin.

Note : m, n, please fit the following to the applicable product groups on this document.

Group1:m,n=1,0 Group2:m,n=0,0

2. Conditions

It occurs when it corresponds to all of following conditions.

1. Slave transmission/reception function is used in “Clocked communication function that uses three lines (SCK, SI, SO) with SPI function” mode.
2. SSImn pin is set to enable (SSEmn=1) in Serial slave select function enable register m.
3. The shift clock phase is specified as "forward"(CKPmn=0) in Serial communication operation setting register mn (SCRmn)

3. Countermeasures

Please correspond with either of the following countermeasures.

- Please use shift clock phase as “reverse” (CKPmn = 1) by setting of Serial communication operation setting register mn (SCRmn).
- Please use the communication function without SSImn pin (SSEmn = 0) by setting of Serial slave select function enable register m (SSEmn).
  -> Polling the SSI signal by general purpose port, and start the communication by software
  -> Accept SSI signal by external interrupt pin, and start the communication by software.

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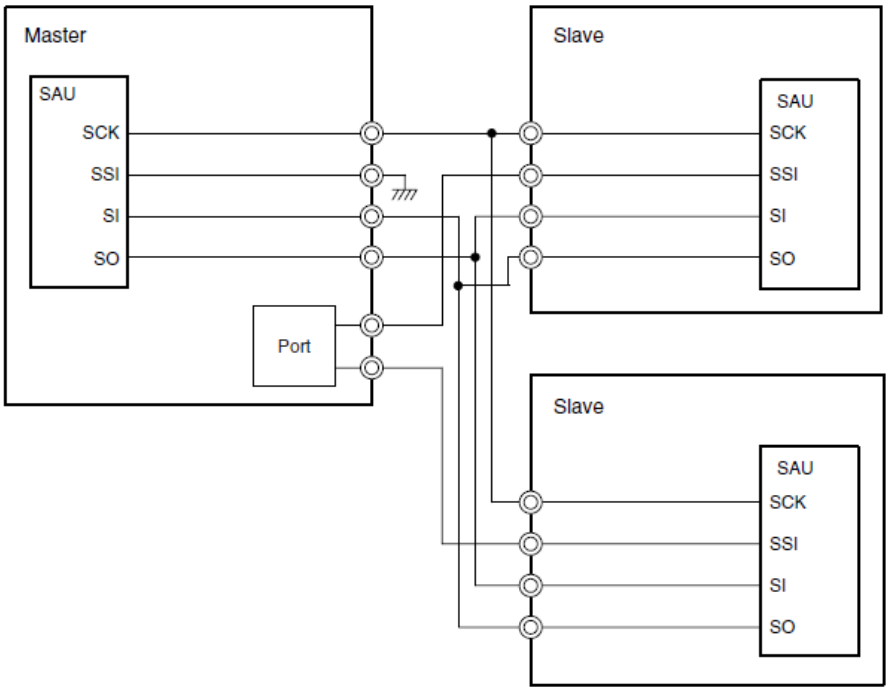
4. Revised the contents of the User's Manual

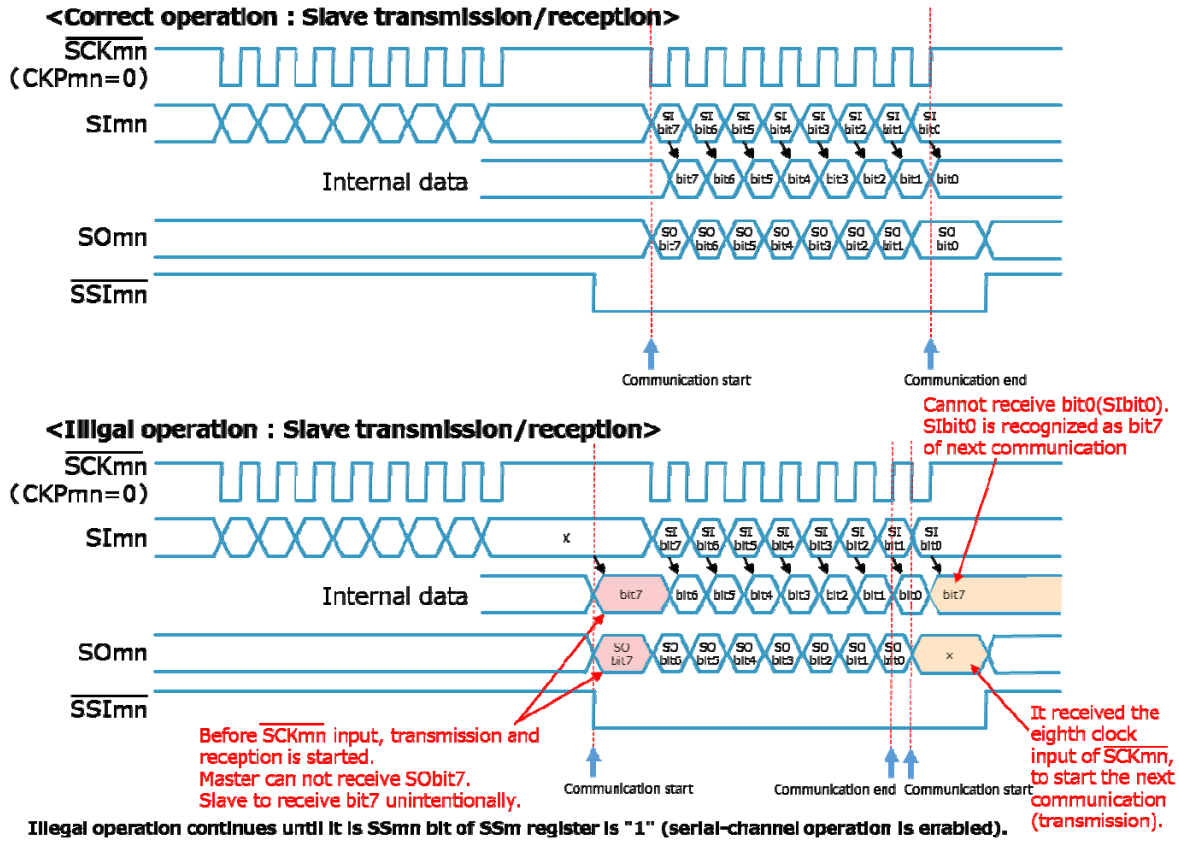
When the user's manual revision, the following note is appended all products as a target.

"SSImn case to be used (slave selection input), please to CKPmn bit of SCRmn register to " 1 "(inverting the clock phase) (m = 0, 1, n = 0, 1)."

(For the purpose of common specifications in the series, it will be described in all products.)

Example of SPI Function Configuration





Applicable Products		Target channel
Group 1	R5F10AME, R5F10AMF, R5F10AMG R5F10ALF, R5F10ALG R5F10BME, R5F10BMF, R5F10BMG R5F10BLC, R5F10BLD, R5F10BLE, R5F10BLF, R5F10BLG, R5F10PME, R5F10PMF R5F10PLE, R5F10PLF	CSI10
Group 2	R5F10PPE, R5F10PPF, R5F10PPG, R5F10PPH, R5F10PPJ R5F10PMG, R5F10PMH, R5F10PMJ R5F10PLG, R5F10PLH, R5F10PLJ R5F10PGG, R5F10PGH, R5F10PGJ	CSI00

That is all