RENESAS TECHNICAL UPDATE

1753, Shimonumabe, Nakahara-ku, Kawasaki-shi, Kanagawa 211-8668 Japan Renesas Electronics Corporation

Product Category	MPU/MCU		Document No.	TN-RX*-A123A/E	Rev.	1.00	
Title		dition usage notes to Manual regarding the Resets d the Clock Generation Circuit in the RX64M Grourp		Technical Notification			
		Lot No.					
Applicable Product	RX64M Group	All	Reference Document	RX64M Group User's Hardware Rev 1.00 (R01UH0377EJ0100	1		
This docume	I nt describes to addition usage notes to section	n 6.Resets、	9. Clock Genera	L ation Circuit in RX64M G	Group Use	er's	
Manual:							
Hardware							
• Page 254	of 2903						
6.4 Usage	Notes is added as follows:						
After correcti	on						
6.4 Usage No	otes						
-	on Using Power-On Reset and PLL Circuit Tog	ether					
When using a	a power-on reset and the PLL circuit together,	set the LVD	1CR1.LVD1IDTS	SEL[1:0] bits or			
-	D2IDTSEL[1:0] bits to 01b, and select the volt	age monitor	ing interrupt to b	e generated when a dro	op (Vcc		
-	D2IDTSEL[1:0] bits to 01b, and select the volt	age monitor	ing interrupt to b	e generated when a dro	op (Vcc		
LVD2CR1.LV < Vdet) is de	D2IDTSEL[1:0] bits to 01b, and select the volt	-	-	-			
LVD2CR1.LV < Vdet) is de In addition, a	D2IDTSEL[1:0] bits to 01b, and select the volt	e, set the SC	CKCR3.CKSEL[2	2:0] bits to a value other	than		
LVD2CR1.LV < Vdet) is de In addition, a	D2IDTSEL[1:0] bits to 01b, and select the volt tected. t the beginning of the interrupt handling routing	e, set the SC	CKCR3.CKSEL[2	2:0] bits to a value other	than		
LVD2CR1.LV < Vdet) is de In addition, a	D2IDTSEL[1:0] bits to 01b, and select the volt tected. t the beginning of the interrupt handling routine of a clock source other than the PLL circuit, the	e, set the SC	CKCR3.CKSEL[2	2:0] bits to a value other	than		
LVD2CR1.LV < Vdet) is de In addition, a 100b to select	D2IDTSEL[1:0] bits to 01b, and select the volt tected. t the beginning of the interrupt handling routine of a clock source other than the PLL circuit, the	e, set the SC	CKCR3.CKSEL[2	2:0] bits to a value other	than		
LVD2CR1.LV < Vdet) is de In addition, a 100b to select	D2IDTSEL[1:0] bits to 01b, and select the volt tected. It the beginning of the interrupt handling routine of a clock source other than the PLL circuit, the of 2903 es is added to 9.10 Usage Notes as follows.	e, set the SC	CKCR3.CKSEL[2	2:0] bits to a value other	than		
LVD2CR1.LV < Vdet) is de In addition, a 100b to select • Page 332 o 9.10.7 Not <u>After correction</u>	D2IDTSEL[1:0] bits to 01b, and select the volt tected. It the beginning of the interrupt handling routine of a clock source other than the PLL circuit, the of 2903 es is added to 9.10 Usage Notes as follows.	e, set the SC	CKCR3.CKSEL[2	2:0] bits to a value other	than		
LVD2CR1.LV < Vdet) is de In addition, a 100b to selec • Page 332 c 9.10.7 Not <u>After correcti</u> 9.10.7 Notes	D2IDTSEL[1:0] bits to 01b, and select the volt tected. It the beginning of the interrupt handling routine of a clock source other than the PLL circuit, the of 2903 es is added to 9.10 Usage Notes as follows.	e, set the SC en set the PL gether	CKCR3.CKSEL[2	2:0] bits to a value other it to 1 to stop the PLL cir	than		
LVD2CR1.LV < Vdet) is de In addition, a 100b to selec • Page 332 o 9.10.7 Notes 9.10.7 Notes When using a	D2IDTSEL[1:0] bits to 01b, and select the volt tected. It the beginning of the interrupt handling routine of a clock source other than the PLL circuit, the of 2903 es is added to 9.10 Usage Notes as follows. <u>on</u> on Using Power-On Reset and PLL Circuit To	e, set the SC en set the PL gether set the LVD	CKCR3.CKSEL[2 LCR2.PLLEN b	2:0] bits to a value other it to 1 to stop the PLL cir SEL[1:0] bits or	than rcuit.		
LVD2CR1.LV < Vdet) is de In addition, a 100b to selec • Page 332 o 9.10.7 Notes 9.10.7 Notes When using a	D2IDTSEL[1:0] bits to 01b, and select the volt tected. It the beginning of the interrupt handling routine of a clock source other than the PLL circuit, the of 2903 es is added to 9.10 Usage Notes as follows. On on Using Power-On Reset and PLL Circuit To a power-on reset and the PLL circuit together, D2IDTSEL[1:0] bits to 01b, and select the volt	e, set the SC en set the PL gether set the LVD	CKCR3.CKSEL[2 LCR2.PLLEN b	2:0] bits to a value other it to 1 to stop the PLL cir SEL[1:0] bits or	than rcuit.		
LVD2CR1.LV < Vdet) is de In addition, a 100b to selec • Page 332 c 9.10.7 Not <u>After correcti</u> 9.10.7 Notes When using a LVD2CR1.LV < Vdet) is de	D2IDTSEL[1:0] bits to 01b, and select the volt tected. It the beginning of the interrupt handling routine of a clock source other than the PLL circuit, the of 2903 es is added to 9.10 Usage Notes as follows. On on Using Power-On Reset and PLL Circuit To a power-on reset and the PLL circuit together, D2IDTSEL[1:0] bits to 01b, and select the volt	e, set the SC en set the PL gether set the LVD	CKCR3.CKSEL[2 LCR2.PLLEN b 1CR1.LVD1IDTS ing interrupt to b	2:0] bits to a value other it to 1 to stop the PLL cir SEL[1:0] bits or be generated when a dro	than rcuit. op (Vcc		

