Date: Jan. 24, 2017

RENESAS TECHNICAL UPDATE

TOYOSU FORESIA, 3-2-24, Toyosu, Koto-ku, Tokyo 135-0061, Japan
Renesas Electronics Corporation

Product Category	MPU/MCU		Document No.	TN-RL*-A072A/E	Rev.	1.00
Title	Adding contents in the hardware user's manual Invalid Memory Access Detection Function		Information Category	Technical Notification		
Applicable Product	ROM capacities 8/16/24/32/48KB products in RL78/F12 ROM capacities 16/32/48/96KB products in RL78/F13, F14	Lot No. All Lots	Reference Document	User's Manual: Hardware of applicable products		

There are corrections on the following User's Manual.

- RL78/F12 User's Manual: Hardware Rev.1.11 (R01UH0231EJ0111)
- RL78/F13, F14 User's Manual: Hardware Rev.2.10 (R01UH0368EJ0210)

Corrections in the User's Manual: Hardware

- RL78/F12 User's Manual: Hardware Rev.1.11 (R01UH0231EJ0111)

Application Item	Applicable Page (R01UH0231EJ0111)	Contents
24.3.6 Invalid Memory Access Detection Function Figure 24-10. Invalid Memory Access Detection Space	p.949	Contents added

- RL78/F13, F14 User's Manual: Hardware Rev.2.10 (R01UH0368EJ0210)

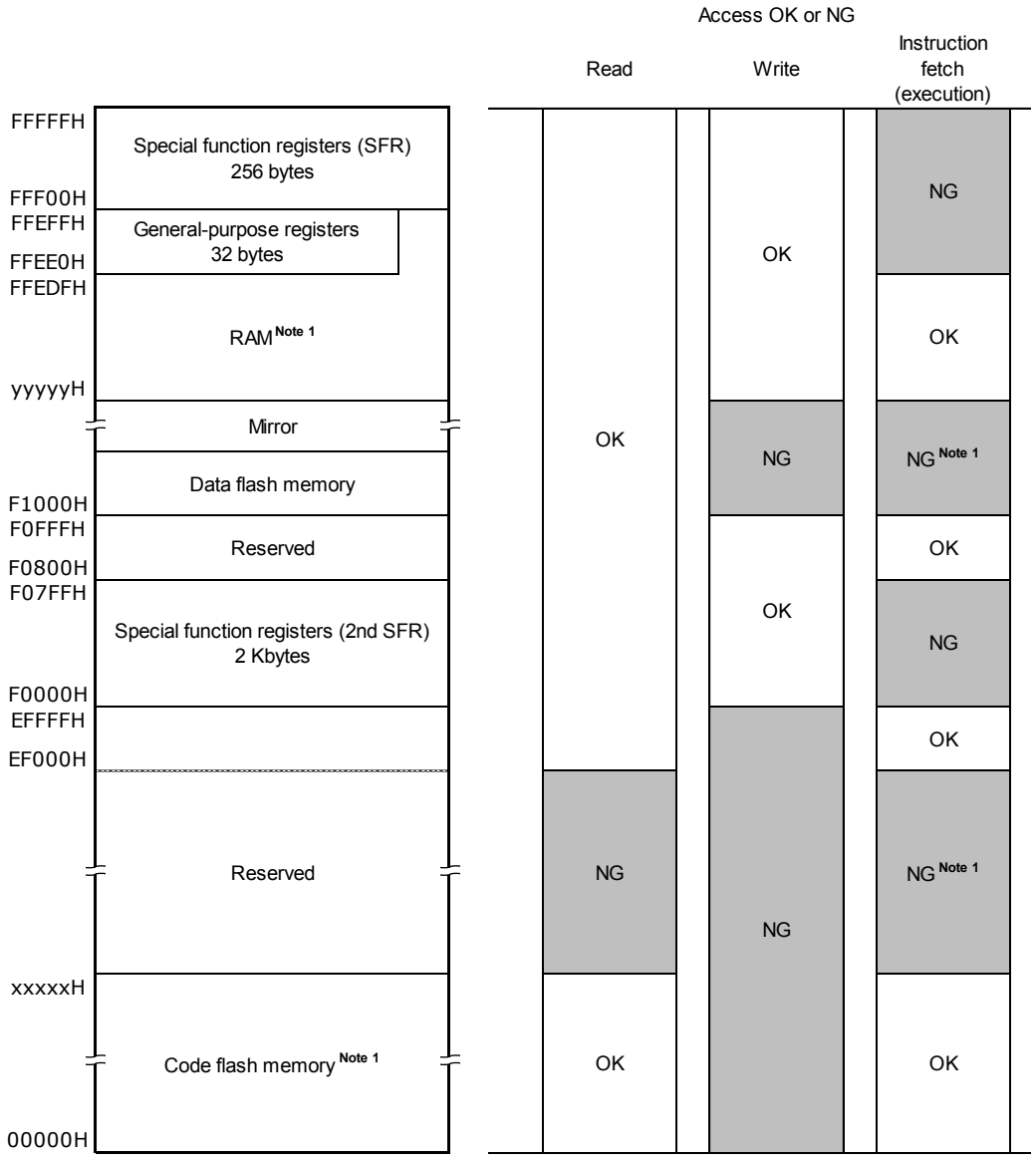
Application Item	Applicable Page (R01UH0368EJ0210)	Contents
27.3.8 Invalid memory access detection function Figure 27-21. Invalid access detection area	p.1602	Contents added

Adding contents are shown as **gray hatching**.

・RL78/F12 User's Manual: Hardware Rev.1.11 (R01UH0231EJ0111)

24.3.6 Invalid Memory Access Detection Function

Figure 24-10. Invalid Memory Access Detection Space



Notes 1. The addresses of the RAM and code flash memory are shown below according to the product type.

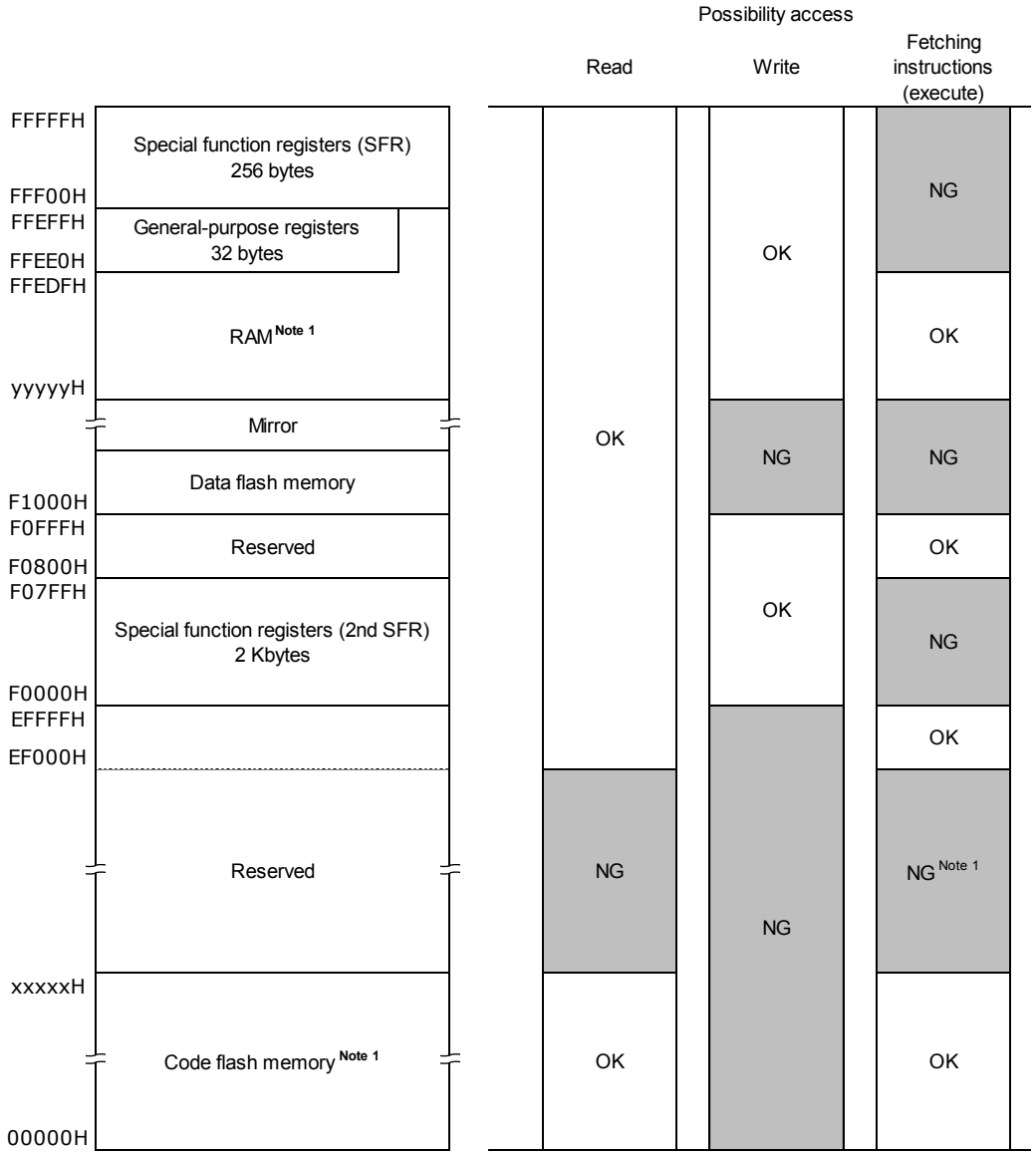
Product Type	Code Flash Memory (00000H-xxxxxH)	RAM (yyyyyH-FFEFFH)
R5F10968	8192×8 bits (00000H-01FFFH) Note 2	512×8 bits (FFD00H-FFEFFH)
R5F109xA (x = 6, A, B, G, L)	16384×8 bits (00000H-03FFFH) Note 2	1024×8 bits (FFB00H-FFEFFH)
R5F109xB (x = 6, A, B, G, L)	24576×8 bits (00000H-05FFFH) Note 2	1536×8 bits (FF900H-FFEFFH) Note 3
R5F109xC (x = 6, A, B, G, L)	32768×8 bits (00000H-07FFFH) Note 2	2048×8 bits (FF700H-FFEFFH)
R5F109xD (x = 6, A, B, G, L)	49152×8 bits (00000H-0BFFFH) Note 2	3072×8 bits (FF700H-FFEFFH)
R5F109xE (x = 6, A, B, G, L)	65536×8 bits (00000H-0FFFFH)	4096×8 bits (FF700H-FFEFFH)

2. Fetching of an instruction (for execution) by illegal to a location in the area from xxxxxH to 0FFFFH leads to the generation of a reset due the execution of an illegal instruction rather than being handled as illegal memory access. In case of reading a reset does not generate and "FFH" is read.
3. Fetching of an instruction (for execution) by illegal to a location in the area from FF700H to FF8FFH, a reset does not generate by invalid memory access detection but it may generate by RAM parity error. In case of writing, it does not generate by invalid memory access detection.

・RL78/F13, F14 User's Manual: Hardware Rev.2.10 (R01UH0368EJ0210)

27.3.8 Invalid memory access detection function

Figure 27-21. Invalid access detection area



Notes 1. Code flash memory and RAM address of each product are as follows.

- RL78/F13 (LIN incorporated)

ROM size	Code flash memory (00000H to xxxxxH)
16 Kbytes	16384 x 8 bits (00000H to 03FFFH) Note2
32 Kbytes	32768 x 8 bits (00000H to 07FFFH) Note2
48 Kbytes	49152 x 8 bits (00000H to 0BFFFH) Note2
64 Kbytes	65536 x 8 bits (00000H to 0FFFFH)
96 Kbytes	98304 x 8 bits (00000H to 17FFFH) Note3
128 Kbytes	131072 x 8 bits (00000H to 1FFFFH)

RAM size	RAM (yyyyyH to FFEFFH)
1 Kbytes	1024 x 8 bits (FFB00H to FFEFFH)
2 Kbytes	2048 x 8 bits (FF700H to FFEFFH)
3 Kbytes	3072 x 8 bits (FF300H to FFEFFH)
4 Kbytes	4096 x 8 bits (FEF00H to FFEFFH)
6 Kbytes	6144 x 8 bits (FE700H to FFEFFH)
8 Kbytes	8192 x 8 bits (FDF00H to FFEFFH)

- RL78/F13 (CAN and LIN incorporated)

ROM size	Code flash memory (00000H to xxxxxH)
32 Kbytes	32768 x 8 bits (00000H to 07FFFH) Note2
48 Kbytes	49152 x 8 bits (00000H to 0BFFFH) Note2
64 Kbytes	65536 x 8 bits (00000H to 0FFFFH)
96 Kbytes	98304 x 8 bits (00000H to 17FFFH) Note3
128 Kbytes	131072 x 8 bits (00000H to 1FFFFH)

RAM size	RAM (yyyyyH to FFEFFH)
2 Kbytes	2048 x 8 bits (FF700H to FFEFFH)
3 Kbytes	3072 x 8 bits (FF300H to FFEFFH)
4 Kbytes	4096 x 8 bits (FEF00H to FFEFFH)
6 Kbytes	6144 x 8 bits (FE700H to FFEFFH)
8 Kbytes	8192 x 8 bits (FDF00H to FFEFFH)

- RL78/F14

ROM size	Code flash memory (00000H to xxxxxH)
48 Kbytes	49152 x 8 bits (00000H to 0BFFFH) Note2
64 Kbytes	65536 x 8 bits (00000H to 0FFFFH)
96 Kbytes	98304 x 8 bits (00000H to 17FFFH) Note3
128 Kbytes	131072 x 8 bits (00000H to 1FFFFH)
192 Kbytes	196608 x 8 bits (00000H to 2FFFFH)
256 Kbytes	262144 x 8 bits (00000H to 3FFFFH)

RAM size	RAM (yyyyyH to FFEFFH)
4 Kbytes	4096 x 8 bits (FEF00H to FFEFFH)
6 Kbytes	6144 x 8 bits (FE700H to FFEFFH)
8 Kbytes	8192 x 8 bits (FDF00H to FFEFFH)
10 Kbytes	10240 x 8 bits (FD700H to FFEFFH)
16 Kbytes	16384 x 8 bits (FBF00H to FFEFFH)
20 Kbytes	20480 x 8 bits (FAF00H to FFEFFH)

2. Fetching of an instruction (for execution) by illegal access to a location in the area from xxxxxH to 0FFFFH leads to the generation of a reset due to the execution of an illegal instruction rather than being handled as illegal memory access. In case of reading, a reset does not generate and “FFH” is read.

3. Fetching of an instruction (for execution) by illegal access to a location in the area from xxxxxH to 1FFFFH leads to the generation of a reset due to the execution of an illegal instruction rather than being handled as illegal memory access. In case of reading, a reset does not generate and “FFH” is read.