Integrated Device Technology, Inc.
2975 Stender Way, Santa Clara, CA - 95054

PRODUCT/PROCESS CHANGE NOTICE (PCN)

PCN #: SM-0202-02 Date: February 25, 2002

Product Affected: 7132, 7133 and 7134 Families

Manufacturing Location Affected: Salinas, California

Date Effective: May 25, 2002

MEANS OF DISTINGUISHING CHANGED DEVICES:

- ☐ Product Mark
- ☐ Back Mark
- ■ Date Code Top mark will have "4" following the die revision. Refer to page 1 of attachment
- ☐ Other

Contact: George Snell
Title: Quality Assurance Manager
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Attachment:: ■ Yes ☐ No

Samples: Available upon request.

DESCRIPTION AND PURPOSE OF CHANGE:

- ■ Die Technology
- ☐ Wafer Fabrication Process
- ☐ Assembly Process
- ☐ Equipment
- ☐ Material
- ☐ Testing
- ■ Manufacturing Site
- ☐ Data Sheet
- ☐ Other

To consolidate Wafer Fab production from Salinas, California (Fab 2) to Hillsboro, Oregon (Fab 4) these qualified products will be transferred to IDT's Wafer Fab facility in Hillsboro, Oregon. These devices will be upgraded from Cmos 7 (.64µm) to Cmos 8 (.60µm). Cmos 8 is an existing qualified process at Fab 4.

RELIABILITY/QUALIFICATION SUMMARY:

Qualification testing will verify that there is no change to the product reliability. Qualification details are available upon request

CUSTOMER ACKNOWLEDGMENT OF RECEIPT:

IDT records indicate that you require written notification of this change. Please use the acknowledgement below or E-Mail to grant approval or request additional information. If IDT does not receive acknowledgement within 30 days of this notice it will be assumed that this change is acceptable.
IDT reserves the right to ship either version manufactured after the process change effective date until the inventory on the earlier version has been depleted.

Customer: _____ ☐ ***Approval for shipments prior to effective date.***

Name/Date: _____ E-Mail Address: _____

Title: _____ Phone# /Fax# : _____

CUSTOMER COMMENTS: _____

IDT ACKNOWLEDGMENT OF RECEIPT:

RECD. BY: _____ DATE: _____

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ATTACHMENT - PCN #: SM-0202-02

PCN Type: Fab Site Change

Data Sheet Change None Expected

Detail of Change

Transfer existing qualified products from Salinas, California Wafer Fab Facility (Fab 2) to Hillsboro, Oregon Wafer Fab Facility (Fab 4).

	Current Wafer Fab				Transfer Wafer Fab			
Part Name	Manufacturing Site	Technology	Wafer Size	Die Revision	Manufacturing Site	Technology	Wafer Size	Die Revision
7132S	Salinas, CA	Cmos 7	6 inch	S	Hillsboro, OR	Cmos 8	8 inch	S4
7132SF	Salinas, CA	Cmos 7	6 inch	SF	Hillsboro, OR	Cmos 8	8 inch	SF4
7133W	Salinas, CA	Cmos 7	6 inch	W	Hillsboro, OR	Cmos 8	8 inch	W4
7134W	Salinas, CA	Cmos 7	6 inch	W	Hillsboro, OR	Cmos 8	8 inch	W4

Conversion schedule (Estimated)

Base Device	Production Shipments and Sample availability
7132S4	5/25/02
7132SF4	5/25/02
7133W4	6/30/02
7134W4	5/25/02

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PRODUCT/PROCESS CHANGE NOTICE (PCN)

ATTACHMENT - PCN #: SM-0202-02

Qualification Plan: QSM-0201-02

Test Vehicle	Expected Completion Date	
	4/1/2002	
7132S	Required Sample / # Fails	LOT #1
Operating Life Test: Dynamic @+135°C, Vcc=4V for 750 hours	116 / 0	
High Temp. Storage Life Test (Unbiased, 1000 hours @+150°C)	77 / 0	
Bake & Ballshear Test @ 200°C / 4 ball bonds per device	5 / 0	
Temperature Cycling: (-65°C to +150°C, 500 cycles)	45 / 0	
HAST: (Biased, 100 Hrs. @+130°C, +85%RH, 3 Atm.)	45 / 0	
Autoclave:(Unbiased, 2 Atm Saturated Steam, +121°C, 168 Hrs)	45 / 0	
ESD Human Body Model	9 / 0	
ESD Charged Device Model	6 / 0	
Latch up: (Tested to 1.5X Vcc)	10 / 0	

Product release is based on qualification of initial lot.

Qualification Plan : QSM-0201-03

Test Vehicle	Expected Completion Date	
	4/1/2002	
7133W	Required Sample / # Fails	LOT #1
Operating Life Test: Dynamic @+135°C, Vcc=4V for 750 hours	116 / 0	
High Temp. Storage Life Test (Unbiased, 1000 hours @+150°C)	77 / 0	
Bake & Ballshear Test @ 200°C / 4 ball bonds per device	5 / 0	
Temperature Cycling: (-65°C to +150°C, 500 cycles)	45 / 0	
HAST: (Biased, 100 Hrs. @+130°C, +85%RH, 3 Atm.)	45 / 0	
Autoclave:(Unbiased, 2 Atm Saturated Steam, +121°C, 168 Hrs)	45 / 0	
ESD Human Body Model	9 / 0	
ESD Charged Device Model	6 / 0	
Latch up: (Tested to 1.5X Vcc)	10 / 0	

Product release is based on qualification of initial lot.

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PRODUCT/PROCESS CHANGE NOTICE (PCN)

ATTACHMENT - PCN #: SM-0202-02

Qualification Plan : QSM-0201-01

Test Vehicle	Expected Completion Date	
	4/1/2002	
7134W	Required Sample / # Fails	LOT #1
Operating Life Test: Dynamic @+135°C, Vcc=4V for 750 hours	116 / 0	
High Temp. Storage Life Test (Unbiased, 1000 hours @+150°C)	77 / 0	
Bake & Ballshear Test @ 200°C / 4 ball bonds per device	5 / 0	
Temperature Cycling: (-65°C to +150°C, 500 cycles)	45 / 0	
HAST: (Biased, 100 Hrs. @+130°C, +85%RH, 3 Atm.)	45 / 0	
Autoclave:(Unbiased, 2 Atm Saturated Steam, +121°C, 168 Hrs)	45 / 0	
ESD Human Body Model	9 / 0	
ESD Charged Device Model	6 / 0	
Latch up: (Tested to 1.5X Vcc)	10 / 0	

Product release is based on qualification of initial lot.

Characterization Data: Characterization will be completed as part of product qualification and data available upon request. Characterization will verify that there is no change to existing datasheet parameters.

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IDT7132 Family of Parts						
Part Number	Die Rev.	Interface	Vcc	Bus	Depth	Density
IDT7130	S4	Async	5	x8	1K	8K
IDT7132	S4	Async	5	x8	2K	16K
IDT71321	S4	Async	5	x8	2K	16K
IDT7140	S4	Async	5	x8	1K	8K
IDT7142	S4	Async	5	x8	2K	16K
IDT71421	S4	Async	5	x8	2K	16K
IDT7130	SF4	Async	5	x8	1K	8K
IDT7132	SF4	Async	5	x8	2K	16K
IDT71321	SF4	Async	5	x8	2K	16K
IDT7140	SF4	Async	5	x8	1K	8K
IDT7142	SF4	Async	5	x8	2K	16K
IDT71421	SF4	Async	5	x8	2K	16K
IDT71V30	SF4	Async	3.3	x8	1K	8K
IDT71V321	SF4	Async	3.3	x8	2K	16K
IDT7133 Family of Parts						
IDT7133	W4	Async	5	x16	2K	32K
IDT7143	W4	Async	5	x16	2K	32K
IDT7134 Family of Parts						
IDT7134	W4	Async	5	x8	4K	32K
IDT71342	W4	Async	5	x8	4K	32K