User's Manual

SuperH™ Family E10A-USB Emulator

Additional Document for User's Manual
Supplementary Information on Using the SH7256R Group

SH72567R and SH72567BFCC

SuperH™ Family

E10A-USB for SH7256R Group
SH72567R, SH72567BFCC
HS7256KCU01HE

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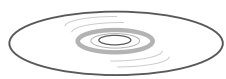
Section 1 Connecting the Emulator with the User System

1.1 Components of the Emulator

The E10A-USB emulator supports the SH7256R Group.

Table 1.1 lists the components of the emulator.

Table 1.1 Components of the Emulator

Classi-fication	Component	Appearance	Quan-tity	Remarks
Hard-ware	Emulator box		1	HS0005KCU01H: Depth: 65.0 mm, Width: 97.0 mm, Height: 20.0 mm, Mass: 72.9 g or HS0005KCU02H: Depth: 65.0 mm, Width: 97.0 mm, Height: 20.0 mm, Mass: 73.7 g
	User system interface cable		1	14-pin type: Length: 20 cm, Mass: 33.1 g
	User system interface cable		1	36-pin type: Length: 20 cm, Mass: 49.2 g (only for HS0005KCU02H)
	USB cable		1	Length: 150 cm, Mass: 50.6 g
Soft-ware	E10A-USB emulator setup program, SuperH™ Family E10A-USB Emulator User's Manual, Supplementary Information on Using the SH7256R Group, and Test program manual for HS0005KCU01H and HS0005KCU02H		1	HS0005KCU01SR, HS0005KCU01HJ, HS0005KCU01HE, HS7256KCU01HJ, HS7256KCU01HE, HS0005TM01HJ, and HS0005TM01HE (provided on a CD-R)

Note: Additional document for the MCUs supported by the emulator is included. Check the target MCU and refer to its additional document.

1.2 Connecting the Emulator with the User System

To connect the E10A-USB emulator (hereinafter referred to as the emulator), the H-UDI port connector must be installed on the user system to connect the user system interface cable. When designing the user system, refer to the recommended circuit between the H-UDI port connector and the MCU. In addition, read the E10A-USB emulator user's manual and hardware manual for the related device.

Table 1.2 shows the type number of the emulator, the corresponding connector type, and the use of AUD function.

Table 1.2 Type Number, AUD Function, and Connector Type

Type Number	Connector	AUD Function
HS0005KCU02H	36-pin connector	Available
HS0005KCU01H, HS0005KCU02H	14-pin connector	Not available
HS0005KCU02H	38-pin connector	Available

The H-UDI port connector has the 36-pin, 14-pin, and 38-pin types as described below. Use them according to the purpose of the usage.

1. 36-pin type (with AUD function)

   The AUD trace function is supported. A large amount of trace information can be acquired in realtime. The window trace function is also supported for acquiring memory access in the specified range (memory access address or memory access data) by tracing.
2. 14-pin type (without AUD function)

   The AUD trace function cannot be used because only the H-UDI function is supported. Since the 14-pin type connector is smaller than the 36-pin type (1/2.5), the size of the area where the connector is installed on the user system can be reduced.
3. 38-pin type (with AUD function)

   The AUD trace function is supported. As well as the 36-pin type, a large amount of trace information can be acquired in realtime. Since the 38-pin type connector is smaller than the 36-pin type (1/2.5), the size of the area where the connector is installed on the user system can be reduced. To use the 38-pin type connector, however, an optional cable (HS0005ECK01H) is required.

1.3 Installing the H-UDI Port Connector on the User System

Table 1.3 shows the recommended H-UDI port connectors for the emulator.

Table 1.3 Recommended H-UDI Port Connectors

Connector	Type Number	Manufacturer	Specifications
36-pin connector	DX10M-36S	Hirose Electric Co., Ltd.	Screw type
	DX10M-36SE, DX10G1M-36SE		Lock-pin type
14-pin connector	2514-6002	Minnesota Mining & Manufacturing Ltd.	14-pin straight type
38-pin connector	2-5767004-2	Tyco Electronics Japan	38-pin Mictor type

Note: When designing the 36-pin connector layout on the user board, do not connect any components under the H-UDI connector. When designing the 14-pin connector layout on the user board, do not place any components within 3 mm of the H-UDI port connector. When designing the 38-pin connector layout on the user board, reduce cross-talk noise etc. by keeping other signal lines out of the region where the H-UDI port connector is situated. As shown in figure 1.1, an upper limit (5 mm) applies to the heights of components mounted around the user system connector.

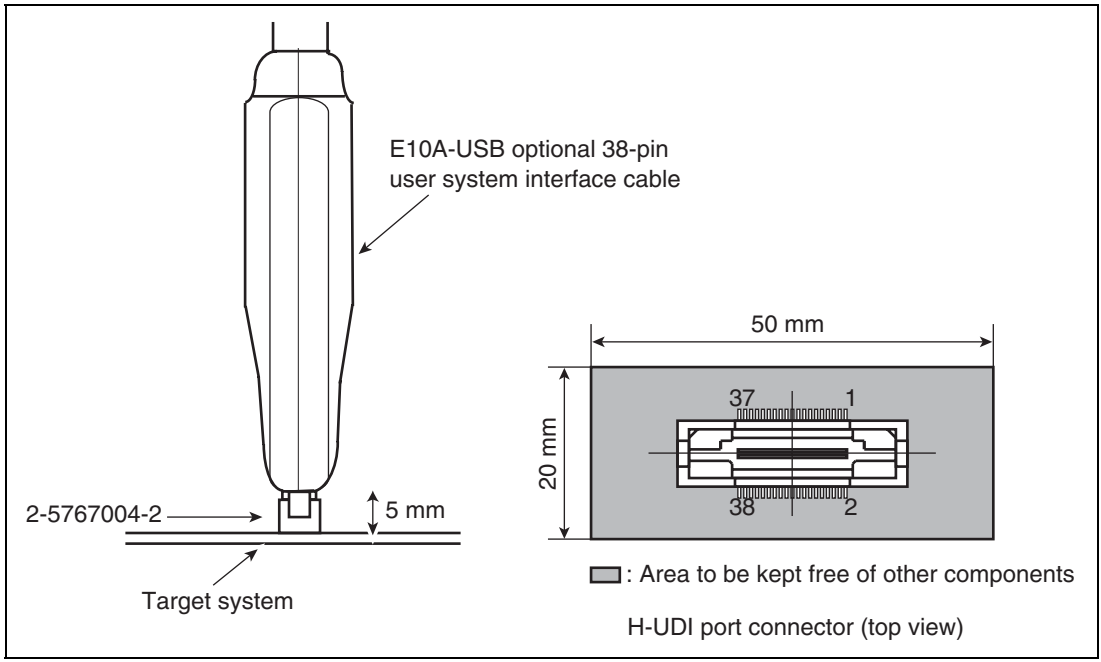


Figure 1.1 Restriction on Component Mounting

1.4 Pin Assignments of the H-UDI Port Connector

Figures 1.2 through 1.4 show the pin assignments of the 36-pin, 14-pin, and 38-pin H-UDI port connectors, respectively.

Note: Note that the pin number assignments of the H-UDI port connector shown on the following pages differ from those of the connector manufacturer.

Pin No.	Signal	Input/ Output*1	SH7256R Pin No.	Note	Pin No.	Signal	Input/ Output*1	SH7256R Pin No.	Note
1	AUDCK	Output	G18		19	TMS	Input	D15	
2	GND	——			20	GND	——		
3	AUDATA0	Output	E18		21	TRST#*2	Input	B17	
4	GND	——			22	GND	——		
5	AUDATA1	Output	E17		23	TDI	Input	A19	
6	GND	——			24	GND	——		
7	AUDATA2	Output	F18		25	TDO	Output	C16	
8	GND	——			26	GND	——		
9	AUDATA3	Output	D17		27	N.C.	——		
10	GND	——			28	GND	——		
11	AUDSYNC#*2	Output	D18		29	UVCC	Output		
12	GND	——			30	GND	——		
13	AUDRST#*2	Input	D16		31	RES#*2	Output	B12	User reset
14	GND	——			32	GND	——		
15	AUDMD	Input	C17		33	GND*3	Output		
16	GND	——			34	GND	——		
17	TCK	Input	B18		35	N.C.	——		
18	GND	——			36	GND	——		

Notes: 1. Input to or output from the user system.
2. The symbol (#) means that the signal is active-low.
3. The emulator monitors the GND signal of the user system and detects whether or not the user system is connected.

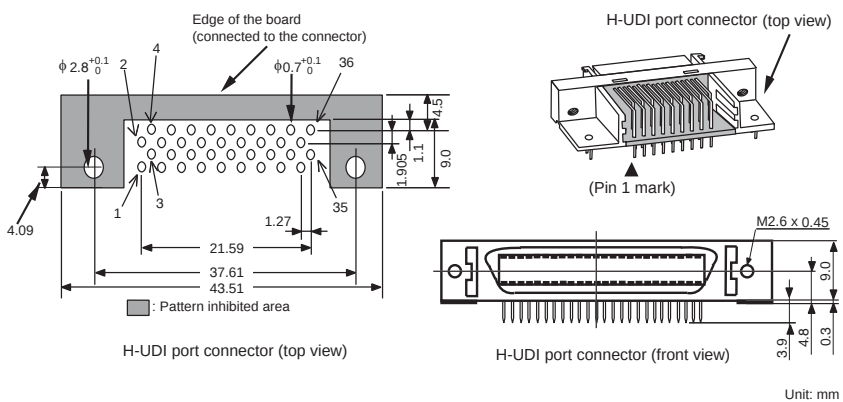


Figure 1.2 Pin Assignments of the H-UDI Port Connector (36 Pins)

Pin No.	Signal		Input/ Output*1	SH7256R Pin No.	Note
1	TCK		Input	B18	
2	TRST#	*2	Input	B17	
3	TDO		Output	C16	
4	N.C.		—		
5	TMS		Input	D15	
6	TDI		Input	A19	
7	RES#	*2	Output	B12	User reset
8	N.C.		—		
9	GND		—		
11	UVCC		Output		
10, 12, and 13	GND		—		
14	GND	*3	Output		

Notes: 1. Input to or output from the user system.
2. The symbol (#) means that the signal is active-low.
3. The emulator monitors the GND signal of the user system and detects whether or not the user system is connected.

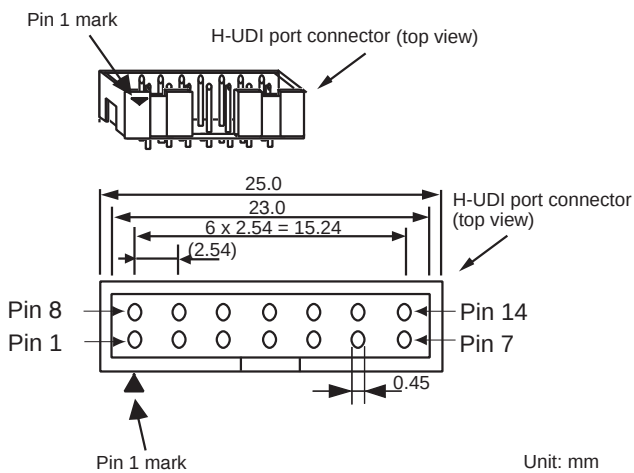
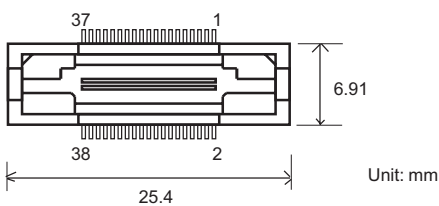


Figure 1.3 Pin Assignments of the H-UDI Port Connector (14 Pins)

Pin No.	Signal	Input/ Output*1	SH7256R Pin No.	Note	Pin No.	Signal	Input/ Output*1	SH7256R Pin No.	Note
1	N.C.	—			20	N.C.	—		
2	N.C.	—			21	TRST#*2	Input	B17	
3	N.C.	—			22	N.C.	—		
4	N.C.	—			23	N.C.	—		
5	UCON# (GND)*3	—			24	AUDATA3	Output	D17	
6	AUDCK	Output	G18		25	N.C.	—		
7	N.C.	—			26	AUDATA2	Output	F18	
8	N.C.	—			27	N.C.	—		
9	RES#*2	Output	B12	User reset	28	AUDATA1	Output	E17	
10	N.C.	—			29	N.C.	—		
11	TDO	Output	C16		30	AUDATA0	Output	E18	
12	UVCC_AUD	Output			31	N.C.	—		
13	N.C.	—			32	AUDSYNC#	Output	D18	
14	UVCC	Output			33	N.C.	—		
15	TCK	Input	B18		34	AUDRST#	Input	D16	
16	N.C.	—			35	N.C.	—		
17	TMS	Input	D15		36	AUDMD	Input	C17	
18	N.C.	—			37	N.C.	—		
19	TDI	Input	A19		38	N.C.	—		

Notes: 1. Input to or output from the user system.
2. The symbol (#) means that the signal is active-low.
3. The emulator monitors the GND signal of the user system and detects whether or not the user system is connected.
4. The GND bus lead at the center of the H-UDI port connector must be grounded.



H-UDI port connector (top view)

Figure 1.4 Pin Assignments of the H-UDI Port Connector (38 Pins)

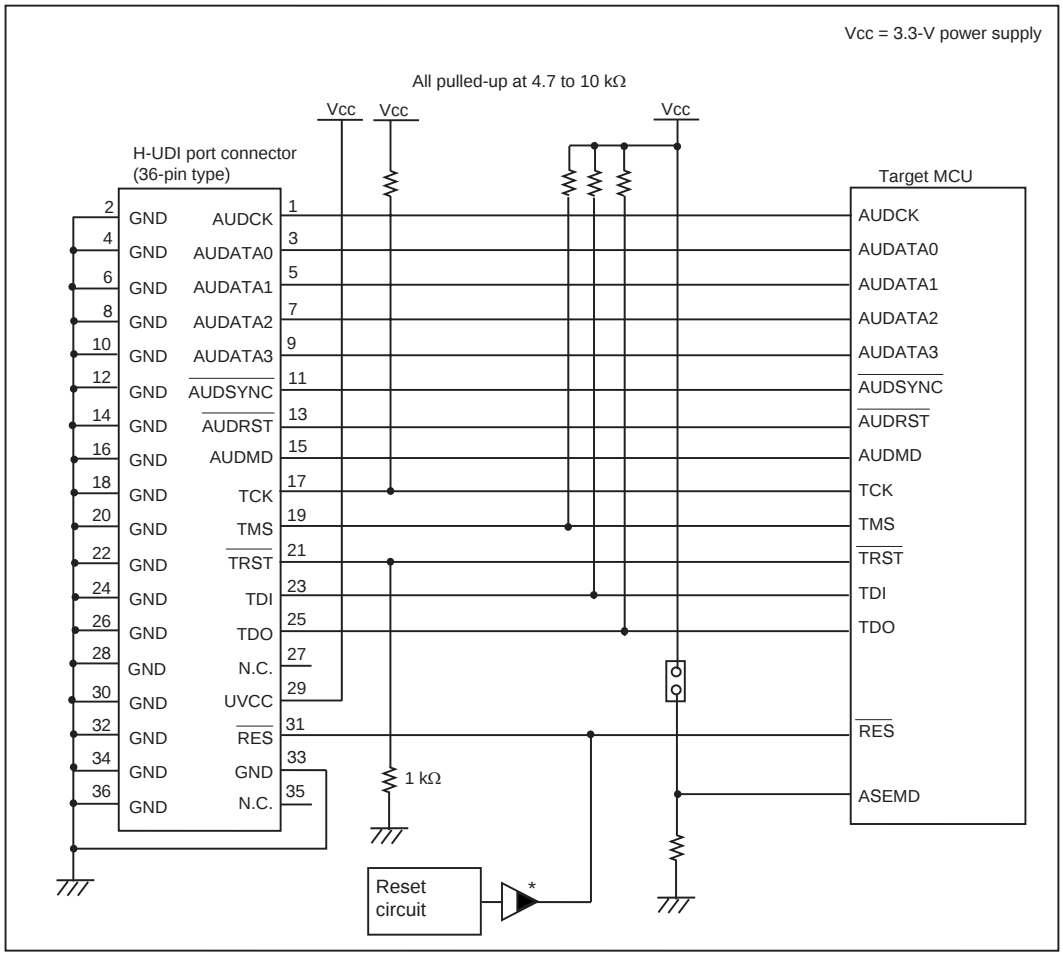
1.5 Recommended Circuit between the H-UDI Port Connector and the MCU

1.5.1 Recommended Circuit (36-Pin Type)

Figure 1.5 shows a recommended circuit for connection between the H-UDI and AUD port connectors (36 pins) and the MCU when the emulator is in use.

Notes:
1. Do not connect anything to the N.C. pins of the H-UDI port connector.
2. The ASEMD pin must be 1 when the emulator is connected and 0 when the emulator is not connected, respectively.
   (1) When the emulator is used: ASEMD = 1
   (2) When the emulator is not used: ASEMD = 0
   Figure 1.5 shows an example of circuits that allow the ASEMD pin to be changed by switches, etc.
3. When a network resistance is used for pull-up, it may be affected by a noise. Separate TCK from other resistances.
4. The pattern between the H-UDI port connector and the MCU must be as short as possible. Do not connect the signal lines to other components on the board.
5. The AUD signals (AUDCK, AUDATA3 to AUDATA0, and AUDSYNC#) operate in high speed. Isometric connection is needed if possible. Do not separate connection nor connect other signal lines adjacently.
6. Since the H-UDI and the AUD of the MCU operate with the Vcc, supply only the Vcc to the UVCC pin. Make the emulator's switch settings so that the user power will be supplied (SW2 = 1 and SW3 = 1).
7. The resistance value shown in figure 1.5 is for reference.
8. For the AUDCK pin, guard the pattern between the H-UDI port connector and the MCU at GND level.
9. For the pin processing in cases where the emulator is not used, refer to the hardware manual of the related MCU.

When the circuit is connected as shown in figure 1.5, the switches of the emulator are set as SW2 = 1 and SW3 = 1. For details, refer to section 3.8, Setting the DIP Switches, in the SuperH™ Family E10A-USB Emulator User's Manual.



Note: If you have selected [Reset assert (Auto Connect)] during the booting-up process to make the emulator output a reset signal, the output of the reset circuit in the user system must be open-drain.

Figure 1.5 Recommended Circuit for Connection between the H-UDI Port Connector and MCU when the Emulator is in Use (36-Pin Type)

CAUTION

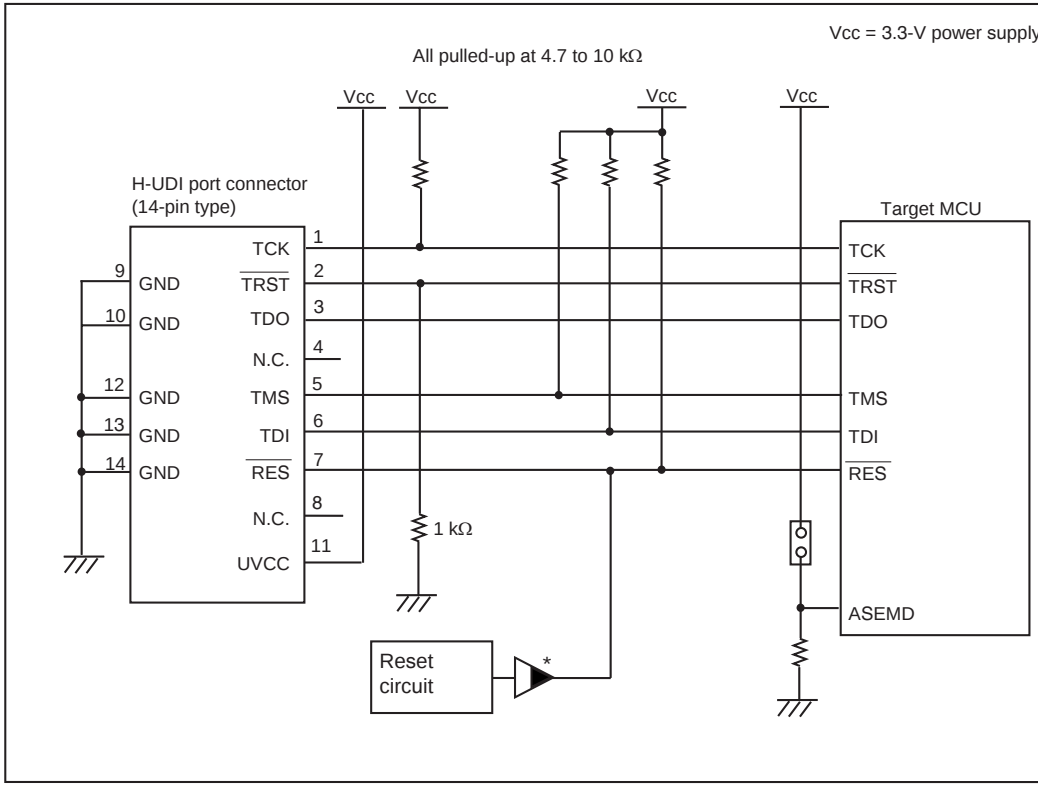
Do not allow the emulator to issue a reset signal unless the output of the reset circuit in use is open-drain. If this is not the case, conflict between signals will damage the user system.

1.5.2 Recommended Circuit (14-Pin Type)

Figure 1.6 shows a recommended circuit for connection between the H-UDI port connector (14 pins) and the MCU when the emulator is in use.

Notes:
1. Do not connect anything to the N.C. pins of the H-UDI port connector.
2. The ASEMD pin must be 1 when the emulator is connected and 0 when the emulator is not connected, respectively.
   (1) When the emulator is used: ASEMD = 1
   (2) When the emulator is not used: ASEMD = 0
   Figure 1.6 shows an example of circuits that allow the ASEMD pin to be changed by switches, etc.
3. When a network resistance is used for pull-up, it may be affected by a noise. Separate TCK from other resistances.
4. The pattern between the H-UDI port connector and the MCU must be as short as possible. Do not connect the signal lines to other components on the board.
5. Since the H-UDI of the MCU operates with the Vcc, supply only the Vcc to the UVCC pin. Make the emulator's switch settings so that the user power will be supplied (SW2 = 1 and SW3 = 1).
6. The resistance value shown in figure 1.6 is for reference.
7. For the pin processing in cases where the emulator is not used, refer to the hardware manual of the related MCU.

When the circuit is connected as shown in figure 1.6, the switches of the emulator are set as SW2 = 1 and SW3 = 1. For details, refer to section 3.8, Setting the DIP Switches, in the SuperH™ Family E10A-USB Emulator User's Manual.



Note: If you have selected [Reset assert (Auto Connect)] during the booting-up process to make the emulator output a reset signal, the output of the reset circuit in the user system must be open-drain.

Figure 1.6 Recommended Circuit for Connection between the H-UDI Port Connector and MCU when the Emulator is in Use (14-Pin Type)

CAUTION

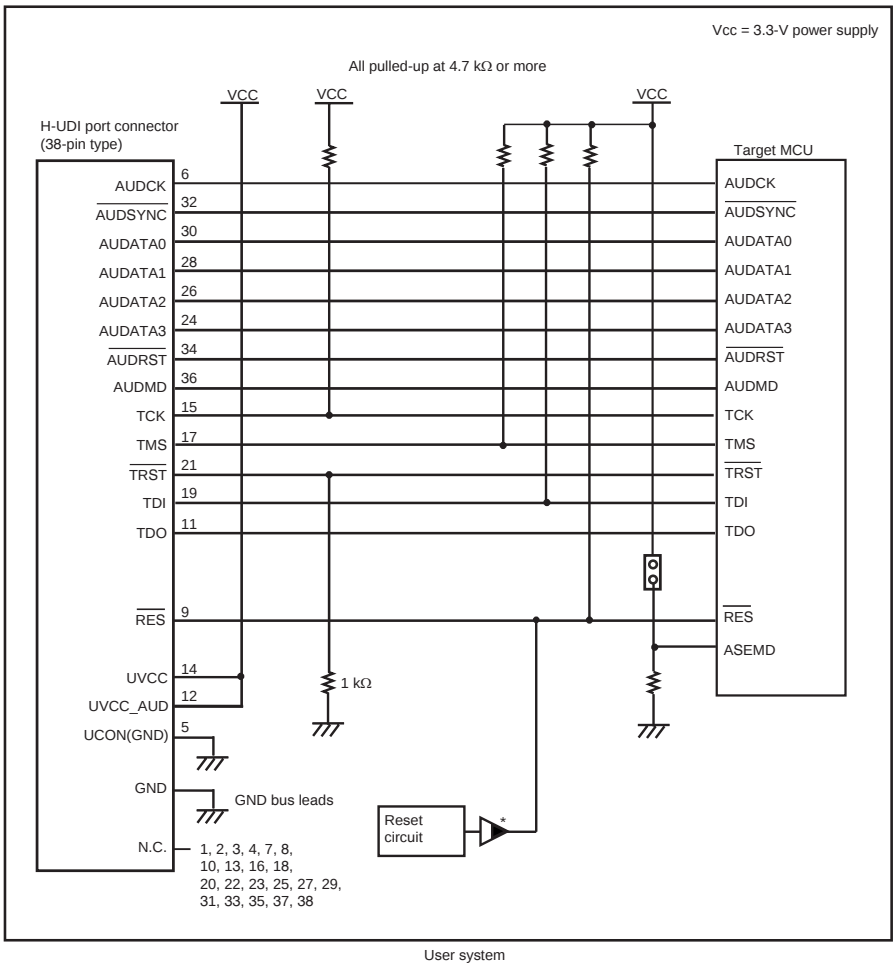
Do not allow the emulator to issue a reset signal unless the output of the reset circuit in use is open-drain. If this is not the case, conflict between signals will damage the user system.

1.5.3 Recommended Circuit (38-Pin Type)

Figure 1.7 shows a recommended circuit for connection between the H-UDI and AUD port connectors (38 pins) and the MCU when the emulator is in use.

Notes:
1. Do not connect anything to the N.C. pins of the H-UDI port connector.
2. The ASEMD pin must be 1 when the emulator is connected and 0 when the emulator is not connected, respectively.
   (1) When the emulator is used: ASEMD = 1
   (2) When the emulator is not used: ASEMD = 0
   Figure 1.7 shows an example of circuits that allow the ASEMD pin to be changed by switches, etc.
3. When a network resistance is used for pull-up, it may be affected by a noise. Separate TCK from other resistances.
4. The pattern between the H-UDI port connector and the MCU must be as short as possible. Do not connect the signal lines to other components on the board.
5. The AUD signals (AUDCK, AUDATA3 to AUDATA0, and AUDSYNC#) operate in high speed. Isometric connection is needed if possible. Do not separate connection nor connect other signal lines adjacently.
6. Since the H-UDI and the AUD of the MCU operate with the Vcc, supply only the Vcc to the UVCC pin. Make the emulator's switch settings so that the user power will be supplied (SW2 = 1 and SW3 = 1).
7. The resistance value shown in figure 1.7 is for reference.
8. For the AUDCK pin, guard the pattern between the H-UDI port connector and the MCU at GND level.
9. The GND bus lead at the center of the H-UDI port connector must be grounded.
10. For the pin processing in cases where the emulator is not used, refer to the hardware manual of the related MCU.

When the circuit is connected as shown in figure 1.7, the switches of the emulator are set as SW2 = 1 and SW3 = 1. For details, refer to section 3.8, Setting the DIP Switches, in the SuperH™ Family E10A-USB Emulator User's Manual.



Note: If you have selected [Reset assert (Auto Connect)] during the booting-up process to make the emulator output a reset signal, the output of the reset circuit in the user system must be open-drain.

Figure 1.7 Recommended Circuit for Connection between the H-UDI Port Connector and MCU when the Emulator is in Use (38-Pin Type)

CAUTION

Do not allow the emulator to issue a reset signal unless the output of the reset circuit in use is open-drain. If this is not the case, conflict between signals will damage the user system.

Section 2 Software Specifications when Using the Emulator

2.1 Differences between the SH7256R and the Emulator

1. When the emulator system is initiated, it initializes the general registers and part of the control registers as shown in table 2.1. The initial values of the MCU are undefined.

Table 2.1 Register Initial Values at Emulator Link Up

Register	Emulator at Link Up
R0 to R14	H'00000000
R15 (SP)	Value of the SP in the power-on reset vector table
PC	Value of the PC in the power-on reset vector table
SR	H'000000F0
GBR	H'00000000
VBR	H'00000000
TBR	H'00000000
MACH	H'00000000
MACL	H'00000000
PR	H'00000000
FPSCR*	H'00040001
FPUL*	H'00000000
FPR0-15*	H'00000000

Note: If the MCU does not incorporate the floating-point unit (FPU), these registers are not displayed.

Note: When a value of the interrupt mask bit in the SR register is changed in the [Registers] window, it is actually reflected in that register immediately before execution of the user program is started. It also applies when the value is changed by the REGISTER_SET command.

2. The emulator uses the H-UDI; do not access the H-UDI.

3. Low-Power States
   - When the emulator is used, the sleep state can be cleared with either the clearing function or with the [STOP] button, and a break will occur.
   - Emulation of the hardware stand-by mode is not supported.
   - Do not stop inputting the clock to the H-UDI module by using the module standby function.

4. Reset Signals

   The MCU reset signals are only valid during emulation started with clicking the GO or STEP-type button. If these signals are enabled on the user system in command input wait state, they are not sent to the MCU.

Note: Do not break the user program when the RES#, BREQ#, or WAIT# signal is being low. A TIMEOUT error will occur. If the BREQ# or WAIT# signal is fixed to low during break, a TIMEOUT error will occur at memory access.

5. Direct Memory Access Controller (DMAC)

   The DMAC operates even when the emulator is used. When a data transfer request is generated, the DMAC executes DMA transfer.

6. Memory Access during User Program Execution

   During execution of the user program, memory is accessed by the following two methods, as shown in table 2.2.

Table 2.2 Memory Access during User Program Execution

Method	Description
H-UDI read/write	The stopping time of the user program is short because memory is accessed by the dedicated bus master.
Short break	This method is not available for this product (do not set short break).

The method for accessing memory during execution of the user program is specified by using the [Configuration] dialog box.

Table 2.3 Stopping Time by Memory Access (Reference)

Method	Condition	Stopping Time
H-UDI read/write	Reading of one longword for the internal RAM	Reading: Maximum three bus clocks (Bϕ)
	Writing of one longword for the internal RAM	Writing: Maximum two bus clocks (Bϕ)
Short break	CPU clock: 160 MHz JTAG clock: 20 MHz Reading or writing of one longword for the external area	About 50 ms

7. Memory Access to the External Flash Memory Area

   The emulator can download the load module to the external flash memory area (for details, refer to section 6.22, Download Function to the Flash Memory Area, in the SuperH™ Family E10A-USB Emulator User's Manual). Other memory write operations are enabled for the RAM and internal flash memory areas. Therefore, an operation such as memory write or BREAKPOINT should be set only for the RAM or internal flash memory area.

8. ROM Cache

For ROM cache in the MCU, the emulator operates as shown in table 2.4.

Table 2.4 Operation for ROM Cache

Function	Operation
Write and erase of the flash memory	Writes or erases all contents of ROM cache.
Download of the program to the flash memory	
Set an overlap of ERAM to the flash memory*	
Change of the setting of an overlap of ERAM to the flash memory*	
Download of a program to ERAM overlapped with the flash memory*	
Rewrite of the memory contents of ERAM overlapped with the flash memory*	
Set a software break to the flash memory and ERAM overlapped with the flash memory*	
Memory read	Accesses the disabled cache area to read the content of internal flash memory.

Note: These functions are only supported by MCUs that have names ending with FCC.

9. Using WDT

The WDT does not operate during break.

10. Loading Sessions

Information in [JTAG clock] of the [Configuration] dialog box cannot be recovered by loading sessions. Thus the TCK value will be as follows:

— When HS0005KCU01H or HS0005KCU02H is used: TCK = 10 MHz

11. [IO] Window

— Display and modification

For each watchdog timer register, there are two registers to be separately used for write and read operations.

Table 2.5 Watchdog Timer Register

Register Name	Usage	Register
WTCR(W)	Write	Watchdog timer control register
WTCNT(W)	Write	Watchdog timer counter
WTCR(R)	Read	Watchdog timer control register
WTCNT(R)	Read	Watchdog timer counter
WTSR(W)	Write	Watchdog timer status register
WTSR(R)	Read	Watchdog timer status register
WRCR(W)	Write	Watchdog reset control register
WRCR(R)	Read	Watchdog reset control register

— Customization of the I/O-register definition file

The internal I/O registers can be accessed from the [IO] window. After the I/O-register definition file is created, the MCU's specifications may be changed. If each I/O register in the I/O-register definition file differs from addresses described in the hardware manual, change the I/O-register definition file according to the description in the hardware manual. The I/O-register definition file can be customized depending on its format. However, the emulator does not support the bit-field function.

— Verify

In the [IO] window, the verify function of the input value is disabled.

12. Illegal Instructions

    Do not execute illegal instructions with STEP-type commands.

13. Reset Input

    During execution of the user program, the emulator may not operate correctly if a contention occurs between the following operations for the emulator and the reset input to the target device:

    — Setting an Event Condition
    — Setting an internal trace
    — Displaying the content acquired by an internal trace
    — Reading or writing of a memory

    Note that those operations should not contend with the reset input to the target device.

14. MCU Operating Mode

    Boot mode is not supported.

15. Writing Flash Memory Mode

    Writing flash memory mode is not supported.

2.2 Specific Functions for the Emulator when Using the SH7256R

2.2.1 Intelligent Flash Security (IFS): Setting and Resetting of Key Codes

This emulator supports the functions to set and reset key codes for intelligent flash security (IFS).

Note: For details on the current security setting and actions triggered by setting or resetting of key codes, refer to the hardware manual or related technical documents for the MCU. If you do not remember the key code for the MCU, the security setting cannot be canceled. Protecting the contents of the ROM is on your own responsibility.

(1) Setting a Key Code

Select [Setup -> Emulator -> Set key code…] or click on the [Set key code] toolbar button to open the [Set key code] dialog box.

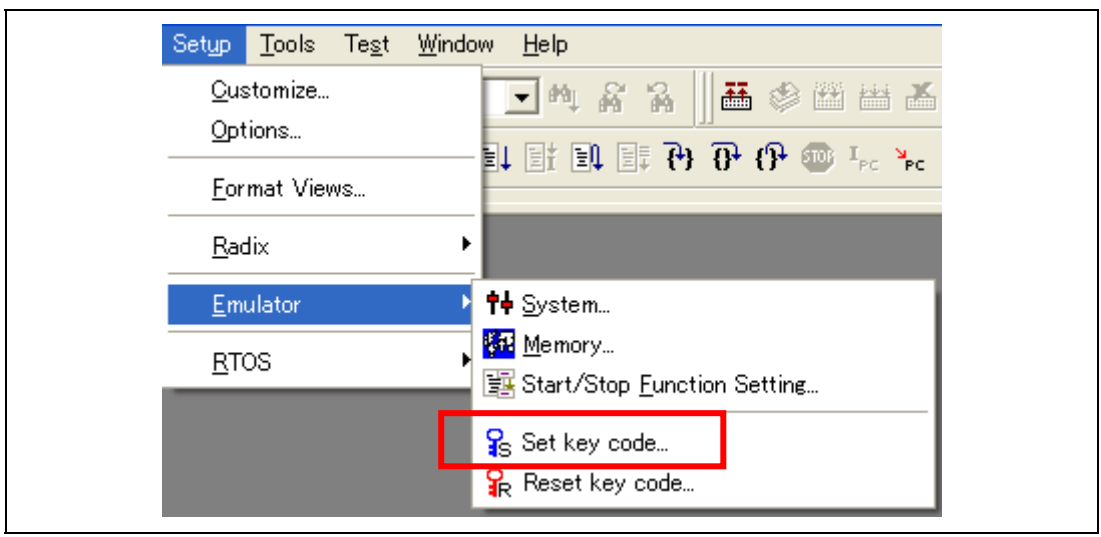


Figure 2.1 [Setup -> Emulator -> Set key code…]

Figure 2.2 [Set key code] Toolbar Button

Enter a key code in the [Set key code] field of the [Set key code] dialog box and click on the [OK] button. This issues the 'key code set' command in the FCU.

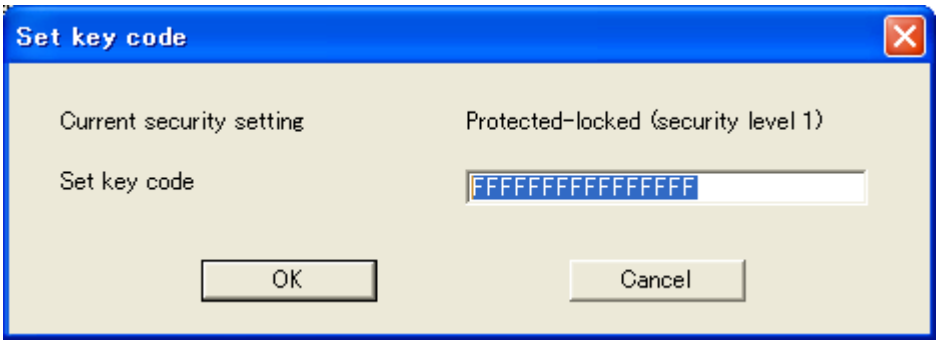


Figure 2.3 [Set key code] Dialog Box

[Current security setting]	Shows the current state of security setting indicated by the IFS status register (IFSSR). The indicated value, however, is invalid in the on-chip ROM disabled mode.
	Unprotected
	Protected-unlocked (security level 1)
	Protected-locked (security level 1)
[Set key code]	Enter a key code.

(2) Resetting a Key Code

Select [Setup -> Emulator -> Reset key code…] or click on the [Reset key code] toolbar button to open the [Current security setting] message box.

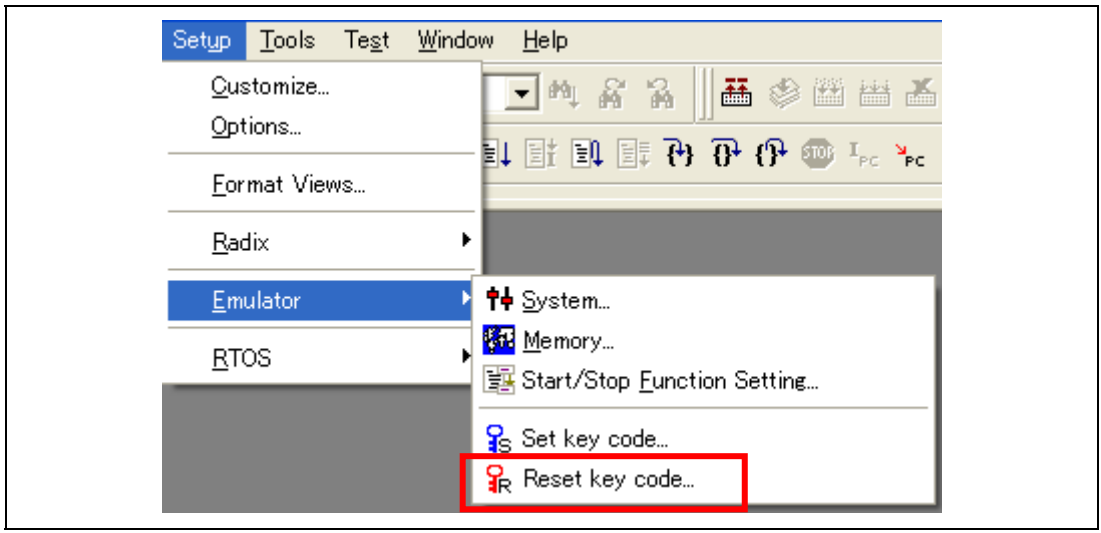


Figure 2.4 [Setup -> Emulator -> Reset key code…]

Figure 2.5 [Reset key code] Toolbar Button

Click on the [OK] button. This issues the ‘key code reset’ command in the FCU.

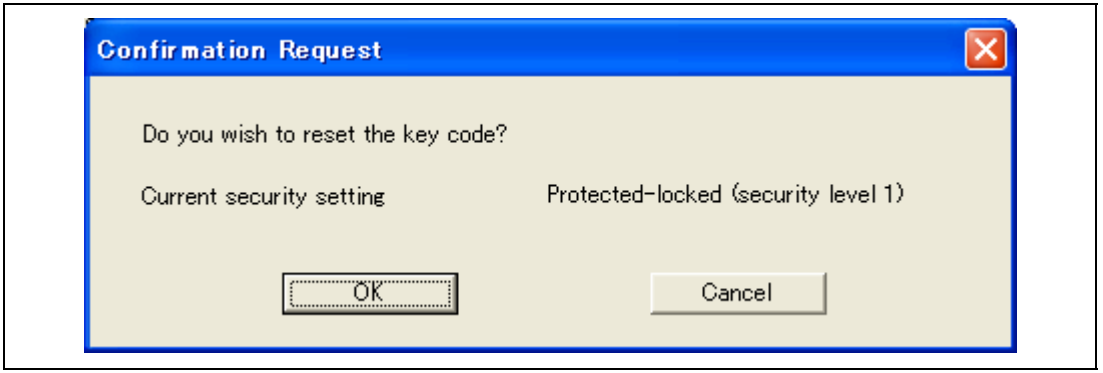


Figure 2.6 [Confirmation Request] Message Box

[Current security setting]	Shows the current state of security setting indicated by the IFS status register (IFSSR). The indicated value, however, is invalid in the on-chip ROM disabled mode.
	Unprotected
	Protected-unlocked (security level 1)
	Protected-locked (security level 1)

(3) Entering a Key Code for Authentication

When you use the function to set or reset a key code in the 'Protected-locked (security level 1)' state, authentication requires the previous key code that was authenticated or set by the emulator. If the authentication of the previous key code fails, the [Enter key code] dialog box appears. Enter a key code for use with the 'key code approval' command in the FCU and click on the [OK] button. This issues the 'key code approval' command.

Figure 2.7 [Enter key code] Dialog Box

[Current security setting]	Shows the current state of security setting indicated by the IFS status register (IFSSR). The indicated value, however, is invalid in the on-chip ROM disabled mode.
	Unprotected
	Protected-unlocked (security level 1)
	Protected-locked (security level 1)
[Enter key code]	Enter a key code for use with the 'key code approval' command in the FCU.

2.2.2 Event Condition Functions

The emulator is used to set event conditions for the following three functions:

- Break of the user program
- Internal trace
- Start or end of performance measurement

Table 2.6 lists the types of Event Condition.

Table 2.6 Types of Event Condition

Event Condition Type	Description
Address bus condition (Address)	Sets a condition when the address bus (data access) value or the program counter value (before or after execution of instructions) is matched.
Data bus condition (Data)	Sets a condition when the data bus value is matched. Byte, word, or longword can be specified as the access data size.
Bus state condition (Bus State)	There are two bus state condition settings: Bus state condition: Sets a condition when the data bus value is matched. Read/Write condition: Sets a condition when the read/write condition is matched.
Count	Sets a condition when the specified other conditions are satisfied for the specified counts.
Reset point	A reset point is set when the count and the sequential condition are specified.
Action	Selects the operation when a condition (such as a break, a trace halt condition, or a trace acquisition condition) is matched.

Using the [Combination action (Sequential or PtoP)] dialog box specifies the sequential condition, the point-to-point of the internal trace, and the start or end of performance measurement.

Table 2.7 lists the combinations of conditions that can be set under Ch1 to Ch11.

Table 2.7 Dialog Boxes for Setting Event Conditions

		Function				
Dialog Box		**Address Bus Condition (Address)**	**Data Bus Condition (Data)**	**Bus State Condition (Bus Status)**	**Count Condition (Count)**	**Action**
[Event Condition 1]	Ch1	O	O	O	O	O (B, T1, and P)
[Event Condition 2]	Ch2	O	O	O	X	O (B, T1, and P)
[Event Condition 3]	Ch3	O	X	X	X	O (B and T2)
[Event Condition 4]	Ch4	O	X	X	X	O (B and T3)
[Event Condition 5]	Ch5	O	X	X	X	O (B and T3)
[Event Condition 6]	Ch6	O	X	X	X	O (B and T2)
[Event Condition 7]	Ch7	O	X	X	X	O (B and T2)
[Event Condition 8]	Ch8	O	X	X	X	O (B and T2)
[Event Condition 9]	Ch9	O	X	X	X	O (B and T2)
[Event Condition 10]	Ch10	O	X	X	X	O (B and T2)
[Event Condition 11]	Ch11	O (reset point)	X	X	X	X

Notes: 1. O: Can be set in the dialog box.
X: Cannot be set in the dialog box.

2. For the Action item,
B: Setting a break is enabled.
T1: Setting the trace halt and acquisition conditions are enabled for the internal trace.
T2: Setting the trace halt is enabled for the internal trace.
T3: Setting the trace halt and point-to-point is enabled for the internal trace.
P: Setting a performance-measurement start or end condition is enabled.
The [Event Condition 11] dialog box is used to specify the count of [Event Condition 1] and becomes a reset point when the sequential condition is specified.

(1) Sequential Setting

Using the [Combination action (Sequential or PtoP)] dialog box specifies the sequential condition and the start or end of performance measurement.

Table 2.8 Conditions to Be Set

Classification	Item	Description
[Ch1, 2, 3] list box	Sets the sequential condition and the start or end of performance measurement using Event Conditions 1 to 3 and 11.	
	Don't care	Sets no sequential condition or the start or end of performance measurement.
	Break: Ch3-2-1	Break in execution when Event Conditions 3, 2, and 1 are satisfied in that order.
	Break: Ch3-2-1, Reset point	Break in execution when Event Conditions 3, 2, and 1 are satisfied in that order. Enables the reset point of Event Condition 11.
	Break: Ch2-1	Break in execution when Event Conditions 2 and 1 are satisfied in that order.
	Break: Ch2-1, Reset point	Break in execution when Event Conditions 2 and 1 are satisfied in that order. Enables the reset point.
	I-Trace stop: Ch3-2-1*	Halts acquisition of an internal trace when Event Conditions 3, 2, and 1 are satisfied in that order.
	I-Trace stop: Ch3-2-1, Reset point*	Halts acquisition of an internal trace when Event Conditions 3, 2, and 1 are satisfied in that order. Enables the reset point.
	I-Trace stop: Ch2-1*	Halts acquisition of an internal trace when Event Conditions 2 and 1 are satisfied in that order.
	I-Trace stop: Ch2-1, Reset point*	Halts acquisition of an internal trace when Event Conditions 2 and 1 are satisfied in that order. Enables the reset point.
	Ch2 to Ch1 PA*	Sets the performance measurement period during the time from the satisfaction of the condition set in Event Condition 2 (start condition) to the satisfaction of the condition set in Event Condition 1 (end condition).

Table 2.8 Conditions to Be Set (cont)

Classification	Item	Description
[Ch1, 2, 3] list box (cont)	Ch1 to Ch2 PA*	Sets the performance measurement period during the time from the satisfaction of the condition set in Event Condition 1 (start condition) to the satisfaction of the condition set in Event Condition 2 (end condition).
[Ch4, 5] list box	Sets the point-to-point of the internal trace (the start or end condition of trace acquisition) using Event Conditions 4 and 5.	
	Don't care	Sets no start or end condition of trace acquisition.
	I-Trace: Ch5 to Ch4 PtoP*	Sets the acquisition period during the time from the satisfaction of the condition set in Event Condition 5 (start condition) to the satisfaction of the condition set in Event Condition 4 (end condition).
	I-Trace: Ch5 to Ch4 PtoP, power-on reset*	Sets the acquisition period during the time from the satisfaction of the condition set in Event Condition 5 (start condition) to the satisfaction of the condition set in Event Condition 4 (end condition) or the power-on reset.

Note: * The internal trace function and performance measurement function cannot be used with the SH7256R, so do not select this item.

- After the sequential condition and the count specification condition of Event Condition 1 have been set, break and trace acquisition will be halted if the sequential condition is satisfied for the specified count.
- If a reset point is satisfied, the satisfaction of the condition set in Event Condition will be disabled. For example, if the condition is satisfied in the order of Event Condition 3, 2, reset point, 1, the break or trace acquisition will not be halted. If the condition is satisfied in the order of Event Condition 3, 2, reset point, 3, 2, 1, the break and trace acquisition will be halted.
- If the start condition is satisfied after the end condition has been satisfied by measuring performance, performance measurement will be restarted. For the measurement result after a break, the measurement results during performance measurement are added.
- If the start condition is satisfied after the end condition has been satisfied by the point-to-point of the internal trace, trace acquisition will be restarted.

(2) Usage Example of Sequential Break Extension Setting

A tutorial program provided for the product is used as an example. For the tutorial program, refer to section 6, Tutorial, in the SuperH™ Family E10A-USB Emulator User's Manual.

The conditions of Event Condition are set as follows:

1. Ch3

   Breaks address H'00001088 when the condition [Only program fetched address after] is satisfied.
2. Ch2

   Breaks address H'000010B0 when the condition [Only program fetched address after] is satisfied.
3. Ch1

   Breaks address H'000010F2 when the condition [Only program fetched address after] is satisfied.

   Note: Do not set other channels.
4. Sets the content of the [Ch1,2,3] list box to [Break: Ch 3-2-1] in the [Combination action (Sequential or PtoP)] dialog box.
5. Enables the condition of Event Condition 1 from the popup menu by clicking the right mouse button on the [Event Condition] sheet.

Then, set the program counter and stack pointer (PC = H'00000800, R15 = H'FFF90000) in the [Registers] window and click the [Go] button. If this does not execute normally, issue a reset and execute the above procedures.

The program is executed up to the condition of Ch1 and halted. Here, the condition is satisfied in the order of Ch3 -> 2 -> 1.

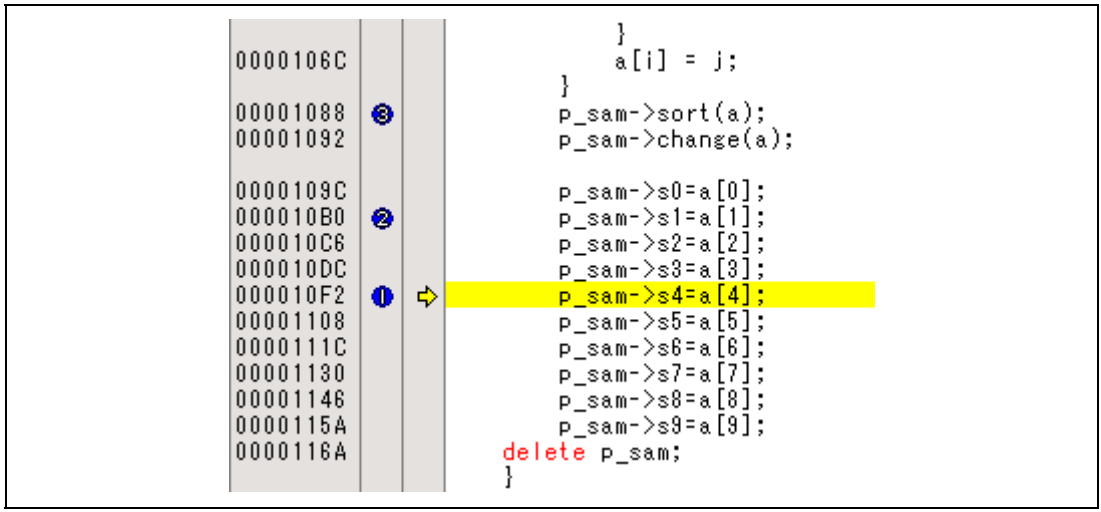


Figure 2.8 [Source] Window at Execution Halted (Sequential Break)

If the sequential condition, performance measurement start/end, or point-to-point for the internal trace is set, conditions of Event Condition to be used will be disabled. Such conditions must be enabled from the popup menu by clicking the right mouse button on the [Event Condition] sheet.

Notes:
1. If the Event condition is set for the slot in the delayed branch instruction by the program counter (after execution of the instruction), the condition is satisfied before executing the instruction in the branch destination (when a break has been set, it occurs before executing the instruction in the branch destination).
2. Do not set the Event condition for the SLEEP instruction by the program counter (after execution of the instruction).
3. When the Event condition is set for the 32-bit instruction by the program counter, set that condition in the upper 16 bits of the instruction.
4. If the power-on reset and the Event condition are matched simultaneously, no condition will be satisfied.
5. Do not set the Event condition for the DIVU or DIVS instruction by the program counter (after execution of the instruction).
6. If a condition of which intervals are satisfied closely is set, no sequential condition will be satisfied.
   - Set the Event conditions, which are satisfied closely, by the program counter with intervals of two or more instructions.
   - After the Event condition has been matched by accessing data, set the Event condition by the program counter with intervals of 17 or more instructions.

7. If the settings of the Event condition or the sequential conditions are changed during execution of the program, execution will be suspended. (The number of clocks to be suspended during execution of the program is a maximum of about 18 peripheral clocks (Pϕ). If the peripheral clock (Pϕ) is 66.6 MHz, the program will be suspended for 0.27 μs.)
8. If the settings of Event conditions or the sequential conditions are changed during execution of the program, the emulator temporarily disables all Event conditions to change the settings. During this period, no Event condition will be satisfied.
9. If the break condition before executing an instruction is set to the instruction followed by DIVU and DIVS, the factor for halting a break will be incorrect under the following condition:
   - If a break occurs during execution of the above DIVU and DIVS instructions, the break condition before executing an instruction, which has been set to the next instruction, may be displayed as the factor for halting a break.
10. If the break conditions before and after executing instructions are set to the same address, the factor for halting a break will be incorrectly displayed. The factor for halting a break due to the break condition after executing an instruction will be displayed even if a break is halted by the break condition before executing an instruction.
11. Do not set the break condition after executing instructions and BREAKPOINT (software break) to the same address.
12. When the emulator is being connected, the user break controller (UBC) function is not available.
13. The performance-measurement function is not available for the SH7256R, so do not make the settings “Ch2 to Ch1PA” and “Ch1 to Ch2PA” if this device is in use.

2.2.3 Trace Functions

The emulator supports the trace functions listed in table 2.9.

Table 2.9 Trace Functions

Function	Internal Trace*	AUD Trace
Branch trace	Not supported	Supported
Memory access trace	Not supported	Supported
Software trace	Not supported	Supported

Note: * The internal trace function cannot be used with the SH7256R.

Table 2.10 shows the type numbers that the AUD function can be used.

Table 2.10 Type Number and AUD Function

Type Number	AUD Function
HS0005KCU01H	Not supported
HS0005KCU02H	Supported

AUD trace settings are made in the [Acquisition] dialog box of the [Trace] window.

(1) AUD Trace Functions

This function is operational when the AUD pin of the device is connected to the emulator. Table 2.11 shows the AUD trace acquisition mode that can be set in each trace function.

Table 2.11 AUD Trace Acquisition Mode

Type	Mode	Description
Continuous trace occurs	Realtime trace	When the next branch occurs while the trace information is being output, all the information may not be output. The user program can be executed in realtime, but some trace information will be lost.
	Non realtime trace	When the next branch occurs while the trace information is being output, the CPU stops operations until the information is output. The user program is not executed in realtime.
Trace buffer full	Trace continue	This function overwrites the latest trace information to store the oldest trace information.
	Trace stop	After the trace buffer becomes full, the trace information is no longer acquired. The user program is continuously executed.

To set the AUD trace acquisition mode, click the [Trace] window with the right mouse button and select [Setting] from the pop-up menu to display the [Acquisition] dialog box. The AUD trace acquisition mode can be set in the [AUD mode1] or [AUD mode2] group box in the [Trace mode] page of the [Acquisition] dialog box.

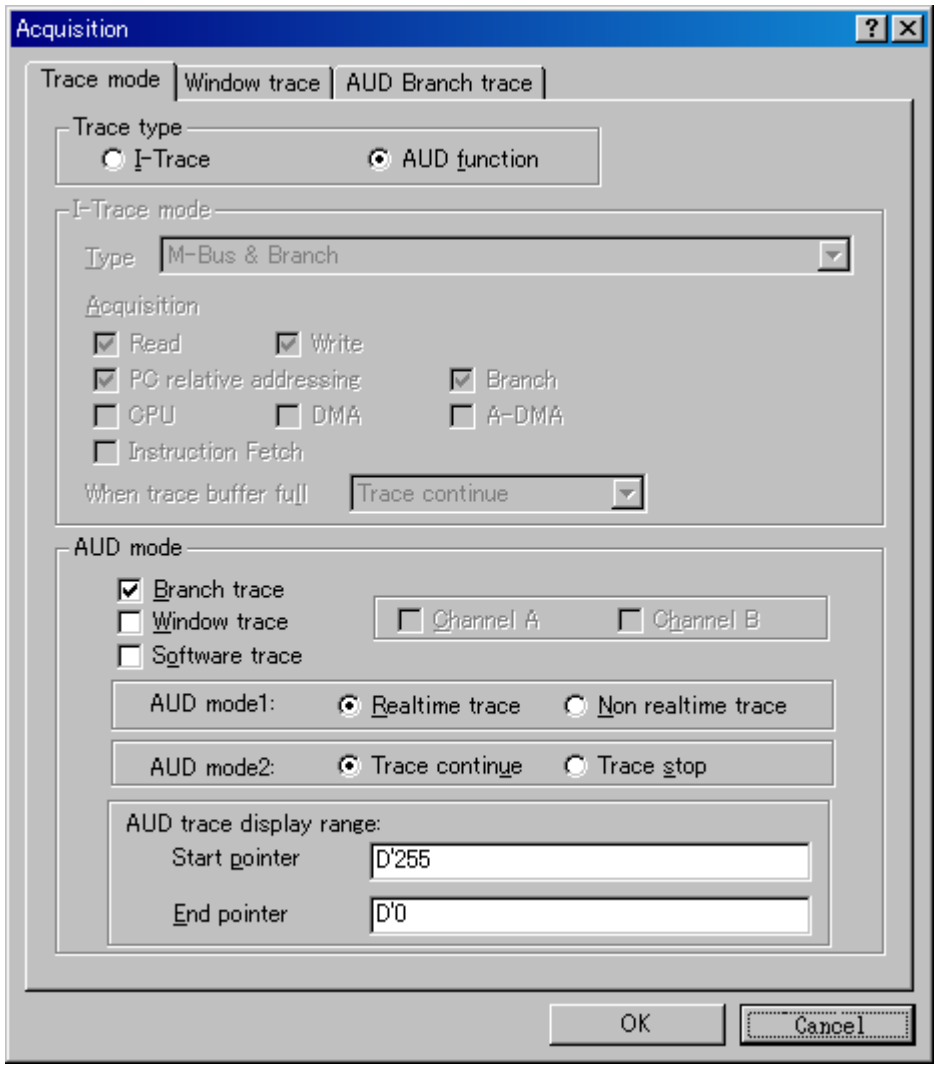


Figure 2.9 [Trace mode] Page

When the AUD trace function is used, select the [AUD function] radio button in the [Trace type] group box of the [Trace mode] page.

(a) Branch Trace Function

The branch source and destination addresses and their source lines are displayed.

Branch trace can be acquired by selecting the [Branch trace] check box in the [AUD function] group box of the [Trace mode] page.

The branch type can be selected in the [AUD Branch trace] page.

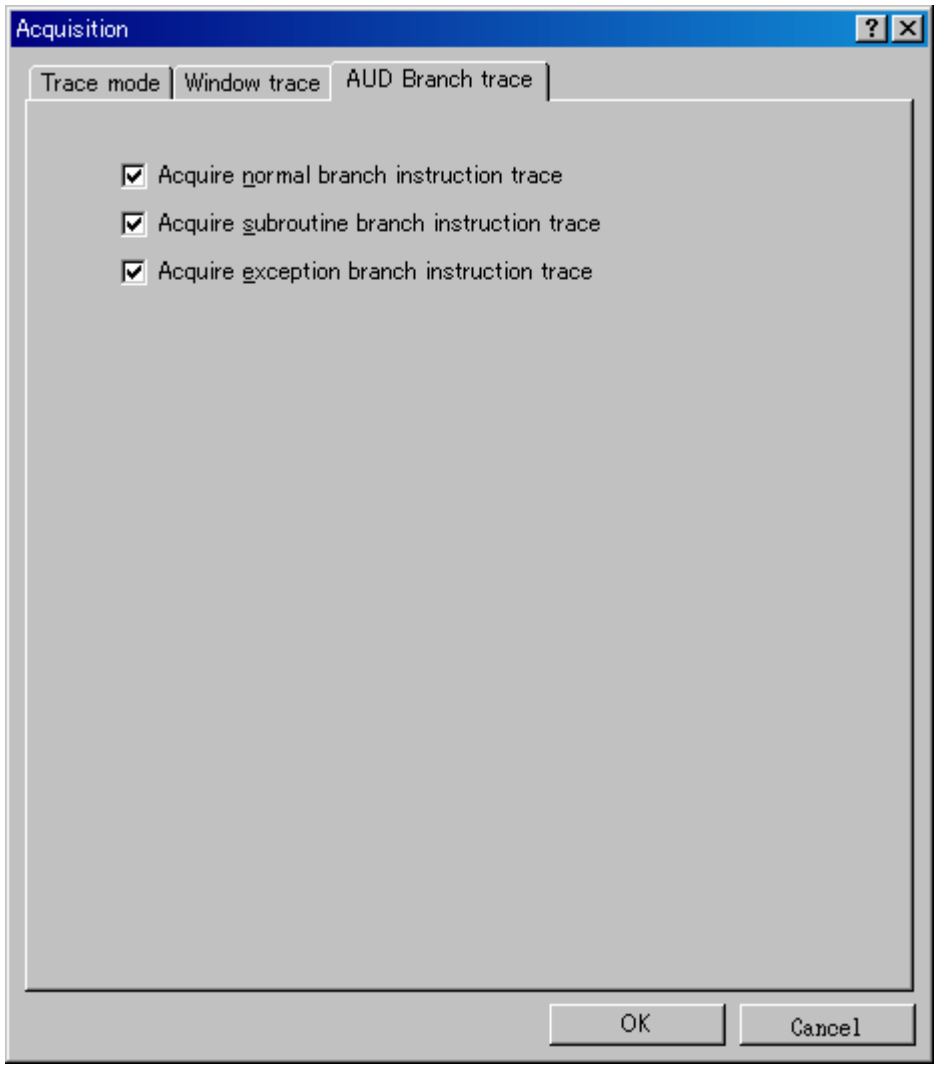


Figure 2.10 [AUD Branch trace] Page

(b) Window Trace Function

Memory access in the specified range can be acquired by trace.

Two memory ranges can be specified for channels A and B. The read, write, or read/write cycle can be selected as the bus cycle for trace acquisition.

[Setting Method]

(i) Select the [Channel A] and [Channel B] check boxes in the [AUD function] group box of the [Trace mode] page. Each channel will become valid.

(ii) Open the [Window trace] page and specify the bus cycle, memory range, and bus type that are to be set for each channel.

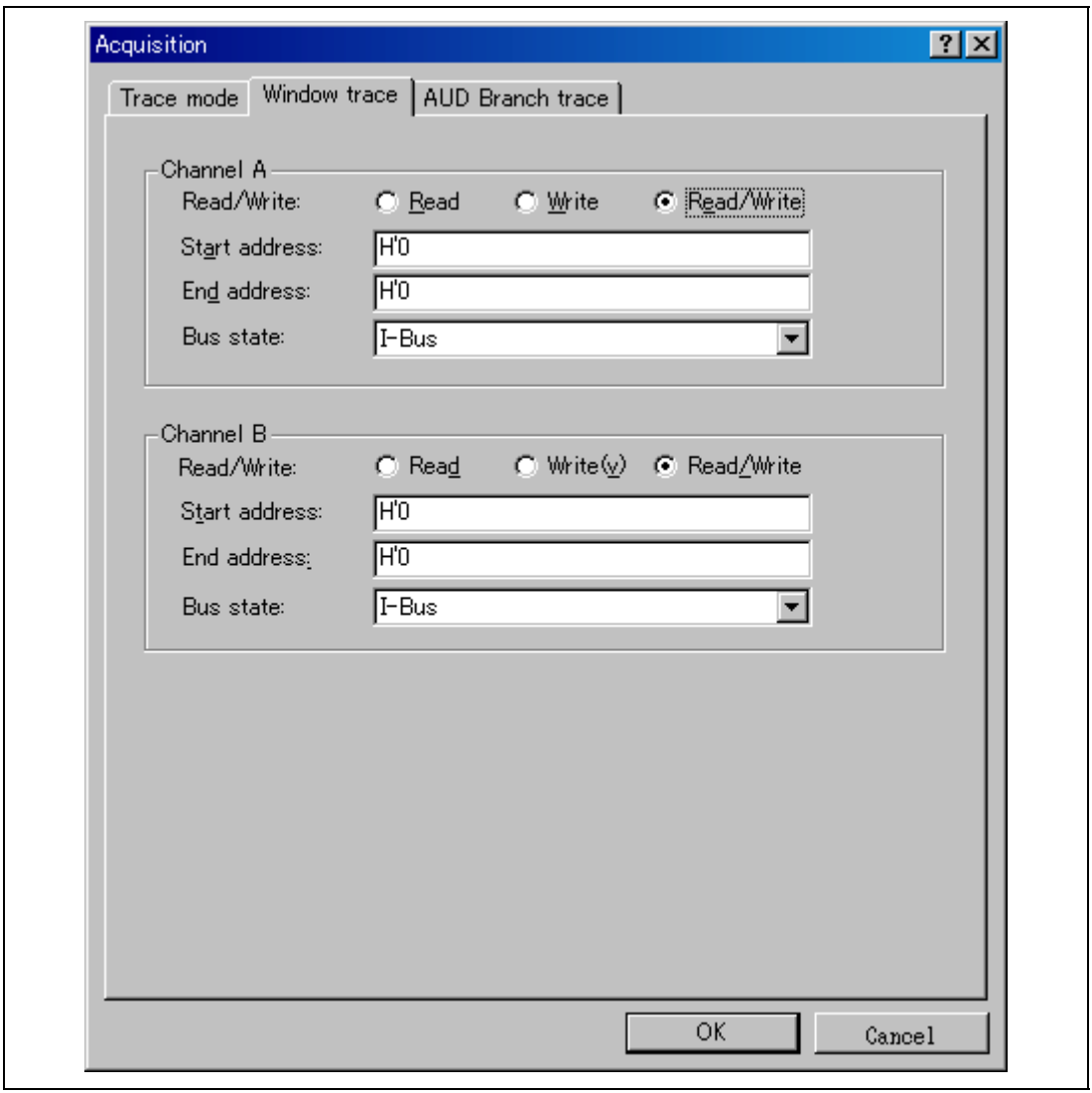


Figure 2.11 [Window trace] Page

Note: When [M-Bus] or [I-Bus] is selected, the following bus cycles will be traced.
- M-Bus: A bus cycle generated by the CPU is acquired.
- I-Bus: A bus cycle generated by the CPU or DMA is acquired.

(c) Software Trace Function

Note: This function can be supported with SHC/C++ compiler (manufactured by Renesas Electronics Corp.; including OEM and bundle products) V7.0 or later.

When a specific instruction is executed, the PC value at execution and the contents of one general register are acquired by trace. Describe the Trace(x) function (x is a variable name) to be compiled and linked beforehand. For details, refer to the SHC manual.

When the load module is downloaded on the target system and is executed while a software trace function is valid, the PC value that has executed the Trace(x) function, the general register value for x, and the source lines are displayed.

To activate the software trace function, select the [Software trace] check box in the [AUD function] group box of the [Trace mode] page.

(2) Notes on AUD Trace

1. When the trace display is performed during user program execution, the mnemonics, operands, or source is not displayed.
2. The AUD trace function outputs the differences between newly output branch source addresses and previously output branch source addresses. The window trace function outputs the differences between newly output addresses and previously output addresses. If the previous branch source address is the same as the upper 16 bits, the lower 16 bits are output. If it matches the upper 24 bits, the lower 8 bits are output. If it matches the upper 28 bits, the lower 4 bits are output.
   The emulator regenerates the 32-bit address from these differences and displays it in the [Trace] window. If the emulator cannot display the 32-bit address, it displays the difference from the previously displayed 32-bit address.
3. If the 32-bit address cannot be displayed, the source line is not displayed.
4. If a completion-type exception occurs during exception branch acquisition, the next address to the address in which an exception occurs is acquired.
5. The AUD trace is disabled while the profiling function is used.
6. Set the AUD clock (AUDCK) frequency to 40 MHz or lower. If the frequency is higher than 40 MHz, the emulator will not operate normally.
7. If breaks occur immediately after executing non-delayed branch and TRAPA instructions and generating a branch due to exception or interrupt, a trace for one branch will not be acquired

immediately before such breaks. However, this does not affect on generation of breaks caused by a BREAKPOINT and a break before executing instructions of Event Condition.

8. The CPU clock ratios 1:1 and 1:2 cannot be used for the AUD clock (AUDCK).

2.2.4 Notes on Using the JTAG (H-UDI) Clock (TCK)

1. Set the JTAG clock (TCK) frequency to lower than the frequency of the peripheral module clock.
2. The initial value of the JTAG clock (TCK) is 10 MHz.
3. A value to be set for the JTAG clock (TCK) is initialized after executing [Reset CPU] or [Reset Go]. Thus the TCK value will be the initial value.

2.2.5 Notes on Setting the [Breakpoint] Dialog Box

1. When an odd address is set, the next lowest even address is used.
2. A BREAKPOINT is accomplished by replacing instructions of the specified address. It cannot be set to the following addresses:
   - An area other than CS and the internal RAM
   - An instruction in which Break Condition 2 is satisfied
   - A slot instruction of a delayed branch instruction
3. During step operation, specifying BREAKPOINTs and Event Condition breaks are disabled.
4. When execution resumes from the address where a BREAKPOINT is specified and a break occurs before Event Condition execution, single-step operation is performed at the address before execution resumes. Therefore, realtime operation cannot be performed.
5. When a BREAKPOINT is set to the slot instruction of a delayed branch instruction, the PC value becomes an illegal value. Accordingly, do not set a BREAKPOINT to the slot instruction of a delayed branch instruction.
6. If an address of a BREAKPOINT cannot be correctly set in the ROM or flash memory area, a mark ● will be displayed in the [BP] area of the address on the [Source] or [Disassembly] window by refreshing the [Memory] window, etc. after Go execution. However, no break will occur at this address. When the program halts with the event condition, the mark ● disappears.

2.2.6 Notes on Setting the [Event Condition] Dialog Box and the BREAKCONDITION_SET Command

1. When [Go to cursor], [Step In], [Step Over], or [Step Out] is selected, the settings of Event Condition 3 are disabled.
2. When an Event Condition is satisfied, emulation may stop after two or more instructions have been executed.

2.2.7 Emulation RAM Setting Function

The emulation RAM can be set in the [Memory Mapping] dialog box which is opened by selecting [Setup] -> [Emulator] -> [Memory…] from the menu.

The emulator incorporates 8-block emulation RAM in each 64-kbyte unit, which can be set in each 64-kbyte boundary within the address ranges from H'00000000 to H'001FFFFF.

The emulation RAM is overlapped with the address of the internal flash memory. Using the emulation RAM proceeds debugging without rewriting the program or data on the internal flash memory.

When the emulation RAM is not used in the emulator, it can be used as the internal RAM for debugging. Note that this function is only supported by MCUs that have names ending with FCC.

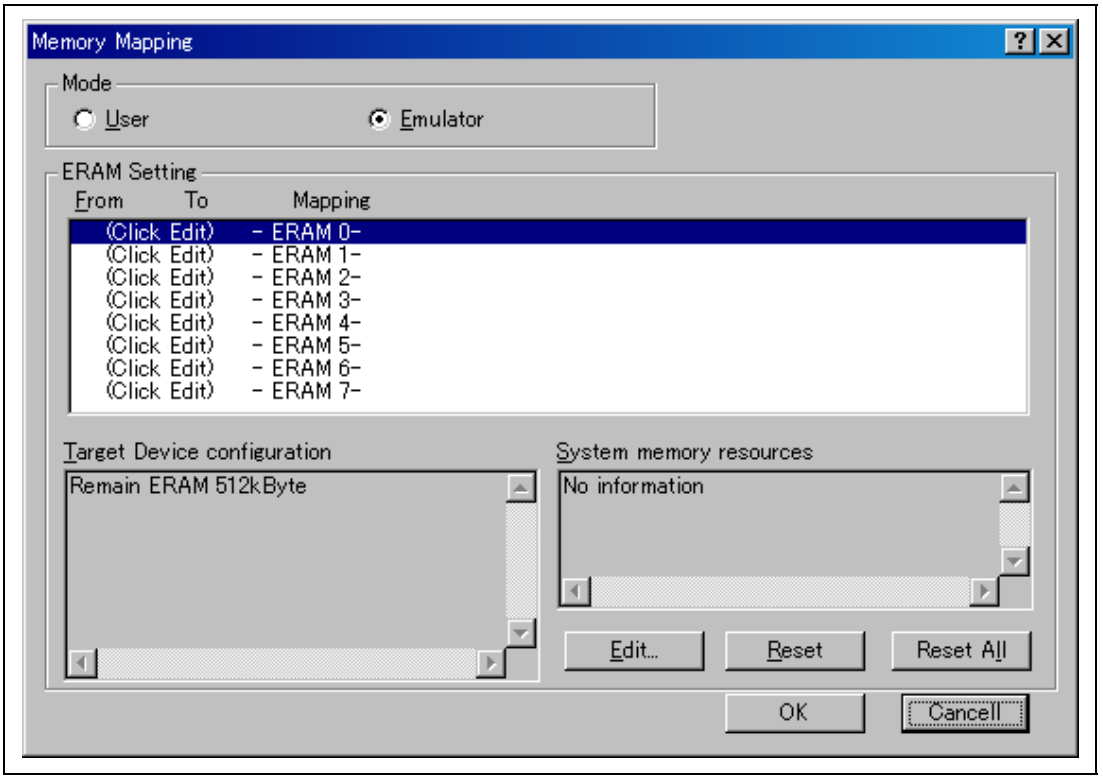


Figure 2.12 [Memory Mapping] Dialog Box

The contents of the [Memory Mapping] dialog box are shown below.

[Mode]		
	[User]	The emulator does not use the emulation RAM.
	[Emulator]	The emulator uses the emulation RAM.
[ERAM Setting]		
	[Edit…]	Open the dialog box for setting [Memory Mapping] to change the address ranges and attributes of the emulation RAM.
	[Reset]	Reset the selected emulation RAM as default.
	[Reset All]	Reset all emulation RAMs as default.
[OK]		Reflect changes and close the [Memory Mapping] dialog box.
[Cancel]		Reflect no changes and close the [Memory Mapping] dialog box.

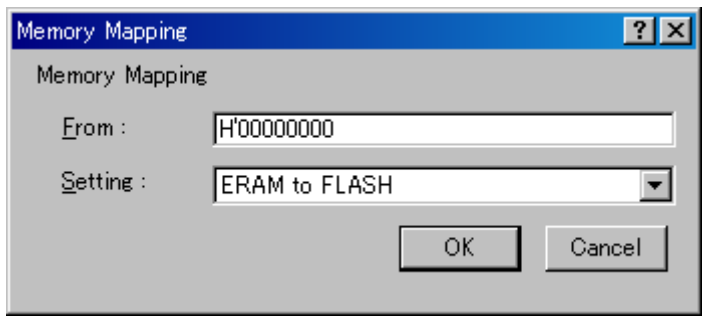


Figure 2.13 Dialog Box for Setting [Memory Mapping]

The contents of the dialog box for setting [Memory Mapping] are shown below.

[From:]		Enter the start address for the ranges.
[Setting:]		
	[ERAM to FLASH]	Reflect the contents of the emulation RAM in the internal flash memory when address allocation is cancelled.
	[ERAM not to FLASH]	Reflect no contents of the emulation RAM in the internal flash memory when address allocation is cancelled.
	[Reset All]	Reset all emulation RAMs as default.
[OK]		Reflect changes and close the dialog box for setting [Memory Mapping].
[Cancel]		Reflect no changes and close the dialog box for setting [Memory Mapping].

Notes: 1. Operation is not guaranteed in cases where registers of the ERAM module are manipulated from the [IO] window or in some other way.
2. For command-line syntax, refer to the online help file.
3. If an area of emulation RAM is not being used by the emulator, the user must not allocate that emulation RAM to a ROM area; instead use the emulation RAM in its original address area.
4. When using the emulation RAM, make the setting to disable flash memory synchronization on halting the user program.

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SH72567R and SH72567BFCC

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Renesas Electronics America Inc.
2880 Scott Boulevard Santa Clara, CA 95050-2554, U.S.A.
Tel: +1-408-588-6000, Fax: +1-408-588-6130

Renesas Electronics Canada Limited
1101 Nicholson Road, Newmarket, Ontario L3Y 9C3, Canada
Tel: +1-905-898-5441, Fax: +1-905-898-3220

Renesas Electronics Europe Limited
Dukes Meadow, Millboard Road, Bourne End, Buckinghamshire, SL8 5FH, U.K
Tel: +44-1628-651-700, Fax: +44-1628-651-804

Renesas Electronics Europe GmbH
Arcadiastrasse 10, 40472 Düsseldorf, Germany
Tel: +49-211-65030, Fax: +49-211-6503-1327

Renesas Electronics (China) Co., Ltd.
7th Floor, Quantum Plaza, No.27 ZhiChunLu Haidian District, Beijing 100083, P.R.China
Tel: +86-10-8235-1155, Fax: +86-10-8235-7679

Renesas Electronics (Shanghai) Co., Ltd.
Unit 204, 205, AZIA Center, No.1233 Lujiazui Ring Rd., Pudong District, Shanghai 200120, China
Tel: +86-21-5877-1818, Fax: +86-21-6887-7858 / -7898

Renesas Electronics Hong Kong Limited
Unit 1601-1613, 16/F., Tower 2, Grand Century Place, 193 Prince Edward Road West, Mongkok, Kowloon, Hong Kong
Tel: +852-2886-9318, Fax: +852 2886-9022/9044

Renesas Electronics Taiwan Co., Ltd.
13F, No. 363, Fu Shing North Road, Taipei, Taiwan
Tel: +886-2-8175-9600, Fax: +886 2-8175-9670

Renesas Electronics Singapore Pte. Ltd.
1 harbourFront Avenue, #06-10, keppel Bay Tower, Singapore 098632
Tel: +65-6213-0200, Fax: +65-6278-8001

Renesas Electronics Malaysia Sdn.Bhd.
Unit 906, Block B, Menara Amcorp, Amcorp Trade Centre, No. 18, Jln Persiaran Barat, 46050 Petaling Jaya, Selangor Darul Ehsan, Malaysia
Tel: +60-3-7955-9390, Fax: +60-3-7955-9510

Renesas Electronics Korea Co., Ltd.
11F., Samik Lavied' or Bldg., 720-2 Yeoksam-Dong, Kangnam-Ku, Seoul 135-080, Korea
Tel: +82-2-558-3737, Fax: +82-2-558-5141

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