User's Manual

SuperH™ Family E10A-USB Emulator

Additional Document for User's Manual

Supplementary Information on Using the SH72A2 and SH72A0 Group

SuperH™ Family

E10A-USB for SH72A2 and SH72A0 Group

HS72A2KCU01HE

Renesas Electronics
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Table of Contents

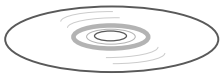
Section 1 Connecting the Emulator with the User System

1.1 Components of the Emulator

The E10A-USB emulator supports the SH72A2 and SH72A0 group.

Table 1.1 lists the components of the emulator.

Table 1.1 Components of the Emulator

Classi-fication	Component	Appearance	Quan-tity	Remarks
Hard-ware	Emulator box		1	HS0005KCU01H: Depth: 65.0 mm, Width: 97.0 mm, Height: 20.0 mm, Mass: 72.9 g or HS0005KCU02H: Depth: 65.0 mm, Width: 97.0 mm, Height: 20.0 mm, Mass: 73.7 g
	User system interface cable		1	14-pin type: Length: 20 cm, Mass: 33.1 g
	User system interface cable		1	36-pin type: Length: 20 cm, Mass: 49.2 g (only for HS0005KCU02H)
	USB cable		1	Length: 150 cm, Mass: 50.6 g
Soft-ware	E10A-USB emulator setup program, SuperH™ Family E10A-USB Emulator User's Manual, Supplementary Information on Using the SH72A2 and SH72A0 Group*, and Test program manual for HS0005KCU01H and HS0005KCU02H		1	HS0005KCU01SR, HS0005KCU01HJ, HS0005KCU01HE, HS72A2KCU01HJ, HS72A2KCU01HE, HS0005TM01HJ, and HS0005TM01HE (provided on a CD-R)

Note: Additional document for the MCUs supported by the emulator is included. Check the target MCU and refer to its additional document.

1.2 Connecting the Emulator with the User System

To connect the E10A-USB emulator (hereinafter referred to as the emulator), the H-UDI port connector must be installed on the user system to connect the user system interface cable. When designing the user system, refer to the recommended circuit between the H-UDI port connector and the MCU. In addition, read the E10A-USB emulator user's manual and hardware manual for the related device.

Table 1.2 shows the type number of the emulator, the corresponding connector type, and the use of AUD function.

Table 1.2 Type Number, AUD Function, and Connector Type

Type Number	Connector	AUD Function
HS0005KCU01H, HS0005KCU02H	14-pin connector	Not available

The H-UDI port connector has the 14-pin type as described below. Use it according to the purpose of the usage.

- 14-pin type (without AUD function)
  The AUD trace function cannot be used because only the H-UDI function is supported. For the trace function, only the internal trace is supported. Since the 14-pin type connector is smaller than the 36-pin type (1/2.5), the size of the area where the connector is installed on the user system can be reduced.

1.3 Installing the H-UDI Port Connector on the User System

Table 1.3 shows the recommended H-UDI port connectors for the emulator.

Table 1.3 Recommended H-UDI Port Connectors

Connector	Type Number	Manufacturer	Specifications
14-pin connector	2514-6002	Minnesota Mining & Manufacturing Ltd.	14-pin straight type

1.4 Pin Assignments of the H-UDI Port Connector

Figure 1.1 shows the pin assignments of the 14-pin H-UDI port connector.

Note: Note that the pin number assignments of the H-UDI port connector shown on the following pages differ from those of the connector manufacturer.

Pin No.	Signal		Input/ Output*1	Note
1	TCK		Input	
2	TRST#	*2	Input	
3	TDO		Output	
4	N.C.		——	
5	TMS		Input	
6	TDI		Input	
7	RES#	*2	Output	User reset
8	N.C.		——	
9	GND		——	
11	UVCC		Output	
10, 12, and 13	GND		——	
14	GND	*3	Output	

Notes: 1. Input to or output from the user system.
2. The symbol (#) means that the signal is active-low.
3. The emulator monitors the GND signal of the user system and detects whether or not the user system is connected.

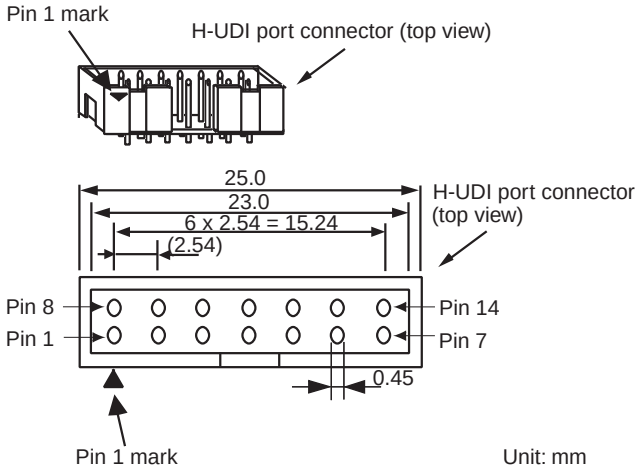


Figure 1.1 Pin Assignments of the H-UDI Port Connector (14 Pins)

1.5 Recommended Circuit between the H-UDI Port Connector and the MCU

1.5.1 Recommended Circuit (14-Pin Type)

Figure 1.2 shows a recommended circuit for connection between the H-UDI port connector (14 pins) and the MCU when the emulator is in use.

Notes:
1. Do not connect anything to the N.C. pins of the H-UDI port connector.
2. The ASEMD pin must be 1 when the emulator is connected and 0 when the emulator is not connected, respectively.
   (1) When the emulator is used: ASEMD = 1
   (2) When the emulator is not used: ASEMD = 0
   Figure 1.2 shows an example of circuits that allow the ASEMD pin to be changed by switches, etc.
3. When a network resistance is used for pull-up, it may be affected by a noise. Separate TCK from other resistances.
4. The pattern between the H-UDI port connector and the MCU must be as short as possible. Do not connect the signal lines to other components on the board.
5. Since the H-UDI of the MCU operates with the Vcc, supply only the Vcc to the UVCC pin. Make the emulator's switch settings so that the user power will be supplied (SW2 = 1 and SW3 = 1).
6. The resistance value shown in figure 1.2 is for reference.
7. For the pin processing in cases where the emulator is not used, refer to the hardware manual of the related MCU.

When the circuit is connected as shown in figure 1.2, the switches of the emulator are set as SW2 = 1 and SW3 = 1. For details, refer to section 3.8, Setting the DIP Switches, in the SuperH™ Family E10A-USB Emulator User's Manual.

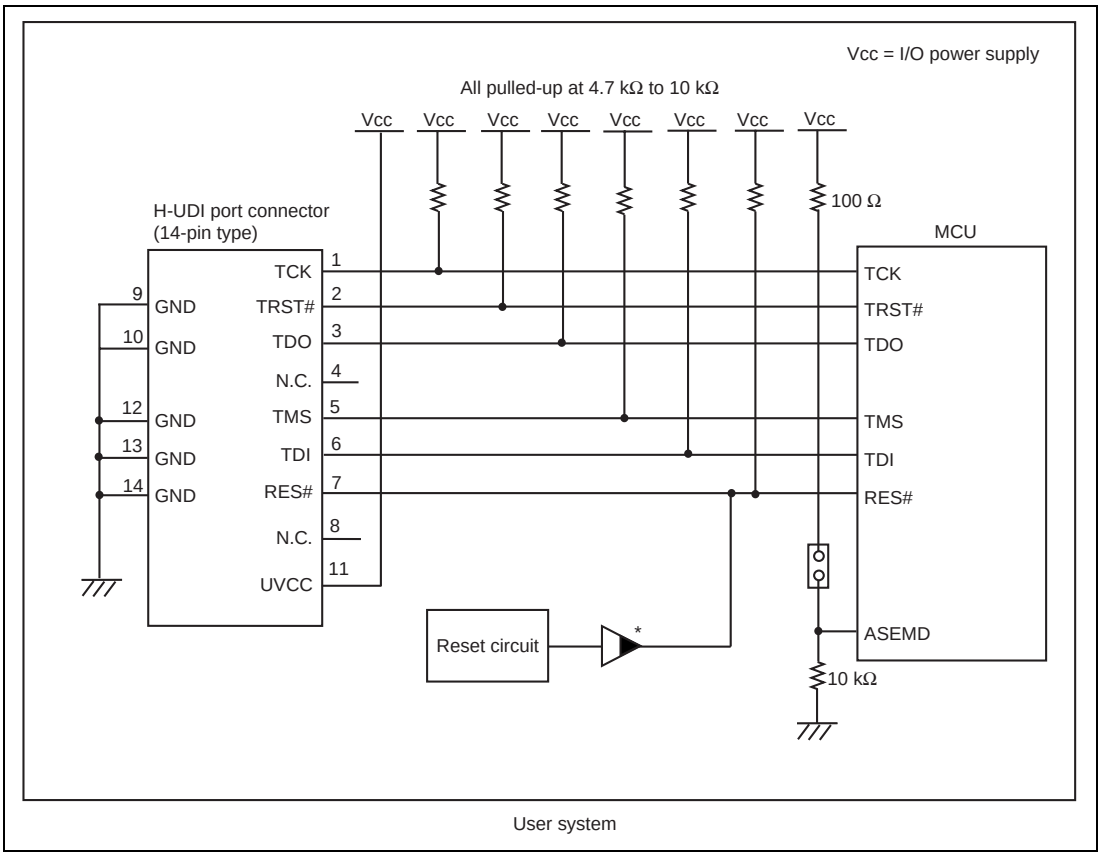


Figure 1.2 Recommended Circuit for Connection between the H-UDI Port Connector and MCU when the Emulator is in Use (14-Pin Type)

Note: If the function for the output of a reset signal from the emulator by selecting the [Reset assert (Auto Connect)] checkbox when the HEW is linked up is in use, the reset circuit of the user system must be configured for an open-drain output.

⚠CAUTION

If the reset circuit is not configured for an open-drain output, do not issue a reset signal from the emulator. Attempting to do so will cause a signal conflict, which may lead to a malfunction of the user system.

Section 2 Software Specifications when Using the Emulator

2.1 Differences between the SH72A2, SH72A0, and the Emulator

1. When the emulator system is initiated, it initializes the general registers and part of the control registers as shown in table 2.1. The initial values of the MCU are undefined.

Table 2.1 Register Initial Values at Emulator Link Up

Register	Emulator at Link Up
R0 to R14	H'00000000
R15 (SP)	Value of the SP in the power-on reset vector table
PC	Value of the PC in the power-on reset vector table
SR	H'000000F0
GBR	H'00000000
VBR	H'00000000
TBR	H'00000000
MACH	H'00000000
MACL	H'00000000
PR	H'00000000
FPSCR*	H'00040001
FPUL*	H'00000000
FPR0-15*	H'00000000

Note: If the MCU does not incorporate the floating-point unit (FPU), these registers are not displayed.

Note: When a value of the interrupt mask bit in the SR register is changed in the [Registers] window, it is actually reflected in that register immediately before execution of the user program is started. It also applies when the value is changed by the REGISTER_SET command.

2. The emulator uses the H-UDI; do not access the H-UDI.
3. Low-Power States
   — When the emulator is used, the sleep state can be cleared with either the clearing function or with the [STOP] button, and a break will occur.
   — Before stopping the supply of a clock signal to the FPU, be sure to use the command-line window to prohibit access to the FPU registers. Once this setting is made, H'FF is always indicated as the read value of each of the FPU registers in the register window, and writing becomes ineffective. For details, see [Help] -> [Emulator Help] -> [Command Line Interface] -> [FPU_ACCESS] on the menu bar of the High-performance Embedded Workshop.
4. Reset Signals

   The MCU reset signals are only valid during emulation started with clicking the GO or STEP-type button. If these signals are enabled on the user system in command input wait state, they are not sent to the MCU.

Note: Do not break the user program when the /RES signal is being low. A TIMEOUT error will occur.

5. Direct Memory Access Controller (DMAC)

   The DMAC operates even when the emulator is used. When a data transfer request is generated, the DMAC executes DMA transfer.

6. Memory Access during User Program Execution

   During execution of the user program, memory is accessed by the following two methods, as shown in table 2.2.

Table 2.2 Memory Access during User Program Execution

Method	Description
H-UDI read/write	The stopping time of the user program is short because memory is accessed by the dedicated bus master.
Short break	This method is not available for this product (do not set short break).

The method for accessing memory during execution of the user program is specified by using the [Configuration] dialog box.

Table 2.3 Stopping Time by Memory Access (Reference)

Method	Condition	Stopping Time
H-UDI read/write	Reading of one longword for the internal RAM	Reading: Maximum three bus clocks (Bϕ)
	Writing of one longword for the internal RAM	Writing: Maximum two bus clocks (Bϕ)
Short break	CPU clock: 100 MHz JTAG clock: 20 MHz Reading or writing of one longword for the external area	About 50 ms

7. Memory Access to the External Flash Memory Area

   The emulator can download the load module to the external flash memory area (for details, refer to section 6.22, Download Function to the Flash Memory Area, in the SuperH™ Family E10A-USB Emulator User's Manual). Other memory write operations are enabled for the RAM area. Therefore, an operation such as memory write or BREAKPOINT should be set only for the RAM area.

8. ROM Cache

   For ROM cache in the MCU, the emulator operates as shown in table 2.4.

Table 2.4 Operation for ROM Cache

Function	Operation
Write and erase of the flash memory	Writes or erases all contents of ROM cache.
Download of the program to the flash memory	
Memory read	Accesses the disabled cache area to read the content of internal flash memory.

9. Using WDT

   The WDT does not operate during break.

10. Loading Sessions

    Information in [JTAG clock] of the [Configuration] dialog box cannot be recovered by loading sessions. Thus the TCK value will be as follows:

    — When HS0005KCU01H or HS0005KCU02H is used: TCK = 2.5 MHz

11. [IO] Window

    — Customization of the I/O-register definition file

      The internal I/O registers can be accessed from the [IO] window. The I/O-register definition file for the SH72A2 and SH72A0 group does not include entries for all of the I/O registers described in the hardware manual.

      After the I/O-register definition file is created, the MCU's specifications may be changed. If each I/O register in the I/O-register definition file is at an address that differs from that given in the hardware manual, change the I/O-register definition file accordingly. The I/O-register definition file can be customized in accord with the prescribed format. Refer to appendix E, I/O File Formats, in the SuperH™ Family E10A-USB Emulator User's Manual, when modifying or customizing the file of I/O-register definitions. However, the emulator does not support the bit-field function.

      A file of I/O-register definitions is stored in the location below.

      \(Hew)\Tools\Renesas\DebugComp\Platform\E10A-USB\SH-2A\SH-2A_CUSTOM1 \IOFiles

      The location of the Hew folder will vary according to where the customer has installed it. As a default, the folder is installed in the C:\Program Files\Renesas\Hew folder.

    — Verify

      In the [IO] window, the verify function of the input value is disabled.

12. Illegal Instructions

    Do not execute illegal instructions with STEP-type commands.

13. Reset Input

    During execution of the user program, the emulator may not operate correctly if a contention occurs between the following operations for the emulator and the reset input to the target device:

    — Setting an Event Condition
    — Setting an internal trace
    — Displaying the content acquired by an internal trace
    — Reading or writing of a memory

    Note that those operations should not contend with the reset input to the target device.

14. MCU Operating Mode

    Note that the emulator does not support the boot mode.

    When starting up in the user boot mode, do not set a software breakpoint. Use an event point.

15. Writing Flash Memory Mode

    Writing flash memory mode is not supported for the SH72A2 and SH72A0.

16. ID Code

    ID codes are checked when starting up the emulator and when the CPU is reset (including in the case of [Reset Go] operations).

2.2 Specific Functions for the Emulator when Using the SH72A2 and SH72A0

2.2.1 Event Condition Functions

The emulator is used to set event conditions for the following three functions:

- Break of the user program
- Internal trace
- Start or end of performance measurement

Table 2.5 lists the types of Event Condition.

Table 2.5 Types of Event Condition

Event Condition Type	Description
Address bus condition (Address)	Sets a condition when the address bus (data access) value or the program counter value (before or after execution of instructions) is matched.
Data bus condition (Data)	Sets a condition when the data bus value is matched. Byte, word, or longword can be specified as the access data size.
Bus state condition (Bus State)	There are two bus state condition settings: Bus state condition: Sets a condition when the data bus value is matched. Read/Write condition: Sets a condition when the read/write condition is matched.
Count	Sets a condition when the specified other conditions are satisfied for the specified counts.
Reset point	A reset point is set when the count and the sequential condition are specified.
Action	Selects the operation when a condition (such as a break, a trace halt condition, or a trace acquisition condition) is matched.

Using the [Combination action (Sequential or PtoP)] dialog box specifies the sequential condition, the point-to-point of the internal trace, and the start or end of performance measurement.

Table 2.6 lists the combinations of conditions that can be set under Ch1 to Ch11.

Table 2.6 Dialog Boxes for Setting Event Conditions

		Function				
Dialog Box		**Address Bus Condition (Address)**	**Data Bus Condition (Data)**	**Bus State Condition (Bus Status)**	**Count Condition (Count)**	**Action**
[Event Condition 1]	Ch1	O	O	O	O	O (B, T1, and P)
[Event Condition 2]	Ch2	O	O	O	X	O (B, T1, and P)
[Event Condition 3]	Ch3	O	X	X	X	O (B and T2)
[Event Condition 4]	Ch4	O	X	X	X	O (B and T3)
[Event Condition 5]	Ch5	O	X	X	X	O (B and T3)
[Event Condition 6]	Ch6	O	X	X	X	O (B and T2)
[Event Condition 7]	Ch7	O	X	X	X	O (B and T2)
[Event Condition 8]	Ch8	O	X	X	X	O (B and T2)
[Event Condition 9]	Ch9	O	X	X	X	O (B and T2)
[Event Condition 10]	Ch10	O	X	X	X	O (B and T2)
[Event Condition 11]	Ch11	O (reset point)	X	X	X	X

Notes: 1. O: Can be set in the dialog box.
X: Cannot be set in the dialog box.

2. For the Action item,
B: Setting a break is enabled.
T1: Setting the trace halt and acquisition conditions are enabled for the internal trace.
T2: Setting the trace halt is enabled for the internal trace.
T3: Setting the trace halt and point-to-point is enabled for the internal trace.
P: Setting a performance-measurement start or end condition is enabled.
The [Event Condition 11] dialog box is used to specify the count of [Event Condition 1] and becomes a reset point when the sequential condition is specified.

(1) Sequential Setting

Using the [Combination action (Sequential or PtoP)] dialog box specifies the sequential condition and the start or end of performance measurement.

Table 2.7 Conditions to Be Set

Classification	Item	Description
[Ch1, 2, 3] list box	Sets the sequential condition and the start or end of performance measurement using Event Conditions 1 to 3 and 11.	
	Don't care	Sets no sequential condition or the start or end of performance measurement.
	Break: Ch3-2-1	Break in execution when Event Conditions 3, 2, and 1 are satisfied in that order.
	Break: Ch3-2-1, Reset point	Break in execution when Event Conditions 3, 2, and 1 are satisfied in that order. Enables the reset point of Event Condition 11.
	Break: Ch2-1	Break in execution when Event Conditions 2 and 1 are satisfied in that order.
	Break: Ch2-1, Reset point	Break in execution when Event Conditions 2 and 1 are satisfied in that order. Enables the reset point.
	I-Trace stop: Ch3-2-1	Halts acquisition of an internal trace when Event Conditions 3, 2, and 1 are satisfied in that order.
	I-Trace stop: Ch3-2-1, Reset point	Halts acquisition of an internal trace when Event Conditions 3, 2, and 1 are satisfied in that order. Enables the reset point.
	I-Trace stop: Ch2-1	Halts acquisition of an internal trace when Event Conditions 2 and 1 are satisfied in that order.
	I-Trace stop: Ch2-1, Reset point	Halts acquisition of an internal trace when Event Conditions 2 and 1 are satisfied in that order. Enables the reset point.
	Ch2 to Ch1 PA	Sets the performance measurement period during the time from the satisfaction of the condition set in Event Condition 2 (start condition) to the satisfaction of the condition set in Event Condition 1 (end condition).

Table 2.7 Conditions to Be Set (cont)

Classification	Item	Description
[Ch1, 2, 3] list box (cont)	Ch1 to Ch2 PA	Sets the performance measurement period during the time from the satisfaction of the condition set in Event Condition 1 (start condition) to the satisfaction of the condition set in Event Condition 2 (end condition).
[Ch4, 5] list box	Sets the point-to-point of the internal trace (the start or end condition of trace acquisition) using Event Conditions 4 and 5.	
	Don't care	Sets no start or end condition of trace acquisition.
	I-Trace: Ch5 to Ch4 PtoP*	Sets the acquisition period during the time from the satisfaction of the condition set in Event Condition 5 (start condition) to the satisfaction of the condition set in Event Condition 4 (end condition).
	I-Trace: Ch5 to Ch4 PtoP, power-on reset	Sets the acquisition period during the time from the satisfaction of the condition set in Event Condition 5 (start condition) to the satisfaction of the condition set in Event Condition 4 (end condition) or the power-on reset.

- After the sequential condition and the count specification condition of Event Condition 1 have been set, break and trace acquisition will be halted if the sequential condition is satisfied for the specified count.
- If a reset point is satisfied, the satisfaction of the condition set in Event Condition will be disabled. For example, if the condition is satisfied in the order of Event Condition 3, 2, reset point, 1, the break or trace acquisition will not be halted. If the condition is satisfied in the order of Event Condition 3, 2, reset point, 3, 2, 1, the break and trace acquisition will be halted.
- If the start condition is satisfied after the end condition has been satisfied by measuring performance, performance measurement will be restarted. For the measurement result after a break, the measurement results during performance measurement are added.
- If the start condition is satisfied after the end condition has been satisfied by the point-to-point of the internal trace, trace acquisition will be restarted.

(2) Usage Example of Sequential Break Extension Setting

A tutorial program provided for the product is used as an example. For the tutorial program, refer to section 6, Tutorial, in the SuperH™ Family E10A-USB Emulator User's Manual.

The conditions of Event Condition are set as follows:

1. Ch3

   Breaks address H'00001088 when the condition [Only program fetched address after] is satisfied.
2. Ch2

   Breaks address H'000010B0 when the condition [Only program fetched address after] is satisfied.
3. Ch1

   Breaks address H'000010F2 when the condition [Only program fetched address after] is satisfied.

   Note: Do not set other channels.
4. Sets the content of the [Ch1,2,3] list box to [Break: Ch 3-2-1] in the [Combination action (Sequential or PtoP)] dialog box.
5. Enables the condition of Event Condition 1 from the popup menu by clicking the right mouse button on the [Event Condition] sheet.

Then, set the program counter and stack pointer (PC = H'00000800, R15 = H'FFF90000) in the [Registers] window and click the [Go] button. If this does not execute normally, issue a reset and execute the above procedures.

The program is executed up to the condition of Ch1 and halted. Here, the condition is satisfied in the order of Ch3 -> 2 -> 1.

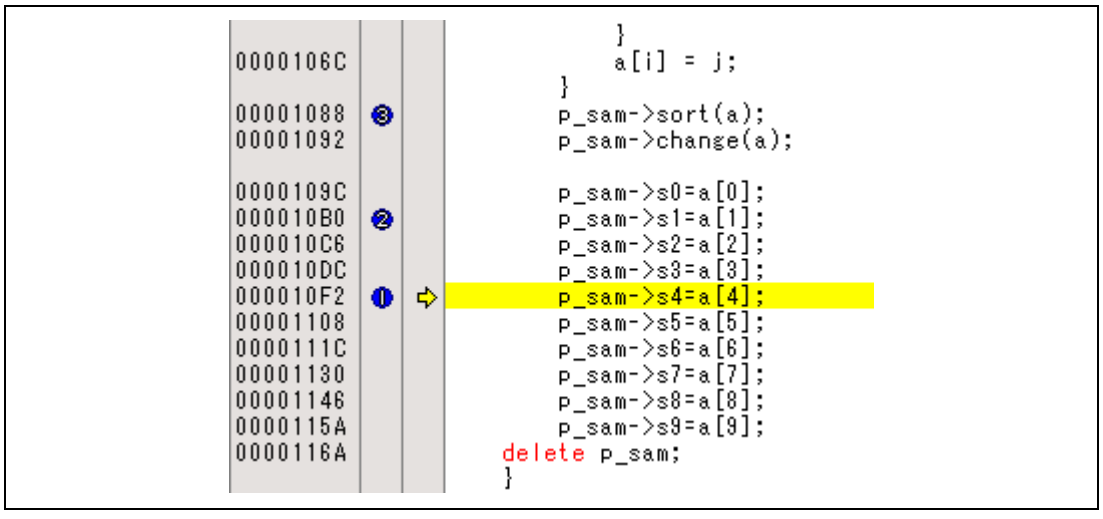


Figure 2.1 [Source] Window at Execution Halted (Sequential Break)

If the sequential condition, performance measurement start/end, or point-to-point for the internal trace is set, conditions of Event Condition to be used will be disabled. Such conditions must be enabled from the popup menu by clicking the right mouse button on the [Event Condition] sheet.

Notes: 1. If the Event condition is set for the slot in the delayed branch instruction by the program counter (after execution of the instruction), the condition is satisfied before executing the instruction in the branch destination (when a break has been set, it occurs before executing the instruction in the branch destination).

2. Do not set the Event condition for the SLEEP instruction by the program counter (after execution of the instruction).
3. When the Event condition is set for the 32-bit instruction by the program counter, set that condition in the upper 16 bits of the instruction.
4. If the power-on reset and the Event condition are matched simultaneously, no condition will be satisfied.
5. Do not set the Event condition for the DIVU or DIVS instruction by the program counter (after execution of the instruction).
6. If a condition of which intervals are satisfied closely is set, no sequential condition will be satisfied.
   - Set the Event conditions, which are satisfied closely, by the program counter with intervals of two or more instructions.
   - After the Event condition has been matched by accessing data, set the Event condition by the program counter with intervals of 17 or more instructions.
7. If the settings of the Event condition or the sequential conditions are changed during execution of the program, execution will be suspended. (The number of clocks to be suspended during execution of the program is a maximum of about 18 peripheral clocks (Pϕ). If the peripheral clock (Pϕ) is 66.6 MHz, the program will be suspended for 0.27 μs.)
8. If the settings of Event conditions or the sequential conditions are changed during execution of the program, the emulator temporarily disables all Event conditions to change the settings. During this period, no Event condition will be satisfied.
9. If the break condition before executing an instruction is set to the instruction followed by DIVU and DIVS, the factor for halting a break will be incorrect under the following condition:
   - If a break occurs during execution of the above DIVU and DIVS instructions, the break condition before executing an instruction, which has been set to the next instruction, may be displayed as the factor for halting a break.
10. If the break conditions before and after executing instructions are set to the same address, the factor for halting a break will be incorrectly displayed. The factor for halting a break due to the break condition after executing an instruction will be displayed even if a break is halted by the break condition before executing an instruction.
11. Do not set the break condition after executing instructions and BREAKPOINT (software break) to the same address.
12. When the emulator is being connected, the user break controller (UBC) function is not available.

2.2.2 Trace Functions

The emulator supports the trace functions listed in table 2.8.

Table 2.8 Trace Functions

Function	Internal Trace
Branch trace	Supported
Memory access trace	Supported
Software trace	Not supported

(1) Internal Trace Function

When [I-Trace] is selected for [Trace type] on the [Trace Mode] page of the [Acquisition] dialog box, the internal trace can be used.

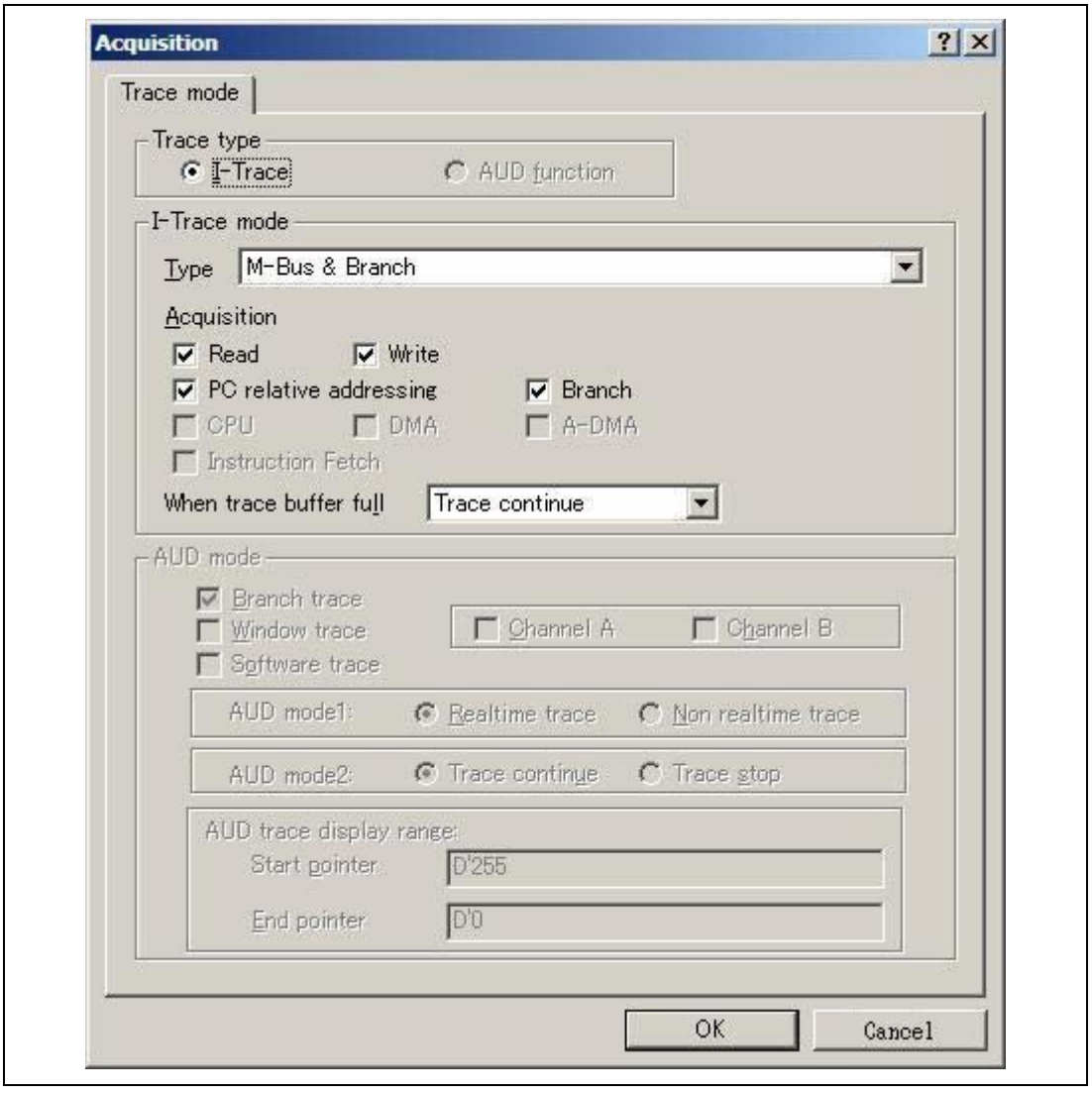


Figure 2.2 [Acquisition] Dialog Box – Internal Trace Function

The following six items can be selected as the internal trace from [Type] of [I-Trace mode].

Table 2.9 Information on Acquiring the Internal Trace

Item	Acquisition Information
[M-Bus & Branch]	Acquires the data and branch information on the M-bus. • Data access (read/write) • PC-relative access • Branch information
[I-Bus]	Acquires the data on the I-bus. • Data access (read/write) • Selection of the bus master on the I-bus (CPU/DMA/A-DMA) • Instruction fetch • When the cache is on, fetching proceeds for non-cacheable areas and when there is a cache miss. • When the cache is off, fetching from the external area.
[F-Bus]	Acquires the instruction fetch information on the F-bus. • Instruction fetch
[I-Bus, M-Bus & Branch]	Acquires the contents of [M-Bus & Branch] and [I-Bus].
[F-Bus, M-Bus & Branch]	Acquires the contents of [M-Bus & Branch] and [F-Bus].
[I-Bus, F-Bus]	Acquires the contents of [I-Bus] and [F-Bus].

After selecting [Type] of [I-Trace mode], select the content to be acquired from [Acquisition]. Typical examples are described below (note that items disabled for [Acquisition] are not acquired).

- Example of acquiring branch information only:
  Select [M-Bus & Branch] from [Type] and enable [Branch] on [Acquisition].
- Example of acquiring the read or write access (M-bus) only by a user program:
  Select [M-Bus & Branch] from [Type] and enable [Read] and [Write] on [Acquisition].
- Example of acquiring the read access only by DMA (I-bus):
  Select [I-Bus] from [Type] and enable [Read] and [DMA] on [Acquisition].

Using Event Condition restricts the condition; the following three items are set as the internal trace conditions.

Table 2.10 Trace Conditions of the Internal Trace

Item	Acquisition Information
Trace halt	Acquires the internal trace until the Event Condition is satisfied. (The trace content is displayed in the [Trace] window after a trace has been halted. No break occurs in the user program.)
Trace acquisition	Acquires only the data access where the Event Condition is satisfied.
Point-to-point	Traces the period from the satisfaction of Event Condition 5 to the satisfaction of Event Condition 4.

To restrict trace acquisition to access for only a specific address or specific function of a program, an Event Condition can be used. Typical examples are described below.

- Example of halting a trace with a write access (M-bus) to H'FFF80000 by the user program as a condition (trace halt):

  Set the condition to be acquired on [I-Trace mode].

  Set the following in the [Event Condition 1] or [Event Condition 2] dialog box:

  Address condition: Set [Address] and H'FFF80000.

  Bus state condition: Set [M-Bus] and [Write].

  Action condition: Deselect the [Acquire Break] checkbox and select [Stop] from the [Acquire Trace] list box.

- Example of acquiring the write access (M-bus) only to H'FFF80000 by the user program (trace acquisition condition):

  Select [M-Bus & Branch] from [Type] and enable [Write] on [Acquisition].

  Set the following in the [Event Condition 1] or [Event Condition 2] dialog box:

  Address condition: Set [Address] and H'FFF80000.

  Bus state condition: Set [M-Bus] and [Write].

  Action condition: Deselect the [Acquire Break] checkbox and select [Condition] from the [Acquire Trace] list box.

  For the trace acquisition condition, the condition to be acquired by Event Condition should be acquired by [I-Trace mode].

- Example of acquiring a trace for the period while the program passes H'1000 through H'2000 (point-to-point):

  Set the condition to be acquired on [I-Trace mode].

  Set the address condition as H'1000 in the [Event Condition 5] dialog box.

  Set the address condition as H'2000 in the [Event Condition 4] dialog box.

  Set [I-Trace] as [Ch5 to Ch4 PtoP] in the [Combination action (Sequential or PtoP)] dialog box.

  When point-to-point and trace acquisition condition are set simultaneously, they are ANDed.

(2) Notes on Internal Trace

- Timestamp

  The timestamp is the clock counts of Pϕ (48-bit counter). Table 2.11 shows the timing for acquiring the timestamp.

Table 2.11 Timing for the Timestamp Acquisition

Item	Acquisition Information	Counter Value Stored in the Trace Memory
M-bus data access		Counter value when data access (read or write) has been completed
Branch		Counter value when the next bus cycle has been completed after a branch
I-bus	Fetch	Counter value when a fetch has been completed
	Data access	Counter value when data access has been completed
F-bus	Fetch	Counter value when a fetch has been completed

- Point-to-point

  The trace-start condition is satisfied when the specified instruction has been fetched. Accordingly, if the trace-start condition has been set for the overrun-fetched instruction (an instruction that is not executed although it has been fetched at a branch or transition to an interrupt), tracing is started during overrun-fetching of the instruction. However, when overrun-fetching is achieved (a branch is completed), tracing is automatically suspended.
  If the start and end conditions are satisfied closely, trace information will not be acquired correctly.
  The execution cycle of the instruction fetched before the start condition is satisfied may be traced.
  When the I-bus is acquired, do not specify point-to-point.
  Memory access may not be acquired by the internal trace if it occurs at several instructions immediately before satisfaction of the point-to-point end condition.

- Halting a trace

  Do not set the trace end condition for the sleep instruction and the branch instruction that the delay slot becomes the sleep instruction.

- Trace acquisition condition

  Do not set the trace end condition for the sleep instruction and the branch instruction according to which the delay slot becomes the sleep instruction.
  When [F-Bus], [F-Bus, M-Bus & Branch], or [I-Bus, F-Bus] is selected, do not set the trace acquisition condition for [Event Condition 1] and [Event Condition 2]. If a trace acquisition condition is set, no trace will be acquired.
  When [I-Bus, M-Bus & Branch] is selected and the trace acquisition condition is set for the M-bus and I-bus with Event Condition, set the M-bus condition and the I-bus condition for [Event Condition 1] and [Event Condition 2], respectively.
  When matching of the program counter value is a condition of Event Condition for internal trace acquisition (i.e. [Only program fetched address] or [Only program fetched address after] is selected), do not specify addresses in the on-chip ROM or on-chip RAM as the address condition.
  If you specify a break (by selecting the [Acquire Break] checkbox) and trace acquisition (by selecting [Condition] from the [Acquire Trace] list box) on the [Action] page as the action to take when a condition of Event Condition is satisfied, setting of the trace acquisition will be ignored.
  If the settings of [I-Trace mode] are changed during execution of the program, execution will be suspended. (The number of clocks to be suspended during execution of the program is a maximum of about 24 peripheral clocks (Pϕ). If the peripheral clock (Pϕ) is 66.6 MHz, the program will be suspended for 0.36 μs.)

- Displaying a trace

  If a trace is displayed during execution of the program, execution will be suspended to acquire the trace information. (The number of clocks to be suspended during execution of the program is a maximum of about 5120 peripheral clocks (Pϕ). If the peripheral clock (Pϕ) is 66.6 MHz, the program will be suspended for 76.87 μs.)

- Branch trace

  If breaks occur immediately after executing non-delayed branch and TRAPA instructions and generating a branch due to exception or interrupt, a trace for one branch will not be acquired immediately before such breaks.
  However, this does not affect on generation of breaks caused by a BREAKPOINT and a break before executing instructions of Event Condition.

- Writing memory immediately before generating a break

  If an instruction is executed to write memory immediately before generating a break, trace acquisition may not be performed.

2.2.3 Notes on Using the JTAG (H-UDI) Clock (TCK)

1. Set the JTAG clock (TCK) frequency to lower than 20 MHz and the frequency of the peripheral module clock.
2. The initial value of the JTAG clock (TCK) is 2.5 MHz.
3. A value to be set for the JTAG clock (TCK) is initialized after executing [Reset CPU] or [Reset Go]. Thus the TCK value will be the initial value.

2.2.4 Notes on Setting the [Breakpoint] Dialog Box

1. When an odd address is set, the next lowest even address is used.
2. A BREAKPOINT is accomplished by replacing instructions of the specified address.
   It cannot be set to the following addresses:
   — An area other than CS and the internal RAM
   — An instruction in which Break Condition 2 is satisfied
   — A slot instruction of a delayed branch instruction
3. During step operation, specifying BREAKPOINTs and Event Condition breaks are disabled.
4. When execution resumes from the address where a BREAKPOINT is specified and a break occurs before Event Condition execution, single-step operation is performed at the address before execution resumes. Therefore, realtime operation cannot be performed.
5. When a BREAKPOINT is set to the slot instruction of a delayed branch instruction, the PC value becomes an illegal value. Accordingly, do not set a BREAKPOINT to the slot instruction of a delayed branch instruction.
6. If an address of a BREAKPOINT cannot be correctly set in the ROM or flash memory area, a mark ● will be displayed in the [BP] area of the address on the [Source] or [Disassembly] window by refreshing the [Memory] window, etc. after Go execution. However, no break will occur at this address. When the program halts with the event condition, the mark ● disappears.

2.2.5 Notes on Setting the [Event Condition] Dialog Box and the BREAKCONDITION_SET Command

1. When [Go to cursor], [Step In], [Step Over], or [Step Out] is selected, the settings of Event Condition 3 are disabled.
2. When an Event Condition is satisfied, emulation may stop after two or more instructions have been executed.

2.2.6 Performance Measurement Function

The emulator supports the performance measurement function.

(1) Setting the Performance Measurement Conditions

To set the performance measurement conditions, use the [Performance Analysis] dialog box and the PERFORMANCE_SET command. When any line in the [Performance Analysis] window is clicked with the right mouse button, a popup menu is displayed and the [Performance Analysis] dialog box can be displayed by selecting [Setting].

Note: For the command line syntax, refer to the online help.

(a) Specifying the Measurement Start/End Conditions

The measurement start/end conditions are specified by using Event Condition 1,2. The [Ch1,2,3] list box of the [Combination action (Sequential or PtoP)] dialog box can be used.

Table 2.12 Measurement Period

Classification	Item	Description
Selection in the [Ch1, 2, 3] list box	Ch2 to Ch1 PA	The period from the satisfaction of the condition set in Event Condition 2 (start condition) to the satisfaction of the condition set in Event Condition 1 (end condition) is set as the performance measurement period.
	Ch1 to Ch2 PA	The period from the satisfaction of the condition set in Event Condition 1 (start condition) to the satisfaction of the condition set in Event Condition 2 (end condition) is set as the performance measurement period.
	Other than above	The period from the start of execution of the user program to the occurrence of a break is measured.

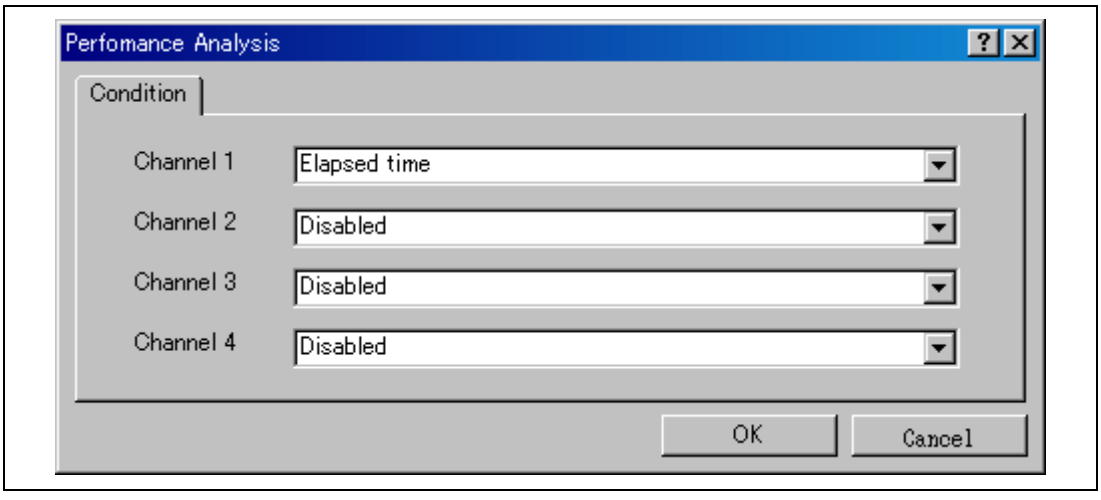


Figure 2.3 [Performance Analysis] Dialog Box

Regarding Errors in Measurement

Errors in the results of the performance measurement function for numbers of cycles of execution are incurred immediately before the start of execution and immediately after a break. The errors differ according to the conditions that are in use. The procedure for evaluating the error is described below.

Procedure

Execute an NOP instruction in the internal RAM area and measure the error by calculating the difference between the result for the number of cycles of execution and the logical value.

This is explained below with an example for the location H'FFF80000 in the internal RAM area and one read cycle set for the RAM area.

1. Change H'FFF80000 to an NOP instruction.
2. Set the PC to H'FFF80000 in the [Register] window.
3. Set the measurement condition for Ch1 to Elapsed time (the number of cycles for execution) in the [Performance Analysis] window.
4. Click on the [Step in] button of the High-performance Embedded Workshop.
5. Check the value in the performance counter following the break.

Executing an NOP instruction in the internal RAM area entails one cycle for reading from that area, so the logical value for the number of cycles will be 1.
When the counter value for the number of cycles is 42, the error can be acquired from the following formula.

Result of the measured number of cycles for execution – logical value of the number of cycles (number of cycles of access to the internal RAM) = 42 - 1 = 41

Note: When [Ch2 to Ch1 PA] or [Ch1 to Ch2 PA] is selected, to execute the user program, specify conditions set in Event Condition 2 and Event Condition 1 and one or more items for performance measurement.

(b) Measurement Item

Items are measured with [Channel 1 to 4] in the [Performance Analysis] dialog box. Maximum four conditions can be specified at the same time.

Table 2.13 Measurement Item

Selected Name	Option
Disabled	None
Elapsed time	AC (The number of execution cycles (Iϕ).)
Branch instruction counts	BT
Number of execution instructions	I
Number of execution 32bit-instructions	I32
Exception/interrupt counts	EA
Interrupt counts	INT
Data cache-miss counts	DC
Instruction cache-miss counts	IC
All area access counts	ARN
All area instruction access counts	ARIN
All area data access counts	ARND
Cacheable area access counts	CDN (data access)
Cacheable area instruction access counts	CIN
Non cacheable area data access counts	NCN
URAM area access counts	UN
URAM area instruction access counts	UIN
URAM area data access counts	UDN
Internal I/O area data access counts	IODN
Internal ROM area access counts	RN
Internal ROM area instruction access counts	RIN
Internal ROM area data access counts	RDN
All area access cycle	ARC
All area instruction access cycle	ARIC
All area data access cycle	ARDC
All area access stall	ARS
All area instruction access stall	ARIS
All area data access stall	ARDS

Note: Selected names are displayed for CONDITION in the [Performance Analysis] window. Options are parameters for <mode> of the PERFORMANCE_SET command.

Notes: 1. In the non-realtime trace mode of the AUD trace, normal counting cannot be performed because the generation state of the stall or the execution cycle is changed.

2. Even when [Exception/interrupt counts (EA)] is selected as the measurement item, no trap-instruction exception caused by TRAPA instructions will be counted.

(2) Displaying the Measured Result

The measured result is displayed in the [Performance Analysis] window or the PERFORMANCE_ANALYSIS command with hexadecimal (32 bits).

Note: If a performance counter overflows as a result of measurement, "********" will be displayed.

(3) Initializing the Measured Result

To initialize the measured result, select [Initialize] from the popup menu in the [Performance Analysis] window or specify INIT with the PERFORMANCE_ANALYSIS command.

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Additional Document for User's Manual
Supplementary Information on Using the SH72A2 and SH72A0 Group

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Colophon 1.2

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