BCPX3 Evaluation Kit

PLC Evaluation Board Design Guideline

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Introduction

This document is a design guide that is described about attentions to parts placement, PCB layout and wiring of PLC evaluation board with PLC modem LSI (CPX3), Power Amp (ISL15110) and power supply IC for a direct current power line communication (DC PLC) and in reference to BCPX3 Evaluation kit. PLC evaluation board has two kinds of a drive method, CPX3 direct drive (after, CPX drive) type or CPX3+Power Amp drive (after, PA drive) type. As for the PA drive, an output level has a bigger 20dB than CPX drive, PA drive is used in a case with long transmission distance or many connection number. This document explains it when you use each drive type.

[Note]

The attention to describe with this document made the PLC board of BCPX3 evaluation kit J80D1 and J80D2 an example. Depending on board size, parts, layout of a customer's evaluation board, there is the case that is not necessarily effective.

Contents

1. The circuit constitution by the drive type

This chapter shows circuit constitution of CPX drive and PA drive to Figure 1-1, Figure 1-2.

1.1 CPX drive (CPX3 direct drive)

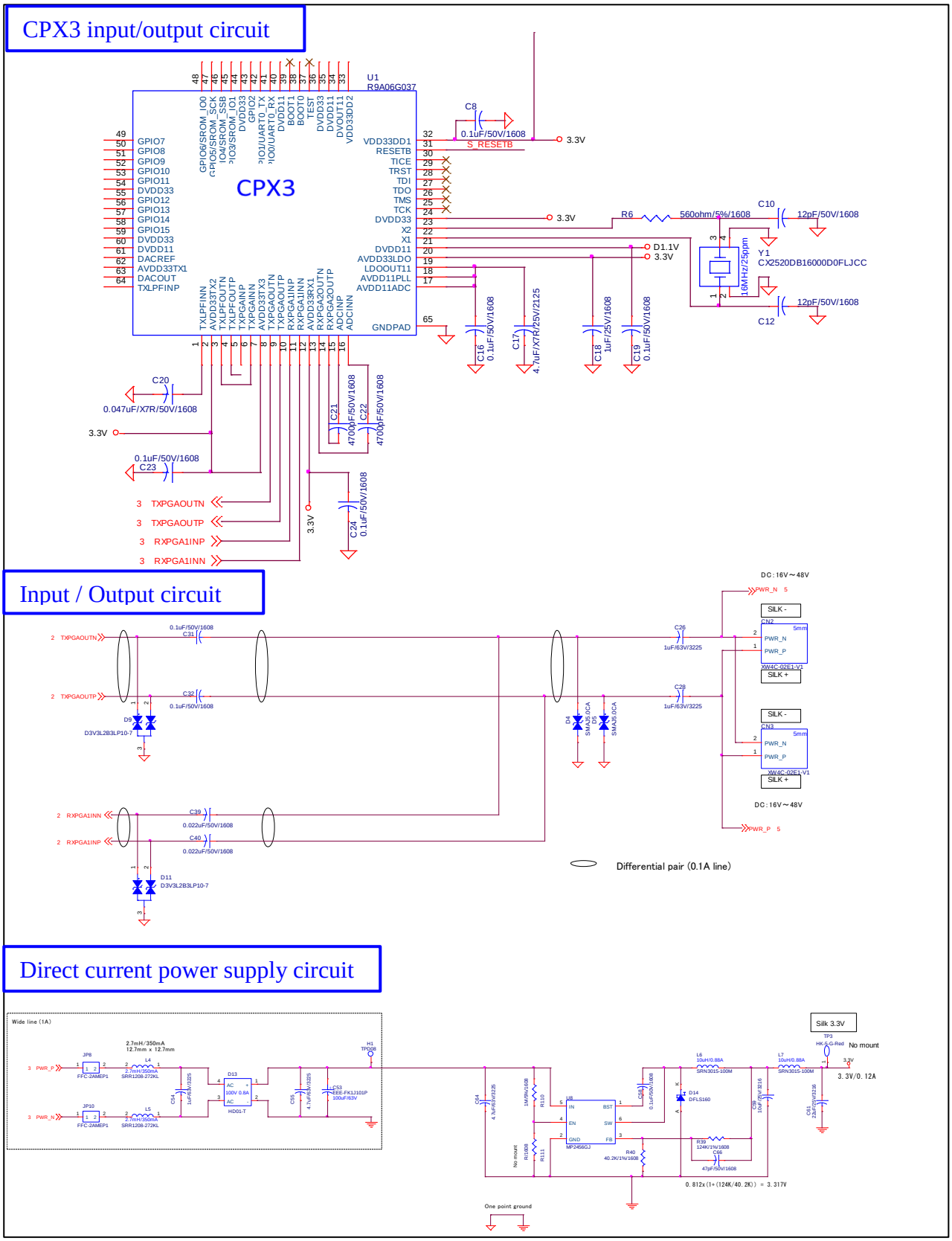
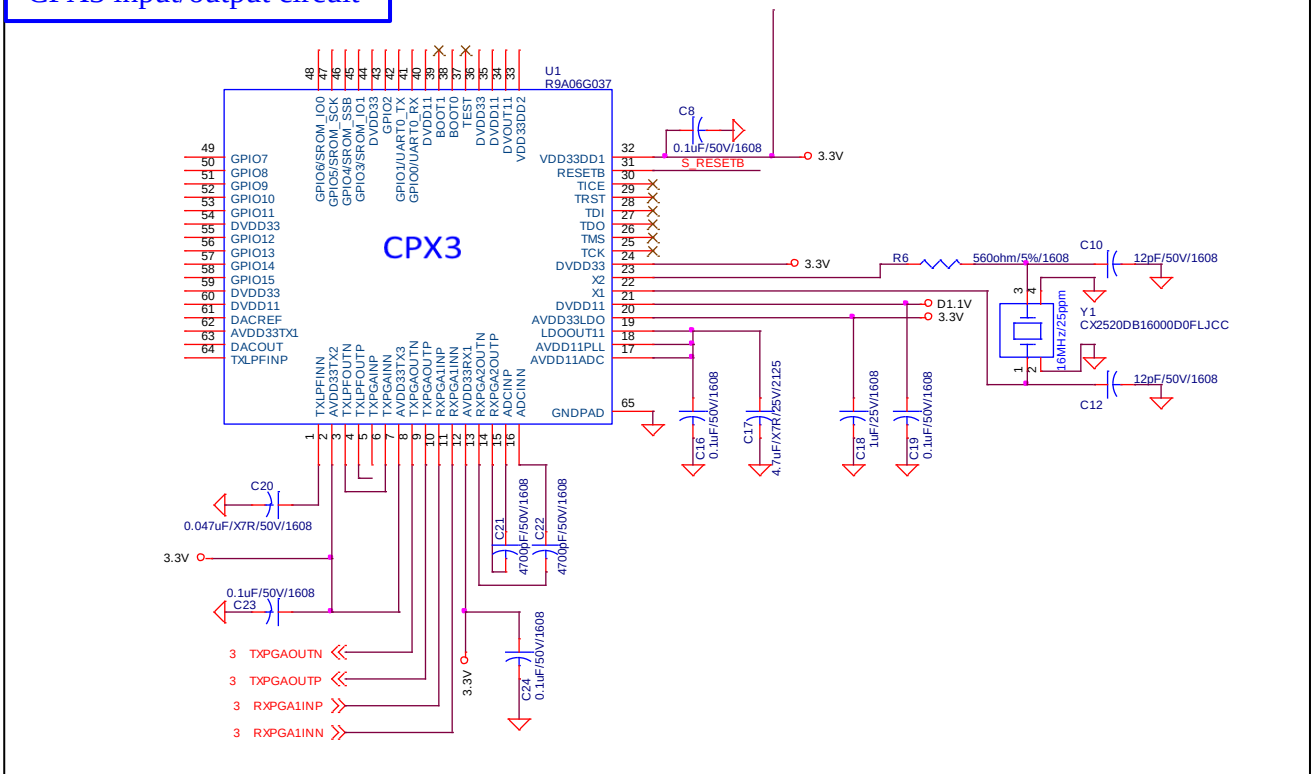


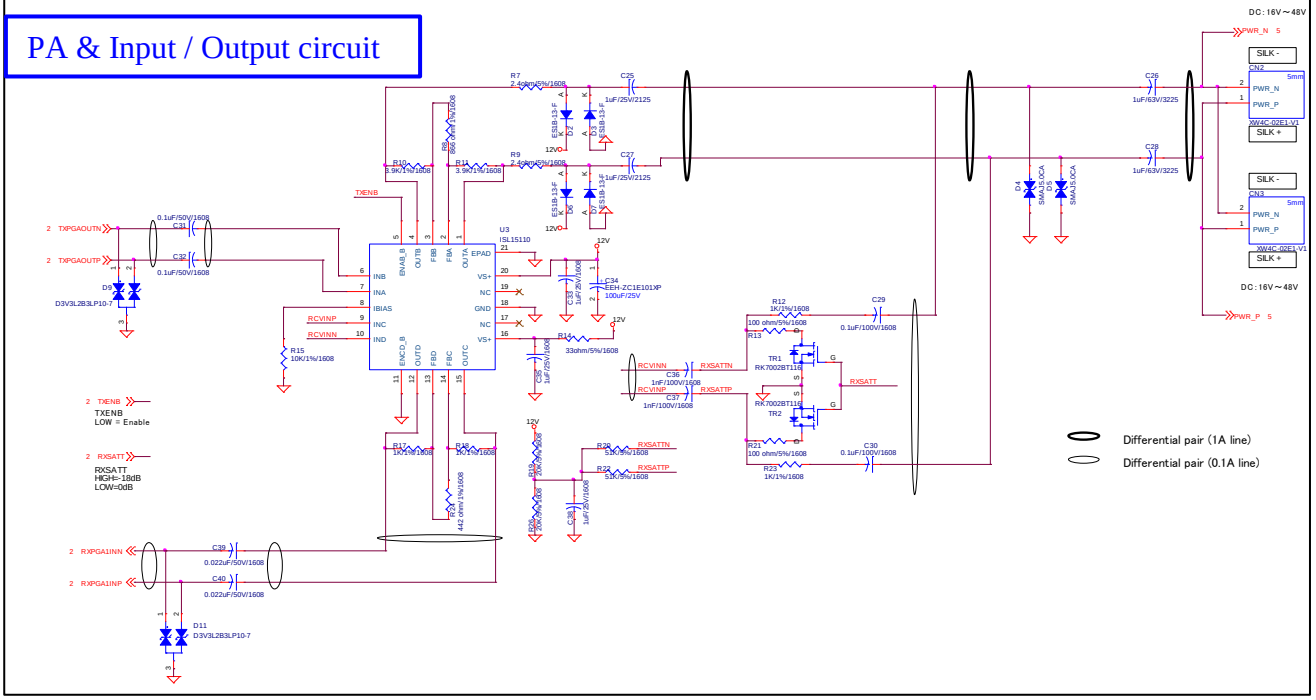
Figure 1-1 Constitution of the main part (CPX drive)

1.2 PA (CPX3+Power Amp) drive

CPX3 input/output circuit



PA & Input / Output circuit



Direct current power supply circuit

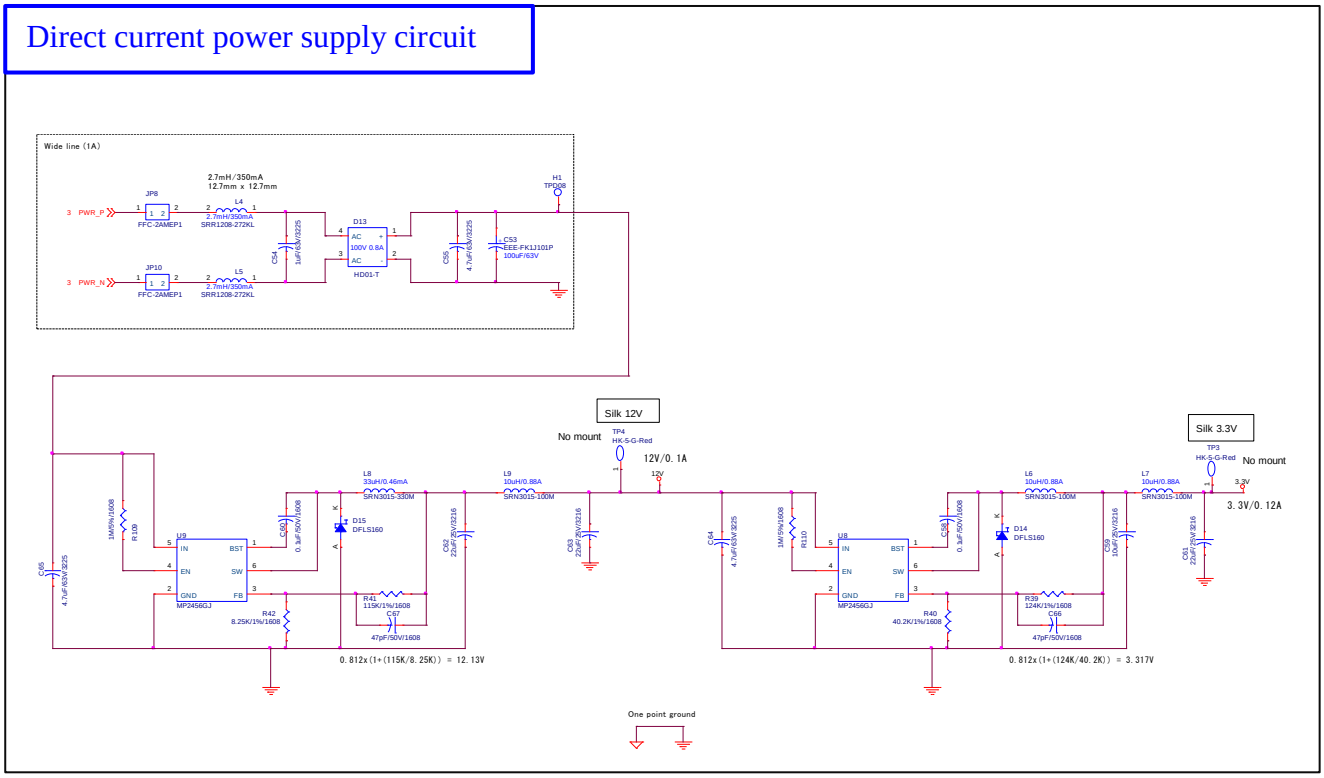


Figure 1-2 Constitution of the main part (PA drive)

2. Instructions about parts placement

2.1 Placement of the decoupling capacitors

2.1.1 U1 (CPX3) neighborhood parts (CPX drive/PA drive common)

About the decoupling capacitors C2 ~ C9, C11, C14, C16, C17, C23, C24 of U1 (CPX3), please places it in the neighborhood of each terminal to Figure 2-1 and shorten a wiring pattern. Please refer to chapter 3.7 too, about product placement.

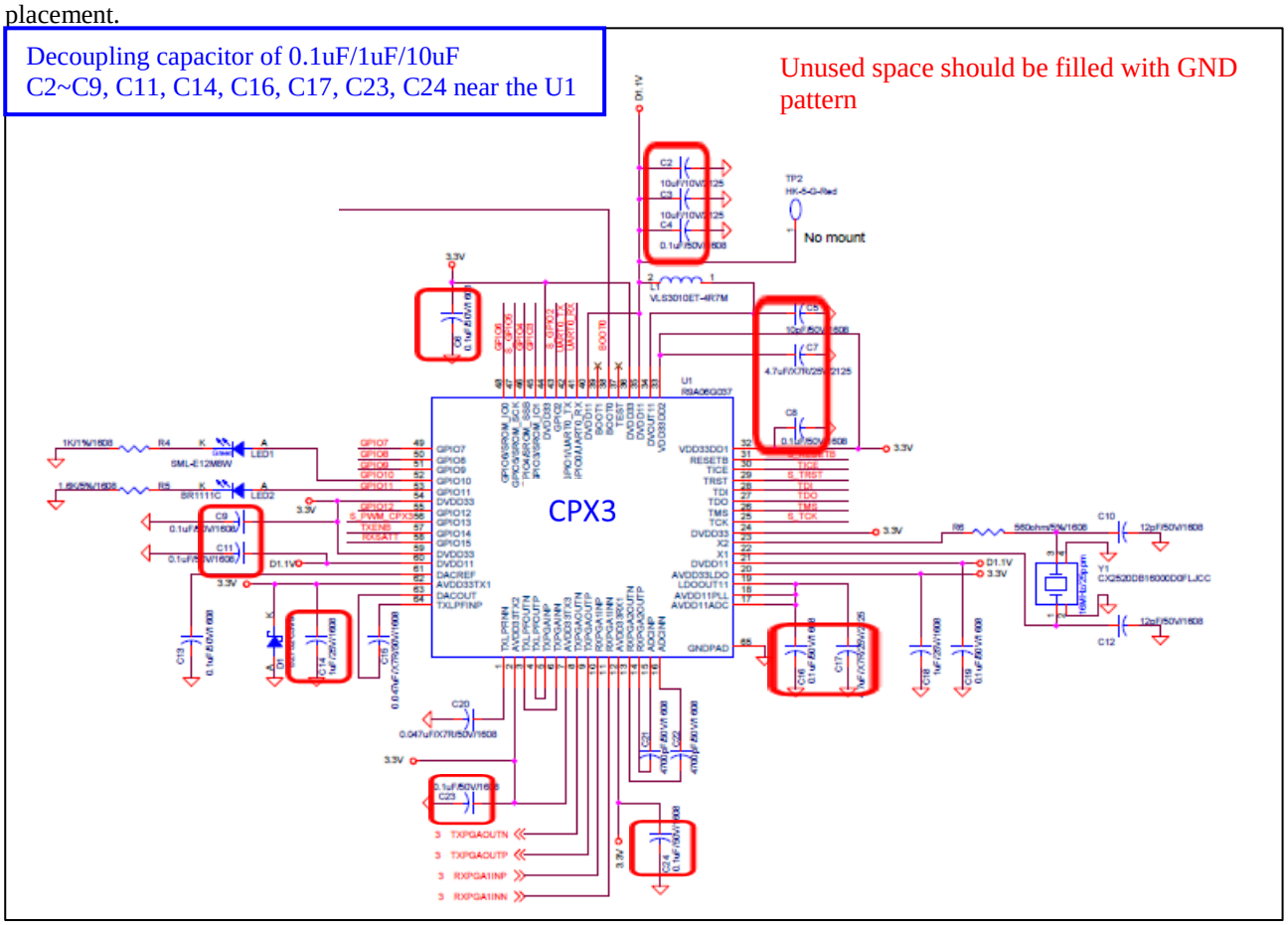


Figure 2-1 Decoupling capacitors to place in the U1 (CPX3) neighborhood

Example:
Figure 2-2 shows placement example of the decoupling capacitor with L-1/L-4 of the U1 (CPX3) neighborhood.

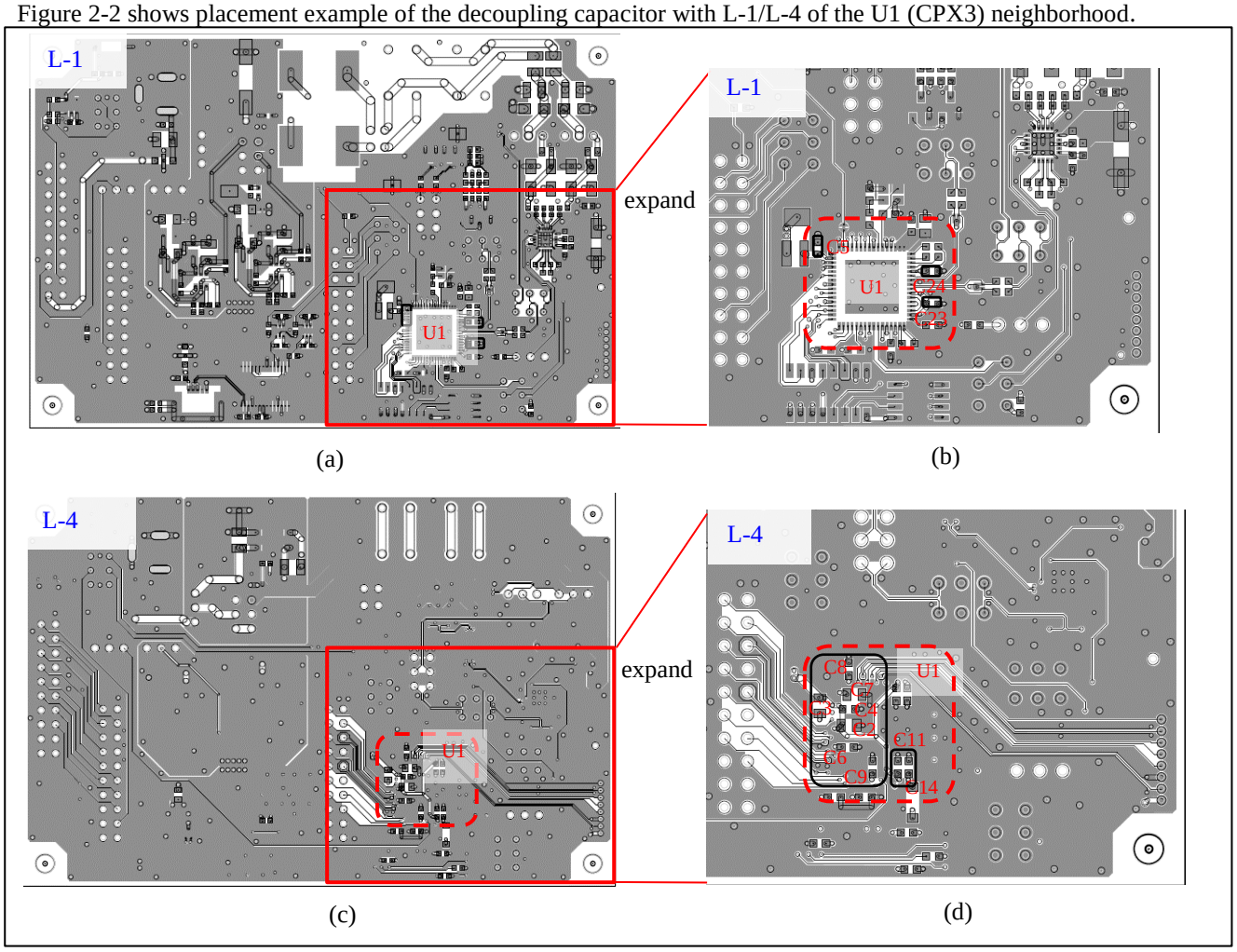


Figure 2-2 Example of the decoupling capacitor with L-1/L-4 of the U1 (CPX3) neighborhood.

2.1.2 U3 (ISL15110) neighborhood parts (PA drive)

About the decoupling capacitors C33 ~ C35 of U3 (ISL15110), please places it in the neighborhood of each terminal to Figure 2-3 and shorten a wiring pattern. Please refer to chapter 3.8 too, about product placement.

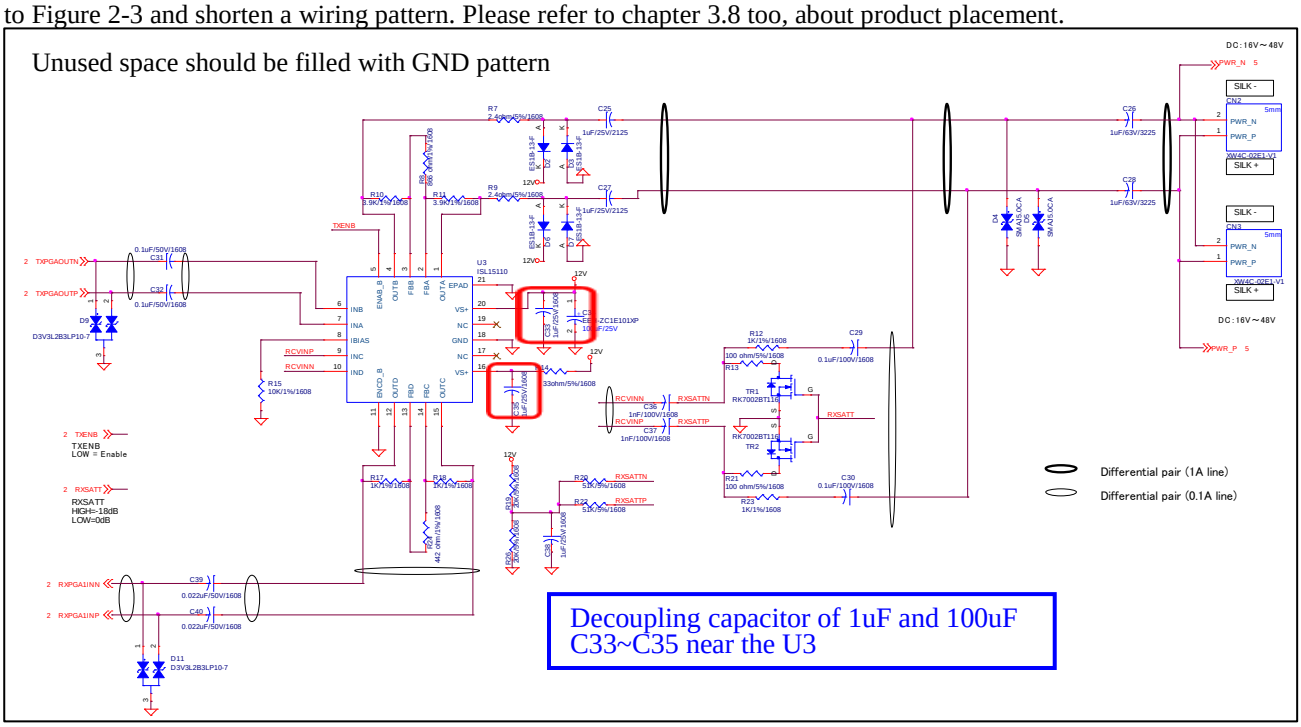


Figure 2-3 Decoupling capacitors to place in the U3 (ISL15110) neighborhood

Example:
Figure 2-4 shows placement example of the decoupling capacitor with L-1/L-4 of the U3 (ISL15110) neighborhood.

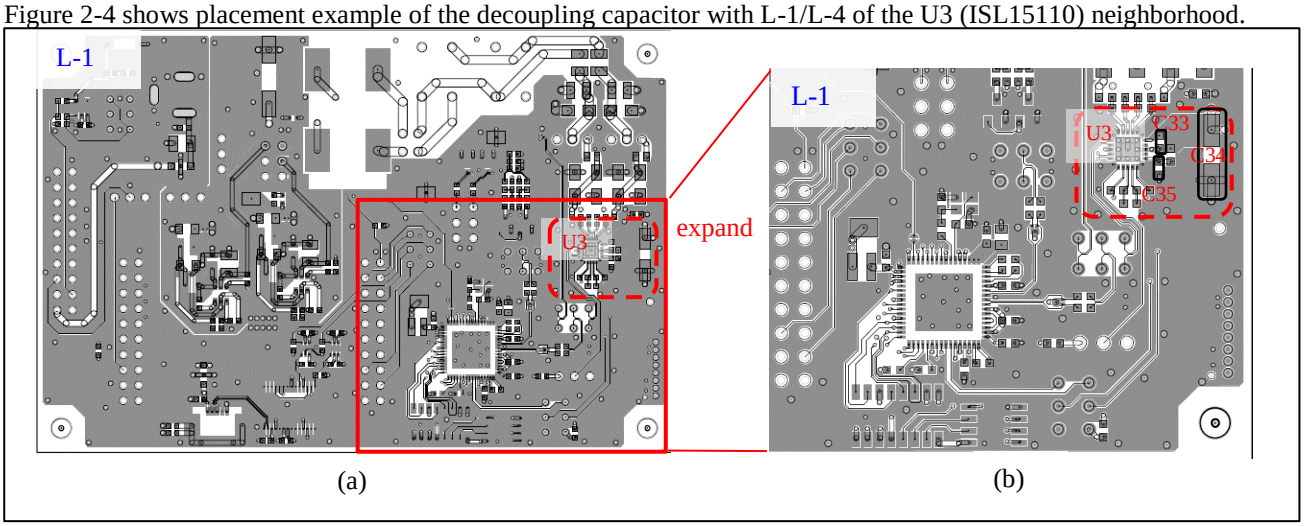


Figure 2-4 Example of decoupling capacitor placement of U3 (ISL15110)

2.2 Placement of crystal oscillation's neighboring circuit (CPX drive/PA drive common)

Crystal oscillation (Y1), R6, C10, C12 place the near U1 (CPX3) as much as possible to Figure 2-5 and shorten a wiring pattern. Moreover, under of crystal oscillation and neighboring place GND stereotypical pattern.

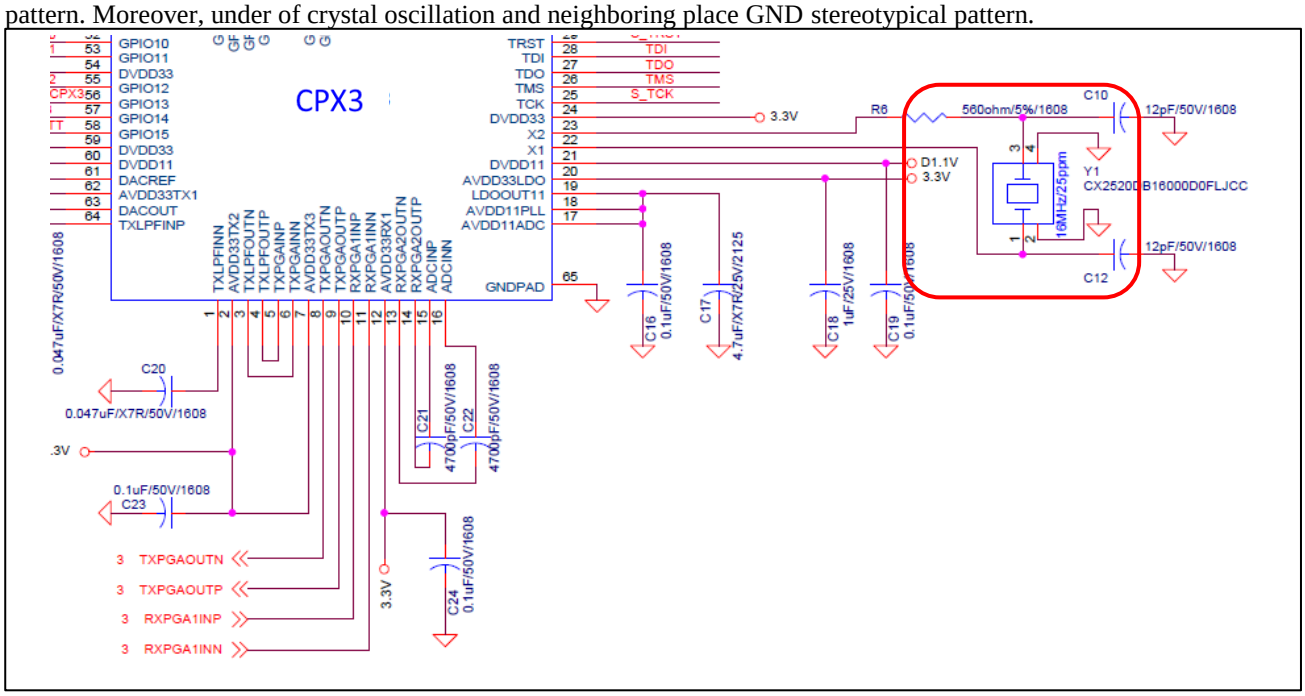


Figure 2-5 Neighboring circuit of crystal oscillation

Example: Figure 2-6 shows placement example of Crystal(Y1) , R6, C10 and C12.

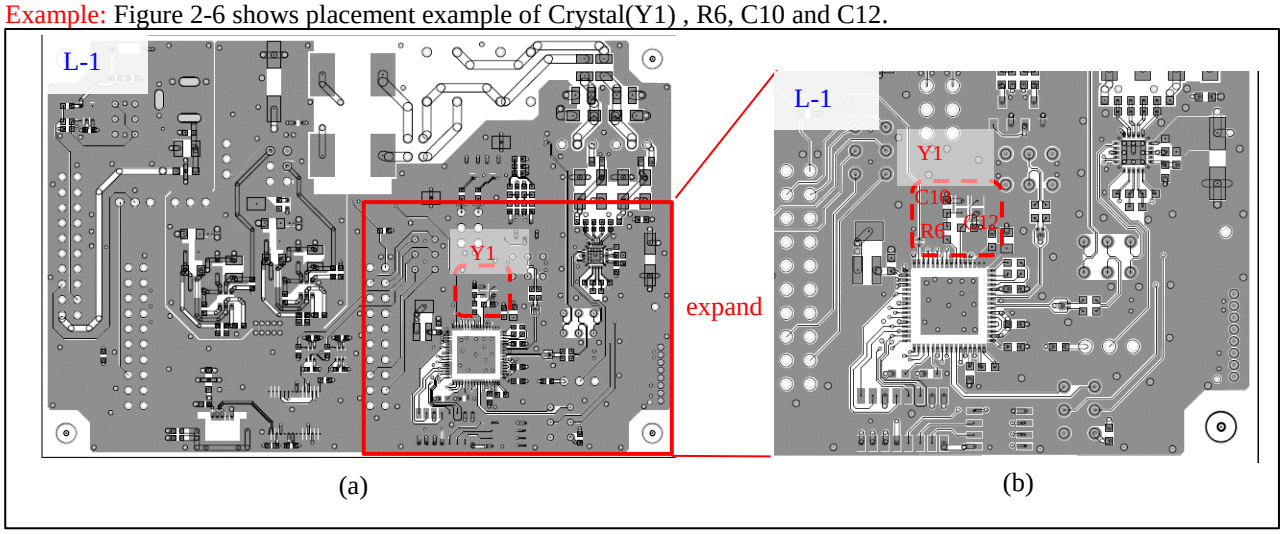


Figure 2-6 Example of crystal oscillation and neighboring circuit placement

2.3 Direct current power supply circuit (CPX drive/PA drive common)

About inductance (L4, L5) and capacity (C54), we recommend that you insert it as impedance upper so that didn't affect by the impedance of the power supply circuit for the DC PLC communication to Figure 2-7. About the choice of the inductance (L4, L5), because the input impedance of the DC PLC reception department is 1-2kΩ, the impedance of the power supply circuit side sets more than double the impedance of using frequency band so that it doesn't affect the DC PLC reception department input impedance. the evaluation board is L=2.7mH, for example, impedance Z_L in 150kHz becomes the following expressions;

$$ZL = 2\pi fL = 2 \times 3.14 \times 150kHz \times 2.7mH = 2.54k\Omega$$

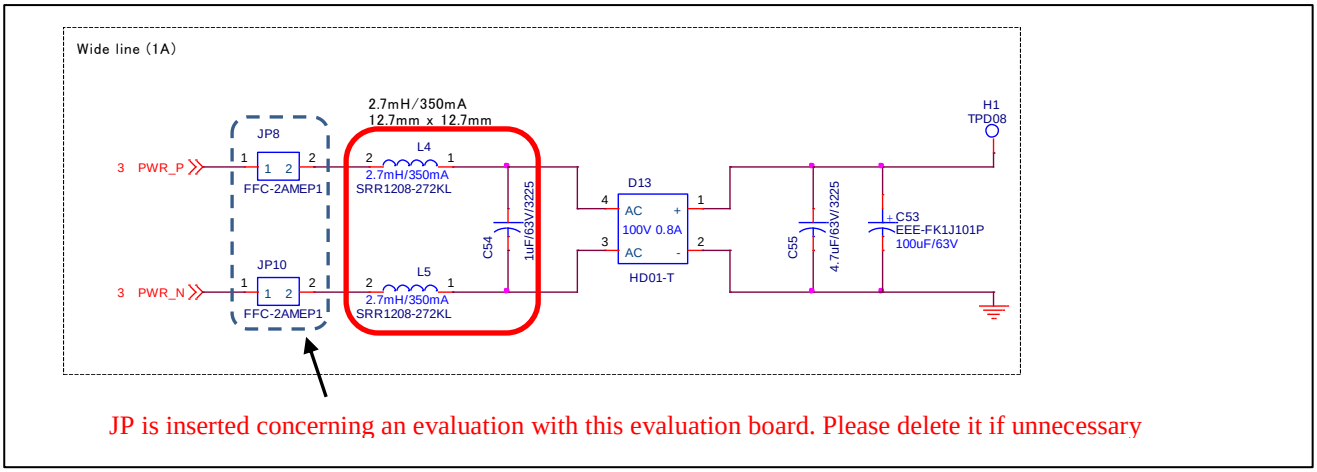


Figure 2-7 Direct current power supply circuit

2.4 Input and Output protective circuit (CPX drive/PA drive common)

We recommend that input and output circuit for CPX drive or PA drive of PLC evaluation board insert a protective circuit to Figure 2-8.

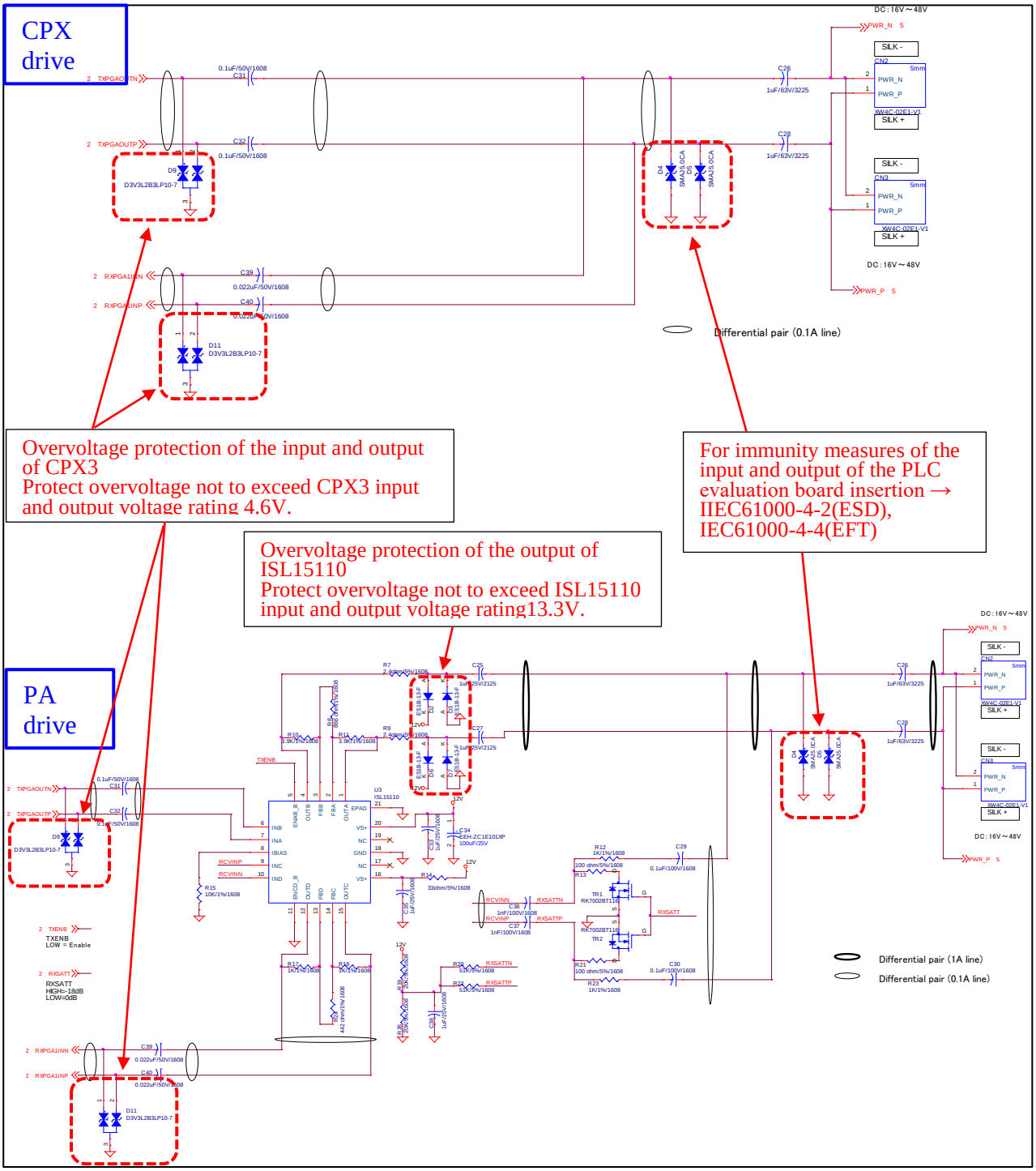


Figure 2-8 Input and Output protective circuit

3. Instructions about the PCB layout

This chapter explains the PCB layout of PLC evaluation board.

3.1 About PCB Layers (CPX drive/PA drive common)

We recommend that you adopt 4 layers PCB, and each layer's usage is shown below. Figure 3-1 shows example of the layer constitution of each layers. In order to keep signal isolation, for noise shielding and for thermal dissipation, the formation of the ground layer in L-2 or L-3 becomes important. For this reason, unused area of L-1 that are the signal layer and L-2 should be used as ground pattern, and L-1 GND & L-2 GND & L-4 GND should be connected with sufficient number of via holes (as many as possible) to strengthen. In addition, U3 (PA: ISL15110) should be fully considered with the thermal design.

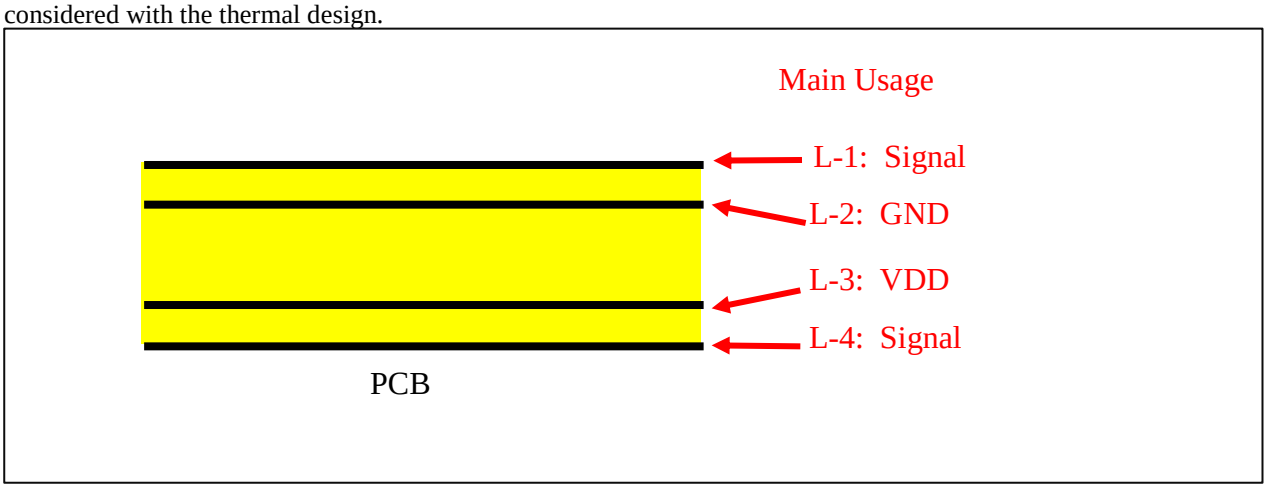


Figure 3-1 Example of the layer constitution of 4 layers board

3.2 About GND layer (CPX drive/PA drive common)

We recommend the GND pattern (L-2 or L-3) constitute in the single layer. the GND pattern is the GND stereotypical pattern without separating analog GND and digital GND. But, if you avoid the influence of the noise from power supply circuit, then it becomes the effective means to isolate between other circuit's analog GND/digital GND and GND stereotypical pattern of power supply circuit. Figure 3-2 shows PCB layout exmple to connect only L-1's one point that it isolates by L-1, L-2, and L-4 between other circuit's analog GND/digital GND and GND stereotypical pattern of power supply circuit.

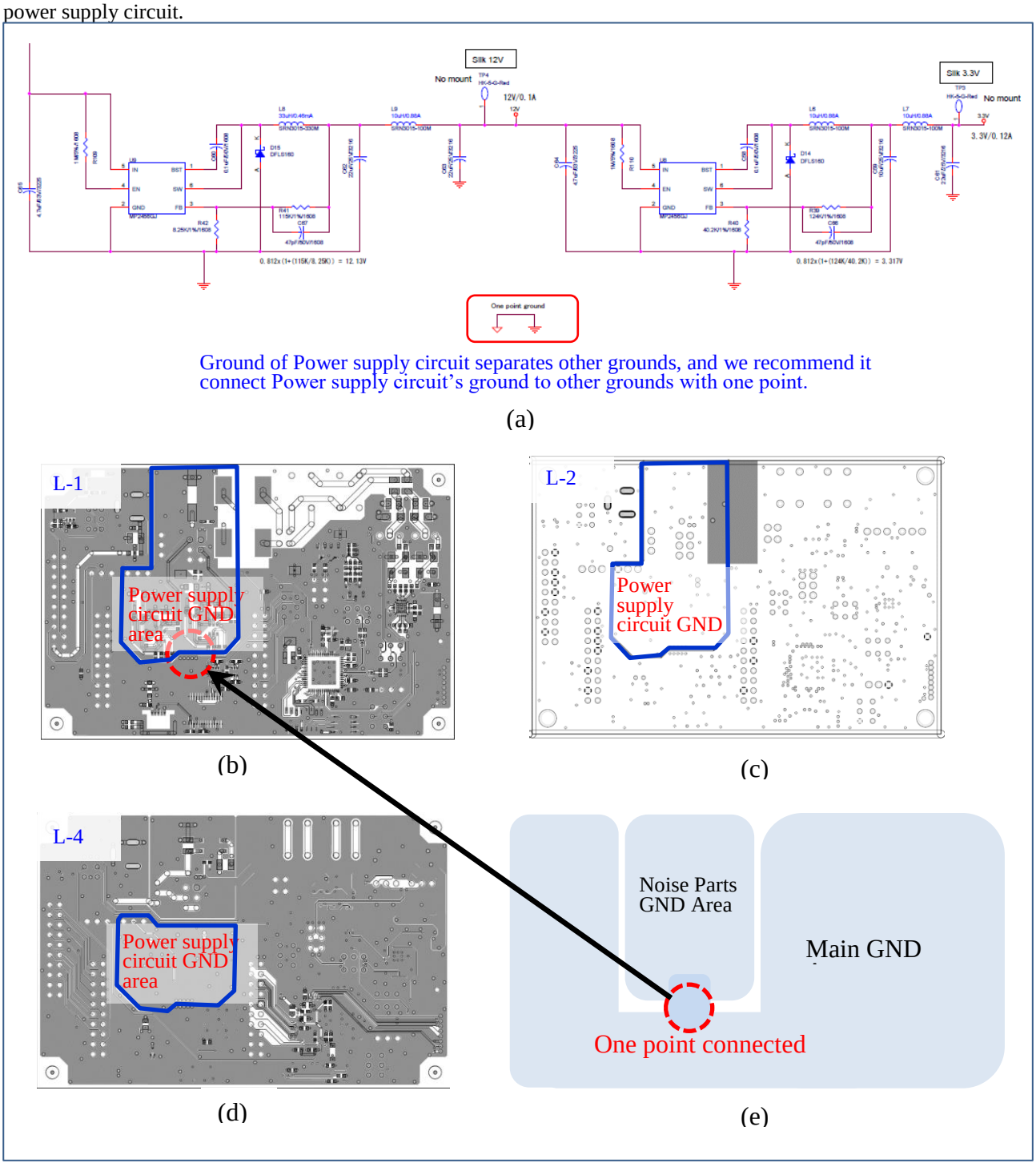
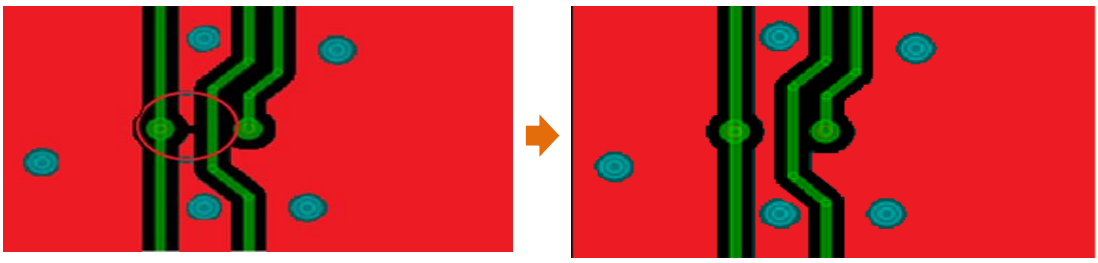
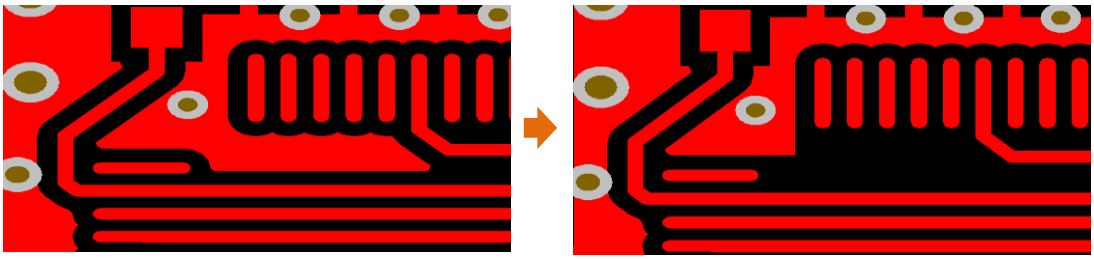


Figure 3-2 Example of GND pattern

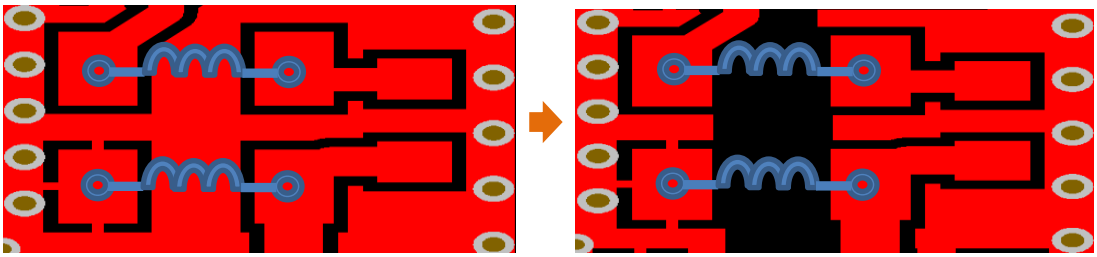
In addition, Figure 3-3 shows the instruction about the GND pattern. Unused area of signal layer fill with GND pattern as much as possible and add a lot of via hall. It's not necessary to bury for GND pattern in the cases that it becomes a floating pattern of GND in the small area or becomes the antenna of the noise by the parallel wiring with signal. Particularly, please don't fill with GND pattern for inductor.



(a) It prevents from being divided the GND pattern.



(b) It doesn't insert GND pattern forcibly, because it becomes the antenna of the noise.



(c) Don't fill with GND pattern for inductor.

Figure 3-3 Instructions of GND pattern

3.3 About power supply layer (CPX drive/PA drive common)

We recommend that the power supply layer place a 3.3V power supply area and a 12V power supply area using with PLC evaluation board, and the part except the power supply area place a GND pattern. Figure 3-4 shows layout patterns example of the power supply layer which constituted to L-3.

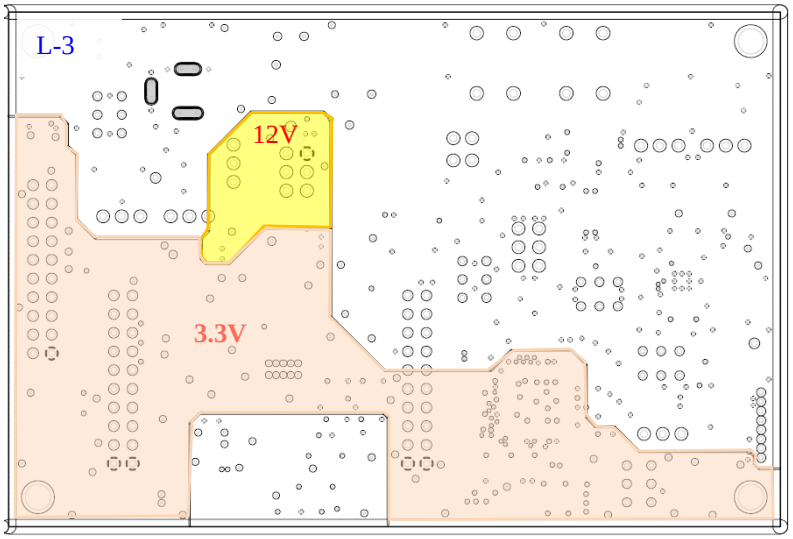


Figure 3-4 Example of the power supply area

In addition, when a power supply noise is big, and there is concern of the interference between power supply area, we recommend that insert GND wiring (secure the space where it can place a via hale for GND) between power supply wiring that minimize the influence of the noise to Figure 3-5.

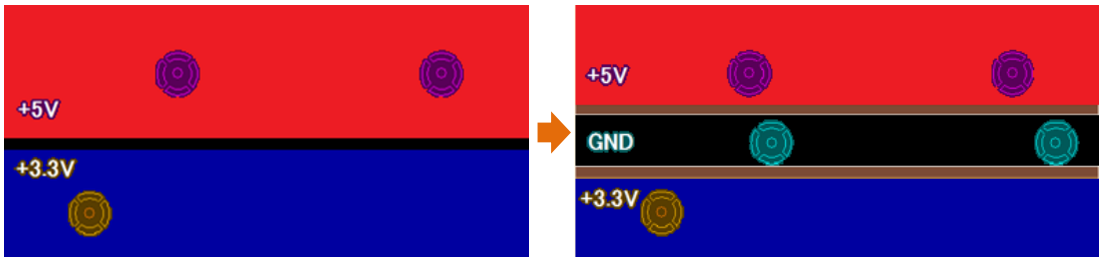


Figure 3-5 Instructions of power supply wiring

3.4 About thermal dissipation and back side GND (CPX drive/PA drive common)

U1(CPX3) and U3(ISL15110) need to consider GND reinforcement and thermal dissipation, it connects back side GND. Figure 3-6 shows GND pattern constitute to each substrare layer for connecting back side PAD, please connect each layer in via hales. GND pattern place via holes (recommendation: ϕ 0.3mm, CPX3: 9 or more, ISL15110: 8 or more). In addtion, the GND pattern connecting back side GND connects big wiring (aim: 3mm or more) with GND pattern stereotypical in L-1 or L-4.

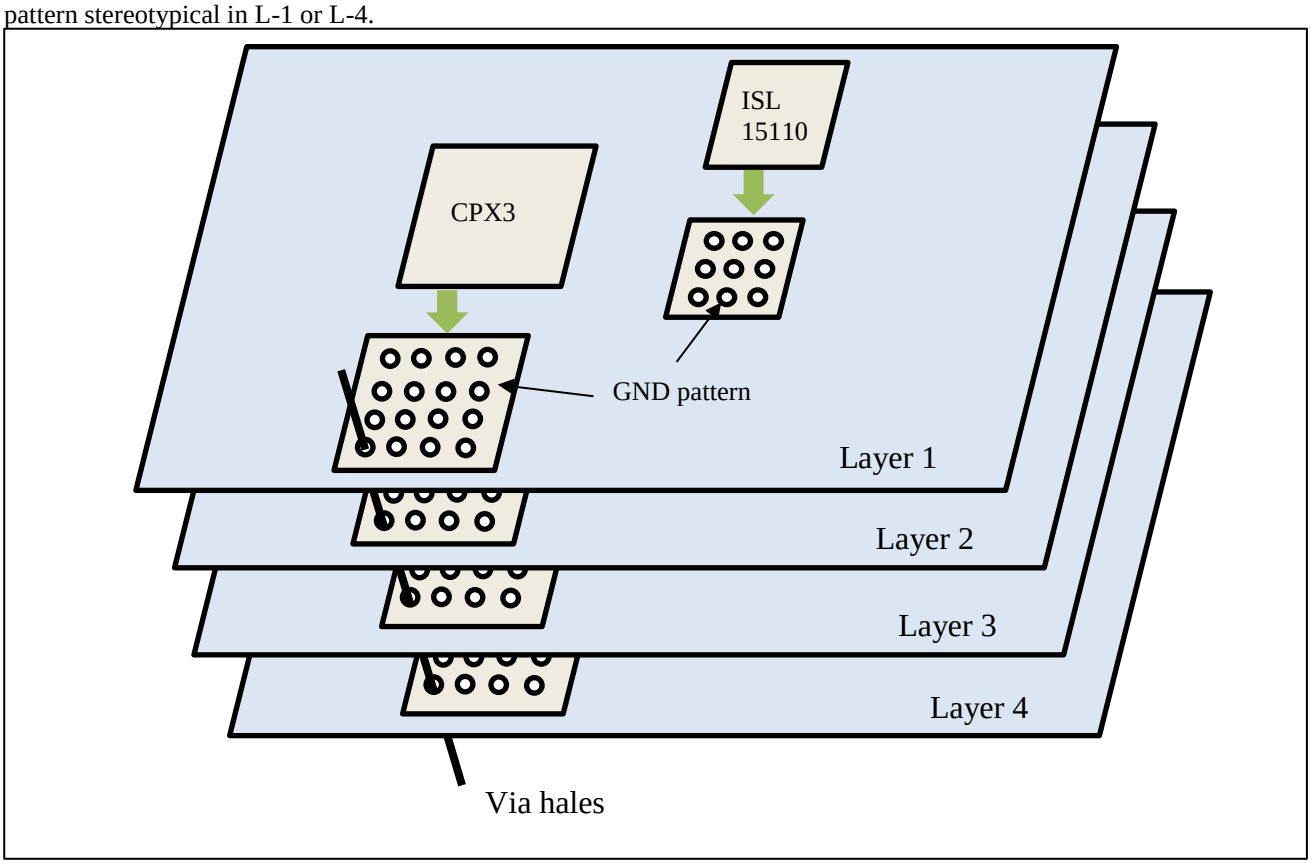
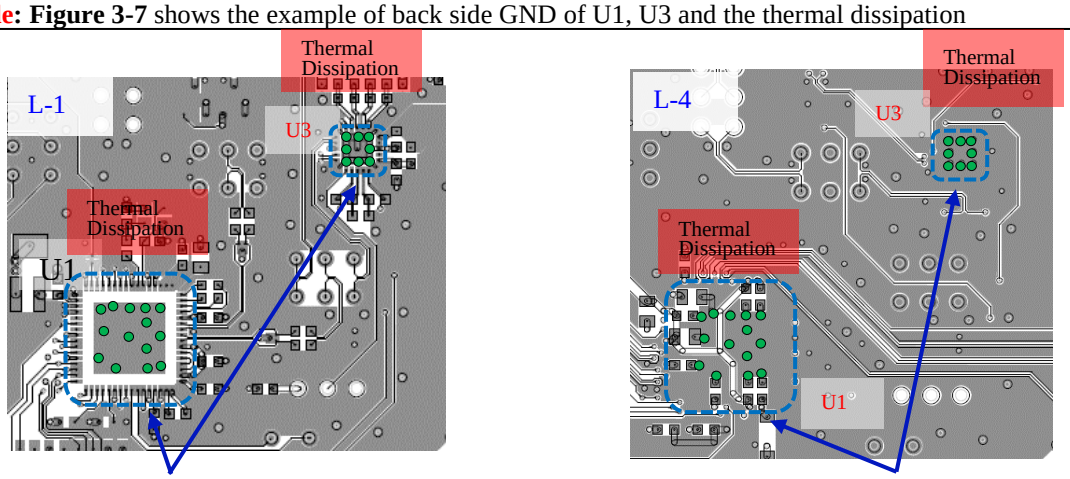


Figure 3-6 Example of thermal dissipation

Example: Figure 3-7 shows the example of back side GND of U1, U3 and the thermal dissipation



The GND pattern connecting back side GND of U1, U3 for GND reinforcement and thermal dissipation that it matched of the back side PAD connected to the stereotypical GND with l-4. Furthermore, these connected to each substrate layer by via hales, CPX3 is 14, ISL15110 is 8.

Figure 3-7 Example of back side GND of U1, U3 and the thermal dissipation

3.5 About U1 (CPX3) & U3 (ISL15110) wiring

3.5.1 About signal wiring of U1 (CPX3) (CPX drive/PA drive common)

TXPGAOUT/RXPGAIN signal of U1 (CPX3) is a differential signal. Please wires in isometry, and shields it in GND.
Figure 3-8 shows instructions of the signal wiring of U1 (CPX3).

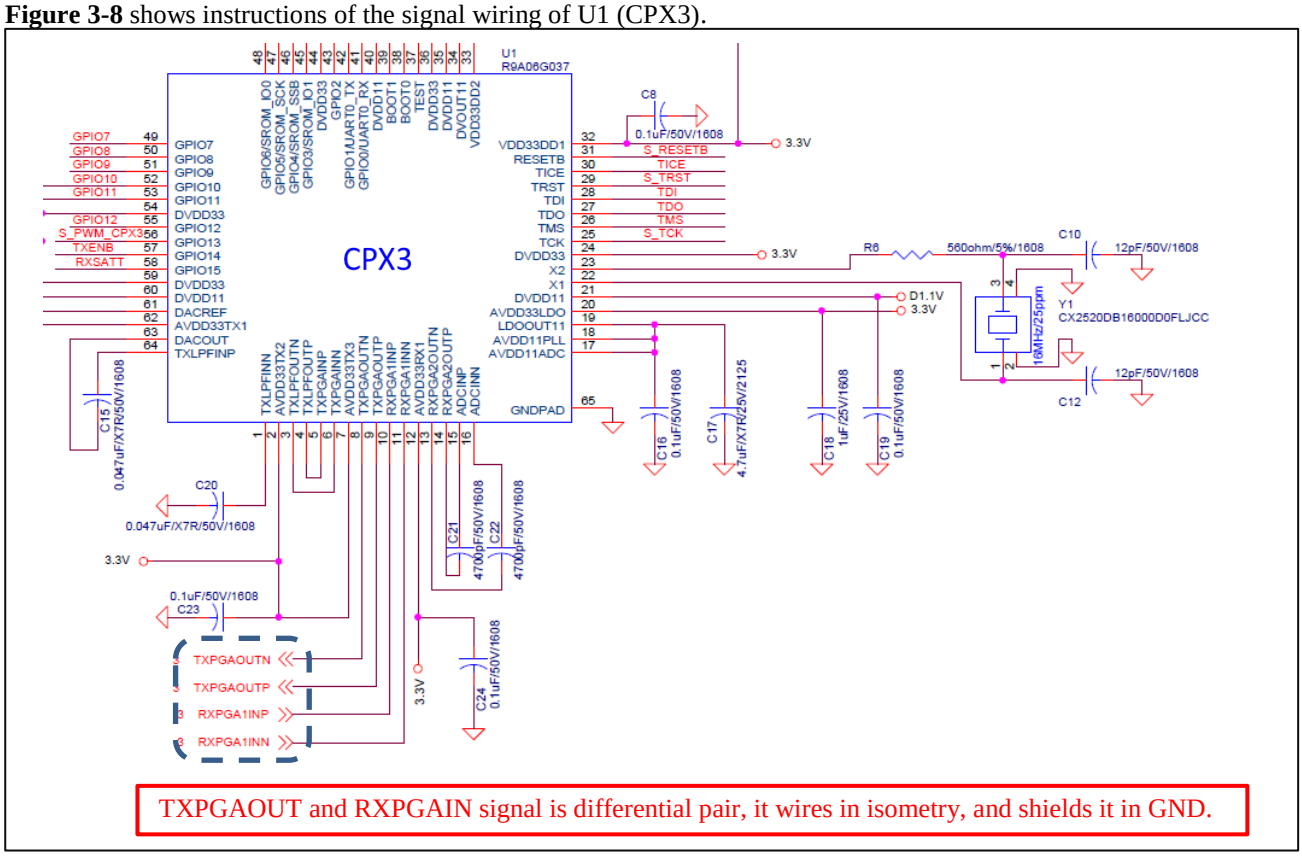


Figure 3-8 Instructions of U1 (CPX3) wiring

Example:
Figure 3-9 shows example of TXPGAOUT/RXPGAIN signals of U1(CPX3). A red broken line is TXPGAOUTP/TXPGAOUTN signals, and a green broken line is RXPGAINN/RXPGAINP signals. It is wiring in isometry between U1 and U3.

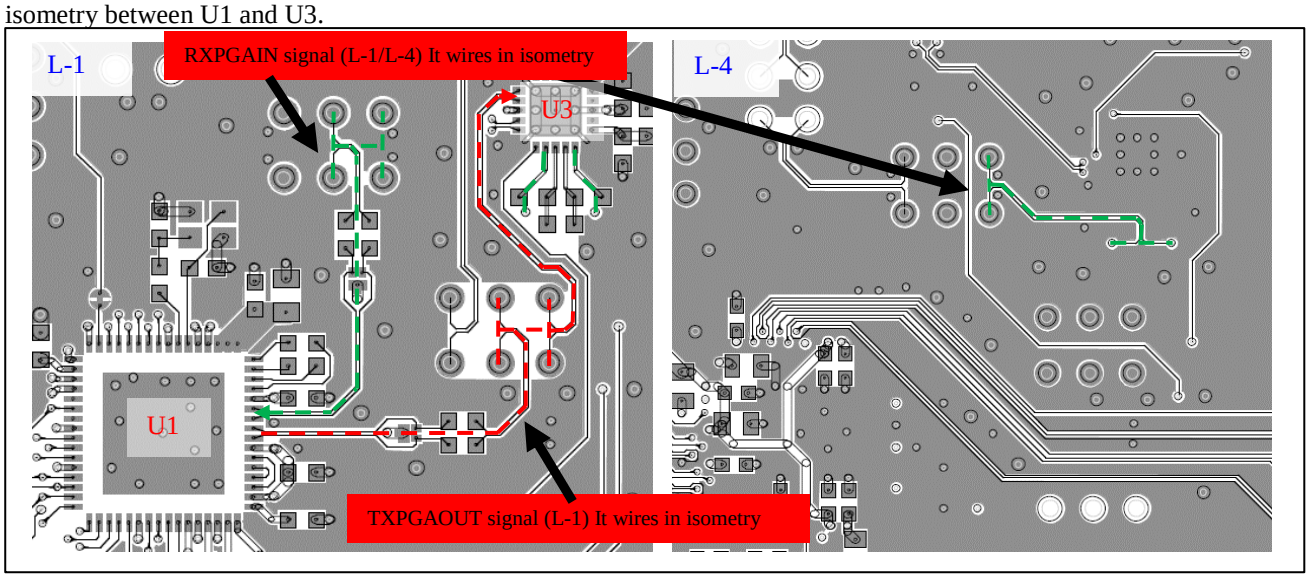


Figure 3-9 Example of TXPGAOUT/TXPGAIN signals of U1(CPX3)

3.5.2 About input/output signal, Power supply and GND of U3 (ISL15110) (PA drive)

Output signal of U3 (ISL15110) flows a large current (Max:1A). Please use wide pattern. The input and output of U3 (ISL15110) is a differential signal. Please wire in isometry, and shields it in GND. **Figure 3-10** shows instructions of the signal wiring of U3 (ISL15110).

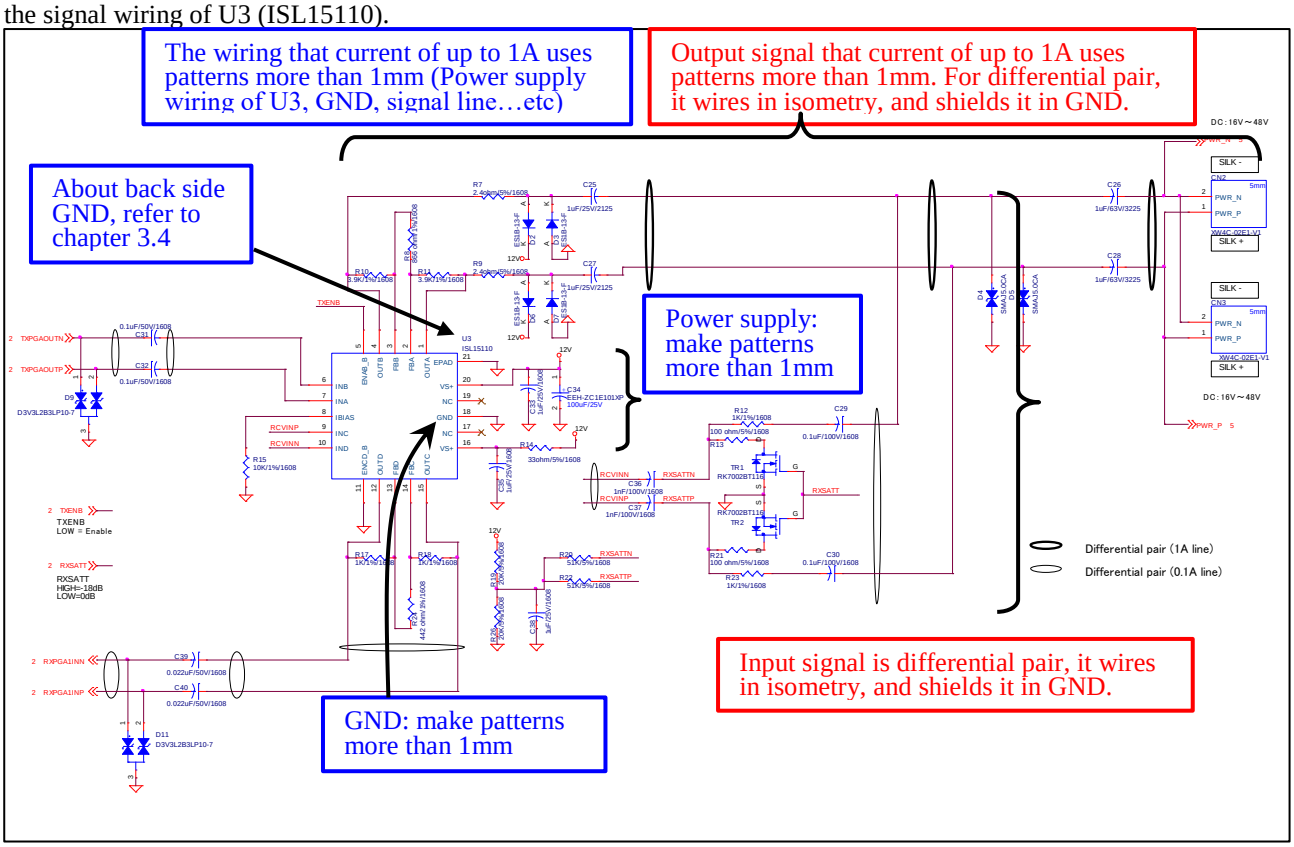


Figure 3-10 Instructions of U3 (ISL15110) wiring

Example:

Figure 3-11 shows the example of the PCB layout around U3 (ISL15110). A red and a green line of ① are output signals, and this signal uses patterns more than 1mm because current of up to 1A flows. A red and a green line surrounded in a broken red line of ② are input signals, and are wiring in isometry. A blue broken arrow line of ③ is 12V wiring pattern, and this signal uses patterns more than 1mm because current of up to 1A flows. GND of U3 of ④ is connected 8 via hales in L-2 (the GND layer) and GND of L-4.

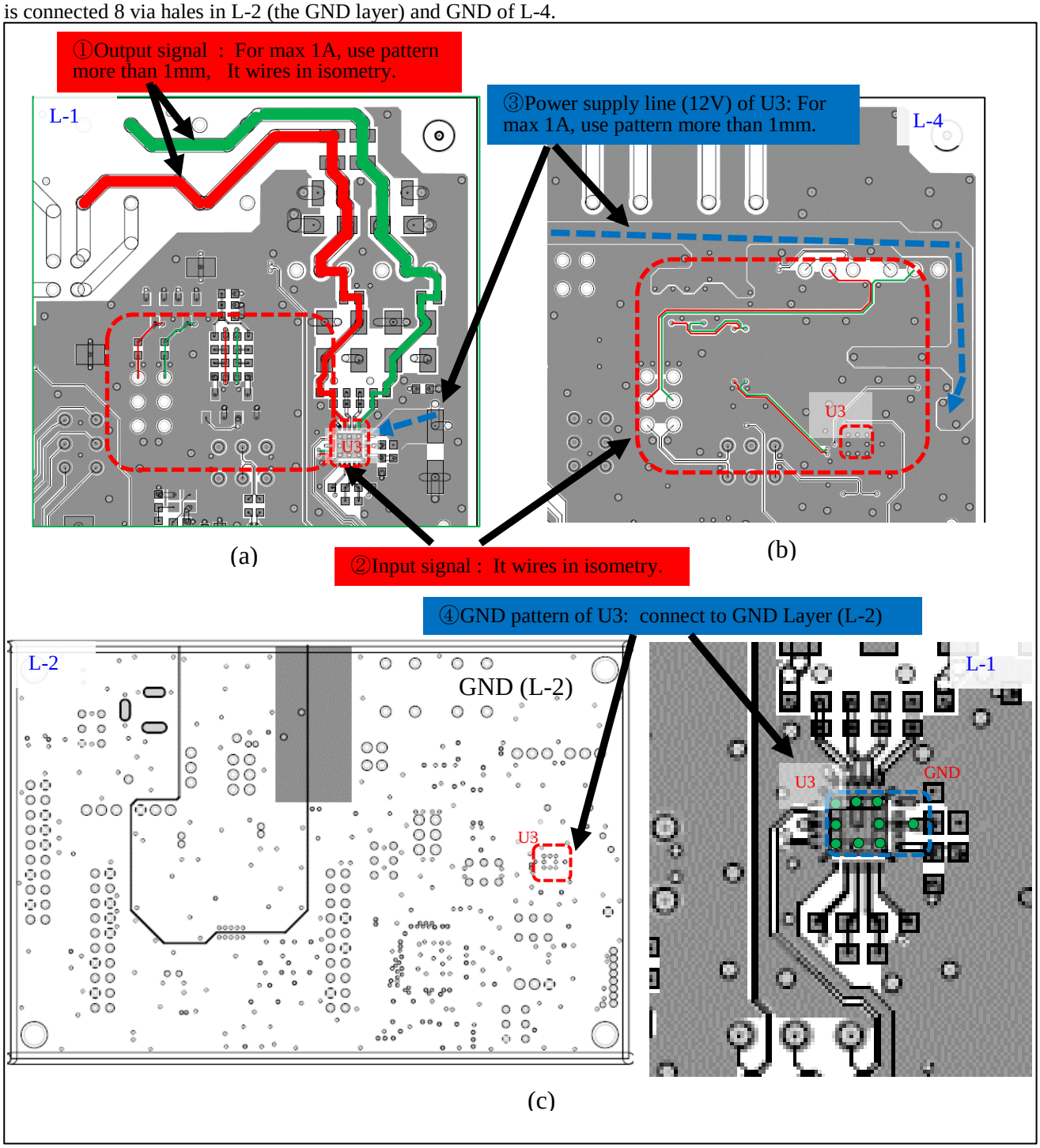


Figure 3-11 Example of the PCB layout around U3 (ISL15110)

3.6 About layout of direct current power supply line (CPX drive/PA drive common)

The power supply line from a direct current power line sets in the most suitable wiring width that accepted the voltage and current of the application to use. This document is that the power supply from a direct current power line designs the wiring that assumed up to 1A. **Figure 3-12** shows instructions of direct current power supply line.

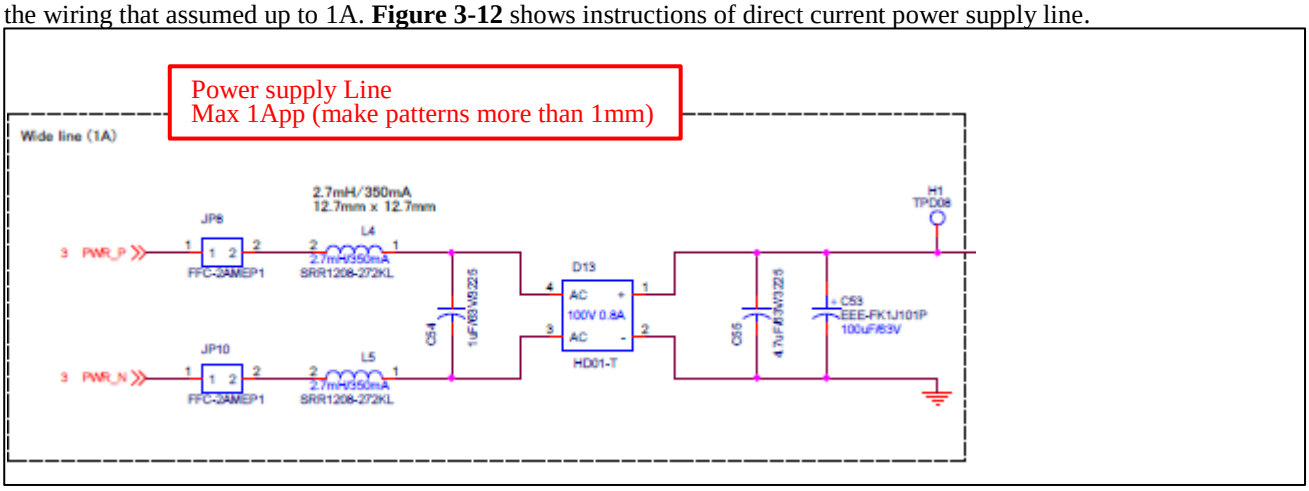


Figure 3-12 Instructions of direct current power supply line

Example: **Figure 3-13** shows the example of the PCB layout for direct current power supply line

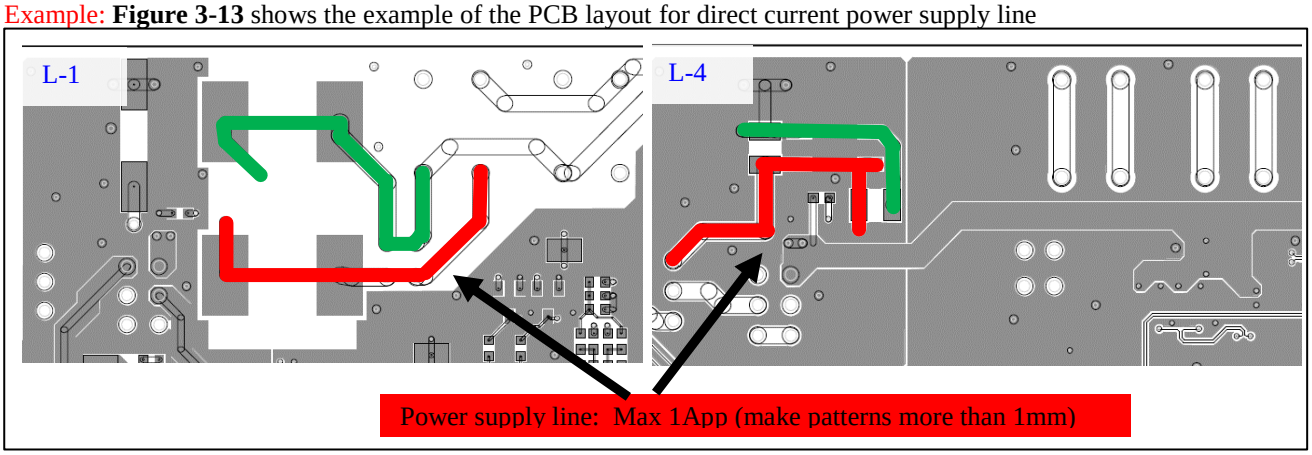


Figure 3-13 Example of direct current power supply line

3.7 About isolation of signal wiring

3.7.1 Isolation of RXPGAIN signal (CPX drive/PA drive common)

When other signals and noises interfere the RXPGAIN signal, reception properties deteriorate. Thus, as for the RXPAGAIN signal, please be careful enough not to interfere other signals and noises. In particular, about between the RXPGAIN signal and crystal oscillation (Y1), X1/X2 signal, between the RXPGAIN signal and RXPGAOUT signal, between the RXPGAIN signal and TXPGAOUT signal, please these signals isolate by keeping distance, by placing shielding GND, by using different layers in consideration of interference. **Figure 3-14** shows instructions of the interference with the RXPGAIN signal.

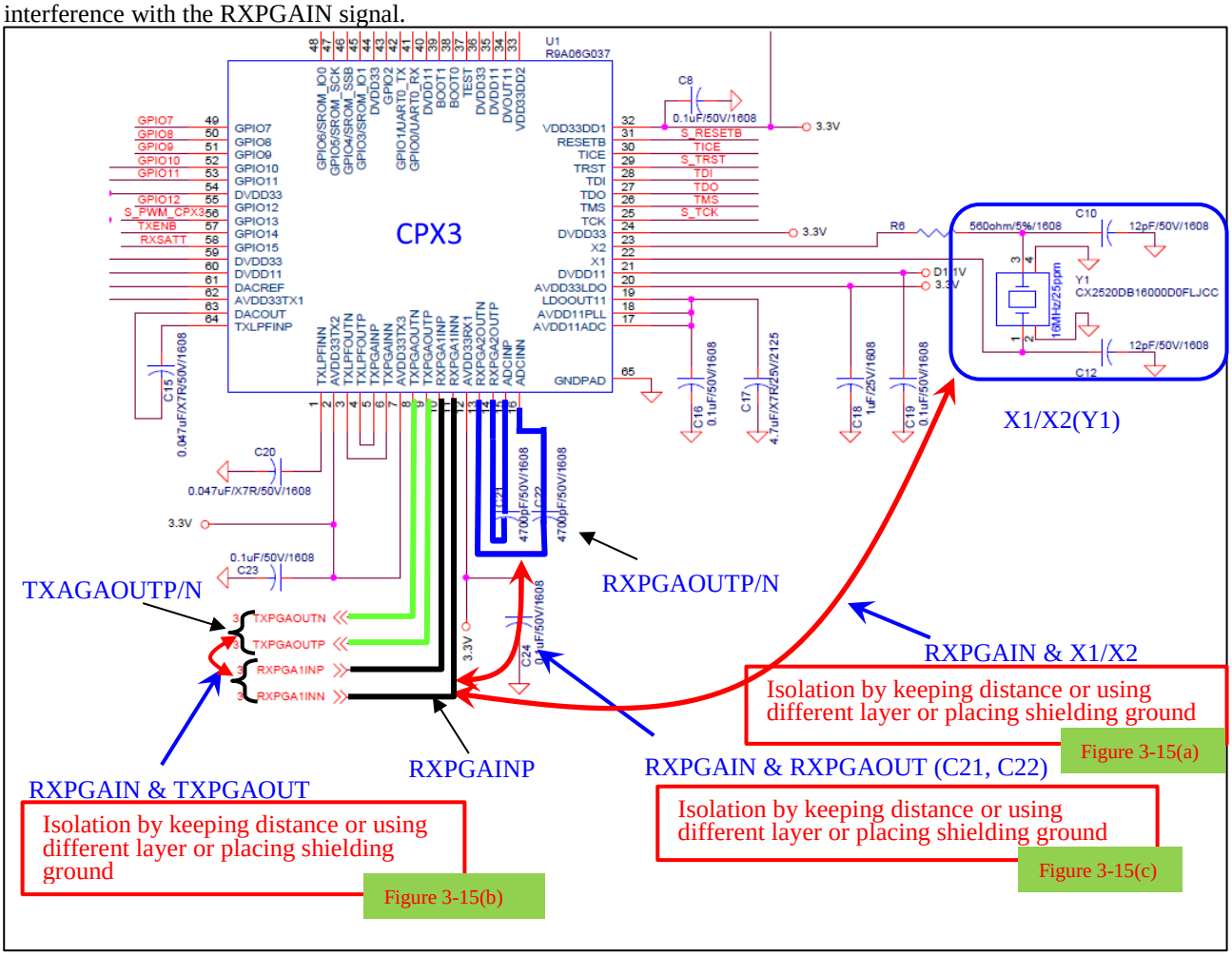


Figure 3-14 Instructions of the interference with the RXPGAIN signal.

Example:

Figure 3-15 shows PCB layout example between the RXPGAIN signal and crystal oscillation (Y1), X1/X2 signal, between the RXPGAIN signal and RXPGAOUT signal, between the RXPGAIN signal and TXPGAOUT signal, in consideration of interference.

(a) RXPGAIN signal is a red line and X1/X2(Y1) is a blue line. These are place same layer on the evaluation board, but isolate by keeping distance.

(b) RXPGAIN signal is a red line and RXPGAOUT signal is a blue line. These are place same layer on the evaluation board, but isolate by placing shielding GND.

(c) RXPGAIN signal is a red line and TXPGAOUT signal is a blue line. These are place same layer on the evaluation board, but isolate by placing shielding GND, these signal don't wire parallel, also these signals don't let intersect.

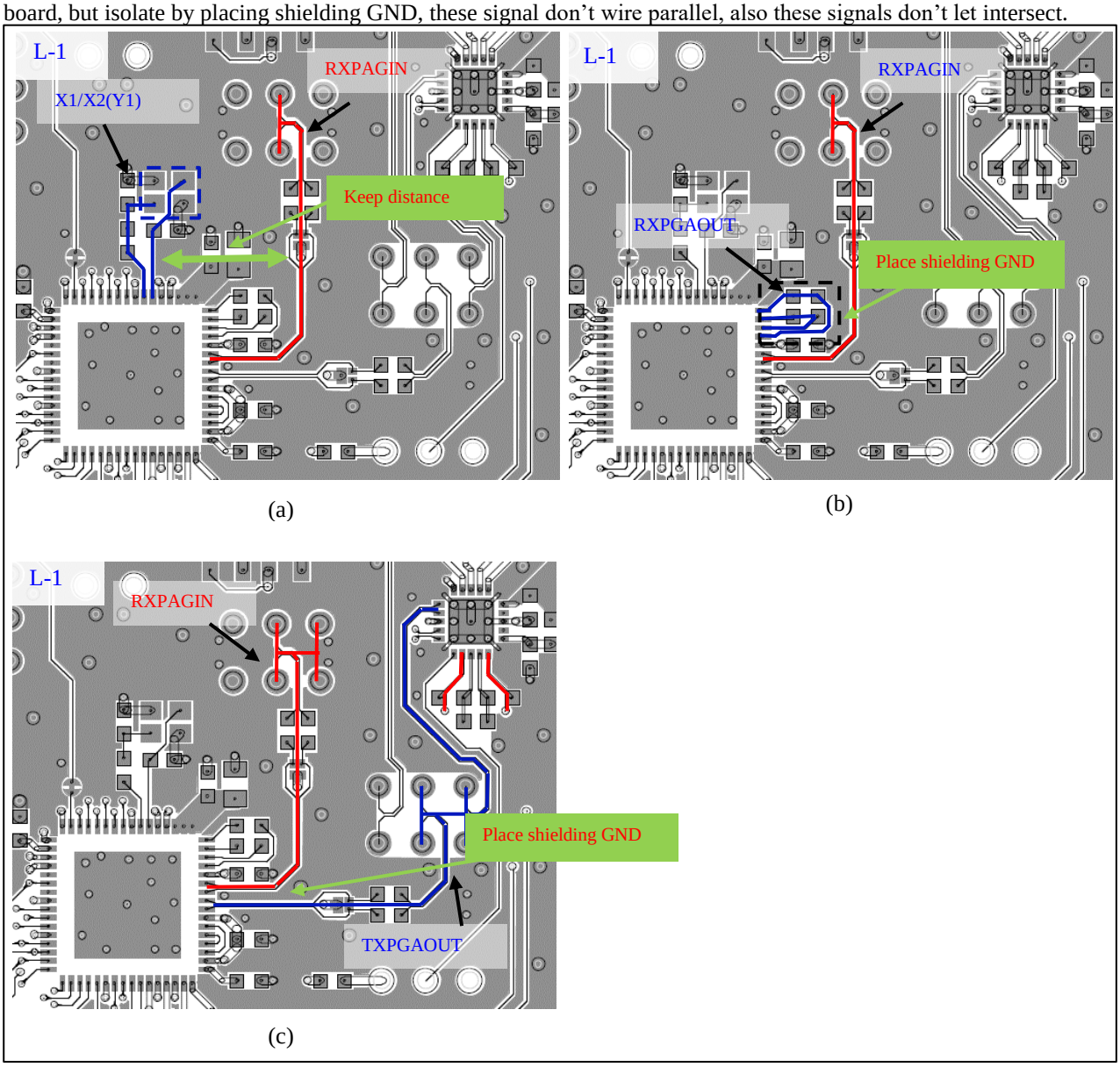


Figure 3-15 PCB layout example of RXPGAIN signal for each signal line

3.7.2 Power supply circuit and RXPGAIN (CPX drive/PA drive common)

Because the RXPGAIN signal is easy to be affected by the noise, please isolate (recommendation: 40mm or more) by keeping distance, by placing shielding GND, by using different layers between the RXPGAIN signal and power supply circuit so that the noise of the power supply circuit does not interfere it. **Figure 3-16** shows instructions of RXPGAIN signal and power supply circuit.

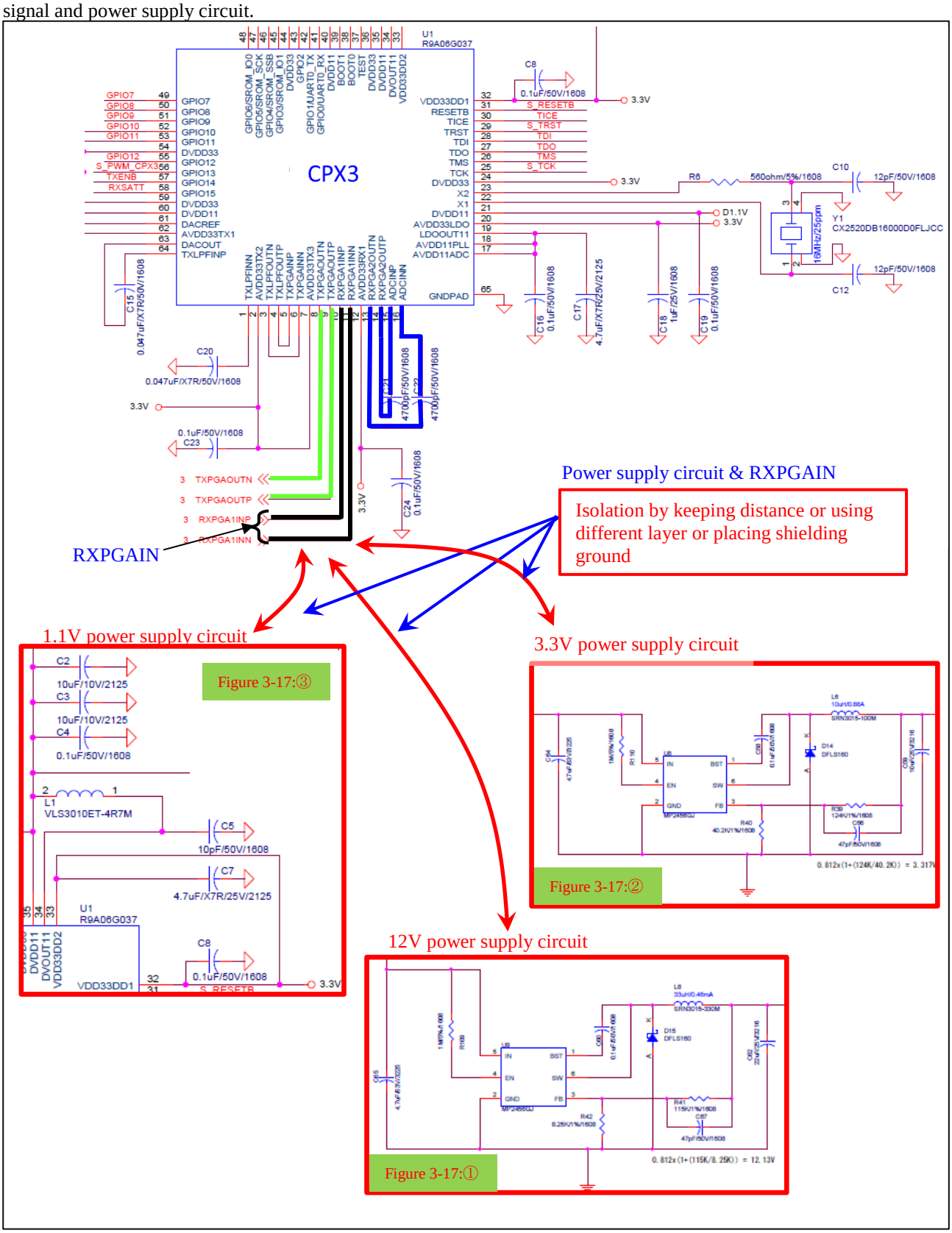


Figure 3-16 Instructions of RXPGAIN signal and Power supply circuit

Example:

Figure 3-17 shows PCB layout example of RXPGAIN signal and the power supply circuit. RXPGAIN signal and the power supply circuit isolated by keeping distance more than 40mm, by placing shielding GND patterns between RXPGAIN signal and the power supply circuit so that the noise of the power supply circuit does not interfere it.

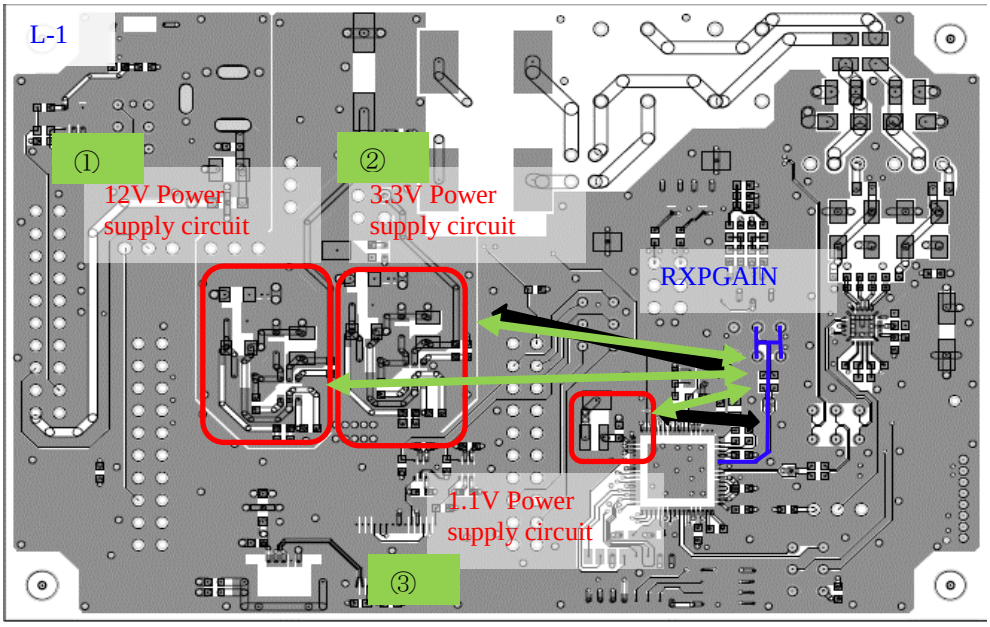
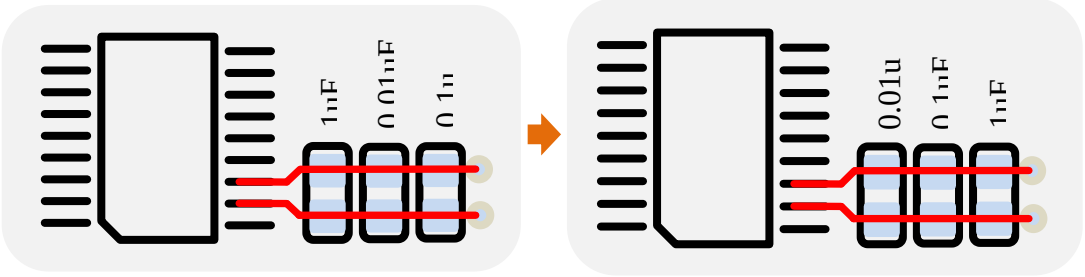


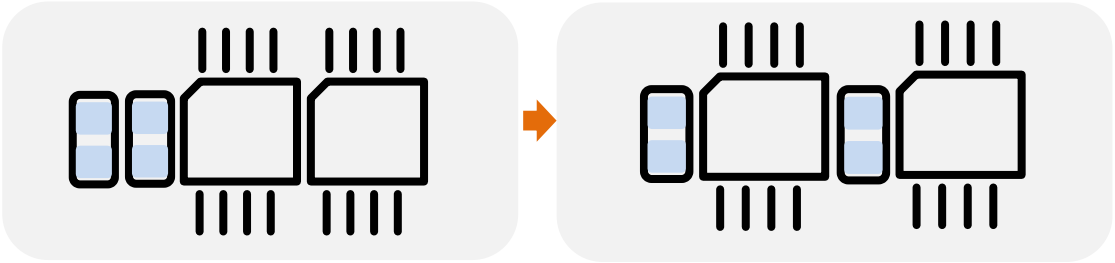
Figure 3-17 PCB layout example of RXPGAIN signal and the power supply circuit

3.8 Others (CPX drive/PA drive common)

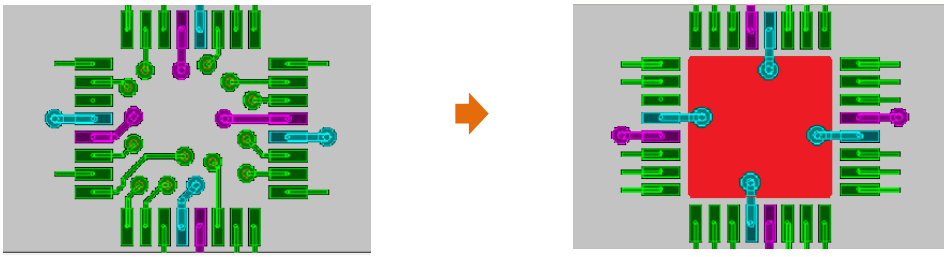
This chapter explains the general instructions for the PCB layout to **Figure 3-18**. When you design the PCB, please refer.



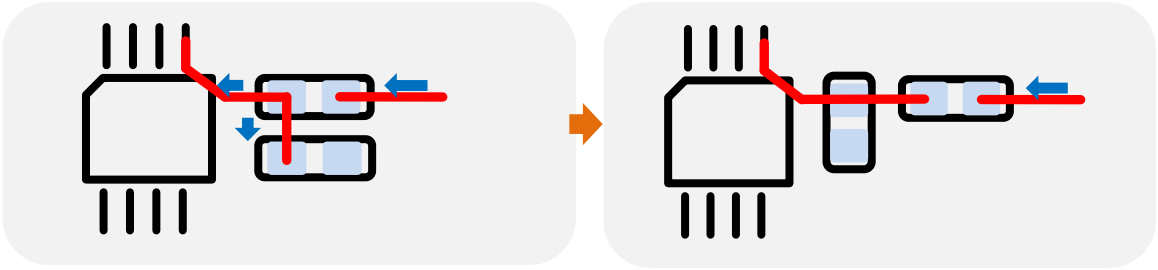
(a) The bypass capacitor connects to the small order.



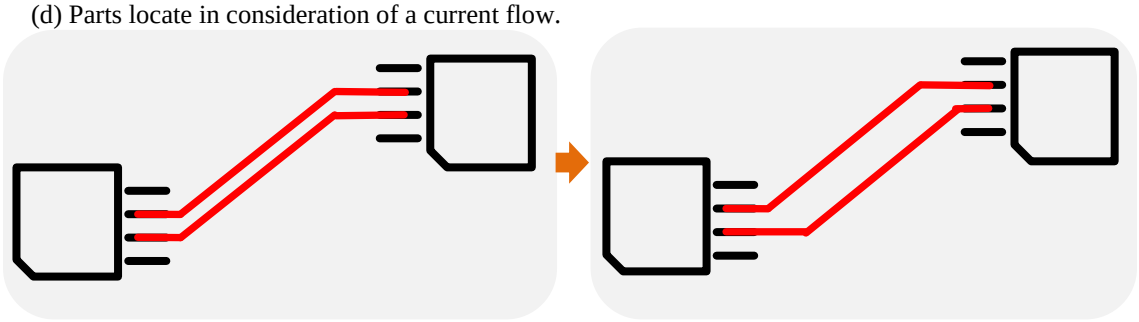
(b) The bypass capacitor locates in the neighborhood of the IC.



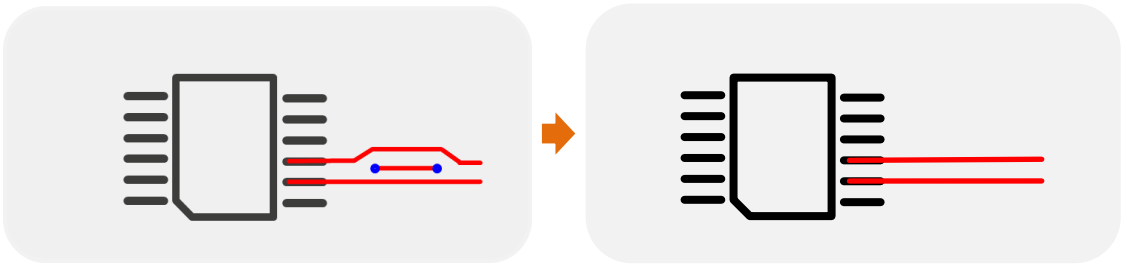
(c) Under of IC pattern inserts a GND pattern.



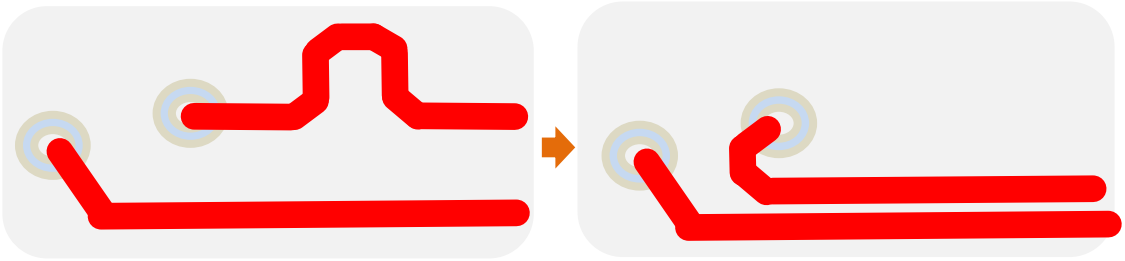
(d) Parts locate in consideration of a current flow.



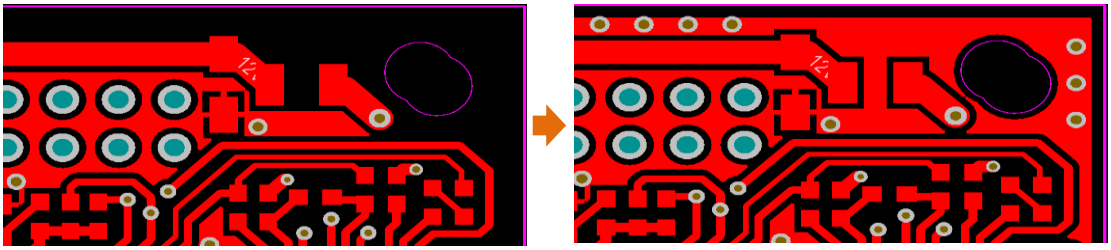
(e) the distance of the parallel wiring shortens it as much as possible.



(f) The differential signal wires it pairwise.



(g) The differential signal draws isometry.



(h) The board circumference inserts GND pattern.

Figure 3-18 General instructions

4. Instructions about the wiring pattern

This chapter shows the general instructions in the wiring pattern. When you design the PCB, please refer.

4.1 Length

Please the signal pattern doesn't bend as much as possible, and wire at the shortest distance.
Please the signal pattern doesn't diverge as much as possible, and wire in a single stroke of the brush.

4.2 Width

Please make the wiring width of a GND pattern and the power supply pattern wide as much as possible to lower impedance. In the case of wiring with current specifications, please secure necessary wiring width. With the PLC evaluation board, the signal wiring that a characteristic doesn't have the current designation does 0.1-0.15mm, the wiring of 1A specifications does wiring width more than 1mm.

4.3 Clearance and Creepage distance

Depending on a system and the use area of the developed PLC modem by customer, there is the case that the clearance and creepage distance are regulated by laws and ordinances. Please confirm them.

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Revision History

Rev	Date	Description	
		Page	Summary
1.00	Nov 01, 2017		First Edition issued

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Renesas Electronics America Inc.
2801 Scott Boulevard Santa Clara, CA 95050-2549, U.S.A.
Tel: +1-408-588-6000, Fax: +1-408-588-6130

Renesas Electronics Canada Limited
9251 Yonge Street, Suite 8309 Richmond Hill, Ontario Canada L4C 9T3
Tel: +1-905-237-2004

Renesas Electronics Europe Limited
Dukes Meadow, Millboard Road, Bourne End, Buckinghamshire, SL8 5FH, U.K
Tel: +44-1628-585-100, Fax: +44-1628-585-900

Renesas Electronics Europe GmbH
Arcadiastrasse 10, 40472 Düsseldorf, Germany
Tel: +49-211-6503-0, Fax: +49-211-6503-1327

Renesas Electronics (China) Co., Ltd.
Room 1709, Quantum Plaza, No.27 ZhiChunLu Haidian District, Beijing 100191, P.R.China
Tel: +86-10-8235-1155, Fax: +86-10-8235-7679

Renesas Electronics (Shanghai) Co., Ltd.
Unit 301, Tower A, Central Towers, 555 Langao Road, Putuo District, Shanghai, P. R. China 200333
Tel: +86-21-2226-0888, Fax: +86-21-2226-0999

Renesas Electronics Hong Kong Limited
Unit 1601-1611, 16/F., Tower 2, Grand Century Place, 193 Prince Edward Road West, Mongkok, Kowloon, Hong Kong
Tel: +852-2265-6688, Fax: +852 2886-9022

Renesas Electronics Taiwan Co., Ltd.
13F, No. 363, Fu Shing North Road, Taipei 10543, Taiwan
Tel: +886-2-8175-9600, Fax: +886 2-8175-9670

Renesas Electronics Singapore Pte. Ltd.
80 Bendemeer Road, Unit #06-02 Hyflux Innovation Centre, Singapore 339949
Tel: +65-6213-0200, Fax: +65-6213-0300

Renesas Electronics Malaysia Sdn.Bhd.
Unit 1207, Block B, Menara Amcorp, Amcorp Trade Centre, No. 18, Jln Persiaran Barat, 46050 Petaling Jaya, Selangor Darul Ehsan, Malaysia
Tel: +60-3-7955-9390, Fax: +60-3-7955-9510

Renesas Electronics India Pvt. Ltd.
No.777C, 100 Feet Road, HALII Stage, Indiranagar, Bangalore, India
Tel: +91-80-67208700, Fax: +91-80-67208777

Renesas Electronics Korea Co., Ltd.
12F., 234 Teheran-ro, Gangnam-Gu, Seoul, 135-080, Korea
Tel: +82-2-558-3737, Fax: +82-2-558-5141

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