R-IN32M4-CL3

Compared to conventional technologies, Ethernet communications in the industrial field are strongly required to have high-performance functions such as higher speed real-time response. These requirements are not necessarily realized by traditional methods such as making the Ethernet processing itself hardware or using a dedicated CPU for high-speed network processing.

The R-IN32M4-CL3 Ethernet communications LSI from Renesas Electronics has the following functions to realize “higher speed real-time response” and “high-accuracy communications control (low jitter communications)” which are important for Ethernet communications in the factory automation field.

■ CPU
- Integrated Arm® Cortex®-M4 core
- Integrated hardware real-time OS accelerator (HW-RTOS)

■ Peripheral
- Timers, WDT, I²C, UART, CSI, CAN, and general-purpose I/O ports (GPIO)
- Serial flash memory controller

■ External memory/external MCU (microcontroller) interface
- External memory connection mode: 16- or 32-bit bus connection to external devices such as SRAM
- External MCU connection mode: 16- or 32-bit bus connection to host MCU

■ Ethernet
- Integrated Gigabit Ethernet MAC
- Integrated switching hub with cut-through transfer, IEEE 1588 timer, and Device Level Ring (DLR) functions
- Integrated 2-port 10/100/1000BASE-PHY
- Dedicated DMA controller and buffer for the network processor

■ Supported industrial Ethernet protocol
- CC-Link IE Field intelligent device station and remote device station
- CC-Link IE TSN remote station (authentication Classes: A and B)
- PROFINET RT
- EtherNet/IP
- Modbus TCP

■ Target application
- Remote I/O
- Inverter and servo drive
- Industrial Ethernet communication unit

■ Others
- Pin assignment considering a replacement from R-IN32M4-CL2
- Integrated 2.5 V regulator for PHY

1. Overview

1.1 Functional Overview

Table 1.1 Functional Overview of R-IN32M4-CL3 (1/3)

Item \ Product	R9A06G064MGBG (23 mm Square Package)	R9A06G064SGBG (17 mm Square Package)
CPU core	Arm Cortex-M4 32-bit RISC CPU + Real-Time OS Accelerator (Hardware Real-Time OS)	
Operating frequency	100 MHz	
Instruction set	Thumb®-2 instruction Armv7-M architecture	
Floating-point UNIT	Armv7M FPv4-SP (32-bit single precision)	
Instruction RAM	768 Kbytes (RAM with ECC)	
Data RAM	512 Kbytes (RAM with ECC)	
Buffer RAM	64 Kbytes (RAM with ECC)	
Network RAM	128 Kbytes (RAM with ECC)	
Internal system bus	32-bit system bus at 100 MHz (AHB-Lite) 64-bit system bus at 125 MHz (AXI) 128-bit communication bus at 100 MHz	
DMA function (system bus side)	4 channels + 1 channel (for real-time port), Supports software and various interrupt-triggered DMA.	
Boot modes	Serial flash ROM boot, External memory boot, External MCU boot	
Support for external memory access	• Bus-size selection (16 or 32 bits) • Paged ROM/ROM/SRAM interface • Synchronous burst memory interface • Programmable wait function	
Chip select signals for static memory	4-line	4- or 3-line*1
External memory space	256 Mbytes	256 or 192 Mbytes
External MCU interface	• Bus-size selection (16 or 32 bits) • General-purpose interface for static memory • Address space: 2 Mbytes (Instruction RAM, Data RAM, Register area) • Internal address space mapping switching function	
Serial flash ROM memory controller	• Supports serial interface compatible with SPI of companies. • Supports direct boot from serial memory device. • Supports Fast Read, Fast Read Dual Output, Fast Read Dual I/O, Fast Read Quad Output, and Fast Read Quad I/O modes. • Direct layout in memory space	
Interrupt	• 30 external interrupt ports	

Note 1. When using an asynchronous SRAM controller in the 17 mm square package, the external memory areas of CSZ0–CSZ2 can be accessed.

Table 1.1 Functional Overview of R-IN32M4-CL3 (2/3)

Item \ Product	R9A06G064MGBG (23 mm Square Package)	R9A06G064SGBG (17 mm Square Package)
Internal peripheral modules		
I/O port	CMOS I/O: 106 maximum	CMOS I/O: 101 maximum
Timers (4 sub-systems)	• Internal timer of hardware RTOS • Internal timer of the CPU • 32-bit timer (4 channels) • 16-bit timer (16 channels)	
Watchdog timer	• 1 channel • Software-triggered start mode • Watchdog error response options: – Generation of a non-maskable interrupt (NMI) – Generation of a reset • Interrupt when the counter reaches 75% of its overflow value	
Asynchronous serial interface	• 2 channels • Full duplex transfer • FIFOs: 10 bits × 16 receive and 8 bits × 16 transmit • Support output of receive errors and status • Character length: 7 or 8 bits • Parity bit options: Odd, even, 0, none • Transmit stop bits: 1 bit or 2 bits	
I^2C serial interface	• 2 channels • Operating modes: Normal or high-speed • Transfer modes: Single-transfer mode or continuous-transfer mode • Transfer data length: 8 bits	
CAN controller	• 2 channels • Conforming to ISO11898 • Support for transmission and reception of standard and expanded frames • Transfer rate: Up to 1 Mbps	Not available
Clocked serial interface	• 2 channels • Synchronized serial data transmission by three-wire system • Master mode or slave mode selectable • Built-in baud-rate generator • Transfer data length: 7 to 16 bits	
10/100/1000Mbps Ethernet MAC	• 1 channel • Built-in 2-port switch	
Ethernet PHY	• 2 ports IEEE 802.3 • 10BASE-T, 100BASE-TX, 1000BASE-T	
CC-Link IE	Two types of CC-Link IE (CC-Link IE Field and CC-Link IE TSN) are supported. They can be used exclusively	
CC-Link IE Field	CC-Link IE Field (intelligent device station / remote device station)	
CC-Link IE TSN	CC-Link IE TSN	

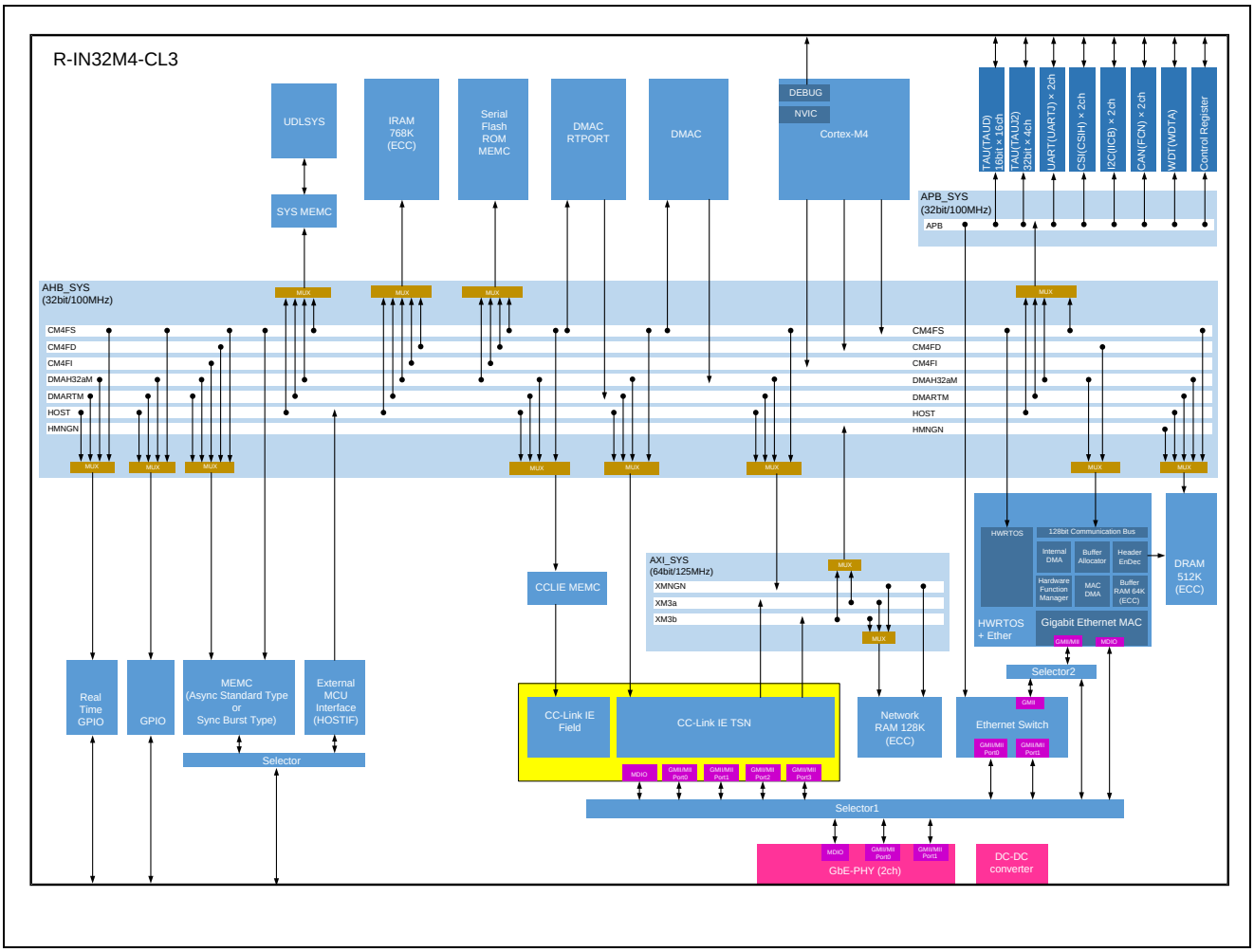
Table 1.1 Functional Overview of R-IN32M4-CL3 (3/3)

Item \ Product	R9A06G064MGBG (23 mm Square Package)	R9A06G064SGBG (17 mm Square Package)
On-chip debugging	• Selecting serial wire or JTAG • Full trace (built-in ETM)	
Internal PLL	Generates various clocks from 25 MHz input clock	
Built-in regulator	2.5V power supply dedicated to PHY can be generated from 3.3V power supply	
Power supply voltage	VDD33 = 3.3 ± 0.165 V*2 VDD11 = 1.15 ± 0.06 V*2 VDD25 = 2.5 ± 0.125 V*1, *2	
Operating temperature	-40°C ≤ Tj ≤ +125°C, -40°C ≤ Ta ≤ +85°C	
Packages	484-ball PBGA 23 mm × 23 mm, 1.0-mm Pitch	356-ball FBGA 17 mm × 17 mm, 0.8-mm Pitch

Note 1. 2.5 V power supply (VDD25) can be generated with the built-in regulator.

2. Ripple incorporated value. As a target value, set the DC component to within ±3% and the ripple component to within ±2%.

1.2 Internal Block Diagram



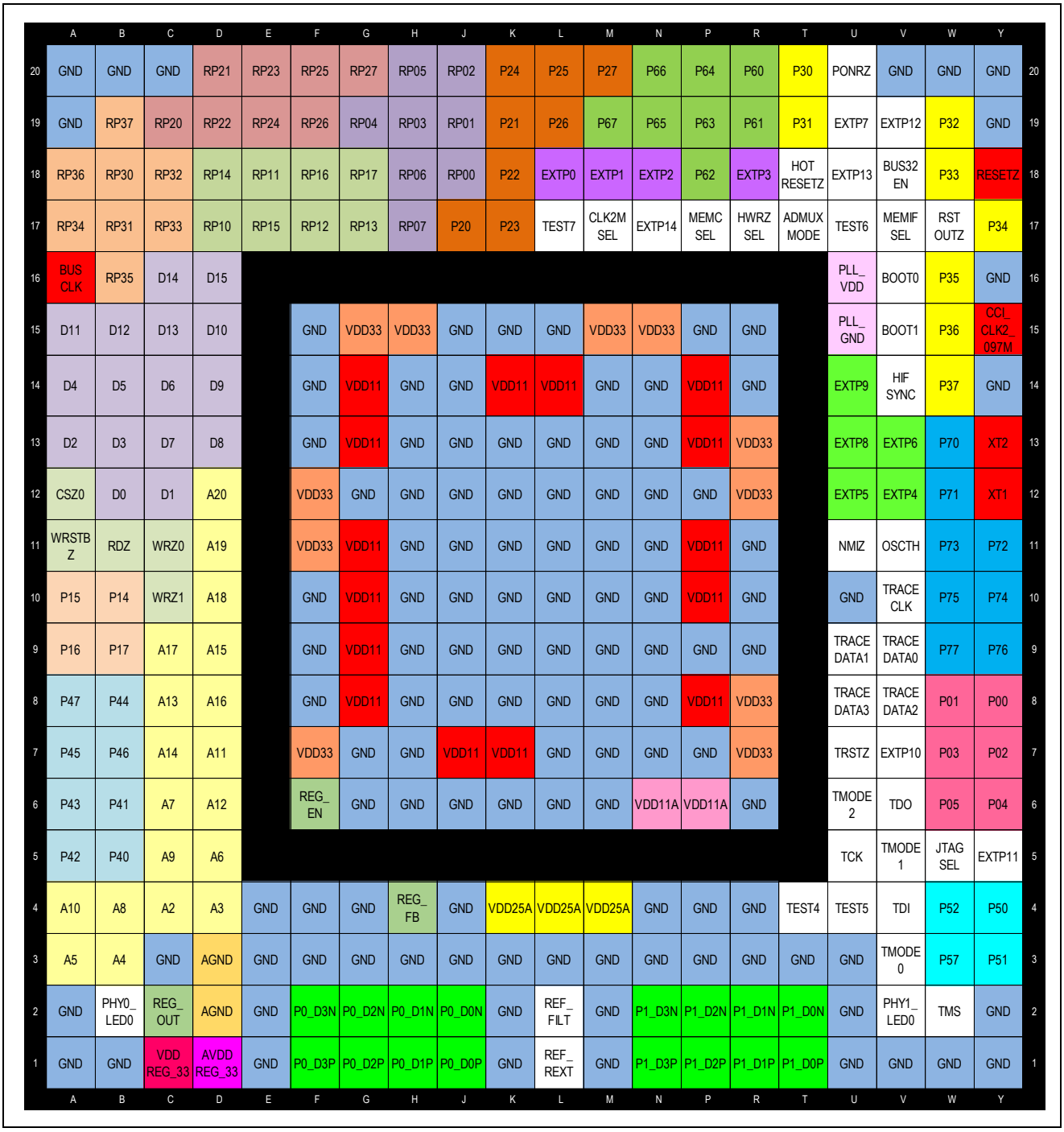
1.3 Pin Assignments (Top View)

1.3.1 23 mm Square Package Pin Assignments (Top View)

	A	B	C	D	E	F	G	H	J	K	L	M	N	P	R	T	U	V	W	Y	AA	AB	
22	GND	GND	RP21	RP23	RP25	RP27	RP02	RP00	GND/ OPEN	GND/ OPEN	GND/ OPEN	P20	P22	P25	GND	P67	P65	P63	P60	P30	GND	GND	22
21	GND	RP20	RP22	RP24	RP26	RP04	RP03	RP01	GND/ OPEN	GND/ OPEN	GND/ OPEN	P21	P23	P26	P27	P66	P64	P62	P61	P31	P32	GND	21
20	RP30	RP32	RP10	RP11	RP12	RP13	RP07	RP05	GND	VDD33	GND/ OPEN	GND	P24	EXTP0	EXTP1	EXTP2	EXTP3	HWRZ SEL	HOT RESETZ	PONRZ	P33	RESETZ	20
19	RP31	RP33	RP37	RP14	RP15	RP16	RP17	RP06	GND	VDD33	GND/ OPEN	GND	GND	TEST7	CLK2M SEL	VDD33	MEMC SEL	ADMUX MODE	BUS32 EN	RST OUTZ	P35	P34	19
18	BUS CLK	RP34	RP36	D15	GND	VDD33	GND	VDD33	GND	VDD33	VDD33	GND	GND	VDD11	GND	GND	VDD33	TEST6	MEMIF SEL	BOOT0	GND	CCI_ CLK2_0 97M	18
17	D6	RP35	D13	D14	TEST3	VDD33	GND	VDD11	VDD11	VDD11	VDD11	VDD11	VDD11	VDD11	VDD11	GND	VDD33	PLL_ VDD	HIF SYNC	BOOT1	P36	GND	17
16	D4	D5	D11	D12	GND	VDD33	GND	VDD11	GND	GND	GND	GND	GND	GND	VDD11	GND	VDD33	PLL_ GND	EXTP9	EXTP8	P37	GND	16
15	D2	D3	D9	D10	GND	GND	GND	VDD11	GND	GND	GND	GND	GND	GND	VDD11	GND	GND	GND	EXTP7	EXTP6	P70	XT2	15
14	D0	D1	D7	D8	GND	VDD33	GND	VDD11	GND	GND	GND	GND	GND	GND	VDD11	GND	GND	GND	EXTP5	EXTP4	P71	XT1	14
13	RDZ	WRSTB Z	CSZ0	A20	GND	GND	GND	VDD11	VDD11	VDD11	VDD11	VDD11	VDD11	VDD11	VDD11	GND	VDD33	GND	OSCTH	NMIZ	P73	P72	13
12	P10	P12	WRZ0	A19	GND	VDD33	VDD33	GND	VDD33	GND	VDD33	VDD33	GND	VDD33	GND	VDD33	VDD33	GND	GND	TRACE CLK	P75	P74	12
11	P11	P13	WRZ1	A18	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	TRACE DATA1	TRACE DATA0	P77	P76	11
10	P14	P15	A17	GND	GND	GND	GND	GND	GND	GND	GND/ OPEN	GND	GND	GND	GND	GND	GND	GND	GND	TRACE DATA2	P01	P00	10
9	P16	P17	A15	A16	GND	GND	GND	GND	VDD33	VDD33	VDD33	VDD33	VDD33	VDD33	GND	GND	GND	GND	TRSTZ	TRACE DATA3	P03	P02	9
8	P47	P44	A13	A14	GND	GND	GND	GND	VDD33	GND	GND	GND	GND	VDD33	GND	GND	GND	GND	TDO	JTAG SEL	P05	P04	8
7	P45	P46	A11	A12	GND	GND	GND	GND	VDD11	GND	GND	GND	GND	VDD11	GND	GND	GND	GND	TCK	TMODE 2	P07	P06	7
6	P43	P41	A9	A10	REG_ EN	GND	AVDD REG_33	GND	VDD11	GND	GND	GND	GND	VDD11	GND	GND	GND	GND	TDI	TMODE 1	P51	P50	6
5	P42	A7	A8	PHY ADD1	AGND	GND	VDD REG_33	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	TMS	TMODE 0	P53	P52	5
4	P40	A5	A6	PHY ADD2	AGND	REG_ OUT	GND	REG_ FB	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	TEST5	TEST4	P55	P54	4
3	A2	A3	A4	PHY ADD3	GND	GND	GND	GND	GND	VDD11A	VDD11A	GND	VDD25A	VDD25A	VDD25A	GND	GND	GND	GND	GND	P57	P56	3
2	GND	PHY0_ LED0	PHY ADD4	GND	GND	GND	P0_D3N	P0_D2N	P0_D1N	P0_D0N	GND	REF_ FILT	GND	P1_D3N	P1_D2N	P1_D1N	P1_D0N	GND	GND	GND	PHY1_ LED0	GND	2
1	GND	GND	GND	GND	GND	GND	P0_D3P	P0_D2P	P0_D1P	P0_D0P	GND	REF_ REXT	GND	P1_D3P	P1_D2P	P1_D1P	P1_D0P	GND	GND	GND	GND	GND	1
	A	B	C	D	E	F	G	H	J	K	L	M	N	P	R	T	U	V	W	Y	AA	AB	

Figure 1.1 23 mm Square Package Pin Assignments (Top View)

1.3.2 17 mm Square Package Pin Assignments (Top View)



	A	B	C	D	E	F	G	H	J	K	L	M	N	P	R	T	U	V	W	Y	
20	GND	GND	GND	RP21	RP23	RP25	RP27	RP05	RP02	P24	P25	P27	P66	P64	P60	P30	PONRZ	GND	GND	GND	20
19	GND	RP37	RP20	RP22	RP24	RP26	RP04	RP03	RP01	P21	P26	P67	P65	P63	P61	P31	EXTP7	EXTP12	P32	GND	19
18	RP36	RP30	RP32	RP14	RP11	RP16	RP17	RP06	RP00	P22	EXTP0	EXTP1	EXTP2	P62	EXTP3	HOT RESETZ	EXTP13	BUS32 EN	P33	RESETZ	18
17	RP34	RP31	RP33	RP10	RP15	RP12	RP13	RP07	P20	P23	TEST7	CLK2M SEL	EXTP14	MEMC SEL	HWRZ SEL	ADMUX MODE	TEST6	MEMIF SEL	RST OUTZ	P34	17
16	BUS CLK	RP35	D14	D15													PLL_ VDD	BOOT0	P35	GND	16
15	D11	D12	D13	D10		GND	VDD33	VDD33	GND	GND	GND	VDD33	VDD33	GND	GND		PLL_ GND	BOOT1	P36	CCI_ CLK2_ 097M	15
14	D4	D5	D6	D9		GND	VDD11	GND	GND	VDD11	VDD11	GND	GND	VDD11	GND		EXTP9	HIF SYNC	P37	GND	14
13	D2	D3	D7	D8		GND	VDD11	GND	GND	GND	GND	GND	GND	VDD11	VDD33		EXTP8	EXTP6	P70	XT2	13
12	CSZ0	D0	D1	A20		VDD33	GND	GND	GND	GND	GND	GND	GND	GND	VDD33		EXTP5	EXTP4	P71	XT1	12
11	WRSTB Z	RDZ	WRZ0	A19		VDD33	VDD11	GND	GND	GND	GND	GND	GND	VDD11	GND		NMIZ	OSCTH	P73	P72	11
10	P15	P14	WRZ1	A18		GND	VDD11	GND	GND	GND	GND	GND	GND	VDD11	GND		GND	TRACE CLK	P75	P74	10
9	P16	P17	A17	A15		GND	VDD11	GND	GND	GND	GND	GND	GND	GND	GND		TRACE DATA1	TRACE DATA0	P77	P76	9
8	P47	P44	A13	A16		GND	VDD11	GND	GND	GND	GND	GND	GND	VDD11	VDD33		TRACE DATA3	TRACE DATA2	P01	P00	8
7	P45	P46	A14	A11		VDD33	GND	GND	VDD11	VDD11	GND	GND	GND	GND	VDD33		TRSTZ	EXTP10	P03	P02	7
6	P43	P41	A7	A12		REG_ EN	GND	GND	GND	GND	GND	GND	VDD11A	VDD11A	GND		TMODE 2	TDO	P05	P04	6
5	P42	P40	A9	A6													TCK	TMODE 1	JTAG SEL	EXTP11	5
4	A10	A8	A2	A3	GND	GND	GND	REG_ FB	GND	VDD25A	VDD25A	VDD25A	GND	GND	GND	TEST4	TEST5	TDI	P52	P50	4
3	A5	A4	GND	AGND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	TMODE 0	P57	P51	3
2	GND	PHY0_ LED0	REG_ OUT	AGND	GND	P0_D3N	P0_D2N	P0_D1N	P0_D0N	GND	REF_ FILT	GND	P1_D3N	P1_D2N	P1_D1N	P1_D0N	GND	PHY1_ LED0	TMS	GND	2
1	GND	GND	VDD REG_33	AVDD REG_33	GND	P0_D3P	P0_D2P	P0_D1P	P0_D0P	GND	REF_ REXT	GND	P1_D3P	P1_D2P	P1_D1P	P1_D0P	GND	GND	GND	GND	1
	A	B	C	D	E	F	G	H	J	K	L	M	N	P	R	T	U	V	W	Y	

Figure 1.2 17 mm Square Package Pin Assignments (Top View)

1.4 External Pin List

1.4.1 23 mm Square Package

Table 1.2 23 mm Square Package External Pin List (1/4)

Pin ID	Pin Name	Pin ID	Pin Name	Pin ID	Pin Name	Pin ID	Pin Name
A1	GND	B15	D3	D7	A12	E21	RP26
A2	GND	B16	D5	D8	A14	E22	RP25
A3	A2	B17	RP35	D9	A16	F1	GND
A4	P40	B18	RP34	D10	GND	F2	GND
A5	P42	B19	RP33	D11	A18	F3	GND
A6	P43	B20	RP32	D12	A19	F4	REG_OUT
A7	P45	B21	RP20	D13	A20	F5	GND
A8	P47	B22	GND	D14	D8	F6	GND
A9	P16	C1	GND	D15	D10	F7	GND
A10	P14	C2	PHYADD4	D16	D12	F8	GND
A11	P11	C3	A4	D17	D14	F9	GND
A12	P10	C4	A6	D18	D15	F10	GND
A13	RDZ	C5	A8	D19	RP14	F11	GND
A14	D0	C6	A9	D20	RP11	F12	VDD33
A15	D2	C7	A11	D21	RP24	F13	GND
A16	D4	C8	A13	D22	RP23	F14	VDD33
A17	D6	C9	A15	E1	GND	F15	GND
A18	BUSCLK	C10	A17	E2	GND	F16	VDD33
A19	RP31	C11	WRZ1	E3	GND	F17	VDD33
A20	RP30	C12	WRZ0	E4	AGND	F18	VDD33
A21	GND	C13	CSZ0	E5	AGND	F19	RP16
A22	GND	C14	D7	E6	REG_EN	F20	RP13
B1	GND	C15	D9	E7	GND	F21	RP04
B2	PHY0_LED0	C16	D11	E8	GND	F22	RP27
B3	A3	C17	D13	E9	GND	G1	P0_D3P
B4	A5	C18	RP36	E10	GND	G2	P0_D3N
B5	A7	C19	RP37	E11	GND	G3	GND
B6	P41	C20	RP10	E12	GND	G4	GND
B7	P46	C21	RP22	E13	GND	G5	VDDREG_33
B8	P44	C22	RP21	E14	GND	G6	AVDDREG_33
B9	P17	D1	GND	E15	GND	G7	GND
B10	P15	D2	GND	E16	GND	G8	GND
B11	P13	D3	PHYADD3	E17	TEST3	G9	GND
B12	P12	D4	PHYADD2	E18	GND	G10	GND
B13	WRSTBZ	D5	PHYADD1	E19	RP15	G11	GND
B14	D1	D6	A10	E20	RP12	G12	VDD33

Table 1.2 23 mm Square Package External Pin List (2/4)

Pin ID	Pin Name	Pin ID	Pin Name	Pin ID	Pin Name	Pin ID	Pin Name
G13	GND	J9	VDD33	L5	GND	N1	GND
G14	GND	J10	GND	L6	GND	N2	GND
G15	GND	J11	GND	L7	GND	N3	VDD25A
G16	GND	J12	VDD33	L8	GND	N4	GND
G17	GND	J13	VDD11	L9	VDD33	N5	GND
G18	GND	J14	GND	L10	GND/OPEN	N6	GND
G19	RP17	J15	GND	L11	GND	N7	GND
G20	RP07	J16	GND	L12	VDD33	N8	GND
G21	RP03	J17	VDD11	L13	VDD11	N9	VDD33
G22	RP02	J18	GND	L14	GND	N10	GND
H1	P0_D2P	J19	GND	L15	GND	N11	GND
H2	P0_D2N	J20	GND	L16	GND	N12	GND
H3	GND	J21	GND/OPEN	L17	VDD11	N13	VDD11
H4	REG_FB	J22	GND/OPEN	L18	VDD33	N14	GND
H5	GND	K1	P0_D0P	L19	GND/OPEN	N15	GND
H6	GND	K2	P0_D0N	L20	GND/OPEN	N16	GND
H7	GND	K3	VDD11A	L21	GND/OPEN	N17	VDD11
H8	GND	K4	GND	L22	GND/OPEN	N18	GND
H9	GND	K5	GND	M1	REF_REXT	N19	GND
H10	GND	K6	GND	M2	REF_FILT	N20	P24
H11	GND	K7	GND	M3	GND	N21	P23
H12	GND	K8	GND	M4	GND	N22	P22
H13	VDD11	K9	VDD33	M5	GND	P1	P1_D3P
H14	VDD11	K10	GND	M6	GND	P2	P1_D3N
H15	VDD11	K11	GND	M7	GND	P3	VDD25A
H16	VDD11	K12	GND	M8	GND	P4	GND
H17	VDD11	K13	VDD11	M9	VDD33	P5	GND
H18	VDD33	K14	GND	M10	GND	P6	VDD11
H19	RP06	K15	GND	M11	GND	P7	VDD11
H20	RP05	K16	GND	M12	VDD33	P8	VDD33
H21	RP01	K17	VDD11	M13	VDD11	P9	VDD33
H22	RP00	K18	VDD33	M14	GND	P10	GND
J1	P0_D1P	K19	VDD33	M15	GND	P11	GND
J2	P0_D1N	K20	VDD33	M16	GND	P12	VDD33
J3	GND	K21	GND/OPEN	M17	VDD11	P13	VDD11
J4	GND	K22	GND/OPEN	M18	GND	P14	GND
J5	GND	L1	GND	M19	GND	P15	GND
J6	VDD11	L2	GND	M20	GND	P16	GND
J7	VDD11	L3	VDD11A	M21	P21	P17	VDD11
J8	VDD33	L4	GND	M22	P20	P18	VDD11

Table 1.2 23 mm Square Package External Pin List (3/4)

Pin ID	Pin Name
P19	TEST7
P20	EXTP0
P21	P26
P22	P25
R1	P1_D2P
R2	P1_D2N
R3	VDD25A
R4	GND
R5	GND
R6	GND
R7	GND
R8	GND
R9	GND
R10	GND
R11	GND
R12	GND
R13	VDD11
R14	VDD11
R15	VDD11
R16	VDD11
R17	VDD11
R18	GND
R19	CLK2MSEL
R20	EXTP1
R21	P27
R22	GND
T1	P1_D1P
T2	P1_D1N
T3	GND
T4	GND
T5	GND
T6	GND
T7	GND
T8	GND
T9	GND
T10	GND
T11	GND
T12	VDD33
T13	GND
T14	GND

Pin ID	Pin Name
T15	GND
T16	GND
T17	GND
T18	GND
T19	VDD33
T20	EXTP2
T21	P66
T22	P67
U1	P1_D0P
U2	P1_D0N
U3	GND
U4	GND
U5	GND
U6	GND
U7	GND
U8	GND
U9	GND
U10	GND
U11	GND
U12	VDD33
U13	VDD33
U14	GND
U15	GND
U16	VDD33
U17	VDD33
U18	VDD33
U19	MEMCSEL
U20	EXTP3
U21	P64
U22	P65
V1	GND
V2	GND
V3	GND
V4	GND
V5	GND
V6	GND
V7	GND
V8	GND
V9	GND
V10	GND

Pin ID	Pin Name
V11	GND
V12	GND
V13	GND
V14	GND
V15	GND
V16	PLL_GND
V17	PLL_VDD
V18	TEST6
V19	ADMUXMODE
V20	HWRZSEL
V21	P62
V22	P63
W1	GND
W2	GND
W3	GND
W4	TEST5
W5	TMS
W6	TDI
W7	TCK
W8	TDO
W9	TRSTZ
W10	GND
W11	TRACEDATA1
W12	GND
W13	OSCTH
W14	EXTP5
W15	EXTP7
W16	EXTP9
W17	HIFSYNC
W18	MEMIFSEL
W19	BUS32EN
W20	HOTRESETZ
W21	P61
W22	P60
Y1	GND
Y2	GND
Y3	GND
Y4	TEST4
Y5	TMODE0
Y6	TMODE1

Pin ID	Pin Name
Y7	TMODE2
Y8	JTAGSEL
Y9	TRACEDATA3
Y10	TRACEDATA2
Y11	TRACEDATA0
Y12	TRACECLK
Y13	NMIZ
Y14	EXTP4
Y15	EXTP6
Y16	EXTP8
Y17	BOOT1
Y18	BOOT0
Y19	RSTOUTZ
Y20	PONRZ
Y21	P31
Y22	P30
AA1	GND
AA2	PHY1_LED0
AA3	P57
AA4	P55
AA5	P53
AA6	P51
AA7	P07
AA8	P05
AA9	P03
AA10	P01
AA11	P77
AA12	P75
AA13	P73
AA14	P71
AA15	P70
AA16	P37
AA17	P36
AA18	GND
AA19	P35
AA20	P33
AA21	P32
AA22	GND
AB1	GND
AB2	GND

Table 1.2 23 mm Square Package External Pin List (4/4)

Pin ID	Pin Name	Pin ID	Pin Name	Pin ID	Pin Name	Pin ID	Pin Name
AB3	P56	AB8	P04	AB13	P72	AB18	CCI_CLK2_097M
AB4	P54	AB9	P02	AB14	XT1	AB19	P34
AB5	P52	AB10	P00	AB15	XT2	AB20	RESETZ
AB6	P50	AB11	P76	AB16	GND	AB21	GND
AB7	P06	AB12	P74	AB17	GND	AB22	GND

1.4.2 17 mm Square Package

Table 1.3 17 mm Square Package External Pin List (1/3)

Pin ID	Pin Name
A1	GND
A2	GND
A3	A5
A4	A10
A5	P42
A6	P43
A7	P45
A8	P47
A9	P16
A10	P15
A11	WRSTBZ
A12	CSZ0
A13	D2
A14	D4
A15	D11
A16	BUSCLK
A17	RP34
A18	RP36
A19	GND
A20	GND
B1	GND
B2	PHY0_LED0
B3	A4
B4	A8
B5	P40
B6	P41
B7	P46
B8	P44
B9	P17
B10	P14
B11	RDZ
B12	D0
B13	D3
B14	D5
B15	D12
B16	RP35
B17	RP31
B18	RP30

Pin ID	Pin Name
B19	RP37
B20	GND
C1	VDDREG_33
C2	REG_OUT
C3	GND
C4	A2
C5	A9
C6	A7
C7	A14
C8	A13
C9	A17
C10	WRZ1
C11	WRZ0
C12	D1
C13	D7
C14	D6
C15	D13
C16	D14
C17	RP33
C18	RP32
C19	RP20
C20	GND
D1	AVDDREG_33
D2	AGND
D3	AGND
D4	A3
D5	A6
D6	A12
D7	A11
D8	A16
D9	A15
D10	A18
D11	A19
D12	A20
D13	D8
D14	D9
D15	D10
D16	D15

Pin ID	Pin Name
D17	RP10
D18	RP14
D19	RP22
D20	RP21
E1	GND
E2	GND
E3	GND
E4	GND
E17	RP15
E18	RP11
E19	RP24
E20	RP23
F1	P0_D3P
F2	P0_D3N
F3	GND
F4	GND
F6	REG_EN
F7	VDD33
F8	GND
F9	GND
F10	GND
F11	VDD33
F12	VDD33
F13	GND
F14	GND
F15	GND
F17	RP12
F18	RP16
F19	RP26
F20	RP25
G1	P0_D2P
G2	P0_D2N
G3	GND
G4	GND
G6	GND
G7	GND
G8	VDD11
G9	VDD11

Pin ID	Pin Name
G10	VDD11
G11	VDD11
G12	GND
G13	VDD11
G14	VDD11
G15	VDD33
G17	RP13
G18	RP17
G19	RP04
G20	RP27
H1	P0_D1P
H2	P0_D1N
H3	GND
H4	REG_FB
H6	GND
H7	GND
H8	GND
H9	GND
H10	GND
H11	GND
H12	GND
H13	GND
H14	GND
H15	VDD33
H17	RP07
H18	RP06
H19	RP03
H20	RP05
J1	P0_D0P
J2	P0_D0N
J3	GND
J4	GND
J6	GND
J7	VDD11
J8	GND
J9	GND
J10	GND
J11	GND

Table 1.3 17 mm Square Package External Pin List (2/3)

Pin ID	Pin Name
J12	GND
J13	GND
J14	GND
J15	GND
J17	P20
J18	RP00
J19	RP01
J20	RP02
K1	GND
K2	GND
K3	GND
K4	VDD25A
K6	GND
K7	VDD11
K8	GND
K9	GND
K10	GND
K11	GND
K12	GND
K13	GND
K14	VDD11
K15	GND
K17	P23
K18	P22
K19	P21
K20	P24
L1	REF_REXT
L2	REF_FILT
L3	GND
L4	VDD25A
L6	GND
L7	GND
L8	GND
L9	GND
L10	GND
L11	GND
L12	GND
L13	GND
L14	VDD11
L15	GND

Pin ID	Pin Name
L17	TEST7
L18	EXTP0
L19	P26
L20	P25
M1	GND
M2	GND
M3	GND
M4	VDD25A
M6	GND
M7	GND
M8	GND
M9	GND
M10	GND
M11	GND
M12	GND
M13	GND
M14	GND
M15	VDD33
M17	CLK2MSEL
M18	EXTP1
M19	P67
M20	P27
N1	P1_D3P
N2	P1_D3N
N3	GND
N4	GND
N6	VDD11A
N7	GND
N8	GND
N9	GND
N10	GND
N11	GND
N12	GND
N13	GND
N14	GND
N15	VDD33
N17	EXTP14
N18	EXTP2
N19	P65
N20	P66

Pin ID	Pin Name
P1	P1_D2P
P2	P1_D2N
P3	GND
P4	GND
P6	VDD11A
P7	GND
P8	VDD11
P9	GND
P10	VDD11
P11	VDD11
P12	GND
P13	VDD11
P14	VDD11
P15	GND
P17	MEMCSEL
P18	P62
P19	P63
P20	P64
R1	P1_D1P
R2	P1_D1N
R3	GND
R4	GND
R6	GND
R7	VDD33
R8	VDD33
R9	GND
R10	GND
R11	GND
R12	VDD33
R13	VDD33
R14	GND
R15	GND
R17	HWRZSEL
R18	EXTP3
R19	P61
R20	P60
T1	P1_D0P
T2	P1_D0N
T3	GND
T4	TEST4

Pin ID	Pin Name
T17	ADMUXMODE
T18	HOTRESETZ
T19	P31
T20	P30
U1	GND
U2	GND
U3	GND
U4	TEST5
U5	TCK
U6	TMODE2
U7	TRSTZ
U8	TRACEDATA3
U9	TRACEDATA1
U10	GND
U11	NMIZ
U12	EXTP5
U13	EXTP8
U14	EXTP9
U15	PLL_GND
U16	PLL_VDD
U17	TEST6
U18	EXTP13
U19	EXTP7
U20	PONRZ
V1	GND
V2	PHY1_LED0
V3	TMODE0
V4	TDI
V5	TMODE1
V6	TDO
V7	EXTP10
V8	TRACEDATA2
V9	TRACEDATA0
V10	TRACECLK
V11	OSCTH
V12	EXTP4
V13	EXTP6
V14	HIFSYNC
V15	BOOT1
V16	BOOT0

Table 1.3 17 mm Square Package External Pin List (3/3)

Pin ID	Pin Name
V17	MEMIFSEL
V18	BUS32EN
V19	EXTP12
V20	GND
W1	GND
W2	TMS
W3	P57
W4	P52
W5	JTAGSEL
W6	P05
W7	P03

Pin ID	Pin Name
W8	P01
W9	P77
W10	P75
W11	P73
W12	P71
W13	P70
W14	P37
W15	P36
W16	P35
W17	RSTOUTZ
W18	P33

Pin ID	Pin Name
W19	P32
W20	GND
Y1	GND
Y2	GND
Y3	P51
Y4	P50
Y5	EXTP11
Y6	P04
Y7	P02
Y8	P00
Y9	P76

Pin ID	Pin Name
Y10	P74
Y11	P72
Y12	XT1
Y13	XT2
Y14	GND
Y15	CCI_CLK2_097M
Y16	GND
Y17	P34
Y18	RESETZ
Y19	GND
Y20	GND

2. Pin List by Function

The following tables list the meanings of the items, symbols, and abbreviations used in each pin table in this chapter. Some pins and functions are not available depending on the type of package. Refer to the PKG column.

Table 2.1 Meanings of the Items in the Pin Lists

Item	Meaning
Function Name	Name of a function of the pin under “Pin Name” below.
Pin Name	Name of the pin shown in Section 1.3 “Pin Assignments (Top View)”.
PKG	Type of package 23□: 23 mm Square Package 17□: 17 mm Square Package
I/O	I/O direction of the given pin
Description	Summary of the given pin function
Active	Active level of the given pin
Level during Reset	The pin state while RSTOUTZ is Low. For details on the reset specifications, refer to the “R-IN32M4-CL3 User’s Manual: Hardware edition”.

Table 2.2 Meanings of the Symbols and Abbreviations in the Pin Lists

Target	Symbol and Abbreviation	Meaning
Pin Name	— (hyphen)	The pin is a dedicated pin that is not multiplexed with a port-pin function.
PKG	○	The pin exists.
	×	The pin does not exist.
I/O	— (hyphen)	The pin does not have an I/O direction, such as a power supply or ground pin.
Active	— (hyphen)	There is no active level (clock pins, data pins, and address pins).
	High	The active level is high.
	Low	The active level is low.
Level during Reset	— (hyphen)	This is an input-dedicated pin that has no initial level or state following a reset.
	High	The pin state during a reset is high.
	Low	The pin state during a reset is low.
	Hi-Z (High)	The pin state during a reset is Hi-Z (high) with the internal pull-up resistor pulling it to the high level.
	Hi-Z (Low)	The pin state during a reset is Hi-Z (Low) with the internal pull-down resistor pulling it to the Low level.

The pins described in Section 2.2 “Ethernet Pins” to Section 2.15 “Operating Mode Setting Pins" are multiplexed with port pins described in Section 2.1 “Port Pins and Real-Time Port Pins”. For details, refer to Multiplexed function 1 to Multiplexed function 4 in Section 2.1 “Port Pins and Real-Time Port Pins”.

2.1 Port Pins and Real-Time Port Pins

The LSI has 13 ports for the 3.3 V interface, all of which are 8-bit ports except for EXTP, which has 15 bits. Grouping them into sets of four ports allows 32-bit access: for example, through ports 0 to 3 (P00–P37), ports 4 to 7 (P40–P77), and real-time ports 0 to 3 (RP00–RP37).

(1/5)

Pin Name	PKG 23□	PKG 17□	Multiplexed Function 1	Multiplexed Function 2	Multiplexed Function 3	Multiplexed Function 4	Level during Reset
P00	○	○	INTPZ0	—	CCI_RUNLEDZ	—	Hi-Z (High)
P01	○	○	INTPZ1	—	—	—	
P02	○	○	INTPZ2	—	CCI_DLINKLEDZ	—	
P03	○	○	INTPZ3	—	CCI_ERRLEDZ	—	
P04	○	○	INTPZ4	—	CCI_LERR1LEDZ	—	
P05	○	○	INTPZ5	—	CCI_LERR2LEDZ	—	
P06	○	×	—	—	CCI_SDLEDZ	—	
P07	○	×	—	—	CCI_RDLEDZ	—	
P10	○	×	SMIO2	—	—	—	
P11	○	×	SMIO3	—	—	—	
P12	○	×	CSZ3	—	CCI_WDTIZ	—	
P13	○	×	CSZ2	—	—	—	
P14	○	○	SMSCK	—	—	—	
P15	○	○	SMIO0	—	—	—	
P16	○	○	SMIO1	—	—	—	
P17	○	○	SMCSZ	—	—	—	
P20	○	○	RXD0	—	—	—	
P21	○	○	TXD0	—	—	—	
P22	○	○	INTPZ8	—	—	—	
P23	○	○	INTPZ9	—	—	—	
P24	○	○	INTPZ10	ETHSWSYNCOUT	—	—	
P25	○	○	WDTOUTZ	—	—	—	
P26	○	○	TINJ1 / TIND5*1	TOUTJ1 / TOUTD5*1	—	—	
P27	○	○	TINJ0 / TIND4*1	TOUTJ0 / TOUTD4*1	—	—	

Note 1. Enabling the TAUJ2 or TAUD pin function is selectable by using the TMISEL register. For details, refer to the "R-IN32M4-CL3 User's Manual: Hardware edition".

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Pin Name	PKG 23□	PKG 17□	Multiplexed Function 1	Multiplexed Function 2	Multiplexed Function 3	Multiplexed Function 4	Level during Reset
P30	○	○	RXD1	—	—	—	Hi-Z (High)
P31	○	○	TXD1	—	—	—	
P32	○	○	DMAREQZ1	—	—	—	
P33	○	○	DMAACKZ1	—	—	—	
P34	○	○	DMATCZ1	—	—	—	
P35	○	○	CSISCK1	INTPZ22	—	—	Hi-Z (Low)
P36	○	○	CSISI1	INTPZ23	—	—	Hi-Z (High)
P37	○	○	CSISO1	INTPZ24	—	—	Hi-Z (Low)
P40	○	○	A1 / MA0	HA1	—	—	Hi-Z (High)
P41	○	○	WAITZ	HWAITZ	INTPZ29	—	
P42	○	○	CSICS00	HERROUTZ	—	—	
P43	○	○	CSICS01	HBUSCLK	—	—	
P44	○	○	CSZ1	HPGCSZ	—	—	
P45	○	○	CSISCK0	WAITZ1	—	—	
P46	○	○	CSISI0	WAITZ2	—	—	
P47	○	○	CSISO0	WAITZ3	—	—	
P50	○	○	INTPZ6	—	—	—	
P51	○	○	INTPZ7	—	—	—	Hi-Z (Low)
P52	○	○	TINJ3 / TIND7*1	TOUTJ3 / TOUTD7*1	CCI_NMIZ	—	Hi-Z (High)
P53	○	×	CRXD0	CCI_INTZ	—	—	
P54	○	×	CTXD0	—	—	—	
P55	○	×	CRXD1	—	—	—	
P56	○	×	CTXD1	—	—	—	
P57	○	○	TINJ2 / TIND6*1	TOUTJ2 / TOUTD6*1	—	—	

Note 1. Enabling the TAUJ2 or TAUD pin function is selectable by using the TMISEL register. For details, refer to the "R-IN32M4-CL3 User's Manual: Hardware edition".

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Pin Name	PKG 23□	PKG 17□	Multiplexed Function 1	Multiplexed Function 2	Multiplexed Function 3	Multiplexed Function 4	Level during Reset
P60	○	○	SCL0	—	—	—	Hi-Z (High)
P61	○	○	SDA0	—	—	—	
P62	○	○	RTDMAREQZ	—	—	—	
P63	○	○	RTDMAACKZ	—	—	—	
P64	○	○	RTDMATCZ	—	—	—	
P65	○	○	DMAREQZ0	—	—	—	
P66	○	○	DMAACKZ0	—	—	—	
P67	○	○	DMATCZ0	—	—	—	
P70	○	○	CSICS10	—	—	—	
P71	○	○	CSICS11	—	—	—	
P72	○	○	SLEEPING	—	—	—	
P73	○	○	INTPZ11	—	—	—	
P74	○	○	INTPZ12	—	—	—	
P75	○	○	INTPZ13	—	—	—	
P76	○	○	INTPZ14	—	—	—	
P77	○	○	INTPZ15	—	—	—	

(4/5)

Pin Name	PKG 23□	PKG 17□	Multiplexed Function 1	Multiplexed Function 2	Multiplexed Function 3	Multiplexed Function 4	Level during Reset
EXTP0	○	○	—	TOUTD0	—	TIND0	Hi-Z (High)
EXTP1	○	○	—	TOUTD1	—	TIND1	
EXTP2	○	○	—	TOUTD2	—	TIND2	
EXTP3	○	○	WDTOUTZ	TOUTD3	—	TIND3	
EXTP4	○	○	—	—	—	—	
EXTP5	○	○	—	—	—	—	
EXTP6	○	○	—	—	—	—	Hi-Z (Low)
EXTP7	○	○	—	—	—	—	Hi-Z (High)
EXTP8	○	○	—	—	—	—	
EXTP9	○	○	—	—	—	—	
EXTP10	×	○	SMIO2	CCI_INTZ	—	—	
EXTP11	×	○	SMIO3	CCI_WDTIZ	—	—	
EXTP12	×	○	CSZ3	CCI_SDLEDZ	—	—	
EXTP13	×	○	CSZ2	CCI_RDLEDZ	—	—	
EXTP14	×	○	IETYPE_LED	—	—	—	

Ports RP0x to RP3x (x: 0–7) operate as real-time ports. These ports can handle input and output in 32-bit units in synchronization with the DMA transfer trigger from the dedicated DMA controller for the real-time ports.

(5/5)

Pin Name	PKG 23□	PKG 17□	Multiplexed Function 1	Multiplexed Function 2	Multiplexed Function 3	Multiplexed Function 4	Level during Reset
RP00	○	○	INTPZ16	SCL1	—	—	Hi-Z (High)
RP01	○	○	INTPZ17	SDA1	—	—	
RP02	○	○	INTPZ18	—	—	—	
RP03	○	○	INTPZ19	—	—	—	
RP04	○	○	INTPZ20	—	—	—	
RP05	○	○	INTPZ21	—	—	—	
RP06	○	○	WRZ2 / BENZ2	HWRZ2 / HBENZ2	—	—	
RP07	○	○	WRZ3 / BENZ3	HWRZ3 / HBENZ3	—	—	
RP10	○	○	D24 / MD24 / HD24	LED0_PHY0	—	—	
RP11	○	○	D25 / MD25 / HD25	LED1_PHY0	—	—	
RP12	○	○	D26 / MD26 / HD26	LED2_PHY0	—	—	
RP13	○	○	D27 / MD27 / HD27	LED3_PHY0	—	—	
RP14	○	○	D28 / MD28 / HD28	LED0_PHY1	—	—	
RP15	○	○	D29 / MD29 / HD29	LED1_PHY1	—	—	
RP16	○	○	D30 / MD30 / HD30	LED2_PHY1	—	—	
RP17	○	○	D31 / MD31 / HD31	LED3_PHY1	—	—	
RP20	○	○	BCYSTZ / ADVZ	HBCYSTZ	—	—	
RP21	○	×	A21 / MA20	—	—	—	Hi-Z (Low)
	×	○					Hi-Z (High)
RP22	○	×	A22 / MA21	—	—	—	Hi-Z (Low)
	×	○					Hi-Z (High)
RP23	○	×	A23 / MA22	—	—	—	Hi-Z (Low)
	×	○					Hi-Z (High)
RP24	○	×	A24 / MA23	INTPZ25	—	—	Hi-Z (Low)
	×	○					Hi-Z (High)
RP25	○	×	A25 / MA24	INTPZ26	—	—	Hi-Z (Low)
	×	○					Hi-Z (High)
RP26	○	×	A26 / MA25	INTPZ27	—	—	Hi-Z (Low)
	×	○					Hi-Z (High)
RP27	○	×	A27 / MA26	INTPZ28	—	—	Hi-Z (Low)
	×	○					Hi-Z (High)
RP30	○	○	D16 / MD16 / HD16	TOUTD8	TIND8	—	
RP31	○	○	D17 / MD17 / HD17	TOUTD9	TIND9	—	
RP32	○	○	D18 / MD18 / HD18	TOUTD10	TIND10	—	
RP33	○	○	D19 / MD19 / HD19	TOUTD11	TIND11	—	
RP34	○	○	D20 / MD20 / HD20	TOUTD12	TIND12	—	
RP35	○	○	D21 / MD21 / HD21	TOUTD13	TIND13	—	
RP36	○	○	D22 / MD22 / HD22	TOUTD14	TIND14	—	
RP37	○	○	D23 / MD23 / HD23	TOUTD15	TIND15	—	

2.2 Ethernet Pins

(1/2)

Function Name	Pin Name	PKG 23□	PKG 17□	I/O	Description	Active	Level during Reset
P0_D0N	—	○	○	I/O	PHY 0 Tx/Rx channel A negative signal	—	—
P0_D0P	—	○	○		PHY 0 Tx/Rx channel A positive signal		
P0_D1N	—	○	○		PHY 0 Tx/Rx channel B negative signal		
P0_D1P	—	○	○		PHY 0 Tx/Rx channel B positive signal		
P0_D2N	—	○	○		PHY 0 Tx/Rx channel C negative signal		
P0_D2P	—	○	○		PHY 0 Tx/Rx channel C positive signal		
P0_D3N	—	○	○		PHY 0 Tx/Rx channel D negative signal		
P0_D3P	—	○	○		PHY 0 Tx/Rx channel D positive signal		
P1_D0N	—	○	○		PHY 1 Tx/Rx channel A negative signal		
P1_D0P	—	○	○		PHY 1 Tx/Rx channel A positive signal		
P1_D1N	—	○	○		PHY 1 Tx/Rx channel B negative signal		
P1_D1P	—	○	○		PHY 1 Tx/Rx channel B positive signal		
P1_D2N	—	○	○		PHY 1 Tx/Rx channel C negative signal		
P1_D2P	—	○	○		PHY 1 Tx/Rx channel C positive signal		
P1_D3N	—	○	○		PHY 1 Tx/Rx channel D negative signal		
P1_D3P	—	○	○		PHY 1 Tx/Rx channel D positive signal		
PHYADD1	—	○	×	I	Device SMI Address bit 1 (with Pull-Down resistance)		
PHYADD2	—	○	×		Device SMI Address bit 2 (with Pull-Down resistance)		
PHYADD3	—	○	×		Device SMI Address bit 3 (with Pull-Down resistance)		
PHYADD4	—	○	×		Device SMI Address bit 4 (with Pull-Down resistance)		
REF_FILT	—	○	○	I/O	Copper media reference filter pin.		
REF_REXT	—	○	○		Copper media reference external pin.		
VDD11A	—	○	○	—	1.15 V analog power requiring additional PCB power supply filtering		
VDD25A	—	○	○		2.5 V general analog power supply		
PHY0_LED0	—	○	○	O	GbE-PHY LED0_PHY0 output signal	Low	High
PHY1_LED0	—	○	○		GbE-PHY LED0_PHY1 output signal		
LED0_PHY0	RP10	○	○		GbE-PHY LED signal output (Same signal as external pin PHY0_LED0)		Hi-Z (High)
LED1_PHY0	RP11	○	○		GbE-PHY LED signal output		
LED2_PHY0	RP12	○	○		GbE-PHY LED signal output		
LED3_PHY0	RP13	○	○		GbE-PHY LED signal output		
LED0_PHY1	RP14	○	○		GbE-PHY LED signal output (Same signal as external pin PHY1_LED0)		
LED1_PHY1	RP15	○	○		GbE-PHY LED signal output		
LED2_PHY1	RP16	○	○		GbE-PHY LED signal output		
LED3_PHY1	RP17	○	○		GbE-PHY LED signal output		
ETHSWSYNCOUT	P24	○	○		Ethernet switch event output	High	

(2/2)

Function Name	Pin Name	PKG 23□	PKG 17□	I/O	Description	Active	Level during Reset
VDDREG_33	—	○	○	—	3.3 V power for 2.5 V regulator	—	—
AVDDREG_33	—	○	○		3.3 V analog power for 2.5 V regulator		
REG_EN	—	○	○	I	2.5 V Regulator enable		
REG_FB	—	○	○		Feedback from the supply regulation point		
AGND	—	○	○	—	Analog ground for regulator		
REG_OUT*1	—	○	○	O	2.5 V Regulator output		

Note 1. The power supply of 2.5 V via the REG_OUT pin is dedicated to the VDD25A. The pin is not available for the power supply of 2.5 V to other devices.

2.3 External SRAM and External MCU Interface Pins

Usage of the external SRAM interface pins and external MCU interface pins is exclusive.
This setting is selected by the level of the MEMIFSEL pin. (Setting value: Low level for the external SRAM interface pins and High level for the external MCU interface pins)

2.3.1 External SRAM Interface Pins

(a) External SRAM Interface Pins (when Asynchronous SRAM Controller is Selected (MEMCSEL = 0))

Function Name	Pin Name	PKG 23□	PKG 17□	I/O	Description	Active	Level during Reset
BUSCLK	—	○	○	O	Bus clock output	—	Clock output
CSZ0	—	○	○		Chip select signal output	Low	Hi-Z (High)
CSZ1	P44	○	○				
CSZ2	P13	○	×				
	EXTP13	×	○				
CSZ3	P12	○	×				
	EXTP12	×	○				
A1	P40	○	○		Address output	—	
A2–A20	—	○	○				Hi-Z (Low)
A21–A27	RP21–RP27	○	○				Hi-Z (High)
D0–D15	—	○	○	I/O	Data bus		Hi-Z (Low)
D16–D31	RP30–RP37, RP10–RP17	○	○				Hi-Z (High)
RDZ	—	○	○	O	Read strobe output	Low	
WRSTBZ	—	○	○		Write strobe output		
WRZ0 / BENZ0*1	WRZ0	○	○		Valid byte lane strobe output		
WRZ1 / BENZ1*1	WRZ1	○	○				
WRZ2 / BENZ2*1	RP06	○	○				
WRZ3 / BENZ3*1	RP07	○	○				
WAITZ	P41	○	○	I	Wait signal input		
BCYSTZ	RP20	○	○	O	Bus cycle start status output		

Remark. The external memory interface pins other than BUSCLK are inputs as long as the internal reset signal (HRESETZ) is active.

Note 1. The WREN register is used to switch the pin functions between WRZ3–WRZ0 and BENZ3–BENZ0. For details on this register, refer to the "R-IN32M4-CL3 User's Manual: Hardware edition".

(b) External SRAM Interface Pins (When Synchronous Burst Access Memory Controller is Selected (MEMCSEL = 1))

Function Name	Pin Name	PKG 23□	PKG 17□	I/O	Description	Active	Level during Reset
BUSCLK	—	○	○	O	Bus clock output	—	Low
CSZ0	—	○	○		Chip select signal output	Low	Hi-Z (High)
CSZ1	P44	○	○				
CSZ2	P13	○	×				
	EXTP13	×	○				
CSZ3	P12	○	×				
	EXTP12	×	○				
MA0	P40	○	○		Address output	—	
MA1–MA19	A2–A20	○	○				Hi-Z (Low)
MA20–MA26	RP21–RP27	○	○				Hi-Z (High)
MD0–MD15 / MA0–MA15*1	D0–D15	○	○	I/O	Data bus		Hi-Z (Low)
MD16–MD31 / MA16–MA31*1	RP30–RP37, RP10–RP17	○	○				Hi-Z (High)
RDZ	—	○	○	O	Read strobe output	Low	
WRSTBZ	—	○	○		Write strobe output		
WRZ0 / BENZ0*2	WRZ0	○	○		Valid byte lane strobe output		
WRZ1 / BENZ1*2	WRZ1	○	○				
WRZ2 / BENZ2*2	RP06	○	○				
WRZ3 / BENZ3*2	RP07	○	○				
WAITZ	P41	○	○	I	Wait signal input		
WAITZ1–WAITZ3	P45–P47	○	○				
ADVZ	RP20	○	○	O	Address valid output		

Remark. The external memory interface pins other than BUSCLK are inputs as long as the internal reset signal (HRESETZ) is active.

Note 1. When the ADMUXMODE pin is at the High level, these pin functions are multiplexed with address pin functions.
ADMUXMODE = 0: MD0–MD31 (separated address and data lines)
ADMUXMODE = 1: MD0–MD31 / MA0 to MA31 (multiplexed address and data lines)

2. The SET_OPMODE register is used to the switch pin functions between WRZ3–WRZ0 and BENZ3–BENZ0.
For details on this register, refer to the "R-IN32M4-CL3 User's Manual: Hardware edition".

2.3.2 External MCU Interface Pins

(a) External MCU Interface Pins (When Asynchronous SRAM Memory Controller is Selected (MEMCSEL = 0))

Function Name	Pin Name	PKG 23□	PKG 17□	I/O	Description	Active	Level during Reset
HBUSCLK*1	P43	○	○	I	Bus clock input	—	Hi-Z (High)
HCSZ	CSZ0	○	○		Chip select signal input	Low	
HPGCSZ	P44	○	○		Page ROM mode chip select signal input		
HWAITZ	P41	○	○	O	Wait signal output		
HA1	P40	○	○	I	Address signal input	—	
HA2–HA20	A2–A20	○	○				Hi-Z (Low)
HD0–HD15	D0–D15	○	○	I/O	Data bus		
HD16–HD31	RP30–RP37, RP10–RP17	○	○				Hi-Z (High)
HRDZ	RDZ	○	○	I	Read strobe input	Low	
HWRSTBZ	WRSTBZ	○	○		Write strobe input		
HWRZ0 / HBENZ0*2	WRZ0	○	○		Valid byte lane strobe input		
HWRZ1 / HBENZ1*2	WRZ1	○	○				
HWRZ2 / HBENZ2*2	RP06	○	○				
HWRZ3 / HBENZ3*2	RP07	○	○				
HERROUTZ	P42	○	○	O	Error interrupt output		High
HBCYSTZ	RP20	○	○	I	Bus cycle input		Hi-Z (High)

Note 1. The HBUSCLK pin is used only in case of synchronous SRAM supported MCU connection mode (HIFSYNC pin is High). The HBUSCLK pin is not used in case of asynchronous SRAM supported MCU connection mode (HIFSYNC pin is Low). Furthermore, the other signal connection is common in each mode.
For details on the connection example, refer to the "R-IN32M4-CL3 User's Manual: Board Design edition".

2. The level being input on the HWRZSEL pin controls switching between HWRZ3–HWRZ0 and HBENZ3–HBENZ0 signals.

Remark. The external MCU interface pins continue to operate as those pins even during a reset.

(b) External MCU Interface Pins (When Synchronous Burst Access Memory Controller is Selected (MEMCSEL = 1))

Function Name	Pin Name	PKG 23□	PKG 17□	I/O	Description	Active	Level during Reset
HBUSCLK	P43	○	○	I	Bus clock input	—	Hi-Z (High)
HCSZ	CSZ0	○	○		Chip select signal input	Low	
HPGCSZ	P44	○	○		Page ROM mode chip select signal input		
HWAITZ	P41	○	○	O	Wait signal output		
HA1*1	P40	○	○	I	Address signal input	—	
HA2–HA20*1	A2–A20	○	○				Hi-Z (Low)
HD0–HD15*1	D0–D15	○	○	I/O	Data bus		
HD16–HD31*1	RP30–RP37, RP10–RP17	○	○				Hi-Z (High)
HRDZ	RDZ	○	○	I	Read strobe input	Low	
HWRSTBZ	WRSTBZ	○	○		Write strobe input		
HWRZ0 / HBENZ0*2	WRZ0	○	○		Valid byte lane strobe input		
HWRZ1 / HBENZ1*2	WRZ1	○	○				
HWRZ2 / HBENZ2*2	RP06	○	○				
HWRZ3 / HBENZ3*2	RP07	○	○				
HERROUTZ	P42	○	○	O	Error interrupt output		High
HBCYSTZ	RP20	○	○	I	Bus cycle input		Hi-Z (High)

Note 1. The address/data pin connection depends on address/data multiplex mode (ADMUXMODE pin is High) or address/data separate mode (ADMUXMODE pin is Low).
For details on the connection example, refer to the "R-IN32M4-CL3 User's Manual: Board Design edition".
2. When the MEMCSEL pin is High, setting the HWRZSEL pin to High is prohibited.

Remark. The external MCU interface pins continue to operate as those pins even during a reset.

2.4 Serial Flash ROM Interface Pins

The serial flash ROM interface pins are the pins of the serial flash ROM controller.
These pins support the following instruction formats: Fast Read, Fast Read Dual Output, Fast Read Dual I/O, Fast Read Quad Output, and Fast Read Quad I/O.

Function Name	Pin Name	PKG 23□	PKG 17□	I/O	Description	Active	Level during Reset
SMSCK	P14	○	○	O	Serial clock output signal for serial flash ROM	—	Hi-Z (High)
SMIO0	P15	○	○	I/O	Serial data I/O signals for serial flash ROM (Connected to the IO0 pin of serial flash ROM)		
SMIO1	P16	○	○		Serial data I/O signals for serial flash ROM (Connected to the IO1 pin of serial flash ROM)		
SMIO2	P10	○	×		Serial data I/O signals for serial flash ROM (Connected to the /WP(IO2) pin of serial flash ROM)		
	EXTP10	×	○				
SMIO3	P11	○	×		Serial data I/O signals for serial flash ROM (Connected to the /HOLD(IO3) pin of serial flash ROM)		
	EXTP11	×	○				
SMCSZ	P17	○	○	O	Chip select output signal for serial flash ROM	Low	

2.5 DMA Interface Pins

The DMA interface pins are the external interface pins of the DMA controllers.
Two types of DMA controllers built into the R-IN32M4-CL3, general-purpose DMA controllers (channels 0 and 1) and real-time port DMA controller, can be used as external DMA interfaces.

Function Name	Pin Name	PKG 23□	PKG 17□	I/O	Description	Active	Level during Reset
RTDMAREQZ	P62	○	○	I	RTDMAC DMA transfer request input	Low	Hi-Z (High)
RTDMAACKZ	P63	○	○	O	RTDMAC DMA acknowledge output		
RTDMATCZ	P64	○	○		RTDMAC terminal count output		
DMAREQZ0	P65	○	○	I	DMA transfer request input 0		
DMAACKZ0	P66	○	○	O	DMA acknowledge output 0		
DMATCZ0	P67	○	○		Terminal count output 0		
DMAREQZ1	P32	○	○	I	DMA transfer request input 1		
DMAACKZ1	P33	○	○	O	DMA acknowledge output 1		
DMATCZ1	P34	○	○		Terminal count output 1		

Note. These pins are fixed to channels of the DMA controllers. The pins cannot be assigned to the desired channel. For details, refer to the "R-IN32M4-CL3 User's Manual: Hardware edition".

2.6 External Interrupt Input Pins

The LSI has one non-maskable interrupt and 30 maskable interrupt input pins.

Function Name	Pin Name	PKG 23□	PKG 17□	I/O	Description	Active	Level during Reset
NMIZ	—	○	○	I	Non-maskable external interrupt input	Low	Hi-Z (High)
INTPZ0–INTPZ5	P00–P05	○	○	I	External interrupt input		
INTPZ6	P50	○	○				
INTPZ7	P51	○	○				Hi-Z (Low)
INTPZ8–INTPZ10	P22–P24	○	○				Hi-Z (High)
INTPZ11–INTPZ15	P73–P77	○	○				
INTPZ16–INTPZ21	RP00–RP05	○	○				
INTPZ22	P35	○	○				Hi-Z (Low)
INTPZ23	P36	○	○				Hi-Z (High)
INTPZ24	P37	○	○				Hi-Z (Low)
INTPZ25–INTPZ28	RP24–RP27	○	○				Hi-Z (High)
INTPZ29	P41	○	○				

2.7 Timer I/O Pins

Function Name	Pin Name	PKG 23□	PKG 17□	I/O	Description	Active	Level during Reset
TINJ0 / TOUTJ0*1	P27	○	○	I/O	Timer TAUJ2 I/O pin	—	Hi-Z (High)
TINJ1 / TOUTJ1*1	P26	○	○				
TINJ2 / TOUTJ2*1	P57	○	○				
TINJ3 / TOUTJ3*1	P52	○	○				
TIND0 / TOUTD0	EXTP0	○	○		Timer TAUD I/O pin		
TIND1 / TOUTD1	EXTP1	○	○				
TIND2 / TOUTD2	EXTP2	○	○				
TIND3 / TOUTD3	EXTP3	○	○				
TIND4 / TOUTD4*1	P27	○	○				
TIND5 / TOUTD5*1	P26	○	○				
TIND6 / TOUTD6*1	P57	○	○				
TIND7 / TOUTD7*1	P52	○	○				
TIND8 / TOUTD8	RP30	○	○				
TIND9 / TOUTD9	RP31	○	○				
TIND10 / TOUTD10	RP32	○	○				
TIND11 / TOUTD11	RP33	○	○				
TIND12 / TOUTD12	RP34	○	○				
TIND13 / TOUTD13	RP35	○	○				
TIND14 / TOUTD14	RP36	○	○				
TIND15 / TOUTD15	RP37	○	○				

Note 1. TINJ0–TINJ3 and TIND4–TIND7, and TOUTJ0–TOUTJ3 and TOUTD4–TOUTD7 are assigned as multiplexed functions of the same port pins. Use the TMISEL register to select the pin functions to be used.
For details on this register, refer to the "R-IN32M4-CL3 User's Manual: Hardware edition".
When the external pin functions such as the interval timer function of the internal clock are not used, both TAUJ2 and TAUD channels can be used at the same time.

2.8 Watchdog Timer Output Pin

Function Name	Pin Name	PKG 23□	PKG 17□	I/O	Description	Active	Level during Reset
WDTOUTZ	P25 / EXTP3	○	○	O	Watchdog timer output pin	Low	Hi-Z (High)

2.9 Serial Interface Pins

Function Name	Pin Name	PKG 23□	PKG 17□	I/O	Description	Active	Level during Reset
TXD0	P21	○	○	O	UART0 serial data output	—	Hi-Z (High)
RXD0	P20	○	○	I	UART0 serial data input		
TXD1	P31	○	○	O	UART1 serial data output		
RXD1	P30	○	○	I	UART1 serial data input		
CSISCK0	P45	○	○	I/O	CSI0 serial clock input/output		
CSISI0	P46	○	○	I	CSI0 serial data input		
CSISO0	P47	○	○	O	CSI0 serial data output		
CSICS00	P42	○	○		CSI0 chip select signal output 0	Low	
CSICS01	P43	○	○		CSI0 chip select signal output 1		
CSISCK1	P35	○	○	I/O	CSI1 serial clock input/output	—	Hi-Z (Low)
CSISI1	P36	○	○	I	CSI1 serial data input		Hi-Z (High)
CSISO1	P37	○	○	O	CSI1 serial data output		Hi-Z (Low)
CSICS10	P70	○	○		CSI1 chip select signal output 0	Low	Hi-Z (High)
CSICS11	P71	○	○		CSI1 chip select signal output 1		
SCL0*1	P60	○	○	I/O	I^2C0 serial clock	—	
SDA0*1	P61	○	○		I^2C0 serial data		
SCL1*1	RP00	○	○		I^2C1 serial clock		
SDA1*1	RP01	○	○		I^2C1 serial data		
CRXD0	P53	○	×	I	CAN0 receive data input (5 V tolerant)		
CTXD0	P54	○	×	O	CAN0 transmit data output (5 V tolerant)		
CRXD1	P55	○	×	I	CAN1 receive data input (5 V tolerant)		
CTXD1	P56	○	×	O	CAN1 transmit data output (5 V tolerant)		

Note 1. The SCLn and SDAn pins (n = 0, 1) are open-drain outputs.
For details, refer to the "R-IN32M4-CL3 User's Manual: Hardware edition".

2.10 CC-Link IE Pins

These pins are used for CC-Link IE Field and CC-Link IE TSN.

Function Name	Pin Name	PKG 23□	PKG 17□	I/O	Description	Active	Level during Reset
CCI_RUNLEDZ	P00	○	○	O	RUN status output	Low	Hi-Z (High)
CCI_DLINKLEDZ	P02	○	○		Cyclic communication status output		
CCI_ERRLEDZ	P03	○	○		Field network error status output		
CCI_LERR1LEDZ	P04	○	○		Link error status output 1		
CCI_LERR2LEDZ	P05	○	○		Link error status output 2		
CCI_SDLEDZ	P06	○	×		Transmission status output		
	EXTP12	×	○				
CCI_RDLEDZ	P07	○	×		Port reception status output		
	EXTP13	×	○				
CCI_NMIZ	P52	○	○		Output NMI interrupt to MCU		
CCI_WDTIZ	P12	○	×	I	Input from external WDT		
	EXTP11	×	○				
CCI_INTZ	P53	○	×	O	Output interrupt to MCU		
	EXTP10	×	○				
CCI_CLK2_097M	—	○	○	I	2.097152 MHz clock (crystal oscillator)	—	—
CLK2MSEL*1	—	○	○		CC-Link IE Field clock selection signal input 0: 2.097152 MHz (CCI_CLK2_097M) 1: 2 MHz (PLL divided clock)		

Note 1. For details, refer to the "R-IN32M4-CL3 User's Manual: Hardware edition".

2.11 System Pins

Function Name	Pin Name	PKG 23□	PKG 17□	I/O	Description	Active	Level during Reset
XT1	—	○	○	O	Clock input pin	—	—
XT2	—	○	○	I	When using an oscillator (OSCTH = 1): XT1 is connected to GND and XT2 is connected to the oscillator. When using a Resonator (OSCTH = 0): XT1 and XT2 are connected to the resonator.		
RESETZ	—	○	○		Reset input	Low	
PONRZ	—	○	○		Power-on reset input		
HOTRESETZ	—	○	○		Hot reset input		
OSCTH	—	○	○		External clock input mode setting 0: Resonator connection mode 1: External clock input mode	High	
JTAGSEL	—	○	○		JTAG pin operating mode setting 0: Cortex-M4 JTAG mode 1: B-SCAN JTAG mode	—	
RSTOUTZ	—	○	○	O	External reset output	Low	Low
PLL_VDD	—	○	○	—	PLL power supply (1.15 V)	—	—
PLL_GND	—	○	○		PLL GND		
VDD33	—	○	○		I/O power supply (3.3 V)		
VDD11	—	○	○		Internal power supply (1.15 V)		
GND	—	○	○		Power supply ground voltage (GND)		
GND/OPEN	—	○	×		Power supply ground voltage (GND) or open		

2.12 Trace Pins

Function Name	Pin Name	PKG 23□	PKG 17□	I/O	Description	Active	Level during Reset
TRACECLK	—	○	○	O	Trace port clock output	—	Clock output
TRACEDATA3*1	—	○	○		Trace port data output		Hi-Z (High)
TRACEDATA2*1	—	○	○				
TRACEDATA1*1	—	○	○				
TRACEDATA0*1	—	○	○				

Note 1. These pins are used as an input port in the initial state. The pins are switched to an output port after the reset state is released (the RSTOUTZ pin is switched from Low to High) and 150 to 170 ns are passed.

2.13 CPU Power Control Pin

Function Name	Pin Name	PKG 23□	PKG 17□	I/O	Description	Active	Level during Reset
SLEEPING	P72	○	○	O	CPU core sleep mode output	High	Hi-Z (High)

2.14 Test Pins

Function Name	Pin Name	PKG 23□	PKG 17□	I/O	Description	Active	Level during Reset
TMODE0–TMODE2	—	○	○	I	Renesas dedicated test pins	—	—
TEST3		○	×				
TEST4, TEST5		○	○	I/O			
TEST6		○	○	I			
TEST7		○	○				
TMS		○	○	I/O	Mode select signal		
TDI		○	○	I	Serial data input		
TDO		○	○	O	Serial data output		
TRSTZ		○	○	I	Reset signal	Low	
TCK		○	○		Clock signal (JTAG clock)	—	

2.15 Operating Mode Setting Pins

Function Name	Pin Name	PKG 23□	PKG 17□	I/O	Description	Active	Level during Reset
BOOT1–BOOT0	—	○	○	I	Boot mode selection 00: External memory boot 01: External serial flash ROM boot 10: External MCU boot 11: Instruction RAM boot (only available for debugging)	—	—
MEMIFSEL	—	○	○		External memory interface selection 0: Slave memory interface 1: External MCU interface		
MEMCSEL	—	○	○		Internal memory controller selection 0: Asynchronous SRAM controller 1: Synchronous burst access memory controller		
BUS32EN	—	○	○		External memory interface bus width selection 0: 16-bit bus 1: 32-bit bus		
HIFSYNC	—	○	○		External MCU interface operating mode selection 0: Asynchronous SRAM interface 1: Synchronous SRAM interface		
HWRZSEL	—	○	○		External MCU interface HWRZ/HBENZ selection 0: Used as HBENZ 1: Used as HWRZ		
ADMUXMODE	—	○	○		Multiplexing of address and data lines 0: Separated address and data lines 1: Multiplexed address and data lines		

The following table lists the combinations of available operating mode setting pins for this product.

Boot mode	External memory boot				External MCU boot				External serial flash ROM boot							
External memory interface	Slave memory interface				External MCU interface				Slave memory interface				External MCU interface			
Memory controller type	Asynchronous		Synchronous		Asynchronous		Synchronous		Asynchronous		Synchronous		Asynchronous		Synchronous	
External bus width	16-bit	32-bit	16-bit	32-bit	16-bit	32-bit	16-bit	32-bit	16-bit	32-bit	16-bit	32-bit	16-bit	32-bit	16-bit	32-bit
BOOT1–0	00	00	00	00	10	10	10	10	01	01	01	01	01	01	01	01
MEMIFSEL	0	0	0	0	1	1	1	1	0	0	0	0	1	1	1	1
MEMCSEL	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1	1
BUS32EN	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1
HIFSYNC	0	0	0	0	*1	*1	1	1	0	0	0	0	*1	*1	1	1
HWRZSEL	0	0	0	0	*2	*2	0	0	0	0	0	0	*2	*2	0	0
ADMUXMODE	0	0	*3	*3	0	0	*3	*3	0	0	*3	*3	0	0	*3	*3

Note. Any combination of operating mode setting pins other than above is prohibited.

Note 1. The mode of the external MCU interface is selectable by the level on the HIFSYNC pin.
HIFSYNC = 0: Asynchronous SRAM supported MCU connection mode
HIFSYNC = 1: Synchronous SRAM supported MCU connection mode
For details, refer to the "R-IN32M4-CL3 User's Manual: Hardware edition".

2. The external MCU interface HWRZ or HBENZ is selectable by the level on the HWRZSEL pin.
For details, refer to the "R-IN32M4-CL3 User's Manual: Hardware edition".

3. Multiplexing of address and data lines is selectable by the level on the ADMUXMODE pin.
For details, refer to the "R-IN32M4-CL3 User's Manual: Hardware edition".

Remarks 1. The combination of operating mode setting pins used to select booting for instruction RAM (BOOT1–0 = 11) is the same as that for booting from external memory (BOOT1–0 = 00).

2. Asynchronous: Asynchronous SRAM controller (MEMCSEL = 0)
Synchronous: Synchronous burst access memory controller (MEMCSEL = 1)

3. Electrical Characteristics

3.1 Terminology

Table 3.1 Terms Used in Absolute Maximum Ratings

Parameter	Symbol	Meaning
Power supply voltage	V_{DD}	Indicates the voltage range within which damage or reduced reliability will not result when power is applied to a VDD pin.
Input voltage	V_I	Indicates the voltage range within which damage or reduced reliability will not result when power is applied to an input pin.
Output voltage	V_O	Indicates the voltage range within which damage or reduced reliability will not result when power is applied to an output pin.
Output current	I_O	Indicates the absolute tolerance value for DC current to prevent damage or reduced reliability when a current flows out of or into an output pin.
Operating ambient temperature	T_A	Indicates the ambient temperature range for normal logic operations.
Storage temperature	$T_{.Sgt.}$	Indicates the element temperature range within which damage or reduced reliability will not result while no voltage or current is being applied to the device.

Table 3.2 Terms Used in Recommended Operating Range

Parameter	Symbol	Meaning
Power supply voltage	V_{DD}	Indicates the voltage range for normal logic operations that occur when VSS = 0 V.
High-level input voltage	V_{IH}	A voltage, which is applied to the input pins of the R-IN32M4-CL3, indicating that the high level state for normal operation of the input buffer. – If a voltage that is equal to or greater than the minimum value is applied, the input voltage is guaranteed as a high level voltage.
Low-level input voltage	V_{IL}	A voltage, which is applied to the input pins of the R-IN32M4-CL3, indicating that the low level state for normal operation of the input buffer. – If a voltage that is equal to or less than the maximum value is applied, the input voltage is guaranteed as a low level voltage.
Positive trigger voltage	V_P	Indicates the input level at which the output level is inverted when the input to the R-IN32M4-CL3 is changed from the low-level side to the high-level side.
Negative trigger voltage	V_N	Indicates the input level at which the output level is inverted when the input to the R-IN32M4-CL3 is changed from the high-level side to the low-level side.
Hysteresis voltage	V_H	Indicates the differential between the positive trigger voltage and the negative trigger voltage.
Input rising time	t_{ried}, t_{ric}, t_{ris}	Indicates the limit value for the time period when an input voltage applied to R-IN32M4-CL3 rises from 10% to 90%. t_{ried}, t_{ric}, and t_{ris} each indicate the input rising time for the data, clock, and Schmitt buffer.
Input falling time	t_{fid}, t_{fic}, t_{fis}	Indicates the limit value for the time period when an input voltage applied to R-IN32M4-CL3 falls from 90% to 10%. t_{fid}, t_{fic}, and t_{fis} each indicate the input falling time for the data, clock, and Schmitt buffer.

Table 3.3 Terms Used for DC Characteristics

Parameter	Symbol	Meaning
Off-state output current	I_{OZ}	Indicates the current that flows via an output pin when the rated voltage is applied when a tri-state output has high impedance.
Output short circuit current	I_{OS}	Indicates the current that flows when the output pins are shorted to the ground when output is at high level.
Input leakage current	I_{LI}	Indicates the current that flows via an input pin when a voltage is applied to that pin.
Low-level output current	I_{OL}	Indicates the current that flows through the output pin when the rated low-level voltage is outputting.
High-level output current	I_{OH}	Indicates the current that flows from the output pin when the rated high-level voltage is outputting.
Low-level output voltage	V_{OL}	Indicates the output voltage at low level.
High-level output voltage	V_{OH}	Indicates the output voltage at high level.

3.2 Absolute Maximum Ratings

Table 3.4 Absolute Maximum Ratings

Item	Symbol	Conditions		Ratings	Unit
Power supply voltage	V_{DD}	1.15 V power supply		−0.3 to +1.265	V
		2.5 V power supply		−0.3 to +2.75	V
		3.3 V power supply		−0.3 to +4.20	V
I/O voltage	V_I /V_O	3.3 V buffer	V_I /V_O < V_{DD} + 0.3 V	−0.3 to +4.20	V
		Gigabit Ethernet PHY MDI (Px_DyP/Px_DyN) x = 0, 1, y = 0 to 3		−0.3 to +2.75	V
	V_I	5 V-tolerant buffer		−0.3 to +5.80	V
	V_O			−0.3 to +4.20	V
Output current (3.3 V buffer)	I_O	8mA type		16.0	mA
		10mA type		22.3	mA
		12mA type		27.6	mA
Output current (5 V-tolerant buffer)	I_O	4mA type (5 V-tolerant buffer)		10.2	mA
Operating ambient temperature	T_A	—		−40 to +85	°C
Storage temperature	$T_{Sgt.}$	—		−55 to +125	°C
Junction temperature	T_j	—		−40 to +125	°C

Note. Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.

Remark. Be sure to apply voltage to the I/O pins only after the supply voltage has been fixed.

3.3 Recommended Operating Conditions

Table 3.5 Recommended Operating Conditions

Item	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Power supply voltage	V_{DD}	1.15 V power supply	1.09	1.15	1.21	V
		2.5 V power supply	2.375	2.5	2.625	V
		3.3 V power supply	3.135	3.3	3.465	V
Negative trigger voltage	V_N	3.3 V buffer	0.8	—	1.8	V
		5 V-tolerant buffer	0.8	—	1.8	V
Positive trigger voltage	V_P	3.3 V buffer	1.1	—	2.4	V
		5 V-tolerant buffer	1.1	—	2.1	V
Hysteresis voltage	V_H	3.3 V buffer	0.15	—	1.1	V
		5 V-tolerant buffer	0.15	—	1.1	V
Low-level input voltage	V_{IL}	3.3 V buffer	−0.3	—	0.8	V
		3.3 V OSC buffer	−0.3	—	0.8	V
		5 V-tolerant buffer	−0.3	—	0.8	V
High-level input voltage	V_{IH}	3.3 V buffer	2.2	—	V_{DD} + 0.3	V
		3.3 V OSC buffer	2.4	—	V_{DD} + 0.3	V
		5 V-tolerant buffer	2.2	—	5.8	V
Input rising/falling time	t_{ried}	—	0	—	200	ns
	t_{fid}	—	0	—	200	ns
Input rising/falling time (clock)	t_{ric}	—	0	—	4	ns
	t_{fic}	—	0	—	4	ns
Input rising/falling time (Schmitt input)	t_{ris}	—	0	—	1	ms
	t_{fis}	—	0	—	1	ms
Operating ambient temperature	T_A	—	−40	—	85	°C

3.4 DC Characteristics

Table 3.6 DC Characteristics (V_{DD} = 3.3 ± 0.165 V, T_A = −40 to +85°C) (1/2)

Item	Symbol	Conditions			MIN.	TYP.	MAX.	Unit
Operating current consumption	I_{DD}	V_I = V_{DD} or GND	Without 2.5-V built-in Regulator	VDD11, VDD11A	—	325	515	mA
				VDD25A	—	280	320	
				VDD33*2	—	28	—	mA
			With 2.5-V built-in Regulator	VDD11, VDD11A	—	325	515	mA
				VDD25A	—	—	—	
				VDD33*2	—	28	—	mA
				VDDREG_33, AVDDREG_33	—	248	289	mA
Off-state current	I_{OZ}	V_I = V_{DD} or GND	3.3 V output		—	—	±10	µA
		V_I = GND	5 V-tolerant buffer		—	—	−10	µA
		V_I ≤ 5.8 V			—	—	+10	µA
Output short circuit current*1	I_{OS}	V_O = GND	—		—	—	−250	mA
Input leakage current (3.3 V buffer)	I_I	V_I = V_{DD} or GND	Normal input		—	—	±10	µA
		V_I = GND	With pull-up resistor (130 kΩ)		−6.7	—	−195	µA
		V_I = V_{DD}	With pull-down resistor (160 kΩ)		6.7	—	195	µA
Input leakage current (5 V-tolerant buffer)	I_I	V_I = GND	With pull-up resistor (130 kΩ)		−6.7	—	−195	µA

Note 1. The output short circuit time is no more than one second and is only for one pin.

2. The operating current of I/O differs depending on the conditions (for example, loads, waveform distortion, and toggle frequency). Measure actual current under the mounting environment.

Remark. The (+) and (–) signs in the table indicate the current direction. Current flowing to the device is indicated by (+) and current flowing out is indicated by (–).

Table 3.7 DC Characteristics (VDD = 3.3 ± 0.165 V, TA = −40 to +85°C) (2/2)

Item	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Low-level output current (3.3 V buffer)	I_{OL}	V_{OL} = 0.4 V	8 mA type	8.0	—	—	mA
			10 mA type	10.0	—	—	mA
			12 mA type	12.0	—	—	mA
Low-level output current (5 V-tolerant buffer)	I_{OL}	V_{OL} = 0.4 V	4 mA type	4.0	—	—	mA
High-level output current (3.3 V buffer)	I_{OH}	$V_{OH} = V_{DD} - 0.4$ V	8 mA type	−8.0	—	—	mA
			10 mA type	−10.0	—	—	mA
			12 mA type	−12.0	—	—	mA
High-level output current (5 V-tolerant buffer)	I_{OH}	$V_{OH} = V_{DD} - 0.4$ V	4 mA type	−4.0	—	—	mA
Low-level output voltage	V_{OL}	I_{OL} = 0 mA	3.3 V buffer	—	—	0.1	V
			5 V-tolerant buffer	—	—	0.1	V
High-level output voltage	V_{OH}	I_{OL} = 0 mA	3.3 V buffer	$V_{DD} - 0.1$ V	—	—	V
			5 V-tolerant buffer	$V_{DD} - 0.1$ V	—	—	V

Table 3.8 DC Characteristics (2.5-V built-in Regulator: V_{DD} = 3.3 ± 0.165 V, T_A = −40 to +85°C)

Item	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Output voltage	V_{DD}	REG_OUT pin*	2.5 − 3%	—	2.5 + 3%	V
Output current	I_O		—	—	400	mA
Conversion efficiency	—	—	—	80	—	%

Note. The power supply of 2.5 V via the REG_OUT pin is dedicated to the VDD25A. The pin is not available for 2.5 V power supply to other devices.

3.5 Pull-Up/Pull-Down Resistor Values

Table 3.9 Pull-Up/Pull-Down Resistor Values (V_{DD} = 3.3 ± 0.165 V, T_A = −40 to +85°C)

Item	Library Specification	MIN.	TYP.	MAX.	Unit
Pull-up resistor (3.3 V buffer)	130 kΩ	18	130	450	kΩ
Pull-down resistor (3.3 V buffer)	160 kΩ	18	160	450	kΩ
Pull-up resistor (5 V-tolerant buffer)	130 kΩ	18	130	450	kΩ

3.6 Pin Capacitance

Table 3.10 Pin Capacitance

Item	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Input buffer	C_B	XT2 pin	—	—	7.0	pF
		Other than XT2 pin	—	—	10.0	pF
Output buffer		—	—	—	10.0	pF
I/O buffer		—	—	—	10.0	pF

3.7 Power-On/Off Sequence

Table 3.11 lists external power supplies to R-IN32M4-CL3. Figure 3.1 and Figure 3.3 show the power-on/off sequence. There is no particular rule for the power-on sequence. We recommend supplying external power voltage VDD11 first and then supplying external power voltage VDD33. On the other hand, when turning off the power, disconnect VDD33, then VDD11.

If VDD33 is supplied first, note that the I/O modes of the I/O buffers are not fixed and outputs become undefined over the period between VDD33 and VDD11 rising to their thresholds.
3.3 V must be applied to the input pins only after the power supply voltages have been applied.

Table 3.11 External Power Supplies

External power supply	Voltage [V]	External pin name
VDD33	3.3 ± 0.165*	VDD33 VDDREG_33 AVDDREG_33
VDD25	2.5 ± 0.125*	VDD25A
VDD11	1.15 ± 0.06*	VDD11 VDD11A PLL_VDD

Note. Ripple incorporated value. As a target value, set the DC component to within ±3% and the ripple component to within ±2%.

3.7.1 Power-On/Off Sequence without 2.5-V built-in Regulator

(1) Supplying Power Voltages

Supply power voltages so that the following two conditions are both satisfied.

1) The period from when VDD33, VDD25, or VDD11 reaches 10% VDD to when all of them reach 90% VDD or higher is within 100 ms.
2) The period from when VDD33, VDD25, or VDD11 reaches 95% VDD to when all of them reach 95% VDD or higher is within 50 ms.

(2) Turning Off Power Voltages

Turn off power voltages so that the following two conditions are both satisfied.

1) The period from when VDD33, VDD25, or VDD11 reaches 90% VDD to when all of them reach 10% VDD or lower is within 100 ms.
2) The period from when VDD33, VDD25, or VDD11 reaches 95% VDD to when all of them reach 95% VDD or lower is within 50 ms.

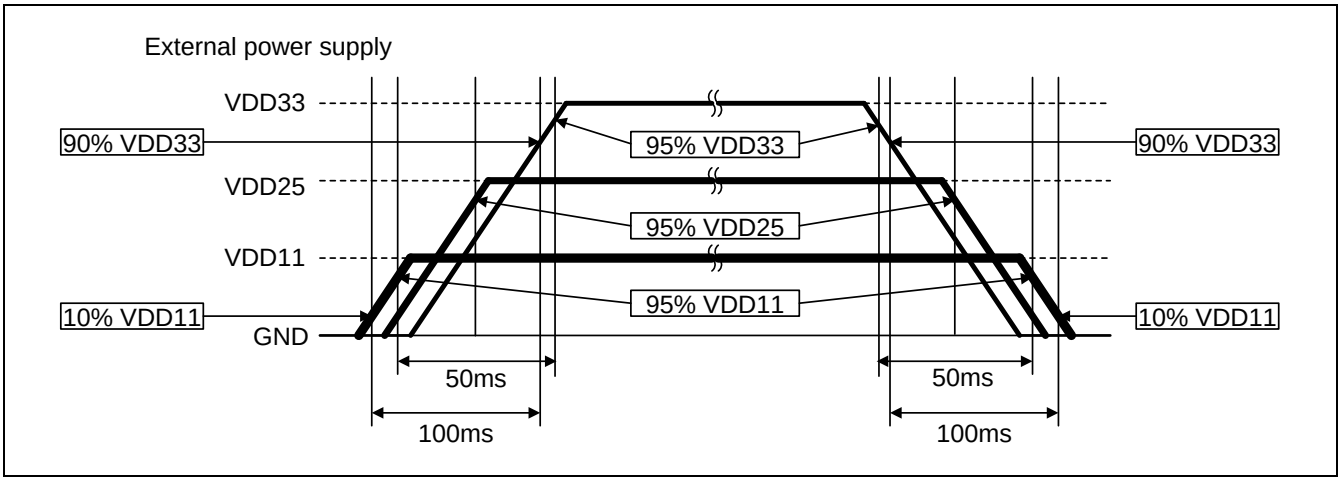


Figure 3.1 Power-On/Off Sequence (without 2.5-V built-in Regulator)

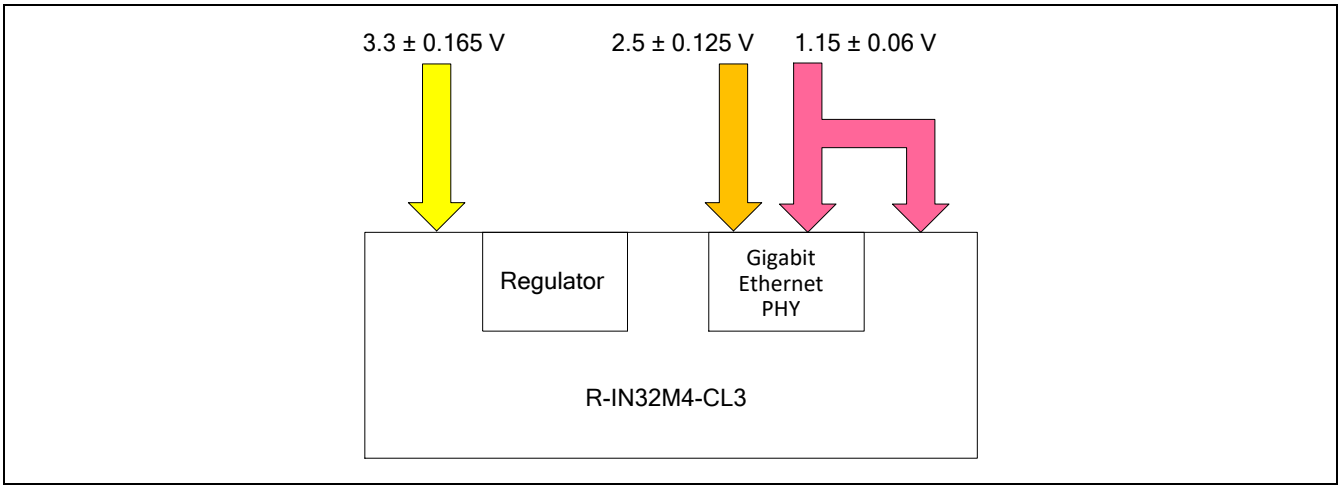


Figure 3.2 Power Supply Path to R-IN32M4-CL3 (without 2.5-V built-in Regulator)

3.7.2 Power-On/Off Sequence with 2.5-V built-in Regulator

(1) Supplying Power Voltages

Supply power voltages so that the following two conditions are both satisfied.

1) The period from when VDD33 or VDD11 reaches 10% VDD to when both of them reach 90% VDD or higher is within 100 ms.
2) The period from when VDD33 or VDD11 reaches 95% VDD to when both of them reach 95% VDD or higher is within 49 ms.

(2) Turning Off Power Voltages

Turn off power voltages so that the following two conditions are both satisfied.

1) The period from when VDD33 or VDD11 reaches 90% VDD to when both of them reach 10% VDD or lower is within 100 ms.
2) The period from when VDD33 or VDD11 reaches 95% VDD to when both of them reach 95% VDD or lower is within 49 ms.

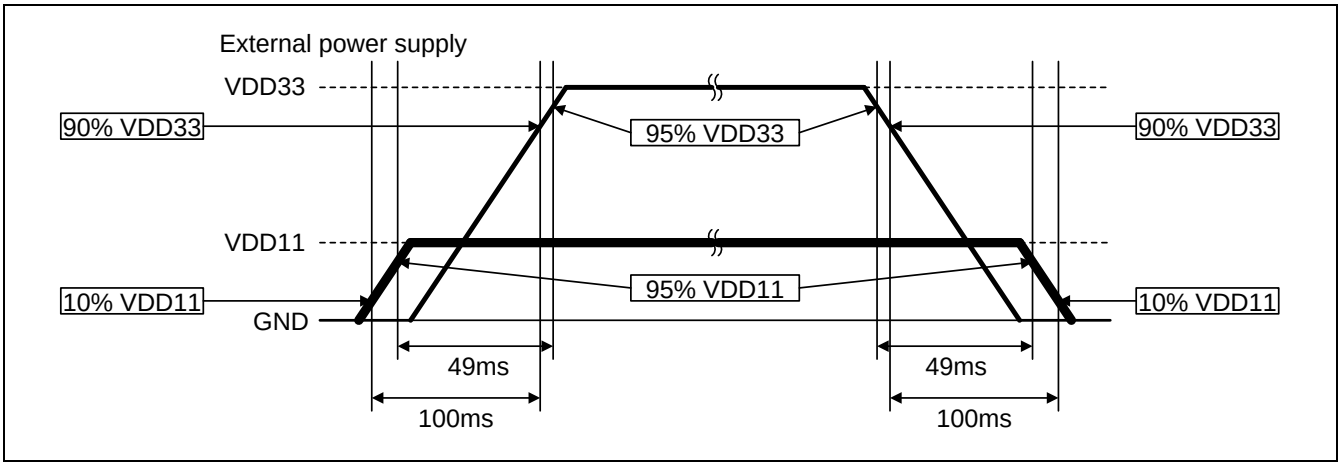


Figure 3.3 Power-On/Off Sequence (with 2.5-V built-in Regulator)

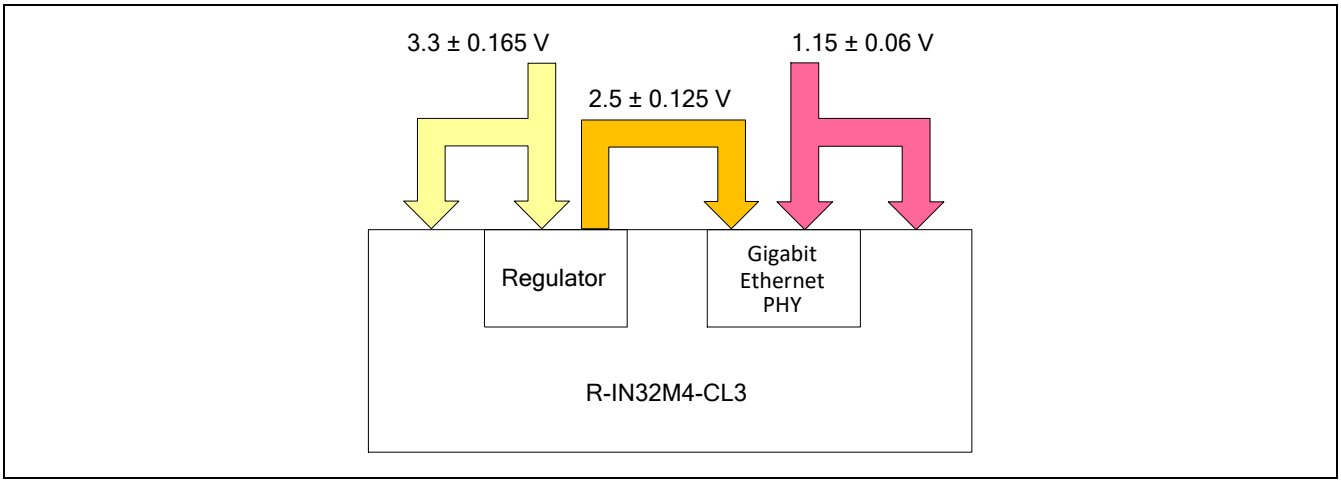


Figure 3.4 Power Supply Path to R-IN32M4-CL3 (with 2.5-V built-in Regulator)

3.8 AC Characteristics

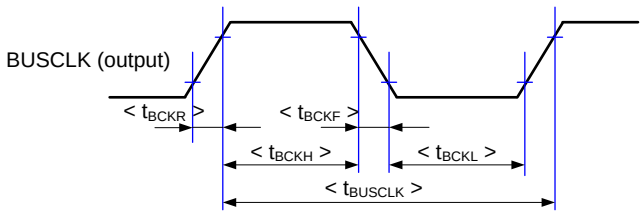
3.8.1 Clock Pins

(1) Input Clocks

Item	Symbol	Conditions	MIN	MAX	Unit
XT1 and XT2 clock frequency	t_{SYSCLK}	When the resonator is used (OSCTH pin = 0)	25 ± 50 ppm, 5 ps–rms		MHz
XT2 clock frequency		When the oscillator is used (OSCTH pin = 1)	25 ± 50 ppm, 5 ps–rms		MHz
XT2 clock duty			45	55	%
CCI_CLK2_097M	$t_{CCLIECLK}$	—	2.097152 ± 100 ppm		MHz
HBUSCLK	$t_{HBUSCLK}$	—	—	50	MHz
CSISCK0, CSISCK1	$t_{CSISSCK}$	Slave mode	—	16.6	MHz
TCK	t_{TCK}	—	—	50	MHz

(2) Output Clocks

Item	Symbol	Conditions	MIN	MAX	Unit
BUSCLK output cycle	t_{BUSCLK}	C_L = 15 pF	10	—	ns
BUSCLK High-level width	t_{BCKH}		0.5 × t_{BUSCLK} − 2.0	0.5 × t_{BUSCLK} + 2.0	ns
BUSCLK Low-level width	t_{BCKL}		0.5 × t_{BUSCLK} − 2.0	0.5 × t_{BUSCLK} + 2.0	ns
BUSCLK rising time	t_{BCKR}		—	1.2	ns
BUSCLK falling time	t_{BCKF}		—	1.2	ns
CSISCK0 and CSISCK1 output frequency	$t_{CSIMSCK}$	Master mode C_L = 15 pF	—	25	MHz
SCL0 and SCL1 output frequency	t_{SCL}	High-speed mode C_L = 30 pF	—	400	kHz
SMSCK output frequency	t_{SMSCK}	C_L = 15 pF	—	50	MHz
TRACECLK output frequency	$t_{TRACECLK}$	C_L = 15 pF	—	50	MHz



Note. For other clocks, refer to the AC characteristics of each interface.

Figure 3.5 Output Clock Timing

3.8.2 Reset Pins

Item	Symbol	Conditions	MIN	MAX	Unit
RESETZ input Low-level width	t_{WRSL}	—	Secure the time (oscillation stabilization time of the external oscillator circuit + 1 µ sec).	—	ns
HOTRESETZ input Low-level width	t_{WHRSL}	—		—	ns
PONRZ input Low-level width	t_{WPRSL}	—		—	ns
PONRZ input timing (for RESETZ ↑)	t_{SKPR}	—	0	—	ns

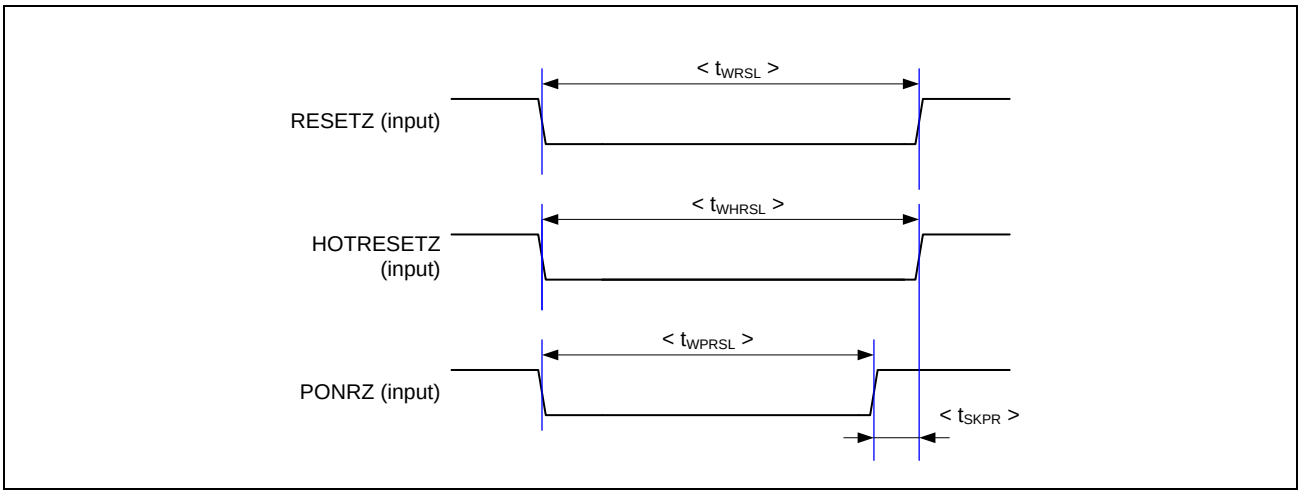


Figure 3.6 Reset Timing

3.8.3 External Memory Interface Pins

(1) How to calculate a delay value due to the external load

For the external memory interface pins of R-IN32M4-CL3, the listed values are for a load of 0 pF, but the actual loads will differ with users. Calculate the timing in accordance with the load conditions of the user. The user must also consider the wiring delay on the board.

Driving Ability	Delay Value per pF (ns)	
	MIN.	MAX.
8 mA	0.024	0.064
12 mA	0.013	0.039

Calculation Example:
When an address pin (8 mA output buffer) has a 30 pF load, the actual delay is as follows.

MIN. 1.0 ns (Minimum delay value for the load of 0 pF) + (0.024 × 30) ns = 1.72 ns
MAX. 7.0 ns (Maximum delay value for the load of 0 pF) + (0.064 × 30) ns = 8.92 ns

(2) Asynchronous SRAM controller access timing

Item	Symbol	MIN	MAX	Unit
Address and CSZ0–CSZ3 output delay time (for BUSCLK ↑)	t_{DKA}	1.0 (1.72)*	7.0 (8.92)*	ns
RDZ output delay time (for BUSCLK ↑)	t_{DKRD}	1.0 (1.72)*	7.0 (8.92)*	ns
WRZ0–WRZ3 (BENZ0–BENZ3) and WRSTBZ output delay time (for BUSCLK ↑)	t_{DKWR}	1.0 (1.72)*	7.0 (8.92)*	ns
BCYSTZ output delay time (for BUSCLK↑)	t_{DKBSL}	1.0 (1.72)*	7.0 (8.92)*	ns
WAITZ input setup time (for BUSCLK↓)	t_{SKW}	4.0	—	ns
WAITZ input hold time (for BUSCLK↓)	t_{HKW}	0	—	ns
Data input setup time (for BUSCLK↑)	t_{SKID}	4.0	—	ns
Data input hold time (for BUSCLK↑)	t_{HKID}	0	—	ns
Data output delay time (for BUSCLK↑)	t_{DKOD}	1.0 (1.72)*	7.0 (8.92)*	ns
Data float delay time (for BUSCLK↑)	t_{HKOD}	1.0 (1.72)*	7.0 (8.92)*	ns

Note. Values in parenthesis are the calculation results for the driving ability of 8 mA and the external load of 30 pF.

(a) Read timing

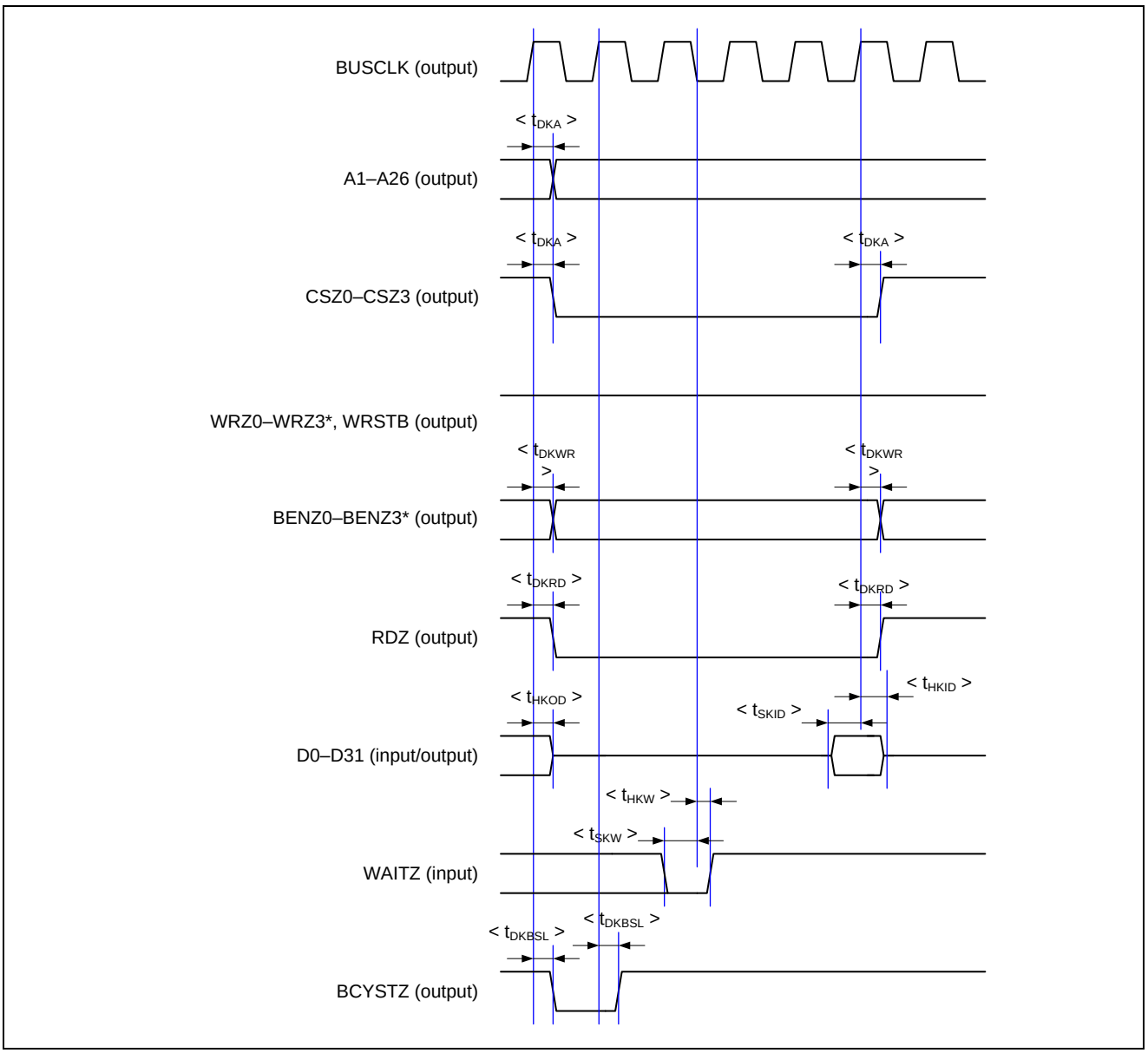


Figure 3.7 Memory Controller Read Timing (Asynchronous Memory)

Note. The WRZ0–WRZ3 pins are multiplexed with the BENZ0–BENZ3 pin functions. The pin names are WRZ0–WRZ3.
The WRZ0–WRZ3 pins are selected by default during a reset. Use the write enable switching register (WREN) to switch the pin functions of these pins.
For register details, refer to the "R-IN32M4-CL3 User's Manual: Hardware edition".

Remark. The above timing is for the case where the settings in the SMCn register for numbers of idle wait cycles, write recovery wait cycles, and address setting wait cycles are 0, and that for data wait cycles is 3.

(b) Write timing

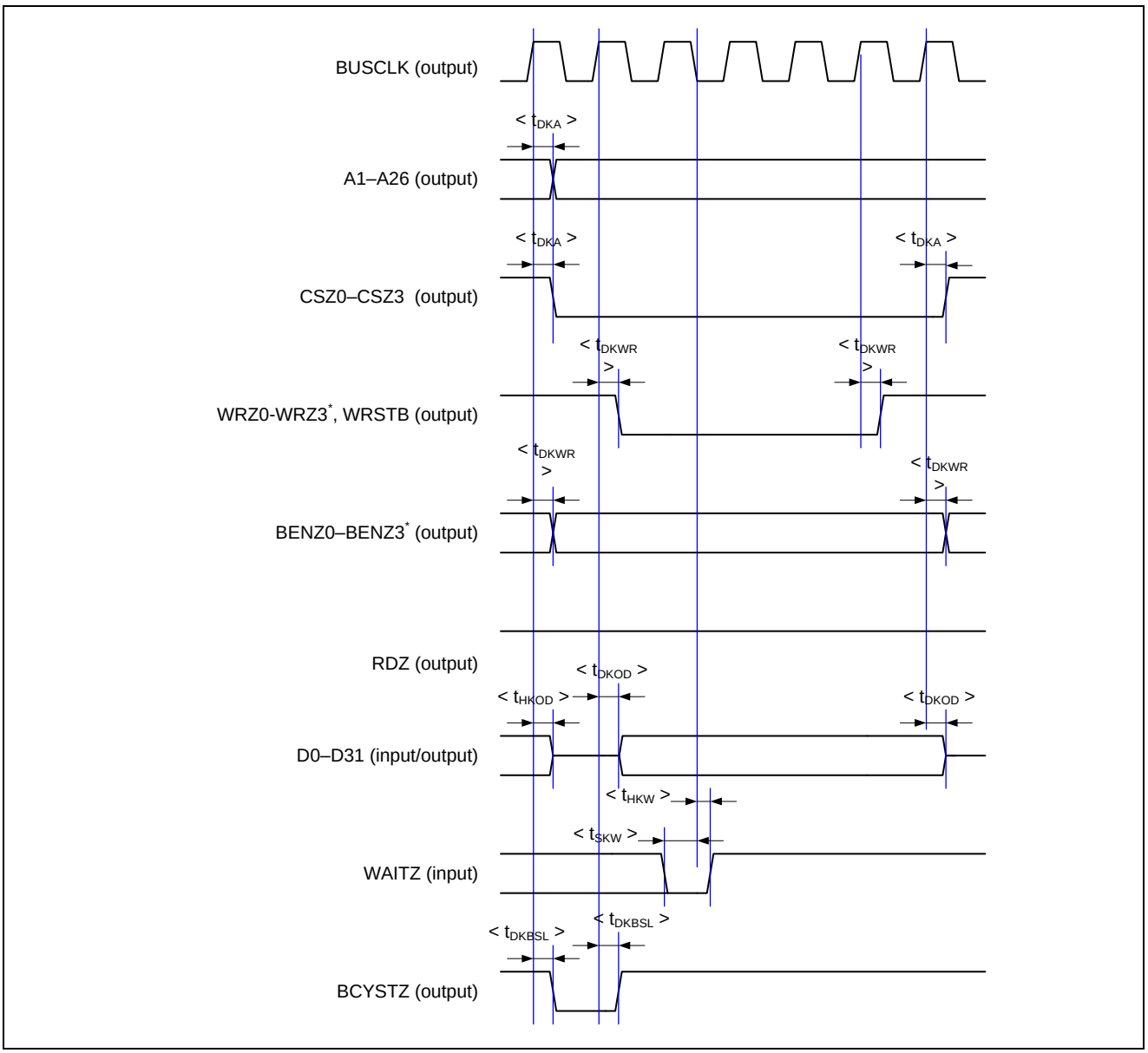


Figure 3.8 Memory Controller Write Timing (Asynchronous Memory)

Note. The WRZ0–WRZ3 pins are multiplexed with the BENZ0–BENZ3 pin functions. The pin names are WRZ0–WRZ3.
The WRZ0–WRZ3 pins are selected by default during a reset. Use the write enable switching register (WREN) to switch the pin functions of these pins.
For register details, refer to the "R-IN32M4-CL3 User's Manual: Hardware edition".

Remark. The above timing is for the case where the settings in the SMCn register for numbers of idle wait cycles, write recovery wait cycles, and address setting wait cycles are 0, and that for data wait cycles is 3.

(3) Synchronous burst access memory controller access timing

Item	Symbol	MIN	MAX	Unit
BUSCLK output frequency	t_{BUSCLK}	—	50	MHz
Address and CSZ0–CSZ3 output delay time	t_{DKA}	1.0 (1.72)*	7.8 (9.72)*	ns
RDZ output delay time	t_{DKRD}	1.0 (1.72)*	7.8 (9.72)*	ns
WRZ0–WRZ3 (BENZ0–BENZ3) and WRSTBZ output delay time	t_{DKWR}	1.0 (1.72)*	7.8 (9.72)*	ns
ADVZ output delay time	t_{DKBSL}	1.0 (1.72)*	7.8 (9.72)*	ns
WAITZ and WAITZ1–WAITZ3 input setup time	t_{SKW}	5.3	—	ns
WAITZ and WAITZ1–WAITZ3 input hold time	t_{HKW}	0	—	ns
Data input setup time	t_{SKID}	5.3	—	ns
Data input hold time	t_{HKID}	0	—	ns
Data output delay time	t_{DKOD}	1.0 (1.72)*	7.8 (9.72)*	ns
Data float delay time	t_{HKOD}	1.0 (1.72)*	7.8 (9.72)*	ns

Note. Values in parenthesis are the calculation results for the driving ability of 8 mA and the external load of 30 pF.

(a) Read timing

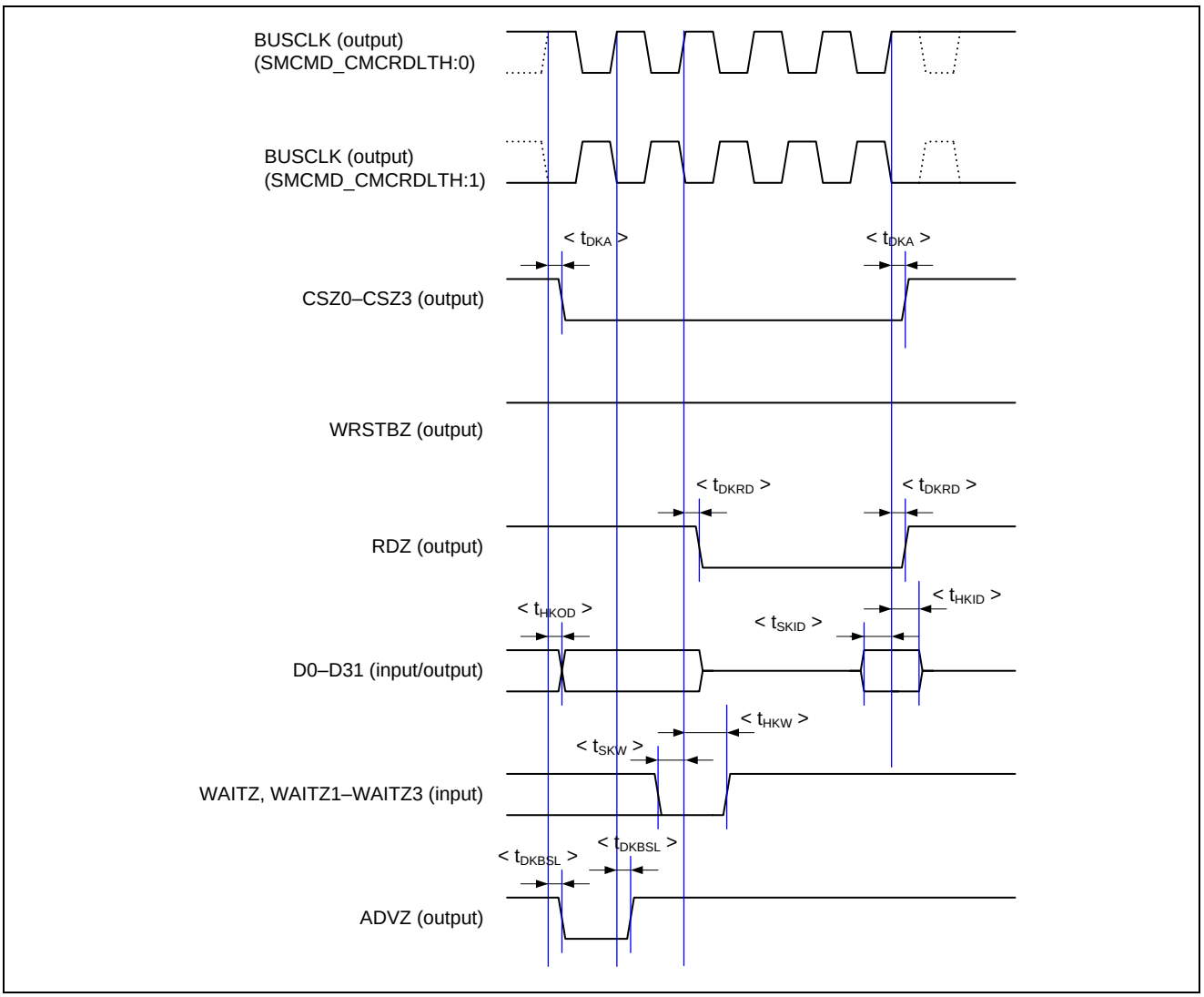


Figure 3.9 Memory Controller Read Timing (Clock Synchronous Memory)

Remark. The above timing is for the case where t_ceoe is 2 and t_rc is 4.

(b) Write timing

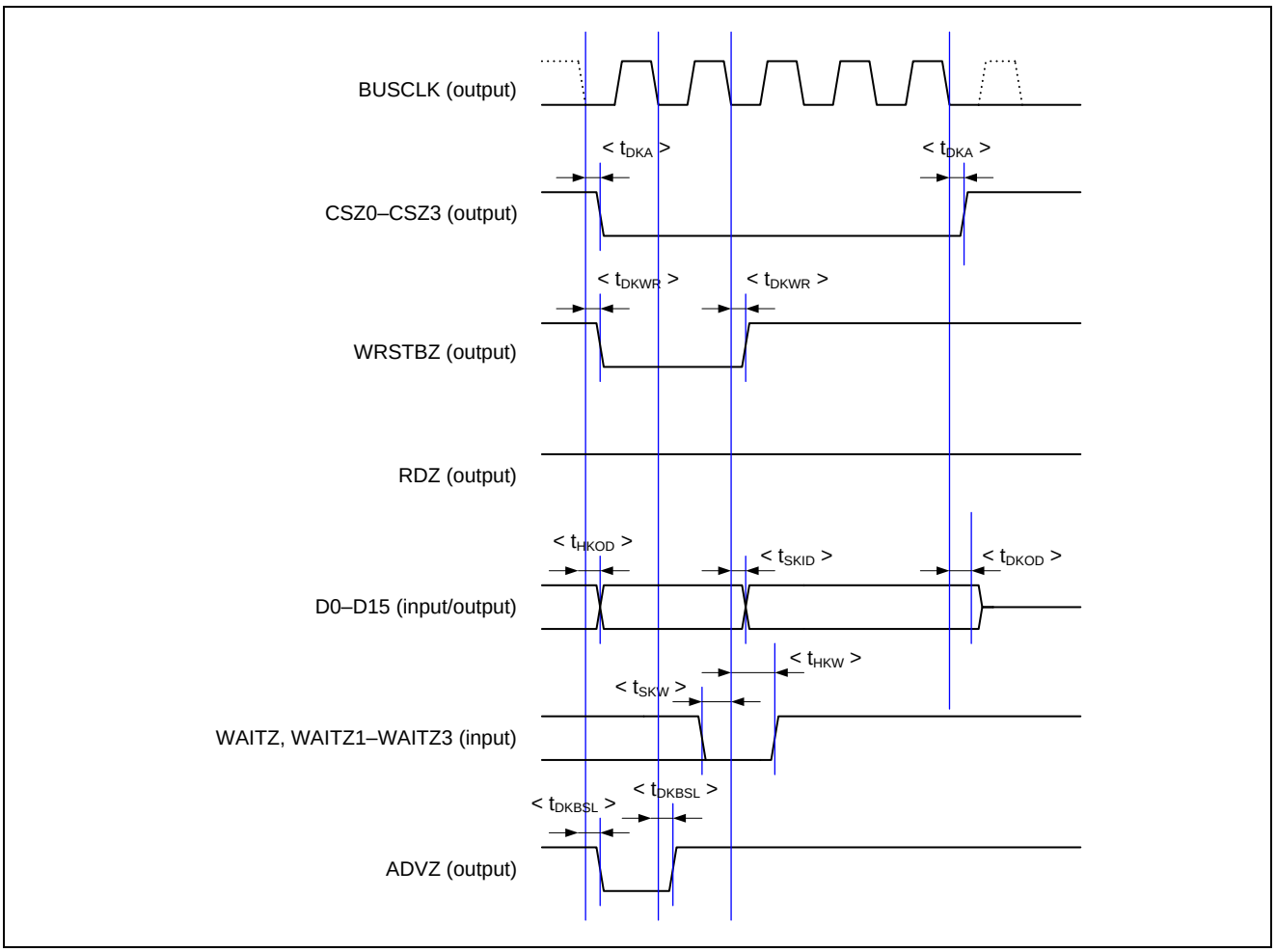


Figure 3.10 Memory Controller Write Timing (Clock Synchronous Memory)

Remark. The above timing is for the case where t_wp is 2 and t_wc is 5.

3.8.4 External MCU Interface Pins

The load condition for the external MCU interface pins: 65 pF (HD pin) and 35 pF (HWAITZ pin).

(1) Synchronous mode

No.	Item	Symbol	MIN	MAX	Unit
1	HBUSCLK High-level width	t_{HBHIGH}	0.5 × $t_{HBUSCLK}$ − 2.1	0.5 × $t_{HBUSCLK}$ + 2.1	ns
2	HBUSCLK Low-level width	t_{HBLOW}	0.5 × $t_{HBUSCLK}$ − 2.1	0.5 × $t_{HBUSCLK}$ + 2.1	ns
3	HBUSCLK input cycle	$t_{HBUSCLK}$	20.0	—	ns
4	Address, HCSZ, HPGCSZ, and HRDZ input setup time (for HBUSCLK ↑)	t_{SKHA}	4.0	—	ns
5	HBENZ0–HBENZ3 (HWRZ0–HWRZ3) and HWRSTBZ input setup time (for HBUSCLK ↑)	t_{SKHWR}	4.0	—	ns
6	Address, HCSZ, HPGCSZ, and HRDZ input hold time (for HBUSCLK ↑)	t_{HKHA}	1.0	—	ns
7	HBENZ0–HBENZ3 (HWRZ0–HWRZ3) and HWRSTBZ input hold time (for HBUSCLK ↑)	t_{HKHWR}	1.0	—	ns
8	HWRZ0–HWRZ3, HWRSTBZ recovery time (High-level width)	t_{WHWR}	35.0	—	ns
9	Data input setup time (for HBUSCLK ↑)	t_{SKIHD}	4.0	—	ns
10	Data input hold time (for HBUSCLK ↑)	t_{HKIHD}	1.0	—	ns
11	HWAITZ output delay time (for HCSZ, HPGCSZ ↓)	t_{DKHD}	2.2	—	ns
12	HWAITZ output delay time (for HWRSTBZ, HWRZ0 to HWRZ3 ↓)	t_{DKHWT}	2.2	—	ns
13	HWAITZ valid data output delay time (for HBUSCLK ↑)	t_{DKHWTV}	2.0	11.0	ns
14	HWAITZ valid data hold time (for HWRSTBZ, HWRZ0–HWRZ3 ↑)	t_{HKHWTV}	4.2	—	ns
15	HWAITZ output hold time (for HWRSTBZ, HWRZ0–HWRZ3 ↑)	t_{HKWTWR}	—	16.8	ns
16	Data and HWAITZ output hold time (for HCSZ, HPGCSZ ↑)	t_{HKWTCS}	—	16.8	ns
17	HRDZ recovery time (High-level width)	t_{WHRD}	35.0	—	ns
18	Data and HWAITZ output delay time (for HRDZ ↓)	t_{DKHDHR}	2.2	—	ns
19	Data fixing time (for HWAITZ ↑)	$t_{SKHDHWT}$	$t_{HBUSCLK}$ − 10.0	—	ns
20	Data and HWAITZ valid data output hold time (for HRDZ ↑)	$t_{HKHWTHR}$	2.2	—	ns
21	Data and HWAITZ output hold time (for HRDZ ↑)	t_{HKOHD}	—	16.8	ns
22	Data and HWAITZ output delay time in on-page access (for addresses)	t_{DKPON}	4.2	15.4	ns
23	Data and HWAITZ output delay time in off-page access (for addresses) (when not crossing a 16-byte boundary)	t_{DKPOFF}	4.2	15.4	ns
	Data and HWAITZ output delay time in off-page access (for addresses) (when crossing a 16-byte boundary)	t_{DKPOFF}	4.2	49.5	ns
24	HWAITZ valid data output delay time (for HCSZ, HPGCSZ ↓)	$t_{DKWTVCS}$	—	15.4	ns

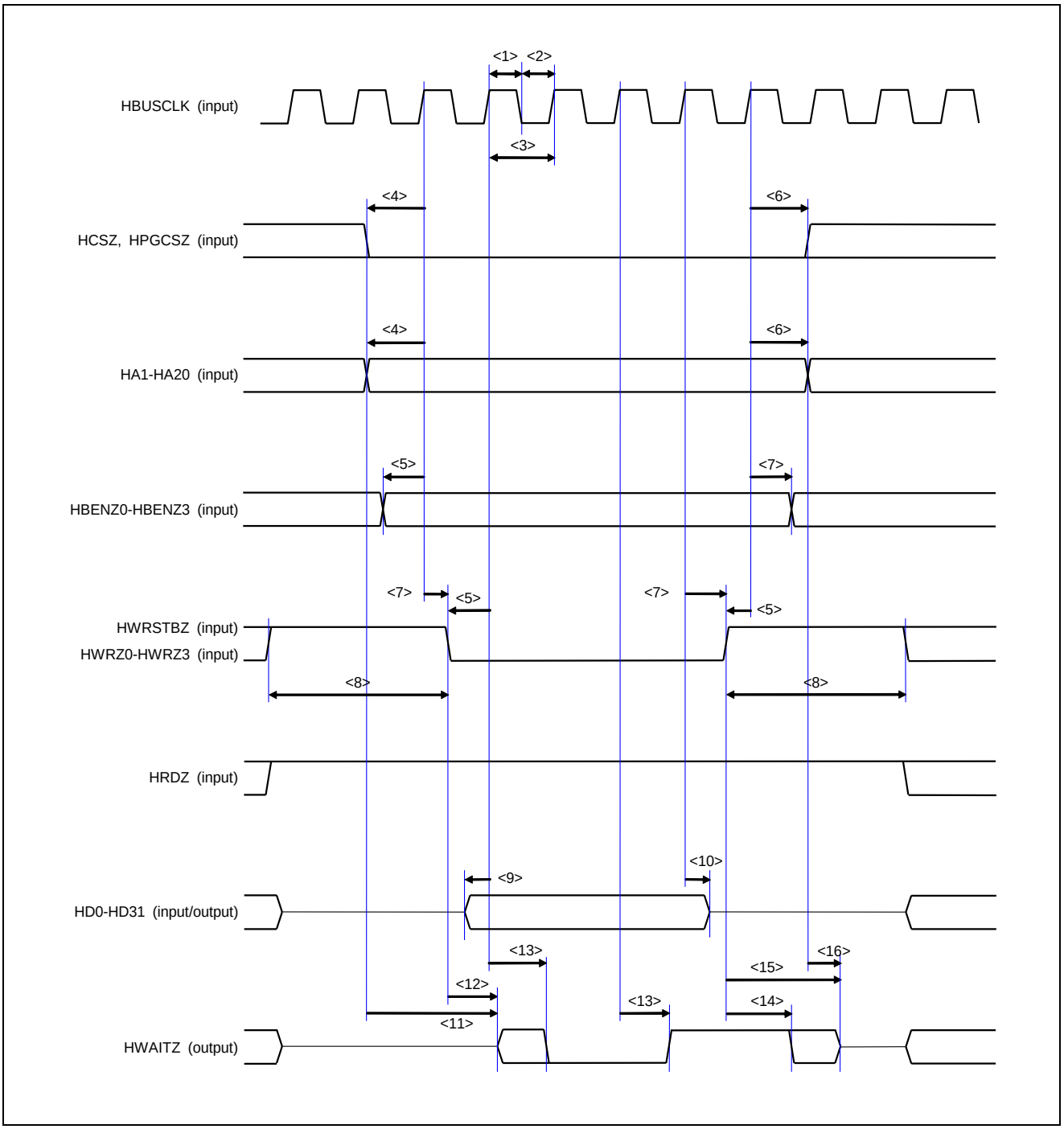


Figure 3.11 External MCU Interface Write Timing (MEMCSEL=L, HIFSYNC=H)

Note. Supply a stable signal to the address, data, and control lines during access.

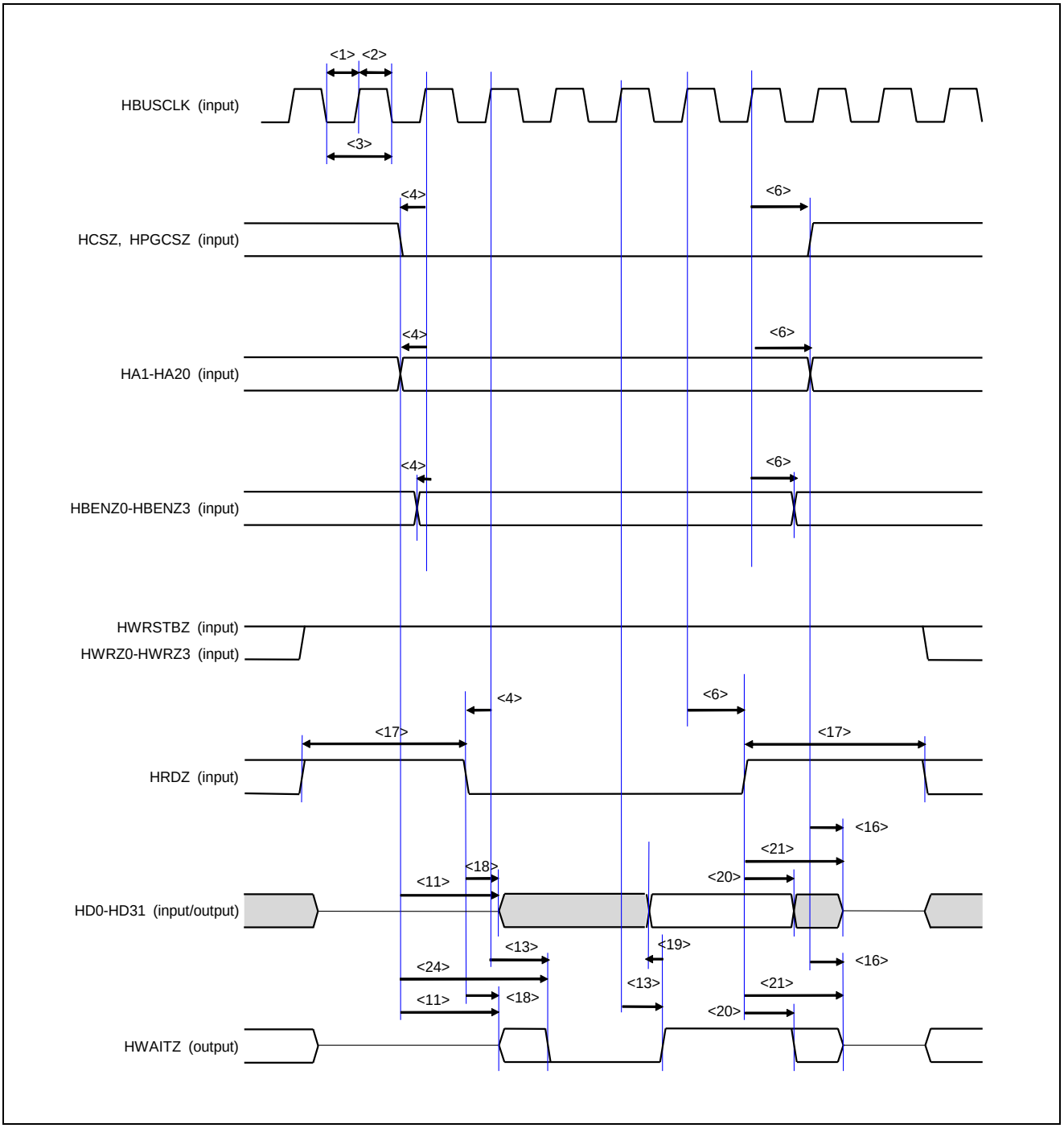


Figure 3.12 External MCU Interface Read Timing (MEMCSEL=L, HIFSYNC=H)

Note. Supply a stable signal to the address, data, and control lines during access.

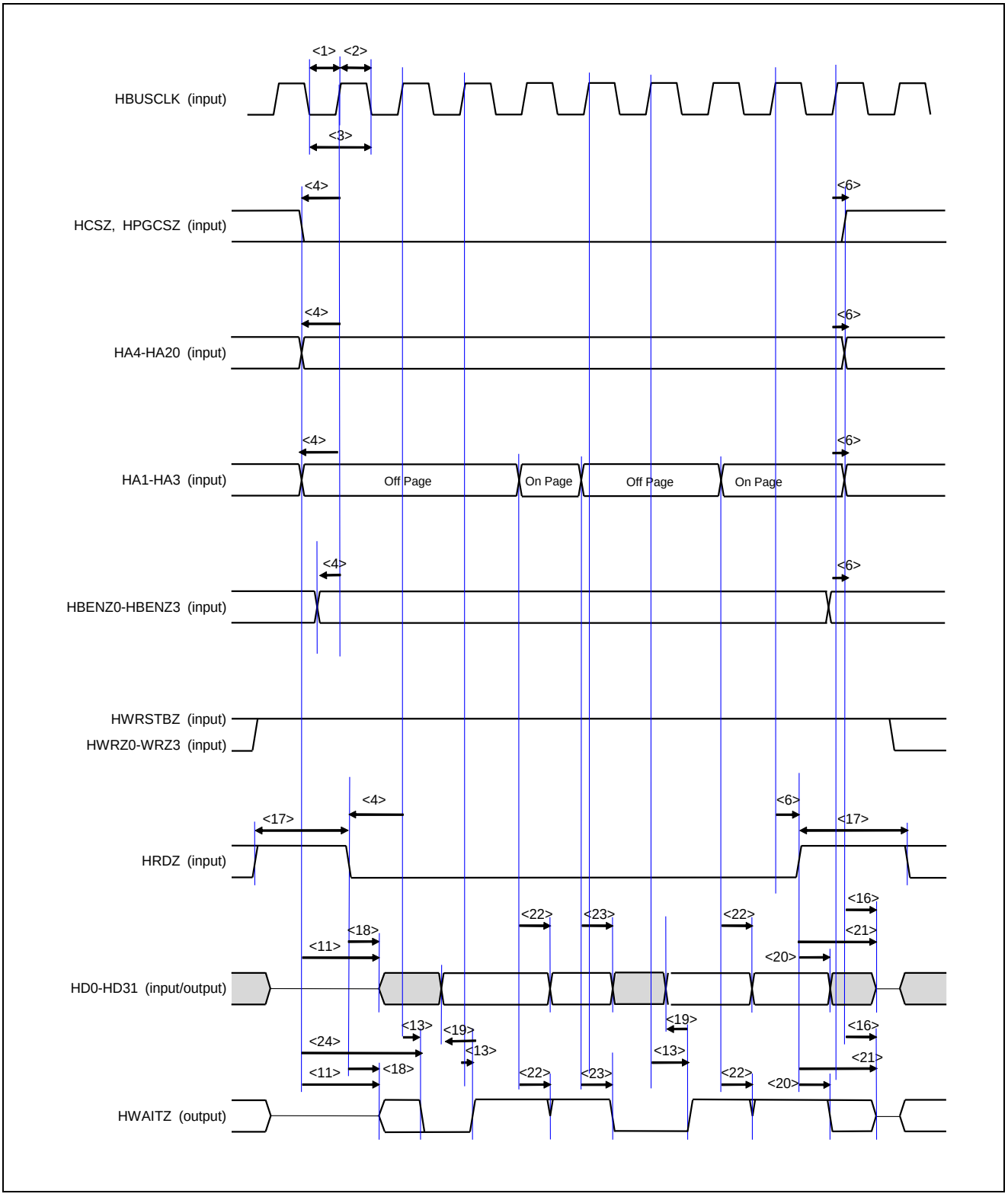


Figure 3.13 External MCU Interface Page Read Timing (MEMCSEL=L, HIFSYNC=H)

Note. Supply a stable signal to the address, data, and control lines during access.

(2) Asynchronous mode

No.	Item	Symbol	MIN	MAX	Unit
1	Address, HCSZ/HPGCSZ, and HBENZ0–HBENZ3 input setup time (for HWRSTBZ, HWRZ0–HWRZ3 ↓)	t_{ADDWRS}	7.0*1 − 10 × n	—	ns
2	HWRZ0–HWRZ3, HWRSTBZ recovery time (High-level width)	t_{WRW}	35.0	—	ns
3	Data input setup time (for HWRSTBZ, HWRZ0–HWRZ3↓)	t_{WRS}	7.0*1 − 10 × n	—	ns
4	Data input hold time (for HWRSTBZ, HWRZ0–HWRZ3↑)	t_{WRH}	7.0	—	ns
5	HWAITZ output delay time (for HCSZ or HPGCSZ↓)	t_{CLZ}	2.2	—	ns
6	HWAITZ output delay time (for HWRSTBZ, HWRZ0–HWRZ3↓)	t_{WAITD}	2.2	—	ns
7	HWAITZ valid data output delay time (for HWRSTBZ, HWRZ0–HWRZ3↓)	$t_{WRWAITF}$	—	15.4	ns
8	HWAITZ valid data output hold time (for HWRSTBZ, HWRZ0–HWRZ3↑)	t_{WAITVH}	4.2	—	ns
9	HWAITZ output hold time (for HWRZ0–3, HWRSTBZ↑)	t_{WAITH}	—	16.8	ns
10	Address and HWAITZ output hold time (for HCSZ, HPGCSZ↑)	t_{CHZ}	—	16.8	ns
11	Address, HCSZ, and HPGCSZ input setup time (for HRDZ↓)	t_{ADDRDS}	6.2*2 − 10 × n	—	ns
12	Address input hold time in page access (for HRDZ↑)	t_{ADDRDH}	7.0	—	ns
13	HRDZ recovery time (High-level width)	t_{RDW}	35.0	—	ns
14	Data and HWAITZ output delay time (for HRDZ↓)	t_{RDLZ}	2.2	—	ns
15	HWAITZ valid data output delay time (for HRDZ↓)	$t_{RDWAITF}$	—	15.4	ns
16	Data fixing time (for HWAITZ↑)	t_{WAITR}	—	−6.2*3 +10 × n	ns
17	Data and HWAITZ valid data output hold time (for HRDZ↑)	t_{DATAOH}	2.2	—	ns
18	Data and HWAITZ output hold time (for HRDZ↑)	t_{RDHZ}	—	16.8	ns
19	Data and HWAITZ output delay time in on-page access (for addresses)	$t_{PAGEOND}$	4.2	15.4	ns
20	Data and HWAITZ output delay time in off-page access (for addresses) (when not crossing a 16-byte boundary)	$t_{PAGEOFD}$	4.2	15.4	ns
	Data and HWAITZ output delay time in off-page access (for addresses) (when crossing a 16-byte boundary)	$t_{PAGEOFD}$	4.2	49.5	ns
21	HWAITZ valid data output delay time (for HCSZ, HPGCSZ↓)	t_{WAITVD}	—	15.4	ns

Note 1. When the value of WRSTD2–WRSTD0 in the HIFBTC register is 000B.
n: Setting of WRSTD2–WRSTD0
2. When the value of RDSTD1–RDSTD0 in the HIFBTC register is 00B.
n: Setting of RDSTD1–RDSTD0
3. When the value of RDDTS1–RDDTS0 in the HIFBTC register is 00B.
n: Setting of RDDTS1–RDDTS0

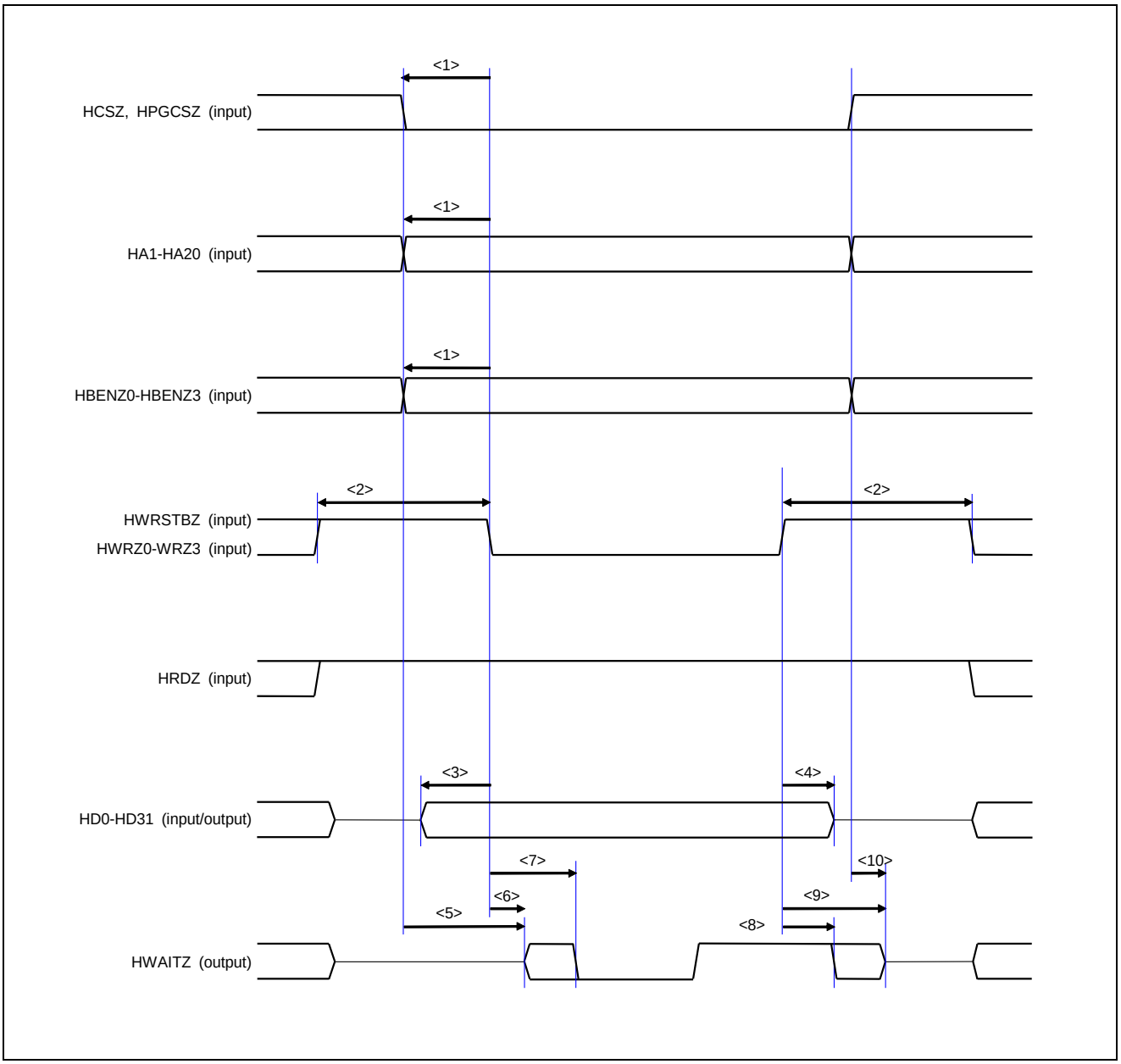


Figure 3.14 External MCU Interface Write Timing (MEMCSEL=L, HIFSYNC=L)

Note. Supply a stable signal to the address, data, and control lines during access.

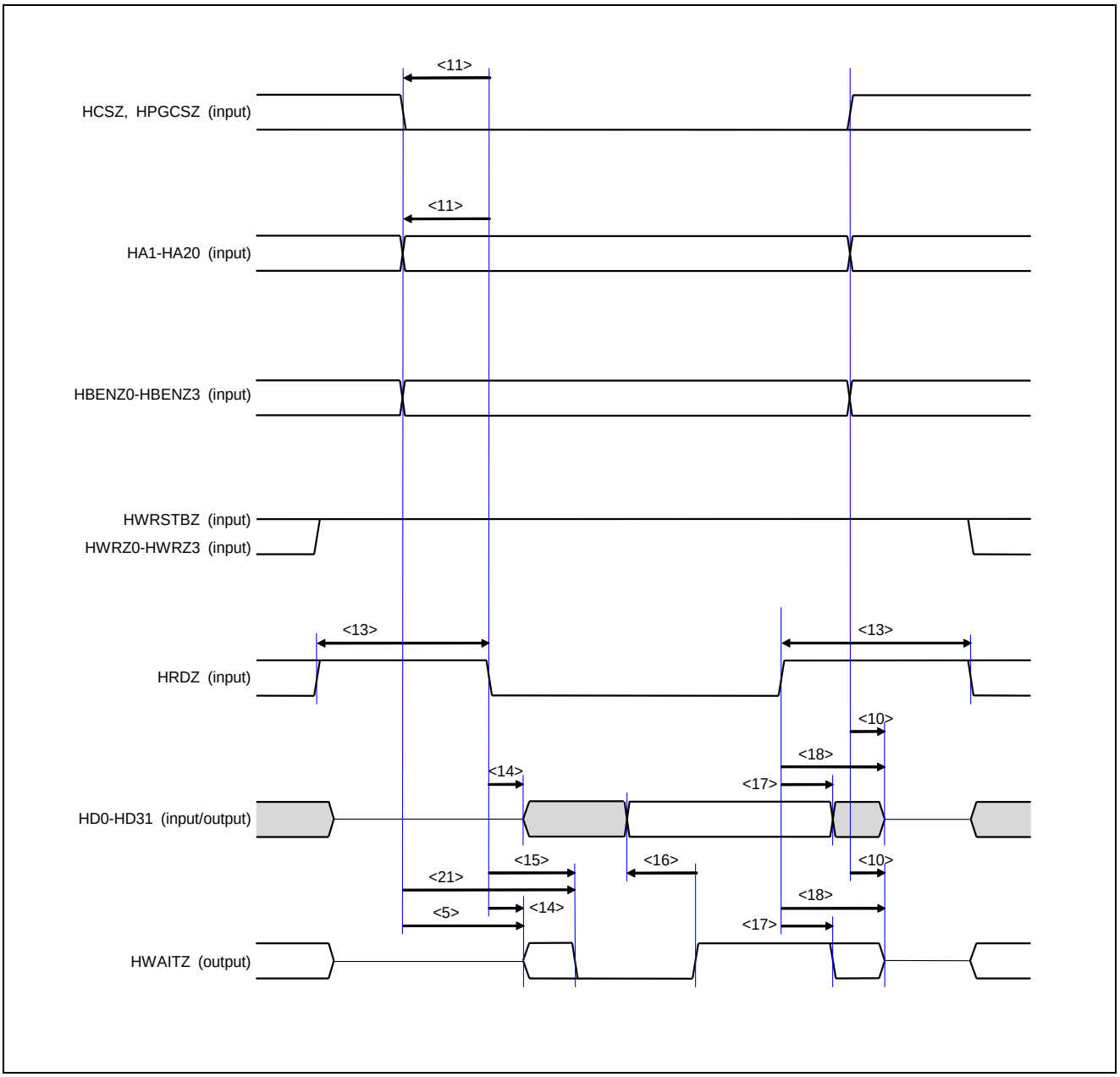


Figure 3.15 External MCU Interface Read Timing (MEMCSEL=L, HIFSYNC=L)

Note. Supply a stable signal to the address, data, and control lines during access.

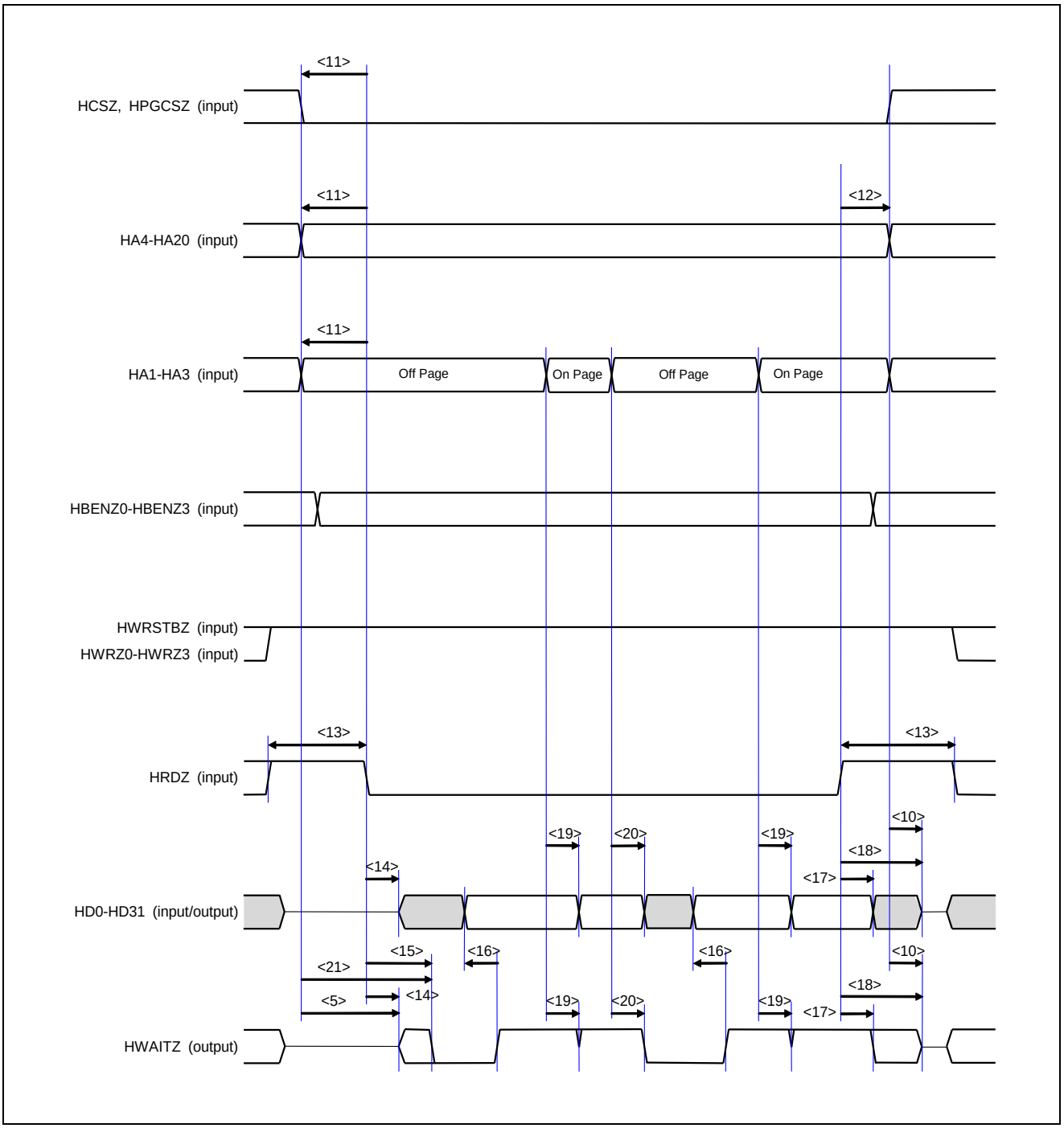


Figure 3.16 External MCU Interface Page Read Timing (MEMCSEL=L, HIFSYNC=L)

Note. Supply a stable signal to the address, data, and control lines during access.

(3) Synchronous SRAM type transfer mode

No.	Item	Symbol	MIN	MAX	Unit
1	HBUSCLK High-level width	t_{HBHIGH}	$0.5 \times t_{HBUSCLK} - 2.1$	$0.5 \times t_{HBUSCLK} + 2.1$	ns
2	HBUSCLK Low-level width	t_{HBLOW}	$0.5 \times t_{HBUSCLK} - 2.1$	$0.5 \times t_{HBUSCLK} + 2.1$	ns
3	HBUSCLK input cycle	$t_{HBUSCLK}$	20	—	ns
4	Address and HCSZ/HPGCSZ input setup time (for HBUSCLK ↑)	t_{SKPHA}	4.0	—	ns
5	Address and HCSZ/HPGCSZ input hold time (for HBUSCLK ↑)	t_{HKPCS}	1.0	—	ns
6	Address and HCSZ/HPGCSZ input setup time (for HBUSCLK ↓)	t_{SKNHA}	4.0	—	ns
7	Address, HCSZ, and HPGCSZ input hold time (for HBUSCLK ↓)	t_{HKNHA}	1.0	—	ns
8	HWRZ0–HWRZ3 input setup time (for HBUSCLK ↑)	t_{SKPHWR}	4.0	—	ns
9	HWRZ0–HWRZ3 input hold time (for HBUSCLK ↑)	t_{HKPHWR}	1.0	—	ns
10	HWRZ0–HWRZ3 input setup time (for HBUSCLK ↓)	t_{SKNHWR}	4.0	—	ns
11	HWRZ0–HWRZ3 input hold time (for HBUSCLK ↓)	t_{HKNHWR}	1.0	—	ns
12	HBCYSTZ, HWRSTBZ input setup time (for HBUSCLK ↑)	$t_{SKPHBCY}$	4.0	—	ns
13	HBCYSTZ, HWRSTBZ input hold time (for HBUSCLK ↑)	$t_{HKPHBCY}$	1.0	—	ns
14	HBCYSTZ, HWRSTBZ input setup time (for HBUSCLK ↓)	$t_{SKNHBCY}$	4.0	—	ns
15	HBCYSTZ, HWRSTBZ input hold time (for HBUSCLK ↓)	$t_{HKNHBCY}$	1.0	—	ns
16	HRDZ input setup time (for HBUSCLK ↑)	t_{SKPHRD}	4.0	—	ns
17	HRDZ input hold time (for HBUSCLK ↑)	t_{HKPHRD}	1.0	—	ns
18	HRDZ input setup time (for HBUSCLK ↓)	t_{SKNHRD}	4.0	—	ns
19	HRDZ input hold time (for HBUSCLK ↓)	t_{HKNHRD}	1.0	—	ns
20	Data input setup time (for HBUSCLK ↑)	t_{SKPHD}	4.0	—	ns
21	Data input hold time (for HBUSCLK ↑)	t_{HKPHD}	1.0	—	ns
22	Data input setup time (for HBUSCLK ↓)	t_{SKNHD}	4.0	—	ns
23	Data input hold time (for HBUSCLK ↓)	t_{HKNHD}	1.0	—	ns
24	Data output delay time (for HRDZ ↓)	t_{DKNHRD}	2.2	—	ns
25	Data output hold time (for HRDZ ↑)	t_{HKPHRD}	—	16.8	ns
26	Data output delay time (for HBUSCLK ↑)	t_{DKPHD}	2.0	10.0	ns
27	Data output delay time (for HBUSCLK ↓)	t_{DKNHD}	2.0	10.0	ns
28	HWAITZ output delay time (for HBUSCLK ↑)	t_{DKPHWT}	2.0	11.0	ns
29	HWAITZ output delay time (for HBUSCLK ↓)	t_{DKNHWT}	2.0	11.0	ns
30	Data output hold time (for HCSZ/HPGCSZ ↑)	t_{HKPHCS}	—	16.8	ns

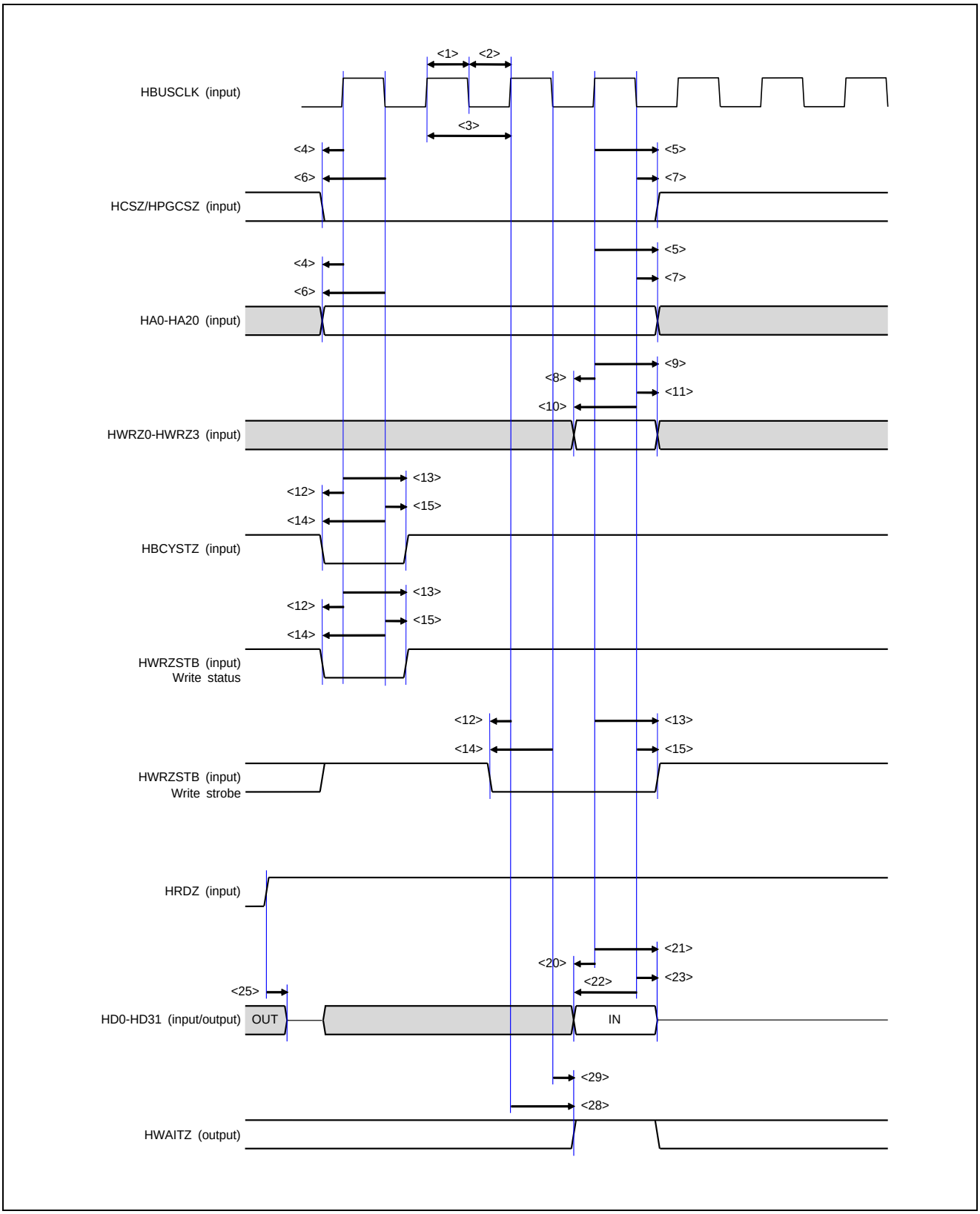


Figure 3.17 External MCU Interface Write Timing (MEMCSEL=H, ADMUXMODE=L)

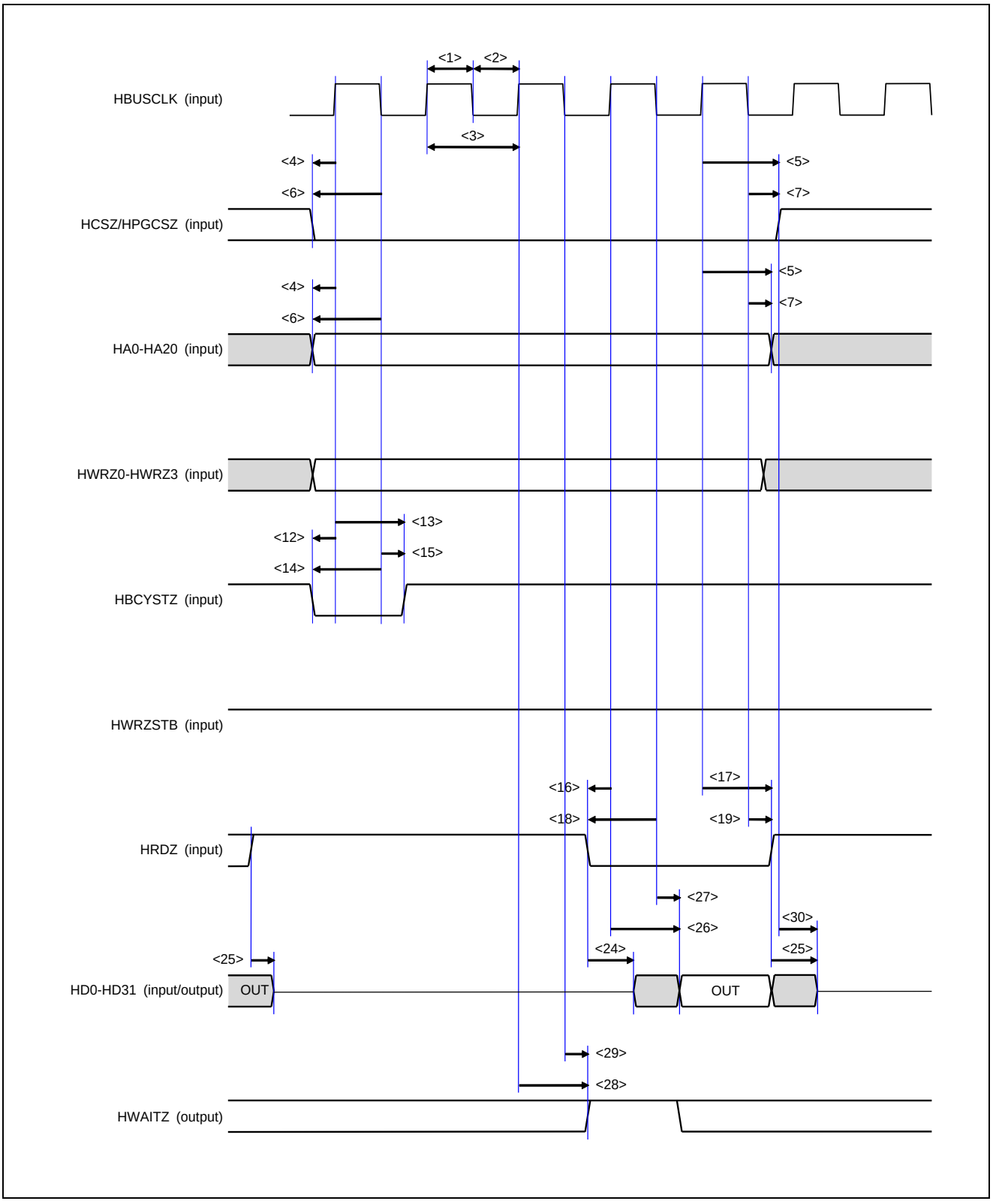


Figure 3.18 External MCU Interface Read Timing (MEMCSEL=H, ADMUXMODE=L)

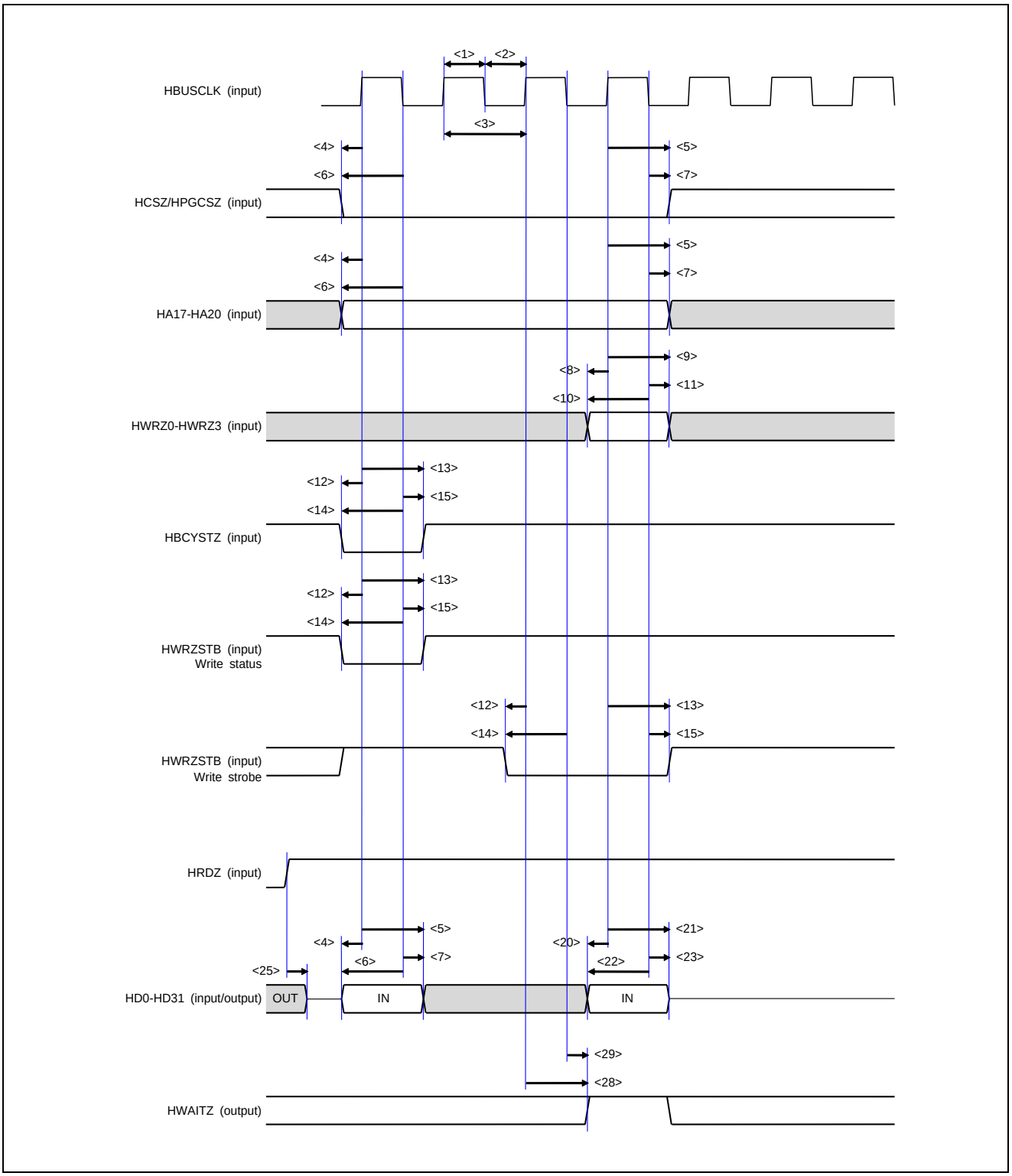


Figure 3.19 External MCU Interface Write Timing (MEMCSEL=H, ADMUXMODE=H)

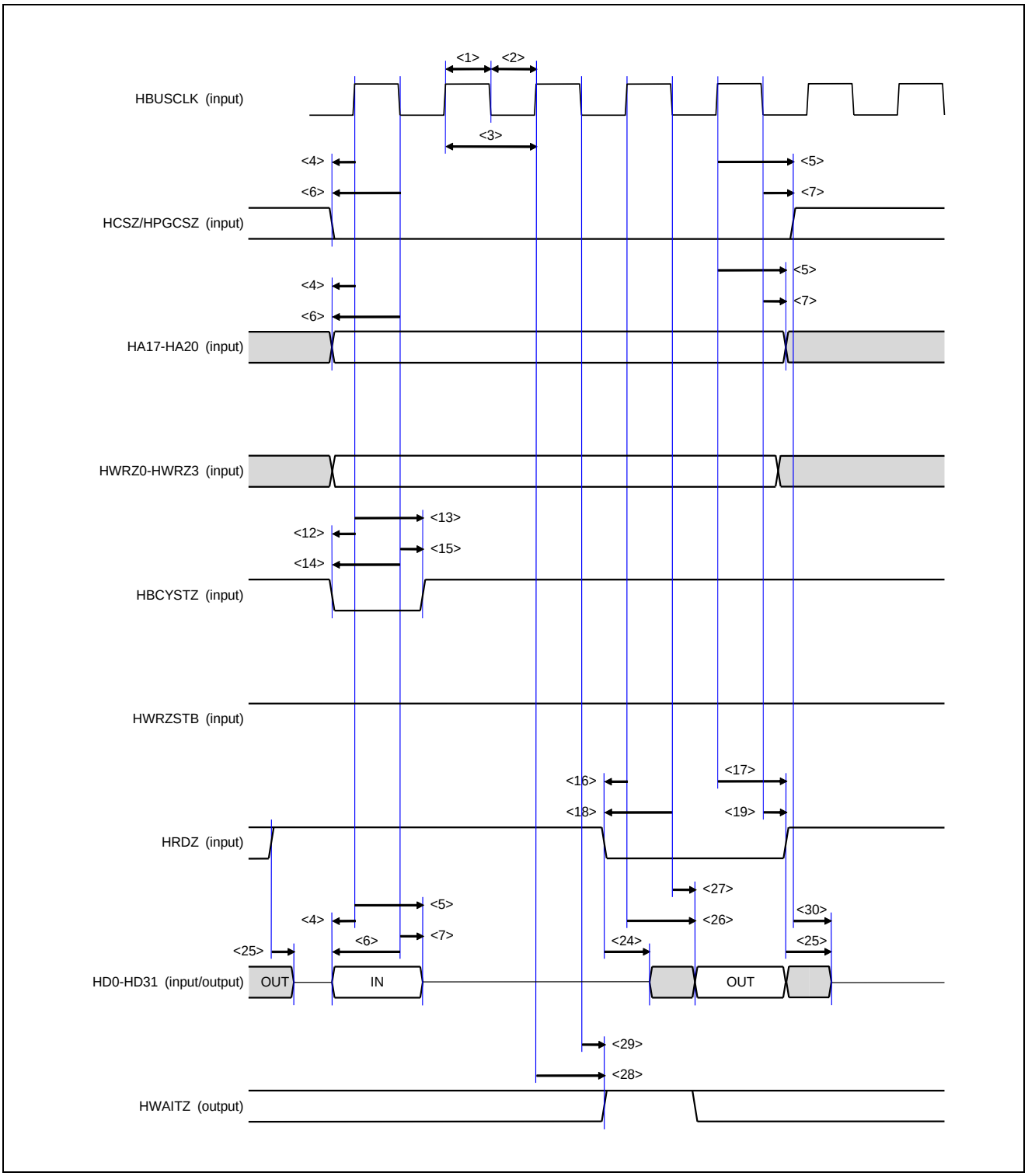


Figure 3.20 External MCU Interface Read Timing (MEMCSEL=H, ADMUXMODE=H)

3.8.5 Serial Flash ROM Interface

Item	Symbol	Conditions	MIN	MAX	Unit
SMSCK output cycle	t_{SFRCYC}	C_L = 15 pF	20	—	ns
SMSCK High-level width	t_{SMCKH}		0.5 × t_{SFRCYC} − 2.0	0.5 × t_{SFRCYC} + 2.0	ns
SMSCK Low-level width	t_{SMCKL}		0.5 × t_{SFRCYC} − 2.0	0.5 × t_{SFRCYC} + 2.0	ns
SMSCK rising time	t_{SMCKR}		—	1.9	ns
SMSCK falling time	t_{SMCKF}		—	1.9	ns
Delay time between SMCSZ falling and SMSCK rising	$t_{DSMCSCK}$	C_L = 15 pF, Freq = 50 MHz	6.0*	—	ns
Hold time from SMSCK rising to SMCSZ rising	$t_{DSMCKCS}$	C_L = 15 pF, Freq = 50 MHz	9.0*	—	ns
SMCSZ High-level width	t_{SMCSH}	C_L = 15 pF	14*	—	ns
SMIO0–SMIO3 input setup time (for SMSCK ↓)	t_{SSMIO}	—	6.0	—	ns
SMIO0–SMIO3 input hold time (for SMSCK ↓)	t_{HSMIO}	—	0	—	ns
SMIO0–SMIO3 output delay time (for SMSCK ↓)	t_{DSMIO}	C_L = 15 pF	−1.0	5.0	ns

Note. The timing can be extended by the setting of the SFMSSC register.
For details, refer to the "R-IN32M4-CL3 User's Manual: Hardware edition".

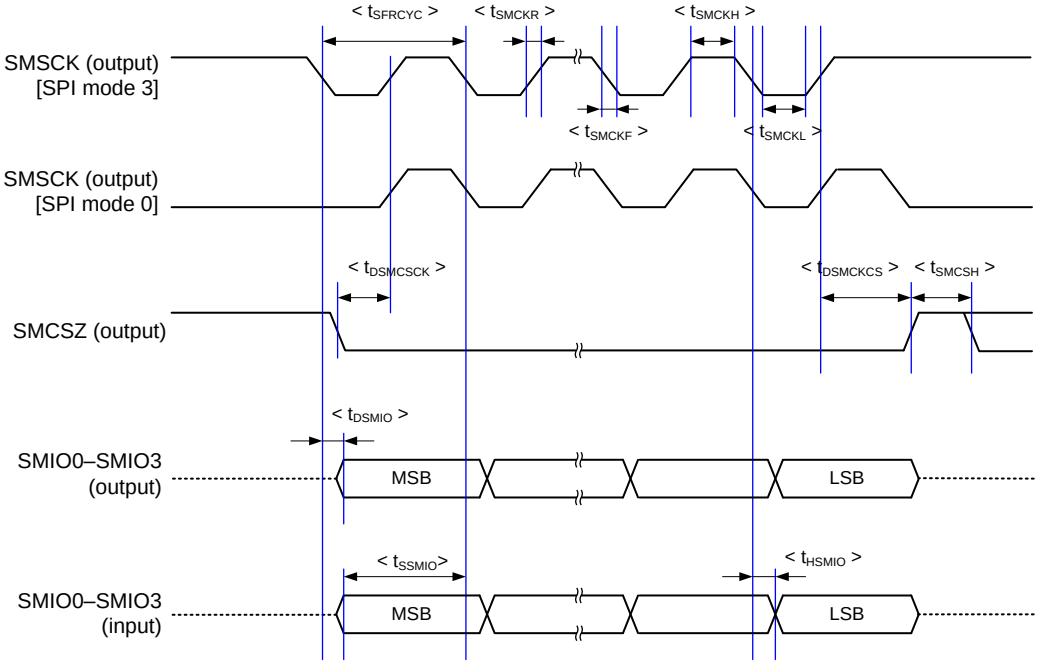


Figure 3.21 Serial Flash Memory Access Timing

3.8.6 External DMA Interface

Item	Symbol	Conditions	MIN	MAX	Unit
DMAREQZn and RTDMAREQZ input setup time (for BUSCLK ↑)	t_{SKDR}	—	7.0	—	ns
DMAREQZn and RTDMAREQZ input hold time 1	t_{HKDR1}	—	Until DMAACKZ↓, RTDMAACKZ↓	—	ns
DMAREQZn and REDMAREQZ input hold time 2 (for BUSCLK ↑)	t_{HKDR2}	—	—	t_{BUSCLK}*1 × m*2 − 7.0	ns
DMAACKZn and RTDMACKZ output delay time (for BUSCLK ↑)	t_{DKDA}	C_L = 30 pF	2.0	10.0	ns
DMAACKZ and RTDMAACKZ output Low-level width	t_{WDAL}	—	t_{BUSCLK}*1 × m*2 − 8	t_{BUSCLK}*1 × m*2 + 8	ns
DMATCZn and RTDMATCZ output delay time (for BUSCLK ↑)	t_{DKTC}	C_L = 30 pF	2.0	10.0	ns

Note 1. t_{BUSCLK} is one cycle (10 ns) of BUSCLK.
2. n = 0, 1, m = 1–31 (DMAIFC0, DMAIFC1, and RTMDAIFC registers)

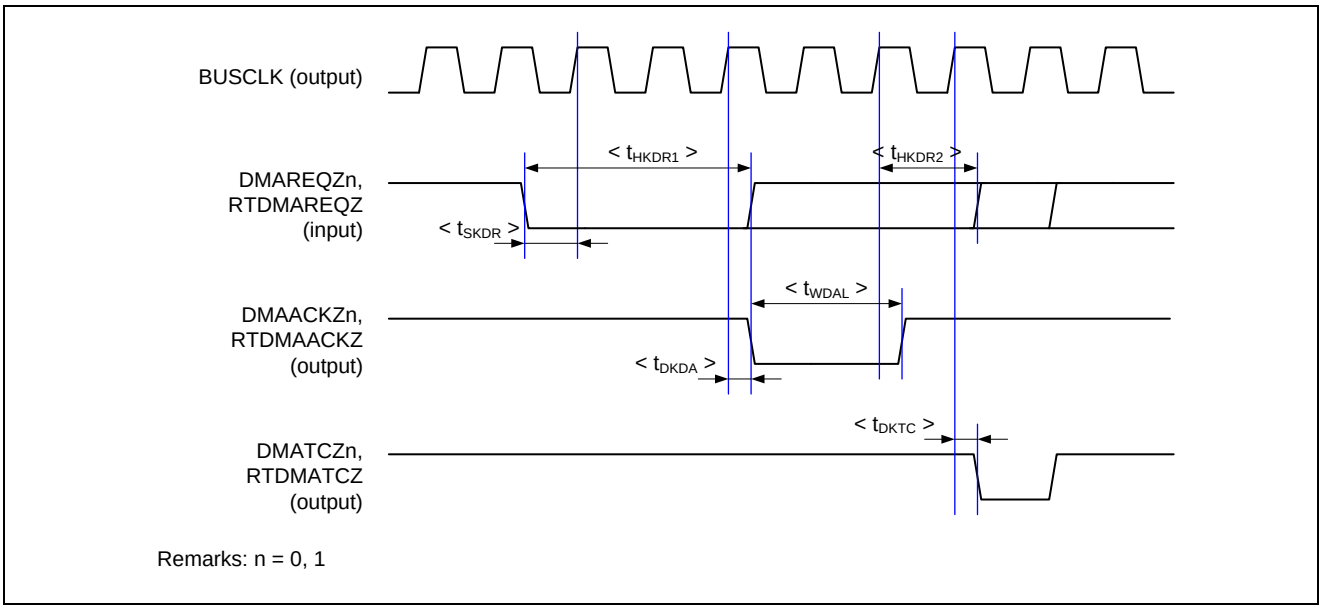


Figure 3.22 External DMA Access Timing

3.8.7 CSI Interface

The clocked serial interface (CSI) supports master mode and slave mode.

(1) Master mode

Item	Symbol	Conditions	MIN	MAX	Unit
CSISCKn output cycle	$t_{CSIMSCK}$	C_L = 15 pF	40	—	ns
CSISCKn output High-level width	t_{WSKH}	C_L = 15 pF	0.5 × $t_{CSIMSCK}$ − 5.0	—	ns
CSISCKn output Low-level width	t_{WSKL}	C_L = 15 pF	0.5 × $t_{CSIMSCK}$ − 5.0	—	ns
CSISIn input setup time (for CSISCKn ↑)	t_{SMSI}	—	8.5	—	ns
CSISIn input setup time (for CSISCKn ↓)	t_{SMSI}	—	8.5	—	ns
CSISIn input hold time (for CSISCKn ↑)	t_{HMSI}	—	7.0	—	ns
CSISIn input hold time (for CSISCKn ↓)	t_{HMSI}	—	7.0	—	ns
CSISOn output delay time (for CSISCKn ↑)	t_{DMSO}	C_L = 15 pF	—	7.0	ns
CSISOn output delay time (for CSISCKn ↓)	t_{DMSO}		—	7.0	ns
CSISOn output hold time (for CSISCKn ↑)	t_{HMSO}		0.5 × $t_{CSIMSCK}$ − 5.0	—	ns
CSISOn output hold time (for CSISCKn ↓)	t_{HMSO}		0.5 × $t_{CSIMSCK}$ − 5.0	—	ns

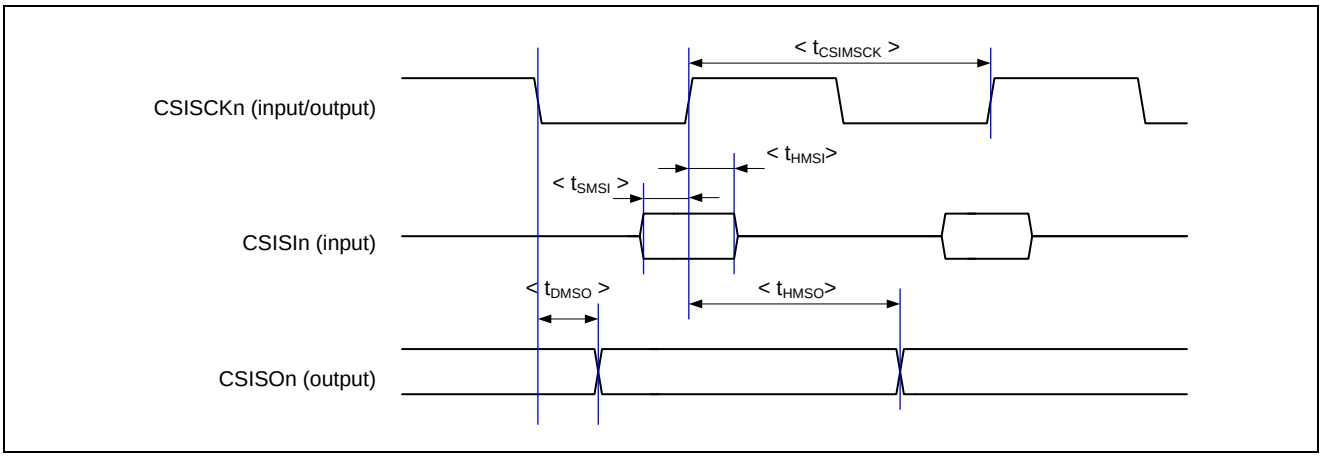


Figure 3.23 CSI Access Timing (Master Mode)

Remarks 1. **n = 0, 1**

2. **The above is an example of the timing for data output of "for CSISCKn ↓" and data input of "for CSISCKn ↑". Read the timing for reference in accordance with the operating mode.**

(2) Slave mode

Item	Symbol	Conditions	MIN	MAX	Unit
CSISCKn input cycle	$t_{CSISSCK}$	—	60	—	ns
CSISCKn input High-level width	t_{WSKH}	—	0.5 × $t_{CSISSCK}$ − 5.0	—	ns
CSISCKn input Low-level width	t_{WSKL}	—	0.5 × $t_{CSISSCK}$ − 5.0	—	ns
CSISIn input setup time (for CSISCKn ↑)	t_{SSSI}	—	10.0	—	ns
CSISIn input setup time (for CSISCKn ↓)	t_{SSSI}	—	10.0	—	ns
CSISIn input hold time (for CSISCKn ↑)	t_{HSSI}	—	15	—	ns
CSISIn input hold time (for CSISCKn ↓)	t_{HSSI}	—	15	—	ns
CSISOn output delay time (for CSISCKn ↑)	t_{DSSO}	C_L = 15 pF	—	10.0	ns
CSISOn output delay time (for CSISCKn ↓)	t_{DSSO}		—	10.0	ns
CSISOn output hold time (for CSISCKn ↑)	t_{HSSO}		0.5 × $t_{CSISSCK}$ − 5.0	—	ns
CSISOn output hold time (for CSISCKn ↓)	t_{HSSO}		0.5 × $t_{CSISSCK}$ − 5.0	—	ns

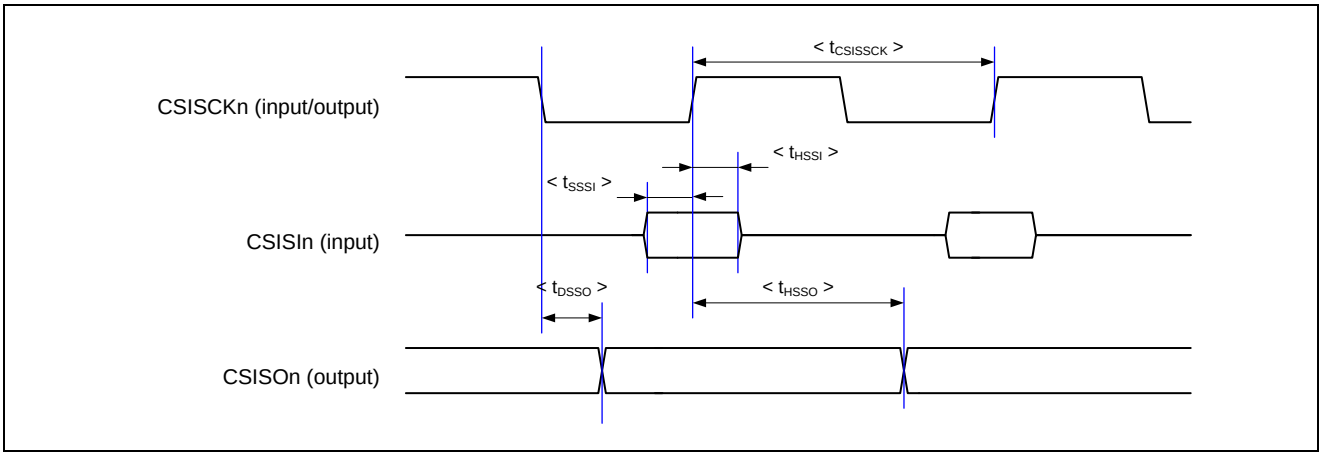


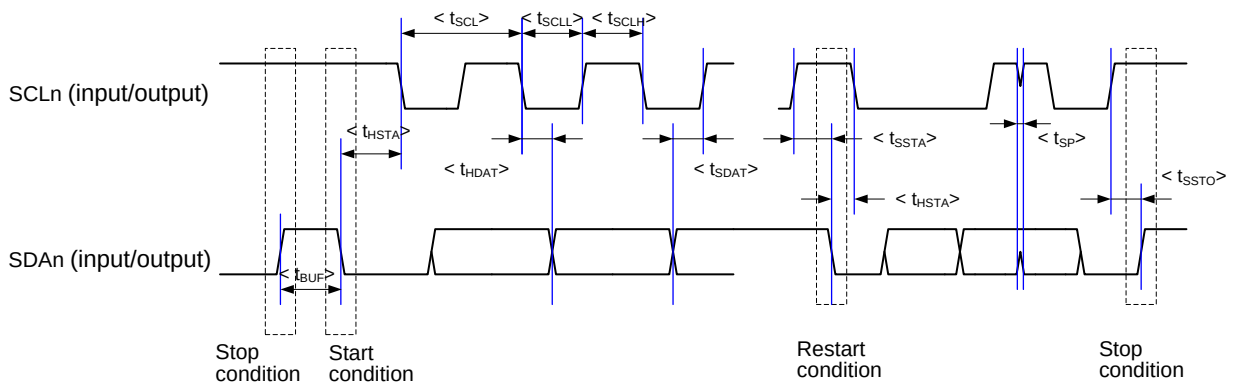
Figure 3.24 CSI Access Timing (Slave Mode)

Remarks 1. n = 0, 1

2. The above is an example of the timing for data output of "for CSISCKn ↓" and data input of "for CSISCKn ↑". Read the timing for reference in accordance with the operating mode.

3.8.8 I²C Interface

Item		Symbol	Conditions	Normal Mode		High-Speed Mode		Unit
				MIN	MAX	MIN	MAX	
SCLn input/output frequency		t_{SCL}	C_L = 30 pF	0	100	0	400	kHz
Bus-free time between the stop condition and start condition		t_{BUF}		4.7	—	1.3	—	µs
Hold time		t_{HSTA}		4.0	—	0.6	—	µs
SCLn clock Low-level width		t_{SCLL}		4.7	—	1.3	—	µs
SCLn clock High-level width		t_{SCLH}		4.0	—	0.6	—	µs
Setup time for the start and restart conditions		t_{SSTA}		4.7	—	0.6	—	µs
Data hold time	For a CBUS compatible master	t_{HDAT}		5.0	—	—	—	µs
	For an I²C bus			0	—	0	0.9	µs
Data setup time		t_{SDAT}		250	—	100	—	ns
SDAn and SCLn rising time		t_{SCLR}		—	1000	20 + 0.1 × C_b	300	ns
SDAn and SCLn falling time		t_{SCLF}		—	300	20 + 0.1 × C_b	300	ns
Setup time for the stop condition		t_{SSTO}		4.0	—	0.6	—	µs
Pulse width of spike suppressed by input filter		t_{SP}		—	—	0	50	ns
Capacitive load of each bus line		C_b	—	—	400	—	400	pF



The figure does not cover t_{SCLR} and t_{SCLF}.

Figure 3.25 I²C Access Timing

Remark. n = 0, 1

3.8.9 CAN Interface

Item	Symbol	Conditions	MIN	MAX	Unit
Internal delay time	t_{NODE}	C_L = 30 pF	—	75	ns

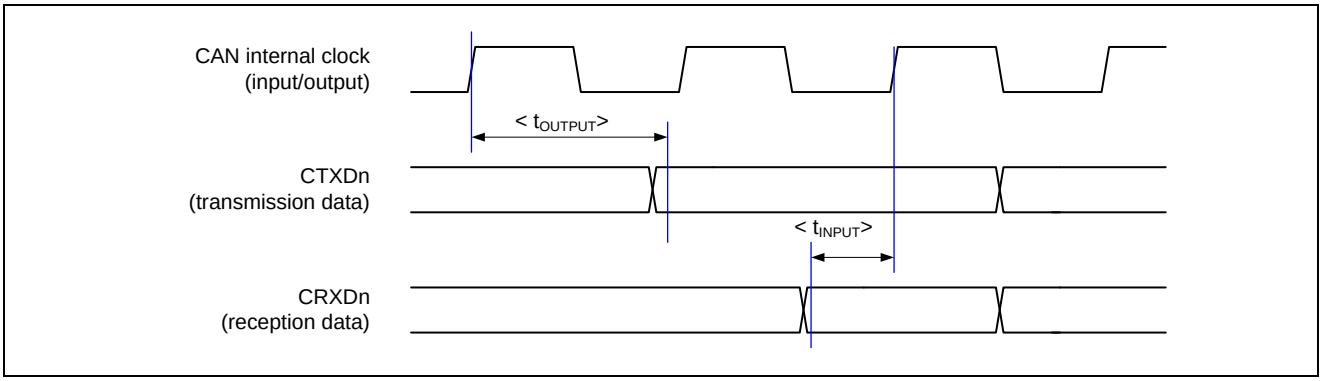


Figure 3.26 CAN Access Timing

Internal delay time (t_{NODE}) = Internal transmission delay time (t_{OUTPUT}) + Internal reception delay time (t_{INPUT})

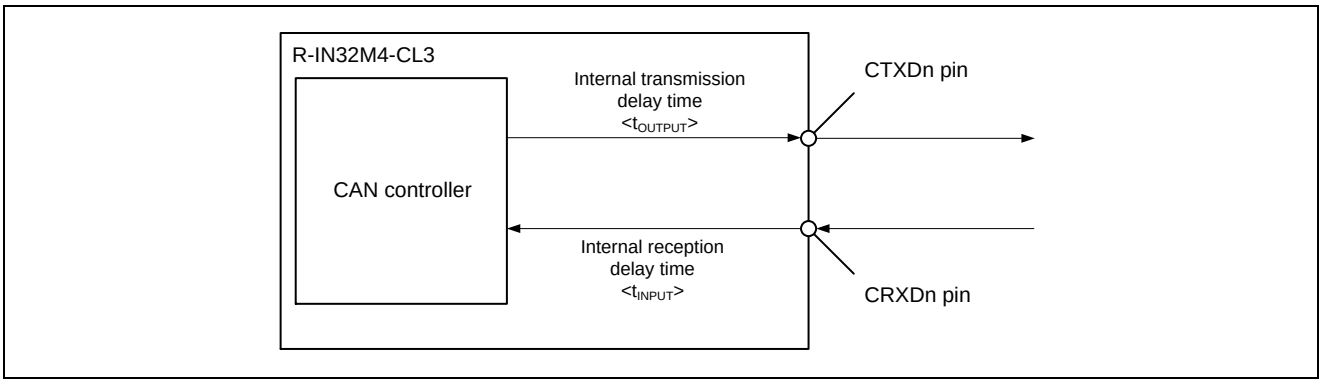


Figure 3.27 CAN Access Timing (Supplement)

Remarks 1. n = 0, 1

2. CAN internal clock (f_{CAN}): CAN baud-rate clock

3.8.10 Debugging Interface

(1) Debugging Serial Interface

Item	Symbol	Conditions	MIN	MAX	Unit
TCK input cycle	t_{TCK}	—	20	—	ns
TMS input setup time (for TCK ↑)	t_{STMS}	—	6.5	—	ns
TMS input hold time (for TCK ↑)	t_{HTMS}	—	0	—	ns
TDI input setup time (for TCK ↑)	t_{STDI}	—	6.5	—	ns
TDI input hold time (for TCK ↑)	t_{HTDI}	—	0	—	ns
TDO output delay time (for TCK ↓)	t_{DTDO}	C_L = 30 pF	3.0	13.0	ns

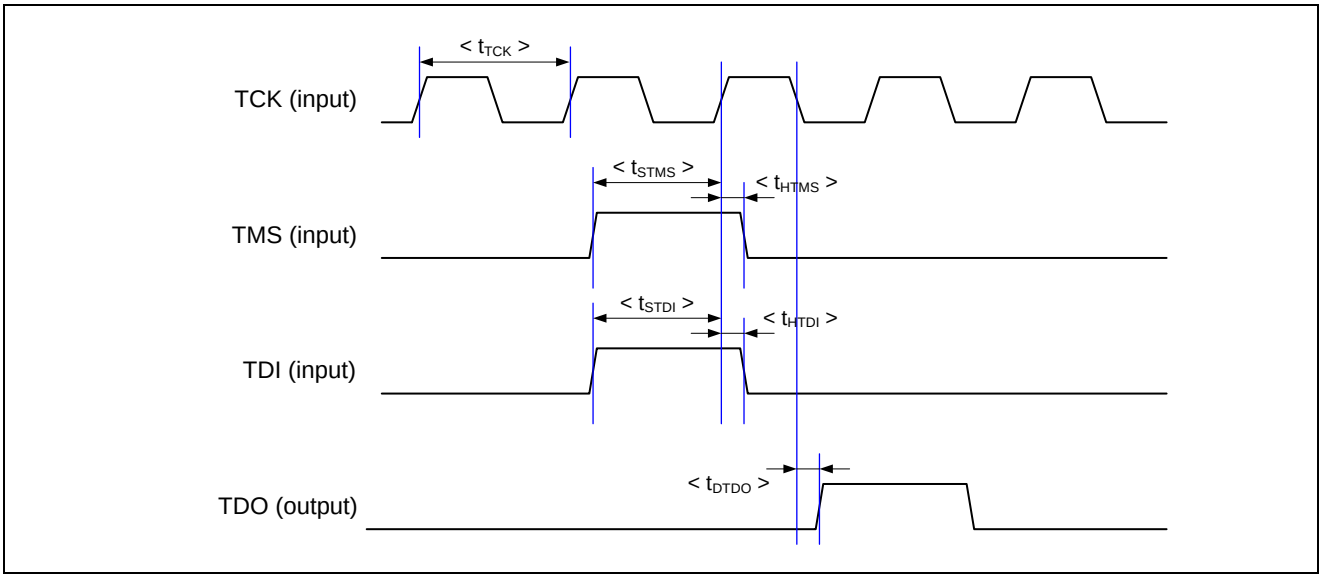


Figure 3.28 Debugging Serial Interface

(2) Trace Interface

Item	Symbol	Conditions	MIN	MAX	Unit
TRACECLK output cycle	t_{TRCCLK}	C_L = 15 pF	20	—	ns
TRACEDATAn output delay time (for TRACECLK)	$t_{DTRCDAT}$	C_L = 15 pF	0.26	8.43	ns

Remark. n = 0–3

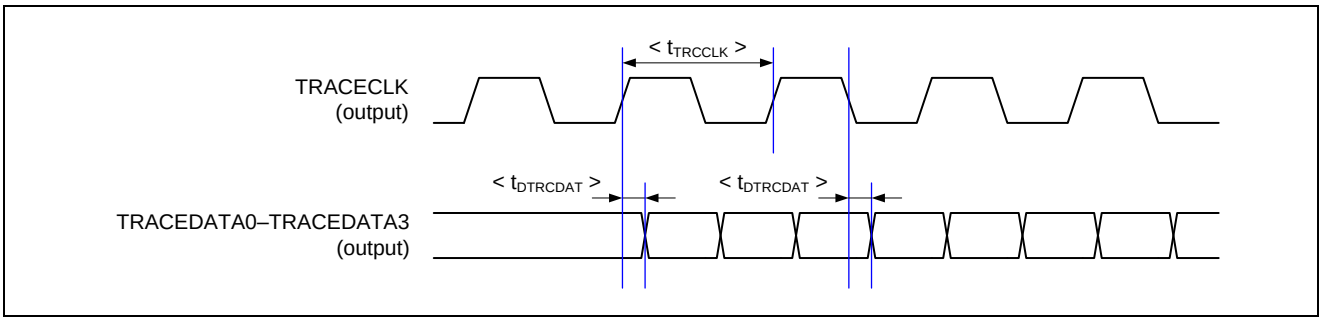


Figure 3.29 Trace Interface

3.9 2.5-V built-in Regulator Characteristics

Item	Symbol	Conditions	MIN	MAX	Unit
VDD25A rising time	$t_{VDD25AH}$	REG_EN = High	—	1*1	ms
VDD25A falling time	$t_{VDD25AL}$	REG_EN = High	—	—*2	ms

Note 1. This specification is based on the peripheral circuit configuration shown in the "R-IN32M4-CL3 User's Manual: Board design edition".

2. There is no timing specification when the AVDDREG_33 and VDDREG_33 are falling since the power will be turned off.

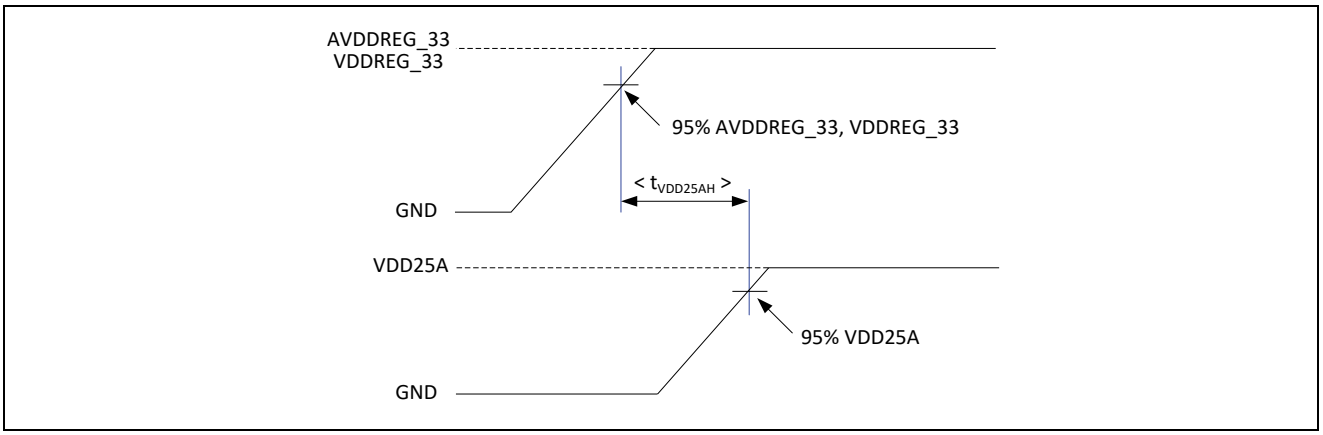


Figure 3.30 VDD25A rise timing

REVISION HISTORY

Rev.	Date	Description	
		Page	Summary
1.00	Nov 21, 2019	—	First Edition issued

General Precautions in the Handling of Microprocessing Unit and Microcontroller Unit Products

The following usage notes are applicable to all Microprocessing unit and Microcontroller unit products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Precaution against Electrostatic Discharge (ESD)
   A strong electrical field, when exposed to a CMOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop the generation of static electricity as much as possible, and quickly dissipate it when it occurs. Environmental control must be adequate. When it is dry, a humidifier should be used. This is recommended to avoid using insulators that can easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors must be grounded. The operator must also be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions must be taken for printed circuit boards with mounted semiconductor devices.
2. Processing at power-on
   The state of the product is undefined at the time when power is supplied. The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the time when power is supplied. In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the time when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the time when power is supplied until the power reaches the level at which resetting is specified.
3. Input of signal during power-off state
   Do not input signals or an I/O pull-up power supply while the device is powered off. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Follow the guideline for input signal during power-off state as described in your product documentation.
4. Handling of unused pins
   Handle unused pins in accordance with the directions given under handling of unused pins in the manual. The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of the LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible.
5. Clock signals
   After applying a reset, only release the reset line after the operating clock signal becomes stable. When switching the clock signal during program execution, wait until the target clock signal is stabilized. When the clock signal is generated with an external resonator or from an external oscillator during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Additionally, when switching to a clock signal produced with an external resonator or by an external oscillator while program execution is in progress, wait until the target clock signal is stable.
6. Voltage application waveform at input pin
   Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between V_{IL} (Max.) and V_{IH} (Min.) due to noise, for example, the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between V_{IL} (Max.) and V_{IH} (Min.).
7. Prohibition of access to reserved addresses
   Access to reserved addresses is prohibited. The reserved addresses are provided for possible future expansion of functions. Do not access these addresses as the correct operation of the LSI is not guaranteed.
8. Differences between products
   Before changing from one product to another, for example to a product with a different part number, confirm that the change will not lead to problems. The characteristics of a microprocessing unit or microcontroller unit products in the same group but having a different part number might differ in terms of internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

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