Renesas Synergy™ Platform

Software Quality Summary for SSP v1.5.0

R11AN0338EU0100
Rev.1.00
Oct 3, 2018

Introduction

This document presents a summary of the results collected by the Software Quality Assurance (SQA) activities performed during final qualification of version 1.5.0 of the Renesas Synergy™ Software Package (SSP). The SQA process itself is documented in the *Synergy™ Software Quality Handbook* available on renesassynergy.com/ssp.

Contents

1. Scope

One of the unique values of the Renesas Synergy™ Platform in the MCU industry is that the Synergy Software Package (SSP) is **warranted** by Renesas to operate within the specifications of a published software datasheet. To achieve this, each minor release of the SSP is **qualified** according to a documented Software Quality Assurance (SQA) process that was developed based on ISO/IEC/IEEE 12207 international standards, that is also used as a basis for significant safety, control, medical and industrial standards such as IEC 61508. The 12207 standard is used by NASA, the US Dept. of Defense, and other organizations that rely on high quality software.

2. How to Read the Synergy Software Quality Summary Report

Synergy Software Package			Quality Matrices					Quality Data					Functional Test		Software Unit Tests										Verification Index Score			
Test ID	SSP Module Name	Quality Index	Clean Build Index	Coverage Index	Complexity Index	Coding Standard Index	Verification Index	Test Coverage (statement/Decision)	Max Complexity	Coding Standard	Warning	Backward Compatible	Automated Test Coverage (Statement / Decision)	Tests	Development Test Coverage (Statement / Decision)	S7G2	S5D9	S5D5	S3A7	S3A6	S3S3	S3A1	S1JA	S128	S124	Tested on HW	Tests Traceable	Tests Passed	Test Matrix Complete
1	bsp	96%	5	5	4	5	5	(100/100)	13	0	0	1	(100/100)	128	(97/92)	36	3	34	32	32	32	32	31	32	30	1	1	2	1
3	r_acmphs	100%	5	5	5	5	5	(100/100)	9	0	0	1	(97/95)	31	(92/88)								9			1	1	2	1
4	r_acmplp	100%	5	5	5	5	5	(100/100)	8	0	0	1	(100/100)	27	(97/92)								10			1	1	2	1
5	r_adc	100%	5	5	5	5	5	(100/100)	10	0	0	1	(99/99)	213	(86/75)	35	35	34	28	28	28	28	27	28	28	1	1	2	1
6	r_agt	100%	5	5	5	5	5	(100/100)	10	0	0	1	(100/100)	95	(42/39)	32	32	32	32	32	32	32	32	32	32	1	1	2	1
7	r_cac	100%	5	5	5	5	5	(100/100)	10	0	0	1	(100/100)	130	(84/76)	24	24	24	24	24	24	24	24	24	24	1	1	2	1
8	r_can	100%	5	5	5	5	5	(100/100)	10	0	0	1	(100/100)	154	(26/17)	40	40	40	40	40	40	40	40	40	40	1	1	2	1
9	r_cgc	80%	5	5	0	5	5	(100/100)	44	0	0	1	(93/86)	203	(98/98)	90	90	90	90	90	90	90	22	19	19	1	1	2	1

Figure 1 Synergy Software Quality Summary report excerpt

2.1 SSP Module Name and Total Quality Index

The SSP Modules Name column of the Quality Summary Report indicates the names of all the individual SSP modules – each module contains many individual software functions and sometimes software frameworks. Each SSP module has an overall Quality Index that is calculated based on the combined results from the five quality metrics – 20% for each metric score of 5 with 100% as best possible score (five metrics with each a score of 5).

In addition, **Backward Compatible** (in Quality Data) indicates whether the SSP module passes the requirements for API compatibility between the version under test, and the previous minor SSP release (1 indicates pass, 0 indicates a failure).

2.2 Quality Metrics, Quality Data, and Functional Tests

The Synergy Software SQA Process defines a set of five key quality metrics that are used to quantify the quality of the SSP modules that make up the SSP. These metrics are as follows:

1. Clean Build index
2. Coverage index
3. Complexity index
4. Coding Standard index
5. Verification index

Each of these software metrics are scored on a scale from 0 to 5, where a score of 5 indicates a fully successful result, according to a set of defined requirement criteria.

For more details on the way the metrics are scored, as well as how the overall quality index is computed, refer to the *Synergy™ Software Quality Handbook*.

2.2.1 Clean Build Index

The **Clean Build Index** (in Quality Metrices) is computed based on the number of warnings that occur during compile and build time – a condition of zero warnings (and zero errors) is reflected as a full score of 5.

The **Warning** (in Quality Data) indicates the clean build score for each SSP module.

2.2.2 Coverage Index

The **Coverage Index** (in Quality Metrices) is computed based on how much code in a SSP module is tested. A score of 5 indicates that all functions, statements, branches/conditions within a SSP module are covered by the test.

Note that **Automated Test Coverage (Statement/Decision)** (in Functional Test) provides results of automated tests run of each SSP module. It is impossible to achieve 100% automated test coverage, manual testing and inspection are

performed to achieve full test coverage that is provided in the **Test Coverage (Statement/Decision)** (in Quality Data). The test coverage consists of conditional statements in the code being tested and all possible conditional outcomes.

2.2.3 Complexity Index

The **Complexity Index** (in Quality Metrices) indicates a derived normalized score of 0 to 5 that represents the cyclomatic complexity - an industry-recognized metric to indicate the **structuredness** of a program, developed by Thomas McCabe in 1976, where a 5 is most favorable. The complexity of each module is calculated using a static analysis tool to measure cyclomatic complexity. Code with lower cyclomatic complexity typically possess attributes of being well structured, modularized, and having a lower number of independent paths through the code. Benefits of favorable cyclonic complexity ratings for code include higher quality and robustness, easier maintenance, and efficient documentation.

The **Max Complexity** (in Quality Data) indicates the cyclomatic complexity measured for each SSP module.

2.2.4 Coding Standard Index

The **Coding Standard Index** (in Quality Metrices) is a composite score from 0 to 5 to represent how well each SSP module complies with the coding standards where 5 means no violations. The Coding Standard index reflects adherence to standards developed by Renesas for best coding practices that include guidance from the industry-recognized Barr Group, and include rules from MISRA C:2012 guidelines (100% of MISRA mandatory rules plus many MISRA Required rules). These coding standards and guidelines include criteria for SSP module size, naming and numbering, header commentary, in-line commentary, local/global data access, parameter passing, and code formatting. Meeting these standards will improve quality, maintenance, and documentation.

The **Coding Standard** (in Quality Data) contains supporting information that indicates the actual number of coding standard violations – zero is best.

2.2.5 Verification Index

The **Verification Index** (in Quality Metrices) indicates how well all the tests were performed by Renesas and is computed based on many test cases that are:

- Built using two separate compilers/C libraries, GCC and IAR.
- Executed on several Synergy MCU groups.
- Verified as traceable back to the specification of the SSP module.

A verification index with a score of 5 means: All planned tests were executed, there were no failures, all tests are traceable back to requirements, and all requirements were fully tested. For more information on the scoring, refer to the *Synergy™ Software Quality Handbook*.

2.3 Software Unit Tests

Software Unit Tests indicate the number of tests that were executed for each Synergy MCU Group. In the event of a failure, the Synergy SQA review board can decide to not take corrective action if the failure is deemed to not have an impact to the functionality of the software. If it has been decided that the corrective action is not necessary or can be deferred, then the issue is included in the SSP Release Notes (available on renesassynergy.com/ssp) and captured in the problem report system as a known issue. Such issues would be corrected in a future SSP release and reflected in the *Synergy™ Software Quality Summary*.

2.4 Verification Index Score

Verification index scores are used to indicate that all tests were executed. **Tested on HW** provides information whether the tests passed on all MCU Groups. **Tests Traceable, Tests Passed** and **Test Matrix Complete** indicate that the tests are traceable back to the specification, and that the test matrix for the SSP module is complete.

3. Additional Information

Note that the test report included in this document only summarizes a subset of all tests that are used to qualify SSP. Additional documentation for specific releases may be available under NDA from Renesas. Contact your local sales office for additional details.

4. Synergy Software Quality Summary for SSP version 1.5.0

Synergy Software Package			Quality Matrices					Quality Data					Functional Test		Software Unit Tests											Verification Index Score		
Test ID	SSP Module Name	Quality Index	Clean Build	Coverage	Complexity	Coding Standard	Verification	Test Coverage (statement/Decision)	Max Complexity	Coding Standard	warning	Backward Compatible	Automated Test Coverage(Statement / Decision)	Tests	Development Test Coverage(Statement / Decision)	s7g2	s5d9	s5d5	s5d3	s3a7	s3a6	s3a3	s3a1	s1ja	s128	s124	Tests Traceable	Tests Passed	Test Matrix Complete
1	bsp	100%	5	5	5	5	5	(100/100)	13	0	0	1	(89/86)	119	(97/92)	32	34	34	34	34	34	34	34	34	32	34	1	2	1
2	r_acmphs	100%	5	5	5	5	5	(100/100)	9	0	0	1	(95/93)	31	(0/0)	9	9	9	9	9				9			1	2	1
3	r_acmplp	96%	5	5	5	5	4	(100/100)	8	0	0	1	(100/100)	27	(0/0)					10	10	10	10	10	10	10	1	2	1
4	r_adc	100%	5	5	5	5	5	(100/100)	10	0	0	1	(100/100)	214	(100/100)	43	43	43	43	43	43	43	43	43	43	43	1	2	1
5	r_agt	100%	5	5	5	5	5	(100/100)	10	0	0	1	(100/100)	95	(92/88)	32	32	32	32	32	32	32	32	32	32	32	1	2	1
6	r_cac	100%	5	5	5	5	5	(100/100)	10	0	0	1	(100/100)	116	(97/92)	24	24	24	24	24	24	24	24	24	24	24	1	2	1
7	r_can	100%	5	5	5	5	5	(100/100)	10	0	0	1	(100/100)	165	(100/100)	40	40	40	40	40	40	40	40	40	40	40	1	2	1
8	r_cgc	80%	5	5	1	5	4	(100/100)	35	0	0	1	(92/91)	236	(74/70)	91	91	91	91	91	91	91	91	23	20	20	1	2	1
9	r_crc	96%	5	5	5	5	4	(100/100)	8	0	0	1	(100/100)	73	(84/76)	9	9	9	9	9	9	9	9	9	9	9	1	2	1
10	r_ctsu	60%	5	5	0	0	5	(100/100)	84	247	0	1	(93/87)	215	(31/21)	14	1	14	1	14	1	1	1	1	13	13	1	2	1
11	r_dac	100%	5	5	5	5	5	(100/100)	10	0	0	1	(99/96)	42	(100/100)	34	34	34	34	34	34	34	34			34	1	2	1
12	r_dac8	100%	5	5	5	5	5	(100/100)	10	0	0	1	(100/100)	50	(95/94)						1	37	1	37	37		1	2	1
13	r_dmac	100%	5	5	5	5	5	(100/100)	10	0	0	1	(100/100)	109	(96/92)	29	29	29	29	29	29	29	29				1	2	1
14	r_doc	100%	5	5	5	5	5	(100/100)	10	0	0	1	(100/100)	46	(99/96)	7	7	7	7	7	7	7	7	7	7	7	1	2	1
15	r_dtc	100%	5	5	5	5	5	(100/100)	10	0	0	1	(100/100)	100	(96/93)	28	28	28	28	28	28	28	28	28	28	28	1	2	1
16	r_elc	100%	5	5	5	5	5	(100/100)	5	0	0	1	(100/100)	36	(80/62)	7	7	7	7	7	7	7	7	7	7	7	1	2	1
17	r_flash_hp	100%	5	5	5	5	5	(100/100)	10	0	0	1	(98/95)	156	(100/100)	26	26	26	26								1	2	1
18	r_flash_lp	100%	5	5	5	5	5	(100/100)	10	0	0	1	(99/99)	202	(94/86)					54	54	54	54	54	54	54	1	2	1
19	r_fmi	100%	5	5	5	5	5	(100/100)	9	0	0	1	(100/100)	56	(80/71)	13	12	12	12	12	12	12	12	12	12	12	1	2	1
20	r_glcd	100%	5	5	5	5	5	(100/100)	10	0	0	1	(100/100)	207	(96/89)	149	149										1	2	1
21	r_gpt	100%	5	5	5	5	5	(100/100)	10	0	0	1	(100/100)	91	(99/99)	32	32	32	32	32	32	32	32	32	32	32	1	2	1
22	r_gpt_input_capture	100%	5	5	5	5	5	(100/100)	9	0	0	1	(100/100)	69	(99/96)	22	22	22	22	22	22	22	22	22	22	22	1	2	1
23	r_icu	100%	5	5	5	5	5	(100/100)	8	0	0	1	(100/100)	37	(86/75)	30	30	30	30	30	30	30	30	30	30	30	1	2	1
24	r_ioport	100%	5	5	5	5	5	(100/100)	6	0	0	1	(100/100)	93	(89/88)	27	27	27	27	27	27	27	27	27	27	27	1	2	1
25	r_iwdt	100%	5	5	5	5	5	(100/100)	7	0	0	1	(100/100)	52	(92/78)	19	19	19	19	19	19	19	19	19	19	19	1	2	1
26	r_jpeg_decode	100%	5	5	5	5	5	(100/100)	10	0	0	1	(100/100)	202	(95/89)	50	50										1	2	1
27	r_jpeg_encode	100%	5	5	5	5	5	(100/100)	9	0	0	1	(100/100)	71	(96/95)	9	9										1	2	1
28	r_kint	100%	5	5	5	5	5	(100/100)	9	0	0	1	(100/100)	55	(100/100)	15	15	15	15	15	15	15	15	15	15	15	1	2	1
29	r_lpmv2	100%	5	5	5	5	5	(100/100)	10	0	0	1	(100/100)	237	(86/75)	17	17	17	17	17	17	17	17	17	17	17	1	2	1
30	r_lvd	100%	5	5	5	5	5	(100/100)	9	0	0	1	(100/100)	44	(97/93)	12	12	12	12	12	12	12	12	12	12	12	1	2	1
31	r_opamp	100%	5	5	5	5	5	(100/100)	10	0	0	1	(100/100)	51	(95/91)					10	10	10	10	10	10		1	2	1
32	r_pdc	96%	5	5	5	5	4	(100/100)	10	0	0	1	(100/100)	79	(94/85)	10		10									1	2	1
33	r_qspi	100%	5	5	5	5	5	(100/100)	8	0	0	1	(100/98)	154	(87/78)	11	11	11	11	11		11	11				1	2	1
34	r_riic	100%	5	5	5	5	5	(100/100)	10	0	0	1	(100/100)	133	(98/96)	36	36	36	36	36	36	36	36	36	36	36	1	2	1
35	r_riic_slave	100%	5	5	5	5	5	(100/100)	10	0	0	1	(100/100)	76	(93/80)	45	45	45	44	45	45	44	45	45	44	45	1	2	1
36	r_rspi	100%	5	5	5	5	5	(100/100)	10	0	0	1	(100/99)	113	(92/82)	21	21	21	21	21	21	21	21	21	21	21	1	2	1
37	r_rtc	100%	5	5	5	5	5	(100/100)	10	0	0	1	(100/100)	244	(100/100)	13	13	13	13	13	13	13	13	13	13	13	1	2	1
38	r_sce	100%	5	5	5	5	5	(100/100)	11	0	0	1	(99/99)	1788	(85/71)	569	569	569	569	190	190	190	190	65	65	65	1	2	1

Synergy Software Package			Quality Matrices					Quality Data					Functional Test		Software Unit Tests											Verification Index Score		
Test ID	SSP Module Name	Quality Index	Clean Build	Coverage	Complexity	Coding Standard	Verification	Test Coverage (statement/Decision)	Max Complexity	Coding Standard	warning	Backward Compatible	Automated Test Coverage(Statement / Decision)	Tests	Development Test Coverage(Statement / Decision)	s7g2	s5d9	s5d5	s5d3	s3a7	s3a6	s3a3	s3a1	s1ja	s128	s124	Tests Traceable	Tests Passed	Test Matrix Complete
39	r_sci_i2c	100%	5	5	5	5	5	(100/100)	10	0	0	1	(100/100)	103	(91/82)	39	39	39	39	39	39	39	39	39	39	39	1	2	1
40	r_sci_spi	100%	5	5	5	5	5	(100/100)	10	0	0	1	(100/100)	85	(86/76)	26	26	26	26	26	26	26	26	26	26	26	1	2	1
41	r_sci_uart	100%	5	5	5	5	5	(100/100)	10	0	0	1	(100/100)	303	(92/88)	146	146	146	146	146	146	146	146	146	146	146	1	2	1
42	r_sdadc	100%	5	5	5	5	5	(100/100)	10	0	0	1	(99/99)	94	(83/76)									25			1	2	1
43	r_sdmmc	100%	5	5	5	5	5	(100/100)	10	0	0	1	(100/100)	220	(11/8)	52	54	52	52	36	1	52	52				1	2	1
44	r_slcdc	100%	5	5	5	5	5	(100/100)	10	0	0	1	(99/99)	115	(77/70)					19	19	19	19				1	2	1
45	r_ssi	100%	5	5	5	5	5	(100/100)	10	0	0	1	(100/100)	192	(94/88)	19	19	19	19	19	19	19	19				1	2	1
46	r_wdt	100%	5	5	5	5	5	(100/100)	9	0	0	1	(100/100)	75	(49/42)	25	25	25	25	25	25	25	25	25	25	25	1	2	1
47	sf_adc_periodic	96%	5	5	5	5	4	(100/100)	9	0	0	1	(100/100)	51	(85/75)	18	17	17	17	17	17	17	17	17	17	17	1	1	1
48	sf_audio_playback	100%	5	5	5	5	5	(100/100)	10	0	0	1	(100/100)	120	(31/23)	34	34	34	34	34	34	34	34	17	17	17	1	2	1
49	sf_audio_record	96%	5	5	5	5	4	(100/100)	9	0	0	1	(100/100)	40	(77/84)	14	14	14	14	14	14	14	1		1	13	1	2	1
50	sf_audio_record_i2s	100%	5	5	5	5	5	(100/100)	8	0	0	1	(100/100)	50	(81/76)	14	14	14	14	14	14	14	14				1	2	1
51	sf_ble_rl78g1d	100%	5	5	5	5	5	(100/100)	10	0	0	1	(98/98)	1167	(65/56)	29	29	29	29	29	29	29	29	1	29	29	1	2	1
52	sf_block_media_lx_nor	100%	5	5	5	5	5	(100/100)	9	0	0	1	(100/100)	45	(92/88)	9	9	9	9	9	1	9	9	1	1	1	1	2	1
53	sf_block_media_qspi	100%	5	5	5	5	5	(100/100)	8	0	0	1	(100/100)	47	(78/72)	9	9	9	9	9	1	9					1	2	1
54	sf_block_media_ram	100%	5	5	5	5	5	(100/100)	7	0	0	1	(100/100)	34	(96/95)	8	8	8	8	8	8	8	8	8	6		1	2	1
55	sf_block_media_sdmm	96%	5	5	5	5	4	(100/100)	10	0	0	1	(98/95)	40	(75/66)	8	8	8	8	8		8	8				1	2	1
56	sf_cellular	96%	5	5	5	5	4	(100/100)	10	0	0	1	(97/95)	1152	(81/72)	8	8	24	24	24	8	24	24				1	2	1
57	sf_comms_telnet	96%	5	5	5	5	4	(100/100)	10	0	0	1	(100/100)	89	(83/72)	17	17	17	17								1	2	1
58	sf_console	96%	5	5	5	5	4	(100/100)	10	0	0	1	(100/100)	82	(47/38)	78	78	78	104	78	78	78	1		78	78	1	2	1
59	sf_crypto	100%	5	5	5	5	5	(100/100)	10	0	0	1	(100/100)	43	(61/51)	12	12	12	12	12	12	12	12	12	12	12	1	2	1
60	sf_crypto_cipher	100%	5	5	5	5	5	(100/100)	10	0	0	1	(99/97)	300	(100/100)	91	91	91	91	57	57	57	57	27	27	27	1	2	1
61	sf_crypto_hash	96%	5	5	5	5	4	(100/100)	9	0	0	1	(100/100)	91	(87/75)	18	18	18	18								1	2	1
62	sf_crypto_key	96%	5	5	5	5	4	(100/100)	10	0	0	1	(100/100)	121	(84/79)	34	34	34	34	7	7	7	7				1	2	1
63	sf_crypto_key_installat	96%	5	5	5	5	4	(100/100)	10	0	0	1	(100/100)	93	(0/0)	25	25	25	25	13	13	13	13				1	2	1
64	sf_crypto_signature	96%	5	5	5	5	4	(100/100)	10	0	0	1	(97/95)	175	(78/70)	28	28	28	28								1	2	1
65	sf_crypto_trng	100%	5	5	5	5	5	(100/100)	9	0	0	1	(100/100)	24	(23/21)	8	8	8	8	8	8	8	8	8	8	8	1	2	1
66	sf_el_fx	100%	5	5	5	5	5	(100/100)	10	0	0	1	(100/100)	30	(91/83)	25	26	25	25	25	25	26	25				1	2	1
67	sf_el_gx	100%	5	5	5	5	5	(100/100)	10	0	0	1	(100/97)	96	(76/60)	33	33										1	2	1
68	sf_el_lx_nor	96%	5	5	5	5	4	(100/100)	9	0	0	1	(100/100)	37	(88/89)	16	16	16	16	16		16	16				1	2	1
69	sf_el_nx	80%	5	5	1	5	4	(100/100)	34	0	0	1	(100/100)	211	(58/51)	15	15	14									1	2	1
70	sf_el_nx_comms	96%	5	5	5	5	4	(100/100)	9	0	0	1	(100/100)	111	(13/10)	17	17	17									1	2	1
71	sf_el_tx	96%	5	5	5	5	4	(100/100)	12	0	0	1	(100/100)	25	(0/0)												1	2	1
72	sf_el_ux	84%	5	5	2	5	4	(100/100)	27	0	0	1	(90 /88)	620	(-1/-1)	28	16	16	14	12	6	12	12	3	3	3	1	2	1
73	sf_el_ux_comms_v2	100%	5	5	5	5	5	(100/100)	9	0	0	1	(100/100)	62	(69/65)	13	13	13	13	13	13	13	13	13	13	13	1	2	1
74	sf_external_irq	100%	5	5	5	5	5	(100/100)	10	0	0	1	(100/100)	44	(100/100)	14	14	14	14	14	14	14	14	14	14	14	1	2	1
75	sf_i2c	96%	5	5	5	5	4	(100/100)	10	0	0	1	(100/100)	78	(79/72)	21	0	21	21	21	21	21	0				1	2	1
76	sf_jpeg_decode	100%	5	5	5	5	5	(100/100)	7	0	0	1	(100/100)	83	(76/64)	14	14										1	2	1

Synergy Software Package			Quality Matrices					Quality Data					Functional Test		Software Unit Tests											Verification Index Score		
Test ID	SSP Module Name	Quality Index	Clean Build	Coverage	Complexity	Coding Standard	Verification	Test Coverage (statement/Decision)	Max Complexity	Coding Standard	warning	Backward Compatible	Automated Test Coverage(Statement / Decision)	Tests	Development Test Coverage(Statement / Decision)	s7g2	s5d9	s5d5	s5d3	s3a7	s3a6	s3a3	s3a1	s1ja	s128	s124	Tests Traceable	Tests Passed	Test Matrix Complete
77	sf_memory_qspi_nor	96%	5	5	5	5	4	(100/100)	8	0	0	1	(100/100)	54	(83/80)	16	16	16	16	16	0	16	16				1	2	1
78	sf_message	96%	5	5	5	5	4	(100/100)	9	0	0	1	(100/100)	74	(100/100)	73	73	73	73	73	73	73	73				1	2	1
79	sf_power_profiles_v2	100%	5	5	5	5	5	(100/100)	7	0	0	1	(96/90)	39	(95/93)	7	7	7	7	7	7	7	7	7	7	7	1	2	1
80	sf_spi	100%	5	5	5	5	5	(100/100)	10	0	0	1	(100/100)	106	(80/ 68)	28	28	28	28	28	28	28	28	28	28	28	1	2	1
81	sf_thread_monitor	100%	5	5	5	5	5	(100/100)	10	0	0	1	(100/100)	60	(33/ 25)	21	21	21	21	21	21	21	21	21	21	21	1	2	1
82	sf_touch_panel_v2	96%	5	5	5	5	4	(100/100)	10	0	0	1	(100/100)	63	(54/40)	14	14										1	2	1
83	sf_uart_comms	100%	5	5	5	5	5	(100/100)	10	0	0	1	(100/100)	83	(86/80)	44	44	44	44	44	44	44	44	44	44	44	1	2	1
84	sf_wifi_gt202	96%	5	5	5	5	4	(100/100)	10	0	0	1	(100/99)	335	(49/69)	22	22	22	22	22		22					1	2	1
85	snmp	Development unit test for partner code						NA	NA			1			(NA/NA)	19			19								1	2	1
86	tls											1				14	14		14								1	2	1
87	mqtt											1				14	14		14								1	2	1
88	NetX SW Crypto											1				14	14	10	10								1	2	1
89	nxd_web_http_client											1				3	3										1	2	1
Average quality index		98%																											

5. Quality Summary Notes

* Module verified by inspection when it could not be tested using the automated test routines.

Notes 1 and 2: Synergy SQA review board waived requirements that module complexity shall be no more than 10, provided that any module exceeding that level of complexity is tested to achieve 100% decision coverage for this release.

Note 3: Some SSP modules have not yet been updated to fully comply with all updated coding standard rules. Because of this, the Synergy SQA review board agreed to waive the coding standard compliance requirement for this release.

Note 4: Software unit test coverage for this module could not be completed, due to a lack of compatible hardware. This will be corrected in upcoming SSP releases.

 The SSP module in question uses hardware features that do not apply for this MCU group.

6. References

Synergy™ Software Quality Handbook (renesassynergy.com/ssp)

Synergy Software Package Release Notes (renesassynergy.com/ssp)

Website and Support

Visit the following vanity URLs to learn about key elements of the Synergy Platform, download components and related documentation, and get support.

Synergy Software	renesassynergy.com/software
Synergy Software Package	renesassynergy.com/ssp
Software add-ons	renesassynergy.com/addons
Software glossary	renesassynergy.com/softwareglossary
Development tools	renesassynergy.com/tools
Synergy Hardware	renesassynergy.com/hardware
Microcontrollers	renesassynergy.com/mcus
MCU glossary	renesassynergy.com/mcuglossary
Parametric search	renesassynergy.com/parametric
Kits	renesassynergy.com/kits
Synergy Solutions Gallery	renesassynergy.com/solutionsgallery
Partner projects	renesassynergy.com/partnerprojects
Application projects	renesassynergy.com/applicationprojects
Self-service support resources:	
Documentation	renesassynergy.com/docs
Knowledgebase	renesassynergy.com/knowledgebase
Forums	renesassynergy.com/forum
Training	renesassynergy.com/training
Videos	renesassynergy.com/videos
Chat and web ticket	renesassynergy.com/support

Revision History

Rev.	Date	Description	
		Page	Summary
1.00	Oct 3, 2018	—	Initial version

Notice

1. Descriptions of circuits, software and other related information in this document are provided only to illustrate the operation of semiconductor products and application examples. You are fully responsible for the incorporation or any other use of the circuits, software, and information in the design of your product or system. Renesas Electronics disclaims any and all liability for any losses and damages incurred by you or third parties arising from the use of these circuits, software, or information.
2. Renesas Electronics hereby expressly disclaims any warranties against and liability for infringement or any other claims involving patents, copyrights, or other intellectual property rights of third parties, by or arising from the use of Renesas Electronics products or technical information described in this document, including but not limited to, the product data, drawings, charts, programs, algorithms, and application examples.
3. No license, express, implied or otherwise, is granted hereby under any patents, copyrights or other intellectual property rights of Renesas Electronics or others.
4. You shall not alter, modify, copy, or reverse engineer any Renesas Electronics product, whether in whole or in part. Renesas Electronics disclaims any and all liability for any losses or damages incurred by you or third parties arising from such alteration, modification, copying or reverse engineering.
5. Renesas Electronics products are classified according to the following two quality grades: “Standard” and “High Quality”. The intended applications for each Renesas Electronics product depends on the product’s quality grade, as indicated below.

   "Standard": Computers; office equipment; communications equipment; test and measurement equipment; audio and visual equipment; home electronic appliances; machine tools; personal electronic equipment; industrial robots; etc.

   "High Quality": Transportation equipment (automobiles, trains, ships, etc.); traffic control (traffic lights); large-scale communication equipment; key financial terminal systems; safety control equipment; etc.

   Unless expressly designated as a high reliability product or a product for harsh environments in a Renesas Electronics data sheet or other Renesas Electronics document, Renesas Electronics products are not intended or authorized for use in products or systems that may pose a direct threat to human life or bodily injury (artificial life support devices or systems; surgical implantations; etc.), or may cause serious property damage (space system; undersea repeaters; nuclear power control systems; aircraft control systems; key plant systems; military equipment; etc.). Renesas Electronics disclaims any and all liability for any damages or losses incurred by you or any third parties arising from the use of any Renesas Electronics product that is inconsistent with any Renesas Electronics data sheet, user’s manual or other Renesas Electronics document.
6. When using Renesas Electronics products, refer to the latest product information (data sheets, user’s manuals, application notes, “General Notes for Handling and Using Semiconductor Devices” in the reliability handbook, etc.), and ensure that usage conditions are within the ranges specified by Renesas Electronics with respect to maximum ratings, operating power supply voltage range, heat dissipation characteristics, installation, etc. Renesas Electronics disclaims any and all liability for any malfunctions, failure or accident arising out of the use of Renesas Electronics products outside of such specified ranges.
7. Although Renesas Electronics endeavors to improve the quality and reliability of Renesas Electronics products, semiconductor products have specific characteristics, such as the occurrence of failure at a certain rate and malfunctions under certain use conditions. Unless designated as a high reliability product or a product for harsh environments in a Renesas Electronics data sheet or other Renesas Electronics document, Renesas Electronics products are not subject to radiation resistance design. You are responsible for implementing safety measures to guard against the possibility of bodily injury, injury or damage caused by fire, and/or danger to the public in the event of a failure or malfunction of Renesas Electronics products, such as safety design for hardware and software, including but not limited to redundancy, fire control and malfunction prevention, appropriate treatment for aging degradation or any other appropriate measures. Because the evaluation of microcomputer software alone is very difficult and impractical, you are responsible for evaluating the safety of the final products or systems manufactured by you.
8. Please contact a Renesas Electronics sales office for details as to environmental matters such as the environmental compatibility of each Renesas Electronics product. You are responsible for carefully and sufficiently investigating applicable laws and regulations that regulate the inclusion or use of controlled substances, including without limitation, the EU RoHS Directive, and using Renesas Electronics products in compliance with all these applicable laws and regulations. Renesas Electronics disclaims any and all liability for damages or losses occurring as a result of your noncompliance with applicable laws and regulations.
9. Renesas Electronics products and technologies shall not be used for or incorporated into any products or systems whose manufacture, use, or sale is prohibited under any applicable domestic or foreign laws or regulations. You shall comply with any applicable export control laws and regulations promulgated and administered by the governments of any countries asserting jurisdiction over the parties or transactions.
10. It is the responsibility of the buyer or distributor of Renesas Electronics products, or any other party who distributes, disposes of, or otherwise sells or transfers the product to a third party, to notify such third party in advance of the contents and conditions set forth in this document.
11. This document shall not be reprinted, reproduced or duplicated in any form, in whole or in part, without prior written consent of Renesas Electronics.
12. Please contact a Renesas Electronics sales office if you have any questions regarding the information contained in this document or Renesas Electronics products.

(Note 1) “Renesas Electronics” as used in this document means Renesas Electronics Corporation and also includes its directly or indirectly controlled subsidiaries.

(Note 2) “Renesas Electronics product(s)” means any product developed or manufactured by or for Renesas Electronics.

(Rev.4.0-1 November 2017)

RENESAS

SALES OFFICES

Renesas Electronics Corporation

http://www.renesas.com

Refer to "http://www.renesas.com/" for the latest and detailed information.

Renesas Electronics Corporation
TOYOSU FORESIA, 3-2-24 Toyosu, Koto-ku, Tokyo 135-0061, Japan

Renesas Electronics America Inc.
1001 Murphy Ranch Road, Milpitas, CA 95035, U.S.A.
Tel: +1-408-432-8888, Fax: +1-408-434-5351

Renesas Electronics Canada Limited
9251 Yonge Street, Suite 8309 Richmond Hill, Ontario Canada L4C 9T3
Tel: +1-905-237-2004

Renesas Electronics Europe Limited
Dukes Meadow, Millboard Road, Bourne End, Buckinghamshire, SL8 5FH, U.K
Tel: +44-1628-651-700

Renesas Electronics Europe GmbH
Arcadiastrasse 10, 40472 Düsseldorf, Germany
Tel: +49-211-6503-0, Fax: +49-211-6503-1327

Renesas Electronics (China) Co., Ltd.
Room 1709 Quantum Plaza, No.27 ZhichunLu, Haidian District, Beijing, 100191 P. R. China
Tel: +86-10-8235-1155, Fax: +86-10-8235-7679

Renesas Electronics (Shanghai) Co., Ltd.
Unit 301, Tower A, Central Towers, 555 Langao Road, Putuo District, Shanghai, 200333 P. R. China
Tel: +86-21-2226-0888, Fax: +86-21-2226-0999

Renesas Electronics Hong Kong Limited
Unit 1601-1611, 16/F., Tower 2, Grand Century Place, 193 Prince Edward Road West, Mongkok, Kowloon, Hong Kong
Tel: +852-2265-6688, Fax: +852 2886-9022

Renesas Electronics Taiwan Co., Ltd.
13F, No. 363, Fu Shing North Road, Taipei 10543, Taiwan
Tel: +886-2-8175-9600, Fax: +886 2-8175-9670

Renesas Electronics Singapore Pte. Ltd.
80 Bendemeer Road, Unit #06-02 Hyflux Innovation Centre, Singapore 339949
Tel: +65-6213-0200, Fax: +65-6213-0300

Renesas Electronics Malaysia Sdn.Bhd.
Unit 1207, Block B, Menara Amcorp, Amcorp Trade Centre, No. 18, Jln Persiaran Barat, 46050 Petaling Jaya, Selangor Darul Ehsan, Malaysia
Tel: +60-3-7955-9390, Fax: +60-3-7955-9510

Renesas Electronics India Pvt. Ltd.
No.777C, 100 Feet Road, HAL 2nd Stage, Indiranagar, Bangalore 560 038, India
Tel: +91-80-67208700, Fax: +91-80-67208777

Renesas Electronics Korea Co., Ltd.
17F, KAMCO Yangjae Tower, 262, Gangnam-daero, Gangnam-gu, Seoul, 06265 Korea
Tel: +82-2-558-3737, Fax: +82-2-558-5338

Colophon 7.2