RZ/G2L RZ/G2LC RZ/G2UL

Setting GPIO with Flexible Software Package

Introduction

This application note describes how to set the GPIO with the Renesas Flexible Software Package (FSP) for writing applications.

Target Device

RZ/G2L RZ/G2LC RZ/G2UL

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1. Introduction

1.1 Overview

This application note describes the following two main points.

- How to set the GPIO with the Renesas Flexible Software Package (FSP) for writing applications in RZ/G FSP v1.2.0 or earlier version.
- How to update an existing project from RZ/G FSP v1.2.0 or earlier version to v2.0.0.

2. What is Configuration a Project?

In e2 studio, all FSP applications are organized in RZ MPU projects. Setting up an RZ MPU project involves:

- Configuring a Project

When the project is created, e2 studio displays a summary of the current project configuration in the RZ MPU Project Editor. Each of the configurable elements in an FSP project can be edited using the appropriate tab in the RZ Configuration editor window.

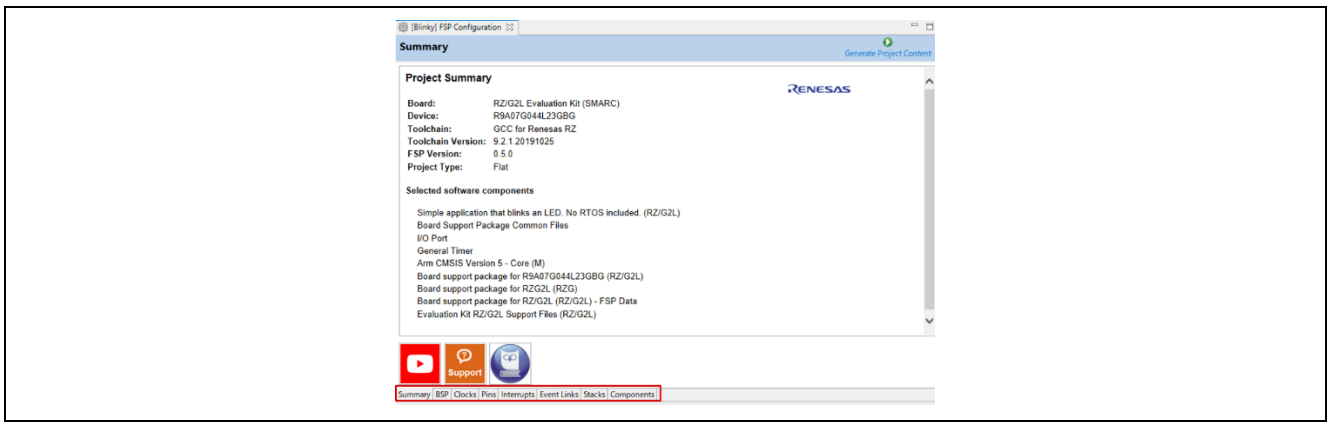


Figure 1: RZ Project Editor tabs

On the bottom of the RZ MPU Project Editor view, you can find the tabs for configuring multiple aspects of your project.

- [Summary] tab
  you can see all they key characteristics of the project: board, device, toolchain, and more.
- [BSP] tab
  you can change board specific parameters from the initial project selection.
- [Clocks] tab
  you can configure the MPU clock settings for your project. For the clock used in the RZ MPU, set the clock frequency by setting the register in the software that operates in main-core (Cortex-A55). In the Clocks tab, you should enter that frequency.
- [Pins] tab
  This tab did not support the target device in RZ/G FSP v1.2.0 or earlier version.
  However, it is supported in RZ/G FSP v2.0.0.
  Please check the chapter 6. to get more information.
- [Interrupts] tab
  you can add new user events/interrupts.
- [Event Links] tab
  This tab does not support the selected device.
- [Stacks] tab
  you can add and configure FSP modules. For each module selected in this tab, the Properties window provides access to the configuration parameters, interrupt selections.
- [Components] tab
  This tab provides an overview of the selected modules. Although you can also add drivers for specific FSP releases and application sample code here, this tab is normally only used for reference.

GPIO settings are made on the Pins tab, but FSP v1.2.0 or earlier version for these devices did not support it. Therefore, when using the I/O port, it was necessary to manually add the used I/O port setting in "src/pin_data.c". This manual describes how to change this.

3. Limitations

RZ/G2L has a multi-core configuration of Cortex-A55 and Cortex-M33. It is possible to use GPIO from each core. This package provides GPIO drivers for Cortex-M33, but GPIO can operate on the assumption that it is not used in Cortex-A55.

4. GPIO setting method

GPIO settings are made for each terminal. There are two items required for setting: Pin identifier and Pin Function Setting (PFS) configuration. The structure (ioport_pin_cfg_t) used for the setting is described below.

```
typedef struct st_ioport_pin_cfg
{
    uint32_t pin_cfg;
    bsp_io_port_pin_t pin;
} ioport_pin_cfg_t;
```

Type Member Name	Description
uint32 pin_cfg	PFS configuration Set using "typedef enume_ioport_cfg_options" and "typedef enume_ioport_peripheral" defined in the "r_ioport_api.h" file.
bsp_io_port_pin_t pin	Pin identifier Set using "typedef enum e_bsp_io_port_pin_t" defined in "bsp_io.h" file.

Add GPIO settings using the above structure to the array data "g_bsp_pin_cfg_data []" described in "pin_data.c". When Cortex-M33 is started, GPIO is set by the initialization function "SystemInit ()".

GPIO setting methods are classified into the following two types. The setting method is described with an example for each item.

- General Purpose Input Output Port (GPIO)
- Port Function Control

4.1 General Purpose Input Output Port (GPIO)

The following is a setting example of General Purpose Input Output Port (GPIO). In the setting example, P41_0 is output (input enabled). The 2nd line sets the Pin identifier, and the 3rd and 4th lines set the PFS configuration. At this time, refer to Table 4-1 for the PFS configuration that can be set.

```
0000 const ioport_pin_cfg_t g_bsp_pin_cfg_data[] = {
0001  {
0002    .pin     = BSP_IO_PORT_41_PIN_00,
0003    .pin_cfg = ((uint32_t) IOPORT_CFG_PORT_DIRECTION_OUTPUT_INPUT |
0004                (uint32_t) IOPORT_CFG_PORT_OUTPUT_HIGH)
0005  },
0006};
```

Table 4-1: PFS configuration for General Purpose Input Output Port

Register Name (Note1)	Definition	Port Mode (Note2)
Port Register (Pn)	IOPORT_CFG_PORT_OUTPUT_LOW IOPORT_CFG_PORT_OUTPUT_HIGH	Optional
Port Mode Register (PMn)	IOPORT_CFG_PORT_DIRECTION_HIZ IOPORT_CFG_PORT_DIRECTION_INPUT IOPORT_CFG_PORT_DIRECTION_OUTPUT IOPORT_CFG_PORT_DIRECTION_OUTPUT_INPUT	Imperative.
Driving Ability Control Register (IOLH)	IOPORT_CFG_DRIVE_B00 IOPORT_CFG_DRIVE_B01 IOPORT_CFG_DRIVE_B10 IOPORT_CFG_DRIVE_B11	Optional
Slew Rate Switching Register (SR)	IOPORT_CFG_SLEW_RATE_SLOW IOPORT_CFG_SLEW_RATE_FAST	Optional
Pull Up/Pull down Switching Register (PUPD)	IOPORT_CFG_PULLUP_PULLDOWN_DISABLE IOPORT_CFG_PULLUP_ENABLE IOPORT_CFG_PULLDOWN_ENABLE	Optional
Digital Noise Filter Switching Register (FILONOFF)	IOPORT_CFG_NOISE_FILTER_OFF IOPORT_CFG_NOISE_FILTER_ON	Optional
Digital Noise Filter Number Register (FILNUM)	IOPORT_CFG_NOISE_FILTER_NUM_4STAGE IOPORT_CFG_NOISE_FILTER_NUM_8STAGE IOPORT_CFG_NOISE_FILTER_NUM_12STAGE IOPORT_CFG_NOISE_FILTER_NUM_16STAGE	Optional
Digital Noise Filter Clock Selection Register (FILCLKSEL)	IOPORT_CFG_NOISE_FILTER_NOT_DIVIDED IOPORT_CFG_NOISE_FILTER_DIVIDED_9000 IOPORT_CFG_NOISE_FILTER_DIVIDED_18000 IOPORT_CFG_NOISE_FILTER_DIVIDED_36000	Optional
Interrupt Enable Control Register (ISEL)	IOPORT_CFG_TINT_DISABLE IOPORT_CFG_TINT_ENABLE	Optional

Notes: 1 For details on registers, refer to the RZ/G2L hardware manual.
2 Some items indicated by "Optional" are not supported depending on the terminal. Sets the items according to the system.

4.2 Port Function Control

The following is a setting example of Port Function Control. In the setting example, P48_0 is set to SCIFA ch2 TXD and P48_1 is set to SCIFA ch2 RXD port. The Pin identifier is set on the 2nd and 7th lines, and the PFS configuration is set on the 3rd to 4th lines and 8 to 9. At this time, refer to Table 4-2 for the PFS configuration that can be set.

```
0000 const ioport_pin_cfg_t g_bsp_pin_cfg_data[] = {
0001   {
0002    .pin     = BSP_IO_PORT_48_PIN_00,
0003    .pin_cfg = ((uint32_t) IOPORT_CFG_PERIPHERAL_PIN |
0004                (uint32_t) IOPORT_PERIPHERAL_MODE1   )
0005   },
0006   {
0007    .pin     = BSP_IO_PORT_48_PIN_01,
0008    .pin_cfg = ((uint32_t) IOPORT_CFG_PERIPHERAL_PIN |
0009                (uint32_t) IOPORT_PERIPHERAL_MODE1   )
0010   },
0006 };
```

Table 4-2: PFS configuration for Port Function Control

Register Name (Note1)	Definition	Peripheral Function Mode
Port Mode Control Register (PMCn)	IOPORT_CFG_PERIPHERAL_PIN	Imperative
Port Function Control Register (PFCm) (Note2)	IOPORT_PERIPHERAL_MODE1 IOPORT_PERIPHERAL_MODE2 IOPORT_PERIPHERAL_MODE3 IOPORT_PERIPHERAL_MODE4 IOPORT_PERIPHERAL_MODE5 IOPORT_PERIPHERAL_MODE6 (Note3) IOPORT_PERIPHERAL_MODE7 (Note3)	Imperative
Driving Ability Control Register (IOLH)	IOPORT_CFG_DRIVE_B00 IOPORT_CFG_DRIVE_B01 IOPORT_CFG_DRIVE_B10 IOPORT_CFG_DRIVE_B11	Optional
Slew Rate Switching Register (SR)	IOPORT_CFG_SLEW_RATE_SLOW IOPORT_CFG_SLEW_RATE_FAST	Optional
Pull Up/Pull down Switching Register (PUPD)	IOPORT_CFG_PULLUP_PULLDOWN_DISABLE IOPORT_CFG_PULLUP_ENABLE IOPORT_CFG_PULLDOWN_ENABLE	Optional
Digital Noise Filter Switching Register (FILONOFF)	IOPORT_CFG_NOISE_FILTER_OFF IOPORT_CFG_NOISE_FILTER_ON	Optional
Digital Noise Filter Number Register (FILNUM)	IOPORT_CFG_NOISE_FILTER_NUM_4STAGE IOPORT_CFG_NOISE_FILTER_NUM_8STAGE IOPORT_CFG_NOISE_FILTER_NUM_12STAGE IOPORT_CFG_NOISE_FILTER_NUM_16STAGE	Optional
Digital Noise Filter Clock Selection Register (FILCLKSEL)	IOPORT_CFG_NOISE_FILTER_NOT_DIVIDED IOPORT_CFG_NOISE_FILTER_DIVIDED_9000 IOPORT_CFG_NOISE_FILTER_DIVIDED_18000 IOPORT_CFG_NOISE_FILTER_DIVIDED_36000	Optional

Notes: 1 For details on registers, refer to the RZ/G2L hardware manual.
2 For details on definition, refer to section "5.Selection of each peripheral function".
3 Not available for RZ/G2L and RZ/G2LC.

5. Selection of each peripheral function

5.1 RZ/G2L, RZ/G2LC

The terminals of multiplexed function for RZ/G2L are listed below.

The terminals that can be assigned to each peripheral function differ depending on each device. Refers user's manual for the device.

Table 5-1: The multiplexed function of P0 pin.

Pin Name	Function 1	Function 2	Function 3	Function 4	Function 5
P0_0	IRQ0	SCI0_RXD	GTIOC0A	MTIOC0A	SCIF3_TXD
P0_1	IRQ1	SCI0_TXD	GTIOC0B	MTIOC0B	SCIF3_RXD

Table 5-2: The multiplexed function of P1 pin.

Pin Name	Function 1	Function 2	Function 3	Function 4	Function 5
P1_0	IRQ2	SCI0_SCK	GTIOC1A	MTIOC0C	SCIF3_SCK
P1_1	IRQ3	SCI0_CTS#/RTS#	GTIOC1B	MTIOC0D	-

Table 5-3: The multiplexed function of P2 pin.

Pin Name	Function 1	Function 2	Function 3	Function 4	Function 5
P2_0	IRQ4	ADC_TRG	GTIOC2A	MTIOC1A	SCIF4_TXD
P2_1	IRQ5	-	GTIOC2B	MTIOC1B	SCIF4_RXD

Table 5-4: The multiplexed function of P3 pin.

Pin Name	Function 1	Function 2	Function 3	Function 4	Function 5
P3_0	IRQ6	RIIC2_SDA	GTIOC3A	MTIOC2A	SCIF4_SCK
P3_1	IRQ7	RIIC2_SCL	GTIOC3B	MTIOC2B	CAM_FIELD

Table 5-5: The multiplexed function of P4 pin.

Pin Name	Function 1	Function 2	Function 3	Function 4	Function 5
P4_0	USB0_VBUSEN	SCIF2_TXD	MTIOC7A	ADC_TRG	-
P4_1	-	SCIF2_RXD	MTIOC7B	-	-

Table 5-6: The multiplexed function of P5 pin.

Pin Name	Function 1	Function 2	Function 3	Function 4	Function 5
P5_0	USB0_OVRCUR	SCIF2_SCK	MTIOC7C	SSI2_BCK	-
P5_1	USB0_OTG_ID	SCIF2_CTS#	MTIOC7D	SSI2_RCK	-
P5_2	USB0_OTG_EXICEN	SCIF2_RTS#	-	SSI2_DATA	-

Table 5-7: The multiplexed function of P6 pin.

Pin Name	Function 1	Function 2	Function 3	Function 4	Function 5
P6_0	DISP_CLK	SSI0_BCK	USB0_VBUSEN	MTIOC1A	-
P6_1	DISP_HSYNC	SSI0_RCK	-	MTIOC1B	-

Table 5-8: The multiplexed function of P7 pin.

Pin Name	Function 1	Function 2	Function 3	Function 4	Function 5
P7_0	DISP_VSYNC	SSI0_TXD	USB0_OVRCUR	MTIC5U	-
P7_1	DISP_DE	SSI0_RXD	USB0_OTG_ID	MTIC5V	-
P7_2	DISP_DATA0	-	USB0_OTG_EXICEN	MTIC5W	-

Table 5-9: The multiplexed function of P8 pin.

Pin Name	Function 1	Function 2	Function 3	Function 4	Function 5
P8_0	DISP_DATA1	USB1_VBUSEN	RSPI2_CK	RIIC3_SCL	-
P8_1	DISP_DATA2	USB1_OVRCUR	RSPI2_MOSI	RIIC3_SDA	-
P8_2	DISP_DATA3	-	RSPI2_MISO	-	-

Table 5-10: The multiplexed function of P9 pin.

Pin Name	Function 1	Function 2	Function 3	Function 4	Function 5
P9_0	DISP_DATA4	ADC_TRG	RSPI2_SSL	MTIOC2A	-
P9_1	DISP_DATA5	-	-	MTIOC2B	-

Table 5-11: The multiplexed function of P10 pin.

Pin Name	Function 1	Function 2	Function 3	Function 4	Function 5
P10_0	DISP_DATA6	CAN_CLK	MTIOC6A	GTETRGA	-
P10_1	DISP_DATA7	CAN0_TX	MTIOC6B	GTETRGB	-

Table 5-12: The multiplexed function of P11 pin.

Pin Name	Function 1	Function 2	Function 3	Function 4	Function 5
P11_0	DISP_DATA8	CAN0_RX	MTIOC6C	GTETRGC	-
P11_1	DISP_DATA9	CAN0_TX_DATARATE_EN	MTIOC6D	GTETRGD	-

Table 5-13: The multiplexed function of P12 pin.

Pin Name	Function 1	Function 2	Function 3	Function 4	Function 5
P12_0	DISP_DATA10	CAN0_RX_DATARATE_EN	POE0_N	GTIOC7A	-
P12_1	DISP_DATA11	CAN1_TX	POE4_N	GTIOC7B	-

Table 5-14: The multiplexed function of P13 pin.

Pin Name	Function 1	Function 2	Function 3	Function 4	Function 5
P13_0	DISP_DATA12	CAN1_RX	POE8_N	IRQ0	-
P13_1	DISP_DATA13	CAN1_TX_DATARATE_EN	POE10_N	IRQ1	-
P13_2	DISP_DATA14	CAN1_RX_DATARATE_EN	IRQ7	IRQ2	-

Table 5-15: The multiplexed function of P14 pin.

Pin Name	Function 1	Function 2	Function 3	Function 4	Function 5
P14_0	DISP_DATA15	SSI1_BCK	SD1_CD	MTCLKA	-
P14_1	DISP_DATA16	SSI1_RCK	SD1_WP	MTCLKB	-

Table 5-16: The multiplexed function of P15 pin.

Pin Name	Function 1	Function 2	Function 3	Function 4	Function 5
P15_0	DISP_DATA17	SSI1_TXD	GTIOC4A	MTCLKC	-
P15_1	DISP_DATA18	SSI1_RXD	GTIOC4B	MTCLKD	-

Table 5-17: The multiplexed function of P16 pin.

Pin Name	Function 1	Function 2	Function 3	Function 4	Function 5
P16_0	DISP_DATA19	SCIF2_TXD	GTIOC5A	IRQ3	-
P16_1	DISP_DATA20	SCIF2_RXD	GTIOC5B	IRQ4	-

Table 5-18: The multiplexed function of P17 pin.

Pin Name	Function 1	Function 2	Function 3	Function 4	Function 5
P17_0	DISP_DATA21	SCIF2_SCK	GTIOC6A	IRQ5	-
P17_1	DISP_DATA22	SCIF2_CTS#	GTIOC6B	IRQ6	-
P17_2	DISP_DATA23	SCIF2_RTS#	-	IRQ7	-

Table 5-19: The multiplexed function of P18 pin.

Pin Name	Function 1	Function 2	Function 3	Function 4	Function 5
P18_0	SD0_CD	GTIOC0A	RIIC3_SDA	MTIOC2A	-
P18_1	SD0_WP	GTIOC0B	RIIC3_SCL	MTIOC2B	-

Table 5-20: The multiplexed function of P19 pin.

Pin Name	Function 1	Function 2	Function 3	Function 4	Function 5
P19_0	SD1_CD	GTIOC3A	MTIOC1A	RIIC2_SDA	-
P19_1	SD1_WP	GTIOC3B	MTIOC1B	RIIC2_SCL	-

Table 5-21: The multiplexed function of P20 pin.

Pin Name	Function 1	Function 2	Function 3	Function 4	Function 5
P20_0	ET0_TXC/TX_CLK	RSPI0_CK	CAN_CLK	-	-
P20_1	ET0_TX_CTL/TX_EN	RSPI0_MOSI	CAN0_TX	-	-
P20_2	ET0_TXD0	RSPI0_MISO	CAN0_RX	-	-

Table 5-22: The multiplexed function of P21 pin.

Pin Name	Function 1	Function 2	Function 3	Function 4	Function 5
P21_0	ET0_TXD1	RSPI0_SSL	CAN0_TX_DATARATE_EN	-	-
P21_1	ET0_TXD2	-	CAN0_RX_DATARATE_EN	-	-

Table 5-23: The multiplexed function of P22 pin.

Pin Name	Function 1	Function 2	Function 3	Function 4	Function 5
P22_0	ET0_TXD3	SSI0_BCK	CAN1_TX	MTCLKA	-
P22_1	ET0_TX_ERR	SSI0_RCK	CAN1_RX	MTCLKB	-

Table 5-24: The multiplexed function of P23 pin.

Pin Name	Function 1	Function 2	Function 3	Function 4	Function 5
P23_0	ET0_TX_COL	SSI0_TXD	CAN1_TX_DATARATE_EN	MTCLKC	-
P23_1	ET0_TX_CRS	SSI0_RXD	CAN1_RX_DATARATE_EN	MTCLKD	-

Table 5-25: The multiplexed function of P24 pin.

Pin Name	Function 1	Function 2	Function 3	Function 4	Function 5
P24_0	ET0_RXC/RX_CLK	SSI1_BCK	POE0_N	-	-
P24_1	ET0_RX_CTL/RX_DV	SSI1_RCK	POE4_N	-	-

Table 5-26: The multiplexed function of P25 pin.

Pin Name	Function 1	Function 2	Function 3	Function 4	Function 5
P25_0	ET0_RXD0	SSI1_TXD	POE8_N	-	-
P25_1	ET0_RXD1	SSI1_RXD	POE10_N	-	-

Table 5-27: The multiplexed function of P26 pin.

Pin Name	Function 1	Function 2	Function 3	Function 4	Function 5
P26_0	ET0_RXD2	RSPI1_CK	MTIOC8A	-	-
P26_1	ET0_RXD3	RSPI1_MOSI	MTIOC8B	-	-

Table 5-28: The multiplexed function of P27 pin.

Pin Name	Function 1	Function 2	Function 3	Function 4	Function 5
P27_0	ET0_RX_ERR	RSPI1_MISO	MTIOC8C	-	-
P27_1	ET0_MDC	RSPI1_SSL	MTIOC8D	-	-

Table 5-29: The multiplexed function of P28 pin.

Pin Name	Function 1	Function 2	Function 3	Function 4	Function 5
P28_0	ET0_MDIO	-	-	-	-
P28_1	ET0_LINKSTA	-	-	-	-

Table 5-30: The multiplexed function of P29 pin.

Pin Name	Function 1	Function 2	Function 3	Function 4	Function 5
P29_0	ET1_TXC/TX_CLK	CAM_PCLK	-	USB1_VBUSEN	SSI2_BCK
P29_1	ET1_TX_CTL/TX_EN	CAM_HREF	-	USB1_OVRCUR	SSI2_RCK

Table 5-31: The multiplexed function of P30 pin.

Pin Name	Function 1	Function 2	Function 3	Function 4	Function 5
P30_0	ET1_TXD0	CAM_VSYNC	-	-	SSI2_DATA
P30_1	ET1_TXD1	CAM_DATA15	-	-	-

Table 5-32: The multiplexed function of P31 pin.

Pin Name	Function 1	Function 2	Function 3	Function 4	Function 5
P31_0	ET1_TXD2	CAM_DATA0	SCI1_RXD	-	SSI3_BCK
P31_1	ET1_TXD3	CAM_DATA1	SCI1_TXD	-	SSI3_RCK

Table 5-33: The multiplexed function of P32 pin.

Pin Name	Function 1	Function 2	Function 3	Function 4	Function 5
P32_0	ET1_TX_ERR	CAM_DATA2	SCI1_SCK	MTIOC3A	SSI3_TXD
P32_1	ET1_TX_COL	CAM_DATA3	SCI1_CTS#/RTS#	MTIOC3B	SSI3_RXD

Table 5-34: The multiplexed function of P33 pin.

Pin Name	Function 1	Function 2	Function 3	Function 4	Function 5
P33_0	ET1_TX_CRS	CAM_DATA4	GTIOC2A	SCIF2_TXD	GTIOC0A
P33_1	ET1_RXC/RX_CLK	CAM_DATA5	GTIOC2B	SCIF2_RXD	GTIOC0B

Table 5-35: The multiplexed function of P34 pin.

Pin Name	Function 1	Function 2	Function 3	Function 4	Function 5
P34_0	ET1_RX_CTL/RX_DV	CAM_DATA6	GTIOC3A	MTIOC0A	GTIOC1A
P34_1	ET1_RXD0	CAM_DATA7	GTIOC3B	MTIOC0B	GTIOC1B

Table 5-36: The multiplexed function of P35 pin.

Pin Name	Function 1	Function 2	Function 3	Function 4	Function 5
P35_0	ET1_RXD1	CAM_DATA8	SSI0_BCK	MTIOC0C	GTIOC2A
P35_1	ET1_RXD2	CAM_DATA9	SSI0_RCK	MTIOC0D	GTIOC2B

Table 5-37: The multiplexed function of P36 pin.

Pin Name	Function 1	Function 2	Function 3	Function 4	Function 5
P36_0	ET1_RXD3	CAM_DATA10	SSI0_TXD	MTIOC3C	GTETRGA
P36_1	ET1_RX_ERR	CAM_DATA11	SSI0_RXD	MTIOC3D	GTETRGB

Table 5-38: The multiplexed function of P37 pin.

Pin Name	Function 1	Function 2	Function 3	Function 4	Function 5
P37_0	ET1_MDC	CAM_DATA12	-	SCIF2_SCK	GTETRGC
P37_1	ET1_MDIO	CAM_DATA13	-	SCIF2_CTS#	GTETRGD
P37_2	ET1_LINKSTA	CAM_DATA14	-	SCIF2_RTS#	-

Table 5-39: The multiplexed function of P38 pin.

Pin Name	Function 1	Function 2	Function 3	Function 4	Function 5
P38_0	SCIF0_TXD	GTETRGA	CAN_CLK	MTIOC4A	USB1_VBUSEN
P38_1	SCIF0_RXD	GTETRGB	CAN0_TX	MTIOC4B	USB1_OVRCUR

Table 5-40: The multiplexed function of P39 pin.

Pin Name	Function 1	Function 2	Function 3	Function 4	Function 5
P39_0	SCIF0_SCK	GTETRGC	CAN0_RX	MTIOC4C	-
P39_1	SCIF0_CTS#	GTETRGD	CAN0_TX_DATARATE_EN	MTIOC4D	-
P39_2	SCIF0_RTS#	-	CAN0_RX_DATARATE_EN	-	-

Table 5-41: The multiplexed function of P40 pin.

Pin Name	Function 1	Function 2	Function 3	Function 4	Function 5
P40_0	SCIF1_TXD	GTIOC6A	CAN1_TX	MTIC5U	SCI0_RXD
P40_1	SCIF1_RXD	GTIOC6B	CAN1_RX	MTIC5V	SCI0_TXD
P40_2	SCIF1_SCK	-	CAN1_TX_DATARATE_EN	MTIC5W	SCI0_SCK

Table 5-42: The multiplexed function of P41 pin.

Pin Name	Function 1	Function 2	Function 3	Function 4	Function 5
P41_0	SCIF1_CTS#	GTIOC7A	CAN1_RX_DATARATE_EN	GTIOC3A	SCI0_CTS#/RTS#
P41_1	SCIF1_RTS#	GTIOC7B	-	GTIOC3B	-

Table 5-43: The multiplexed function of P42 pin.

Pin Name	Function 1	Function 2	Function 3	Function 4	Function 5
P42_0	USB1_VBUSEN	RSPI2_CK	CAN_CLK	SCIF2_TXD	MTIOC7A
P42_1	USB1_OVRCUR	RSPI2_MOSI	CAN0_TX	SCIF2_RXD	MTIOC7B
P42_2	ADC_TRG	RSPI2_MISO	CAN0_RX	SCIF2_SCK	MTIOC7C
P42_3	RIIC2_SDA	RSPI2_SSL	CAN0_TX_DATARATE_EN	SCIF2_CTS#	MTIOC7D
P42_4	RIIC2_SCL	CAM_FIELD	CAN0_RX_DATARATE_EN	SCIF2_RTS#	-

Table 5-44: The multiplexed function of P43 pin.

Pin Name	Function 1	Function 2	Function 3	Function 4	Function 5
P43_0	RSPI0_CK	GTIOC4A	GTIOC6A	IRQ4	MTIOC8A
P43_1	RSPI0_MOSI	GTIOC4B	GTIOC6B	IRQ5	MTIOC8B
P43_2	RSPI0_MISO	GTIOC5A	-	IRQ6	MTIOC8C
P43_3	RSPI0_SSL	GTIOC5B	-	IRQ7	MTIOC8D

Table 5-45: The multiplexed function of P44 pin.

Pin Name	Function 1	Function 2	Function 3	Function 4	Function 5
P44_0	RSPI1_CK	SSI1_BCK	CAN1_TX	MTIOC3A	GTIOC6A
P44_1	RSPI1_MOSI	SSI1_RCK	CAN1_RX	MTIOC3B	GTIOC6B
P44_2	RSPI1_MISO	SSI1_TXD	CAN1_TX_DATARATE_EN	MTIOC3C	GTIOC7A
P44_3	RSPI1_SSL	SSI1_RXD	CAN1_RX_DATARATE_EN	MTIOC3D	GTIOC7B

Table 5-46: The multiplexed function of P45 pin.

Pin Name	Function 1	Function 2	Function 3	Function 4	Function 5
P45_0	SSI0_BCK	POE0#	SCI1_RXD	-	-
P45_1	SSI0_RCK	POE4#	SCI1_TXD	-	-
P45_2	SSI0_TXD	POE8#	SCI1_SCK	-	-
P45_3	SSI0_RXD	POE10#	SCI1_CTS#/RTS#	-	-

Table 5-47: The multiplexed function of P46 pin.

Pin Name	Function 1	Function 2	Function 3	Function 4	Function 5
P46_0	SSI1_BCK	GTETRGA	CAN1_TX	RIIC2_SDA	-
P46_1	SSI1_RCK	GTETRGB	CAN1_RX	RIIC2_SCL	-
P46_2	SSI1_TXD	GTETRGC	CAN1_TX_DATARATE_EN	RIIC3_SDA	-
P46_3	SSI1_RXD	GTETRGD	CAN1_RX_DATARATE_EN	RIIC3_SCL	-

Table 5-48: The multiplexed function of P47 pin.

Pin Name	Function 1	Function 2	Function 3	Function 4	Function 5
P47_0	SCI0_RXD	SD0_CD	IRQ0	SSI1_BCK	RSPI0_CK
P47_1	SCI0_TXD	SD0_WP	IRQ1	SSI1_RCK	RSPI0_MOSI
P47_2	SCI0_SCK	SD1_CD	IRQ2	SSI1_TXD	RSPI0_MISO
P47_3	SCI0_CTS#/RTS#	SD1_WP	IRQ3	SSI1_RXD	RSPI0_SSL

Table 5-49: The multiplexed function of P48 pin.

Pin Name	Function 1	Function 2	Function 3	Function 4	Function 5
P48_0	SCIF2_TXD	RSPI1_CK	RIIC2_SDA	MTCLKA	-
P48_1	SCIF2_RXD	RSPI1_MOSI	RIIC2_SCL	MTCLKB	-
P48_2	SCIF2_SCK	RSPI1_MISO	RIIC3_SDA	MTCLKC	-
P48_3	SCIF2_CTS#	RSPI1_SSL	RIIC3_SCL	MTCLKD	-
P48_4	SCIF2_RTS#	-	ADC_TRG	-	-

5.2 RZ/G2UL

The terminals of multiplexed function for RZ/G2UL are listed below.

The terminals that can be assigned to each peripheral function differ depending on each device. Refers user's manual for the device.

Table 5-50: The multiplexed function of P0 pin.

Pin Name	Function 1	Function 2	Function 3	Function 4	Function 5	Function 6	Function 7
P0_0	SD0_CD	-	RIIC3_SDA	MTIOC2A	SCI0_TXD	-	-
P0_1	SD0_WP	-	RIIC3_SCL	MTIOC2B	SCI0_RXD	-	-
P0_2	SD1_CD	-	MTIOC1A	RIIC2_SDA	-	-	IRQ0
P0_3	SD1_WP	-	MTIOC1B	RIIC2_SCL	-	-	IRQ1

Table 5-51: The multiplexed function of P1 pin.

Pin Name	Function 1	Function 2	Function 3	Function 4	Function 5	Function 6	Function 7
P1_0	ET0_TXC/TX_CLK	RSPI0_CK	CAN_CLK	MTIOC1A	-	-	-
P1_1	ET0_TX_CTL/TX_EN	RSPI0_MOSI	CAN0_TX	MTIOC1B	-	-	-
P1_2	ET0_TXD0	RSPI0_MISO	CAN0_RX	MTIC5U	-	-	-
P1_3	ET0_TXD1	RSPI0_SSL	CAN0_TX_DATARATE_EN	MTIC5V	-	-	-
P1_4	ET0_TXD2	-	CAN0_RX_DATARATE_EN	MTIC5W	-	-	-

Table 5-52: The multiplexed function of P2 pin.

Pin Name	Function 1	Function 2	Function 3	Function 4	Function 5	Function 6	Function 7
P2_0	ET0_TXD3	SSI0_BCK	CAN1_TX	MTCLKA	-	-	-
P2_1	ET0_TX_ERR	SSI0_RCK	CAN1_RX	MTCLKB	SCI0_SCK	RSPI0_CK	-
P2_2	ET0_TX_COL	SSI0_TXD	CAN1_TX_DATARATE_EN	MTCLKC	SCI0_TXD	RSPI0_MOSI	-
P2_3	ET0_TX_CRS	SSI0_RXD	CAN1_RX_DATARATE_EN	MTCLKD	SCI0_RXD	RSPI0_MISO	-

Table 5-53: The multiplexed function of P3 pin.

Pin Name	Function 1	Function 2	Function 3	Function 4	Function 5	Function 6	Function 7
P3_0	ET0_RXC/RX_CLK	SSI1_BCK	POE0#	MTIOC0A	-	-	-
P3_1	ET0_RX_CTL/RX_DV	SSI1_RCK	POE4#	MTIOC0B	-	-	-
P3_2	ET0_RXD0	SSI1_TXD	POE8#	MTIOC0C	-	-	-
P3_3	ET0_RXD1	SSI1_RXD	POE10#	MTIOC0D	-	-	-

Table 5-54: The multiplexed function of P4 pin.

Pin Name	Function 1	Function 2	Function 3	Function 4	Function 5	Function 6	Function 7
P4_0	ET0_RXD2	RSPI1_CK	MTIOC8A	MTIOC2A	USB1_VBUSEN	-	-
P4_1	ET0_RXD3	RSPI1_MOSI	MTIOC8B	MTIOC2B	USB1_OVRCUR	-	-
P4_2	ET0_RX_ERR	RSPI1_MISO	MTIOC8C	MTIOC3A	-	-	-
P4_3	ET0_MDC	RSPI1_SSL	MTIOC8D	MTIOC3B	-	-	-
P4_4	ET0_MDIO	-	-	MTIOC3C	-	-	-
P4_5	ET0_LINKSTA	-	-	MTIOC3D	-	-	-

Table 5-55: The multiplexed function of P5 pin.

Pin Name	Function 1	Function 2	Function 3	Function 4	Function 5	Function 6	Function 7
P5_0	USB0_VBUSEN	SCIF2_TXD	MTIOC7A	-	-	-	-
P5_1	-	SCIF2_RXD	MTIOC7B	ADC_TRG	SCI0_CTS#/RTS#	RSPI0_SSL	-
P5_2	USB0_OVRCUR	SCIF2_SCK	MTIOC7C	SSI2_BCK	-	-	-
P5_3	USB0_OTG_ID	SCIF2_CTS#	MTIOC7D	SSI2_RCK	USB1_VBUSEN	-	-
P5_4	USB0_OTG_EXICEN	SCIF2_RTS#	-	SSI2_DATA	USB1_OVRCUR	-	-

Table 5-56: The multiplexed function of P6 pin.

Pin Name	Function 1	Function 2	Function 3	Function 4	Function 5	Function 6	Function 7
P6_0	USB1_VBUSEN	RSPI2_CK	CAN_CLK	SCIF2_TXD	MTIOC7A	-	-
P6_1	USB1_OVRCUR	RSPI2_MOSI	CAN0_TX	SCIF2_RXD	MTIOC7B	-	-
P6_2	ADC_TRG	RSPI2_MISO	CAN0_RX	SCIF2_SCK	MTIOC7C	-	IRQ2
P6_3	RIIC2_SDA	RSPI2_SSL	CAN0_TX_DATARATE_EN	SCIF2_CTS#	MTIOC7D	SCIF0_RXD	IRQ3
P6_4	RIIC2_SCL	-	CAN0_RX_DATARATE_EN	SCIF2_RTS#	ADC_TRG	SCIF0_TXD	IRQ4

Table 5-57: The multiplexed function of P7 pin.

Pin Name	Function 1	Function 2	Function 3	Function 4	Function 5	Function 6	Function 7
P7_0	ET1_TXC/TX_CLK	ADC_TRG	RSPI2_CK	CAN_CLK	MTIOC0A	SCIF2_TXD	IRQ5
P7_1	ET1_TX_CTL/TX_EN	SCI1_SCK	RSPI2_MOSI	CAN0_TX	MTIOC0B	SCIF2_RXD	-
P7_2	ET1_TXD0	SCI1_TXD	RSPI2_MISO	CAN0_RX	MTIOC0C	SCIF2_SCK	-
P7_3	ET1_TXD1	SCI1_RXD	RSPI2_SSL	CAN0_TX_DATARATE_EN	MTIOC0D	SCIF2_CTS#	-
P7_4	ET1_TXD2	SCI1_CTS#/RTS#	IRQ2	CAN0_RX_DATARATE_EN	-	SCIF2_RTS#	-

Table 5-58: The multiplexed function of P8 pin.

Pin Name	Function 1	Function 2	Function 3	Function 4	Function 5	Function 6	Function 7
P8_0	ET1_TXD3	SCIF0_SCK	SCIF1_RXD	SSI1_BCK	SCI0_SCK	MTIOC7A	IRQ1
P8_1	ET1_TX_ERR	SCIF0_RXD	SCIF1_TXD	SSI1_RCK	SCI0_TXD	MTIOC7B	-
P8_2	ET1_TX_COL	SCIF0_TXD	SCIF1_CTS#	SSI1_TXD	SCI0_RXD	MTIOC7C	-
P8_3	ET1_TX_CRS	SCIF0_CTS#	SCIF1_RTS#	SSI1_RXD	SCI0_CTS#/RTS#	MTIOC7D	-
P8_4	ET1_RXC/RX_CLK	SCIF0_RTS#	-	-	-	-	-

Table 5-59: The multiplexed function of P9 pin.

Pin Name	Function 1	Function 2	Function 3	Function 4	Function 5	Function 6	Function 7
P9_0	ET1_RX_CTL/RX_DV	RSPI0_CK	-	SSI2_BCK	MTIOC4A	SCIF4_SCK	-
P9_1	ET1_RXD0	RSPI0_MOSI	-	SSI2_RCK	MTIOC4B	SCIF4_RXD	-
P9_2	ET1_RXD1	RSPI0_MISO	-	SSI2_DATA	MTIOC4C	SCIF4_TXD	-
P9_3	ET1_RXD2	RSPI0_SSL	IRQ3	-	MTIOC4D	IRQ1	-

Table 5-60: The multiplexed function of P10 pin.

Pin Name	Function 1	Function 2	Function 3	Function 4	Function 5	Function 6	Function 7
P10_0	ET1_RXD3	SSI0_BCK	IRQ4	-	MTIOC6A	IRQ2	-
P10_1	ET1_RX_ERR	SSI0_RCK	SSI3_BCK	-	MTIOC6B	-	-
P10_2	ET1_MDC	SSI0_TXD	SSI3_RCK	-	MTIOC6C	-	-
P10_3	ET1_MDIO	SSI0_RXD	SSI3_TXD	USB1_VBUSEN	MTIOC6D	-	-
P10_4	ET1_LINKSTA	ADC_TRG	SSI3_RXD	USB1_OVRCUR	-	-	-

Table 5-61: The multiplexed function of P11 pin.

Pin Name	Function 1	Function 2	Function 3	Function 4	Function 5	Function 6	Function 7
P11_0	SSI0_BCK	POE0#	SCI1_RXD	RSPI2_CK	-	DISP_HSYNC	-
P11_1	SSI0_RCK	POE4#	SCI1_TXD	RSPI2_MOSI	-	DISP_DE	-
P11_2	SSI0_TXD	POE8#	SCI1_SCK	RSPI2_MISO	-	DISP_DATA0	SCIF1_TXD
P11_3	SSI0_RXD	POE10#	SCI1_CTS#/RTS#	RSPI2_SSL	-	DISP_CLK	-

Table 5-62: The multiplexed function of P12 pin.

Pin Name	Function 1	Function 2	Function 3	Function 4	Function 5	Function 6	Function 7
P12_0	IRQ0	SCI0_RXD	-	MTIOC0A	SCIF3_TXD	DISP_VSYNC	-
P12_1	IRQ1	SCI0_TXD	-	MTIOC0B	SCIF3_RXD	DISP_DATA5	-

Table 5-63: The multiplexed function of P13 pin.

Pin Name	Function 1	Function 2	Function 3	Function 4	Function 5	Function 6	Function 7
P13_0	SCIF0_TXD	-	CAN_CLK	MTIOC4A	USB1_VBUSEN	DISP_DATA2	-
P13_1	SCIF0_RXD	-	CAN0_TX	MTIOC4B	USB1_OVRCUR	DISP_DATA1	SCIF1_RXD
P13_2	SCIF0_SCK	-	CAN0_RX	MTIOC4C	-	DISP_DATA6	-
P13_3	SCIF0_CTS#	-	CAN0_TX_DATARATE_EN	MTIOC4D	-	DISP_DATA4	-
P13_4	SCIF0_RTS#	-	CAN0_RX_DATARATE_EN	-	-	DISP_DATA3	-

Table 5-64: The multiplexed function of P14 pin.

Pin Name	Function 1	Function 2	Function 3	Function 4	Function 5	Function 6	Function 7
P14_0	SCIF1_TXD	-	CAN1_TX	MTIC5U	SCI0_RXD	DISP_DATA7	-
P14_1	SCIF1_RXD	-	CAN1_RX	MTIC5V	SCI0_TXD	DISP_DATA9	IRQ2
P14_2	SCIF1_SCK	ADC_TRG	CAN1_TX_DATARATE_EN	MTIC5W	SCI0_SCK	DISP_DATA8	IRQ3

Table 5-65: The multiplexed function of P15 pin.

Pin Name	Function 1	Function 2	Function 3	Function 4	Function 5	Function 6	Function 7
P15_0	RSPI0_CK	-	-	IRQ4	MTIOC8A	DISP_DATA11	-
P15_1	RSPI0_MOSI	-	-	IRQ5	MTIOC8B	DISP_DATA13	-
P15_2	RSPI0_MISO	-	-	IRQ6	MTIOC8C	DISP_DATA16	SCI1_TXD
P15_3	RSPI0_SSL	-	-	IRQ7	MTIOC8D	DISP_DATA14	-

Table 5-66: The multiplexed function of P16 pin.

Pin Name	Function 1	Function 2	Function 3	Function 4	Function 5	Function 6	Function 7
P16_0	SCIF1_CTS#	-	CAN1_RX_DATARATE_EN	-	SCI0_CTS#/RTS#	DISP_DATA10	-
P16_1	SCIF1_RTS#	-	-	-	-	DISP_DATA12	-

Table 5-67: The multiplexed function of P17 pin.

Pin Name	Function 1	Function 2	Function 3	Function 4	Function 5	Function 6	Function 7
P17_0	RSPI1_CK	SSI1_BCK	CAN1_TX	MTIOC3A	-	DISP_DATA17	SCI1_RXD
P17_1	RSPI1_MOSI	SSI1_RCK	CAN1_RX	MTIOC3B	-	DISP_DATA19	-
P17_2	RSPI1_MISO	SSI1_TXD	CAN1_TX_DATARATE_EN	MTIOC3C	-	DISP_DATA18	-
P17_3	RSPI1_SSL	SSI1_RXD	CAN1_RX_DATARATE_EN	MTIOC3D	-	DISP_DATA22	-

Table 5-68: The multiplexed function of P18 pin.

Pin Name	Function 1	Function 2	Function 3	Function 4	Function 5	Function 6	Function 7
P18_0	IRQ2	ADC_TRG	-	-	SCI0_SCK	DISP_DATA15	SCIF3_SCK
P18_1	IRQ3	-	-	SCIF3_SCK	SCI0_TXD	DISP_DATA20	SCIF3_RXD
P18_2	IRQ4	RSPI0_CK	SCI0_SCK	SCIF3_RXD	SCI0_RXD	DISP_DATA21	SCIF3_TXD
P18_3	IRQ5	RSPI0_MOSI	SCI0_TXD	SCIF3_TXD	SCI0_CTS#/RTS#	DISP_DATA23	SCIF4_SCK
P18_4	IRQ6	RSPI0_MISO	SCI0_RXD	USB1_VBUSEN	ADC_TRG	SCI1_TXD	SCIF4_RXD
P18_5	IRQ7	RSPI0_SSL	SCI0_CTS#/RTS#	USB1_OVRCUR	-	SCI1_RXD	SCIF4_TXD

6. Notes for using your pin_data.c with RZ/G FSP v2.0.0

From RZ/G FSP v2.0.0, we made FSP Pin Configurator support for RZ/G2L, RZ/G2LC and RZ/G2UL. By this support pin_data.c is now generated in rzg_gen, and it conflicts with your existing pin_data.c.

This chapter describes how you can continue to use your pin_data.c with RZ/G FSP v2.0.0. Also, we show how to enable FSP Pin Configurator on your project.

6.1 How to update FSP version in your project

1. Change the FSP version from v1.2.0 to 2.0.0 on BSP tab. And click “OK” when a warning message occurs.

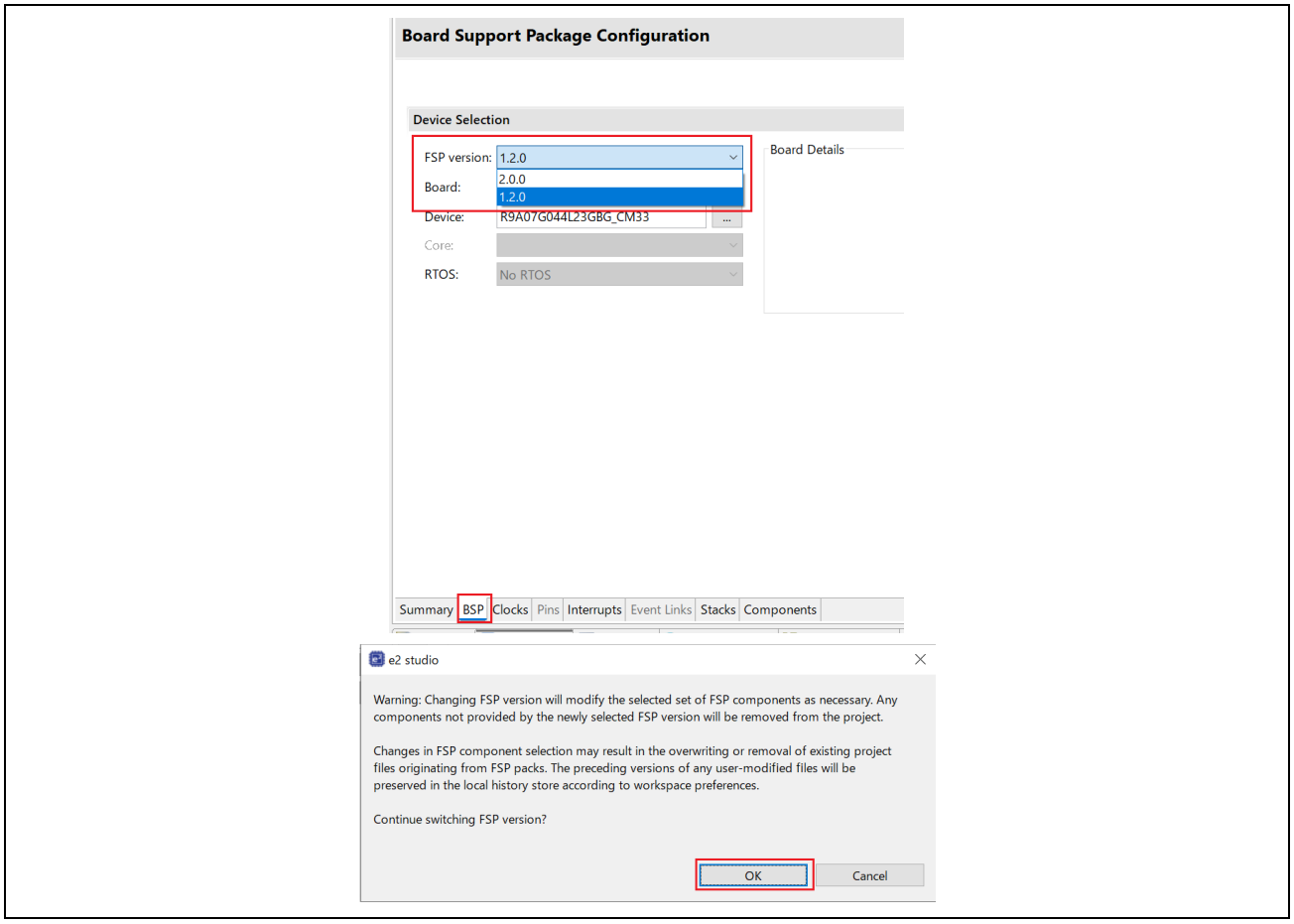


Figure 2: BSP tab

2. Click “Generate Project Content” and restart e2 studio.

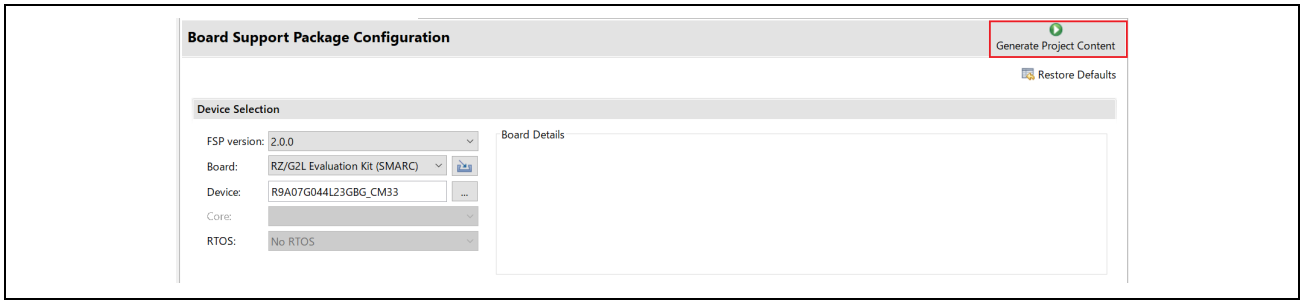


Figure 3: Generate Project Content

3. If FSP version is successfully updated, you can see 2.0.0 should be configured in BSP tab and Pins tab becomes available.

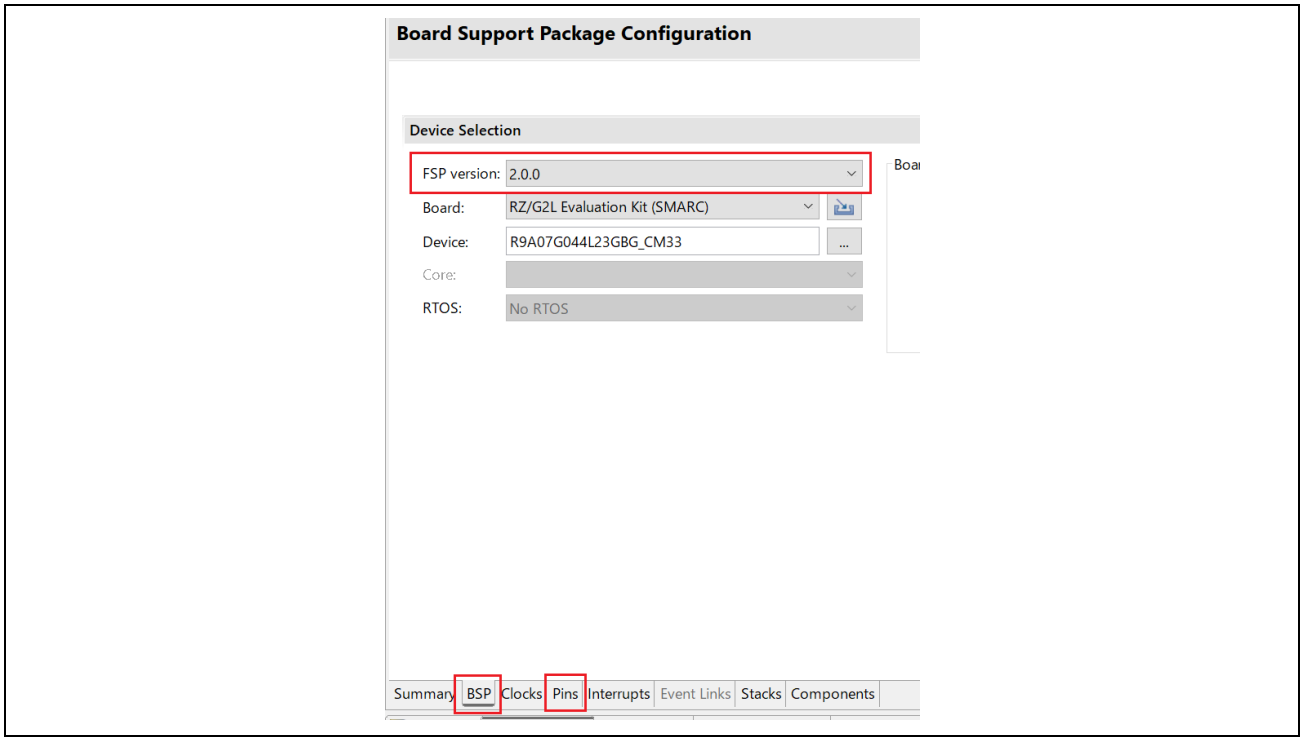


Figure 4: Confirm FSP version and Pins tab

6.2 Procedure to continue to use your pin_data.c

After updating to FSP v2.0.0, you can continue to use src/pin_data.c just like in FSP v1.2.0 by applying the follow steps.

1. Right click **rzg_gen**/pin_data.c and select "Exclude from Build…" from Resource Configurations.

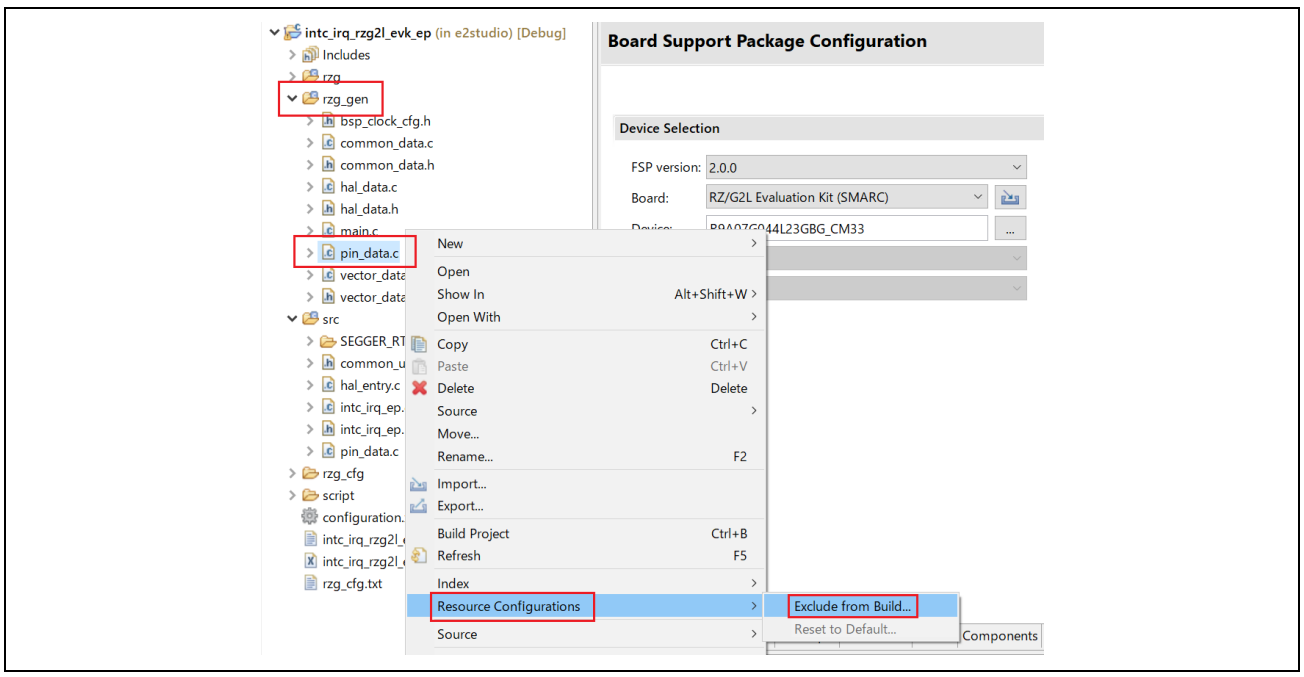


Figure 5: Resource Configurations

2. Click “Select All” and “OK” to save the Resource Configurations.

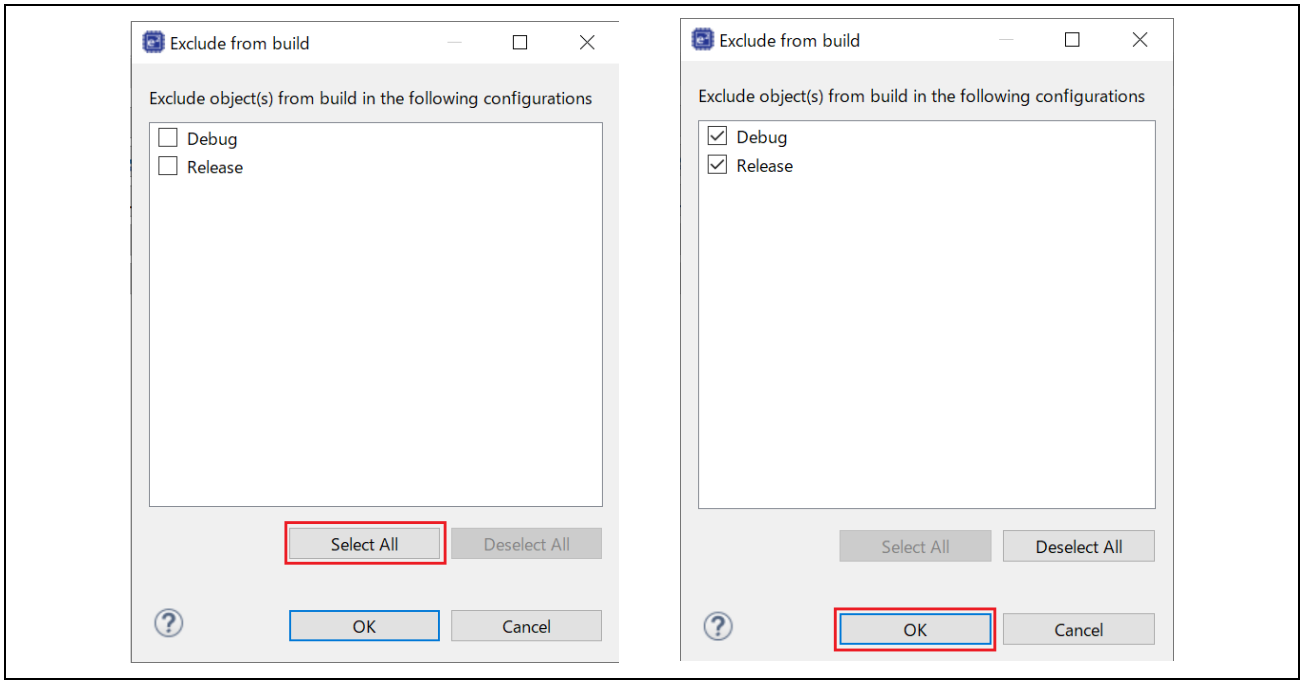


Figure 6: Exclude from build

3. Include “r_ioport.h” header file into **src**/pin_data.c.

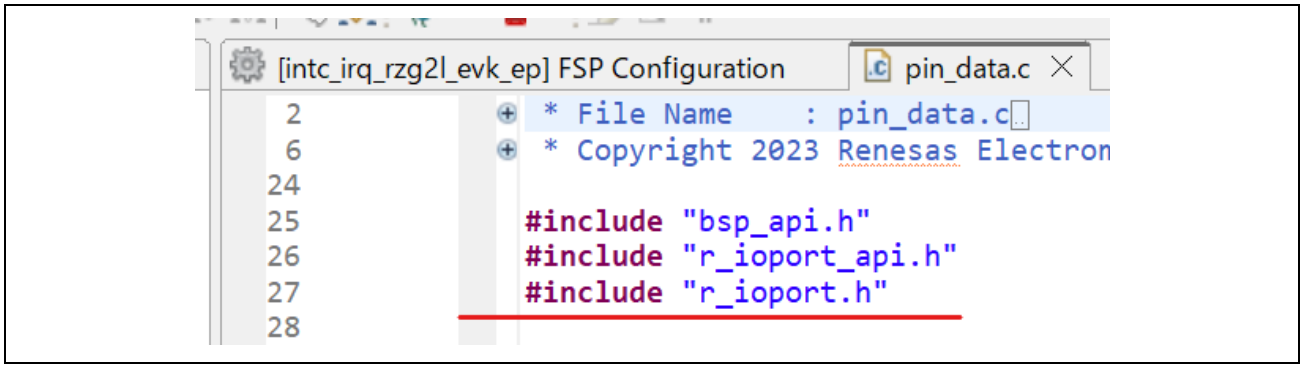


Figure 7: Include the header file

4. Here, when completing the above steps, you can build and debug the project with src/pin_data.c just like in FSP v1.2.0.

6.3 How to enable FSP Pin Configurator

If you would like to use FSP Pin Configurator on your project, please follow the procedure stated below:

1. Uncheck Common – pin_config (version 1.2.0) on Components tab.

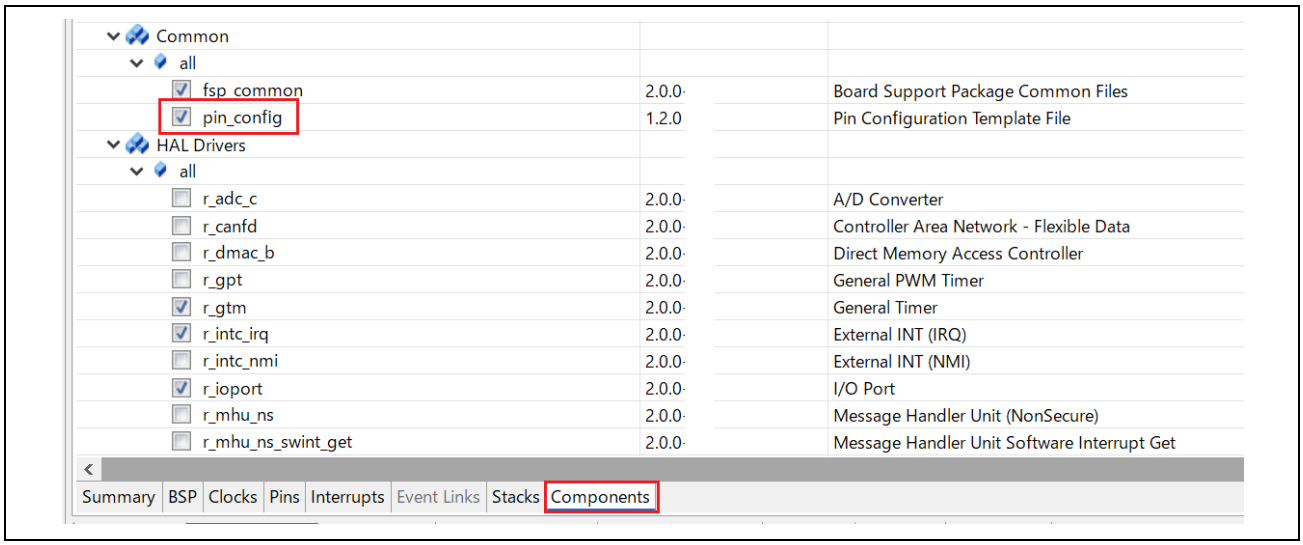


Figure 8: Uncheck pin_config

2. Right click **src**/pin_data.c and select “Exclude from Build…” from Resource Configurations.

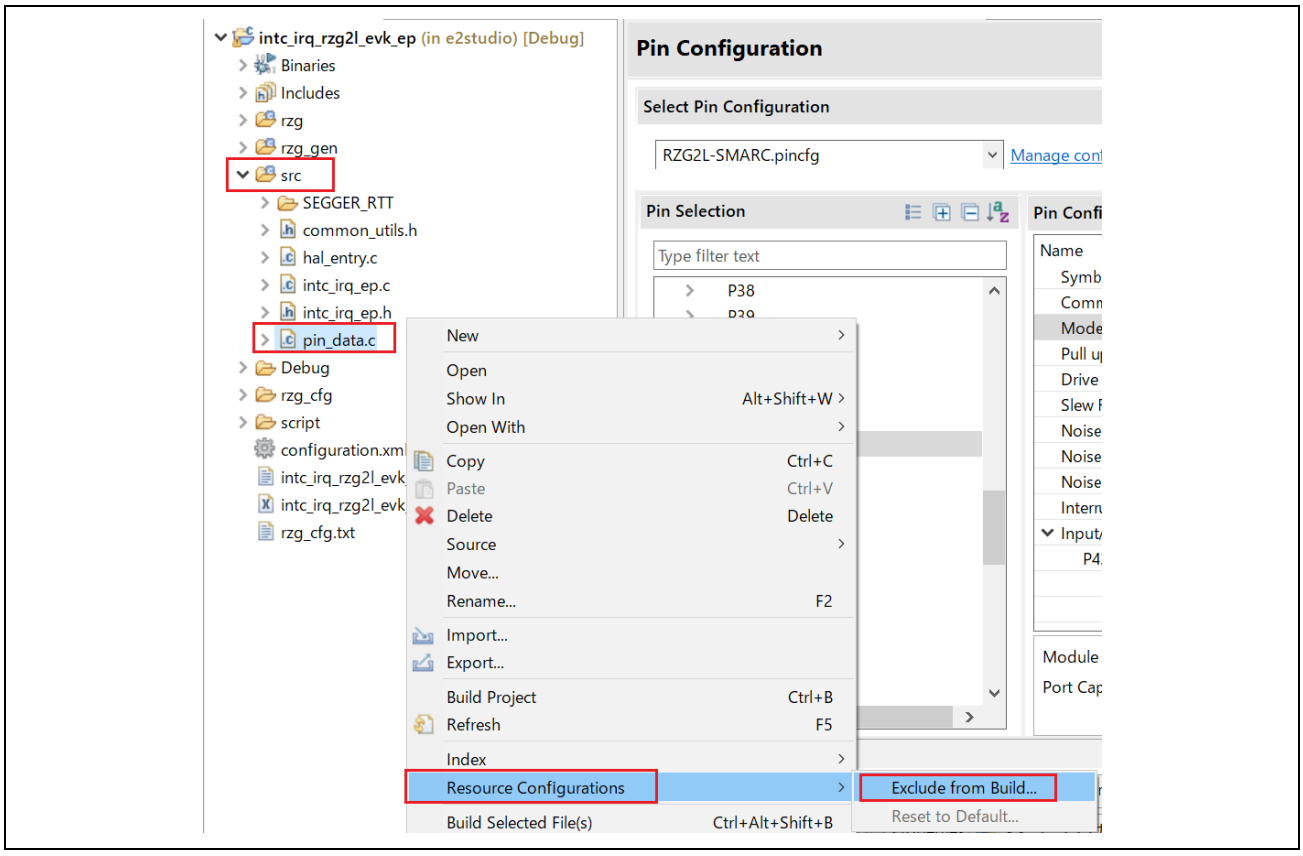


Figure 9: Resource Configurations

3. Click “Select All” and “OK” to save the Resource Configurations.

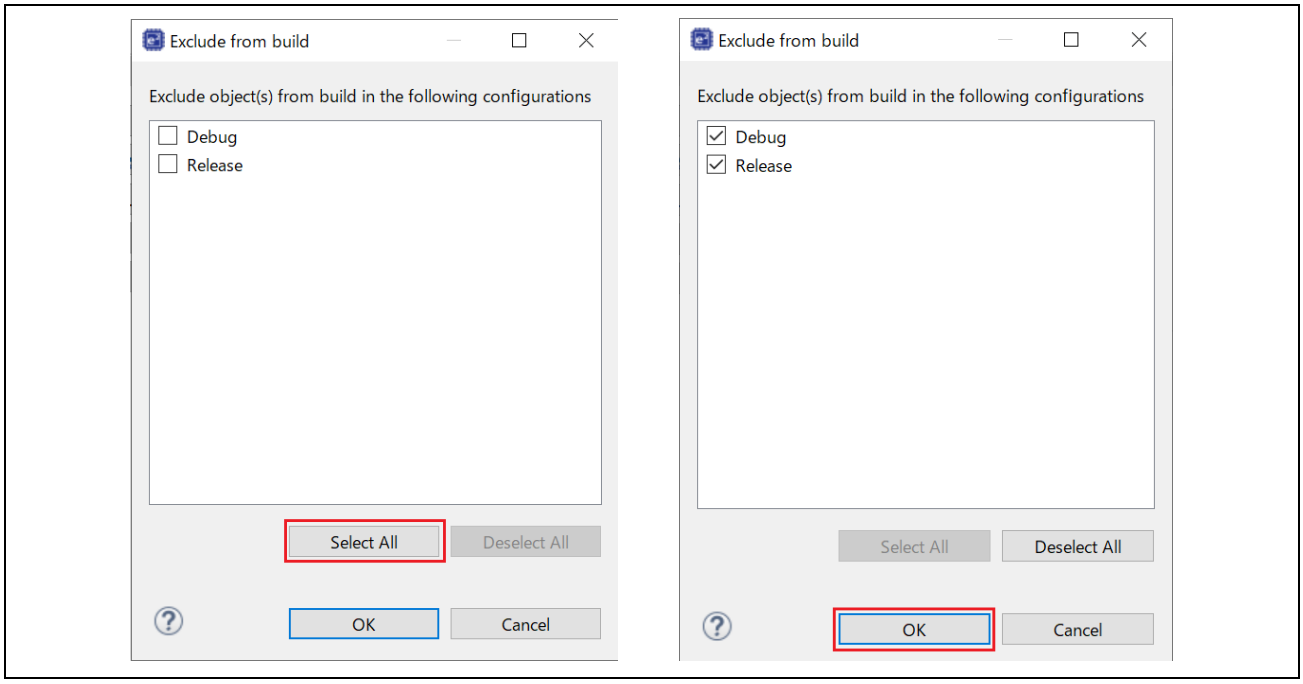


Figure 10: Exclude from build

4. Setup Pin Configuration on Pins tab by following the port setting in **src**/pin_data.c one by one. For example, peripheral function IRQ7 is assigned to P3_1 here. Select peripheral IRQ and change Operation Mode to “Custom”, then set Value for IRQ7 to P3_1.

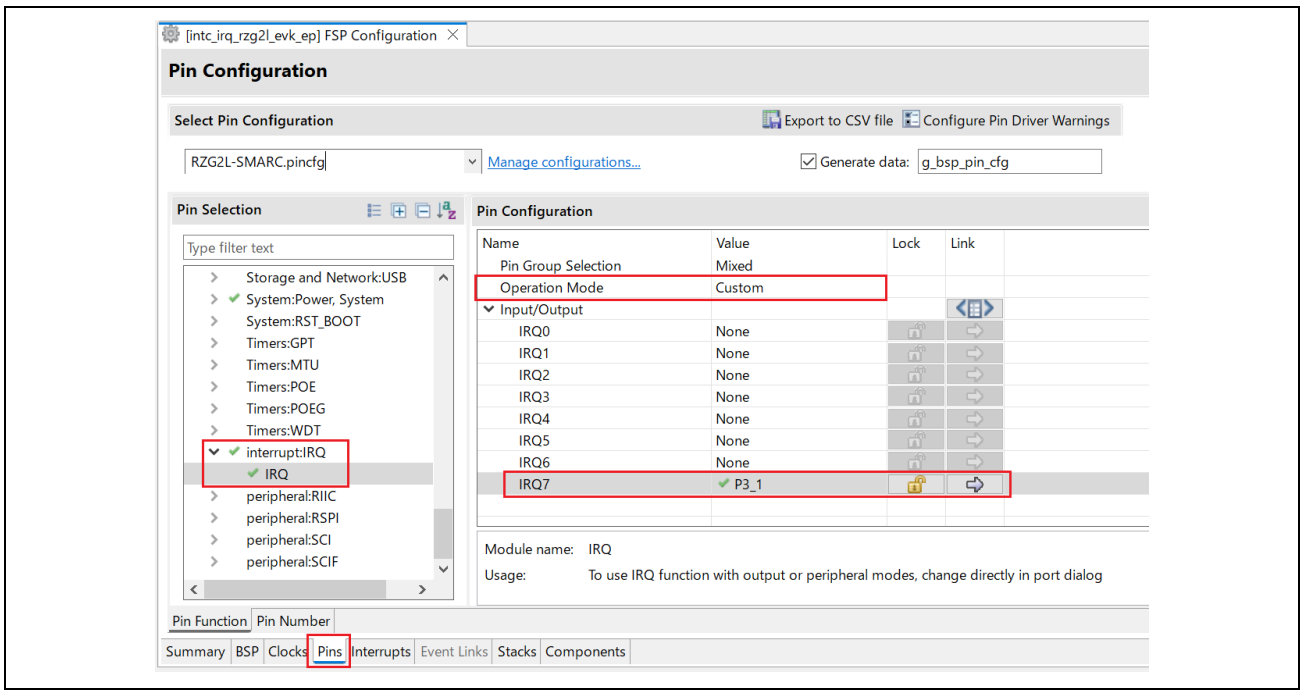


Figure 11: Setup Pin Configuration

5. When all pins setting of **src**/pin_data.c have been transferred to Pin Configuration on Pins tab, click “Generate Project Content” to generate pins setting into **rzg_gen**/pin_data.c automatically. Thereafter, please set the pin information from Pin Configuration on Pins tab.

Revision History

Rev.	Date	Description	
		Page	Summary
1.00	Jul.30.21	-	First edition issued.
1.10	Apr.27.22	6, 14 to17	Added information for RZ/G2UL.
1.20	Nov.30.22	5, 6	Corrected macro name from “IOPORT_CFG_SLEW_RATE_FLAT” to “IOPORT_CFG_SLEW_RATE_FAST”.
2.00	Jan.09.24	2, 3	Modified the description of Pins tab.
		18 to 22	Added the guide on pin_data.c when updating a project from FSP v1.2.0 or earlier version to v2.0.0.

General Precautions in the Handling of Microprocessing Unit and Microcontroller Unit Products

The following usage notes are applicable to all Microprocessing unit and Microcontroller unit products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Precaution against Electrostatic Discharge (ESD)

   A strong electrical field, when exposed to a CMOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop the generation of static electricity as much as possible, and quickly dissipate it when it occurs. Environmental control must be adequate. When it is dry, a humidifier should be used. This is recommended to avoid using insulators that can easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors must be grounded. The operator must also be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions must be taken for printed circuit boards with mounted semiconductor devices.
2. Processing at power-on

   The state of the product is undefined at the time when power is supplied. The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the time when power is supplied. In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the time when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the time when power is supplied until the power reaches the level at which resetting is specified.
3. Input of signal during power-off state

   Do not input signals or an I/O pull-up power supply while the device is powered off. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Follow the guideline for input signal during power-off state as described in your product documentation.
4. Handling of unused pins

   Handle unused pins in accordance with the directions given under handling of unused pins in the manual. The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of the LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible.
5. Clock signals

   After applying a reset, only release the reset line after the operating clock signal becomes stable. When switching the clock signal during program execution, wait until the target clock signal is stabilized. When the clock signal is generated with an external resonator or from an external oscillator during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Additionally, when switching to a clock signal produced with an external resonator or by an external oscillator while program execution is in progress, wait until the target clock signal is stable.
6. Voltage application waveform at input pin

   Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between V_{IL} (Max.) and V_{IH} (Min.) due to noise, for example, the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between V_{IL} (Max.) and V_{IH} (Min.).
7. Prohibition of access to reserved addresses

   Access to reserved addresses is prohibited. The reserved addresses are provided for possible future expansion of functions. Do not access these addresses as the correct operation of the LSI is not guaranteed.
8. Differences between products

   Before changing from one product to another, for example to a product with a different part number, confirm that the change will not lead to problems. The characteristics of a microprocessing unit or microcontroller unit products in the same group but having a different part number might differ in terms of internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

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