RX21A Group

ΔΣ A/D Converter User's Guide

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Abstract

This application note describes the features and usage of the ΔΣ A/D converter module of RX21A Group microcontrollers.

Products

RX21A Group

When using this application note with other Renesas MCUs, careful evaluation is recommended after making modifications to comply with the alternate MCU.

Contents

1. Conversion Methods of A/D Converters

1.1 Comparison of Successive Approximation and ΔΣ Modulation

Table 1.1 shows a comparison of the conversion methods of A/D converters typically incorporated in microcontrollers. The biggest feature of ΔΣ A/D converters is their high resolution. Higher resolution allows more precise measurement of analog signals with a wide dynamic range (a high ratio between the maximum and minimum voltages of the signal being measured). In addition, ΔΣ A/D converters are relatively unaffected by noise and basically do not require mounting of additional devices at the input pins, which contributes to a smaller mounting area and reduced cost. However, ΔΣ A/D converters are inferior to successive approximation A/D converters in terms of conversion time and power consumption.

Table 1.1 Conversion Methods of A/D Converters Incorporated in Microcontrollers

Item	Successive Approximation	ΔΣ Modulation
Resolution	Low	High
Noise tolerance	Poor	Good
External filter	Required	Basically not necessary
Missing codes	Yes	No
Error correction of conversion data	Difficult	Easy
Minimum conversion time	Fast	Slow
Power consumption	Low	High
Frequency band	The maximum frequency band is dependent on the minimum conversion time. There is no lower limit.	Dependent on digital filter.

1.2 Features of Successive Approximation

- The conversion speed is fast. Can be implemented cheaply if the resolution is low.
- Very susceptible to sudden noise, so noise processing such as averaging is necessary. This increases the software requirements.
- For a resolution of n bits, a total of 2n passive components is required. This requires a larger area when implemented on silicon, and inconsistency in fabrication places limits on the precision that can be achieved. Successive approximation conversion is thus not suitable for high-resolution applications.
- The successive approximation A/D converters integrated into microcontrollers typically have a resolution of 10 or 12 bits.

1.3 Successive Approximation Conversion Method

In successive approximation the voltage being measured is compared to a variable reference voltage (which is generated by a D/A converter). It operates in the following manner:

1. The D/A converter output is used as the center value, and the analog voltage to be measured is compared to it.
2. If the result of the comparison is that the analog voltage is higher than the center value, the D/A converter output is set to a new value in the center of the range above the previous center value. If the analog voltage is lower than the center value, a new value in the center of the range below the previous center value is set. Then the comparison is repeated.
3. The above is repeated n times (for a resolution of n bits) before measurement is complete.

Successive approximation is like an algorithm with a binary tree structure. It works by searching for the voltage closest to that of the signal being measured.

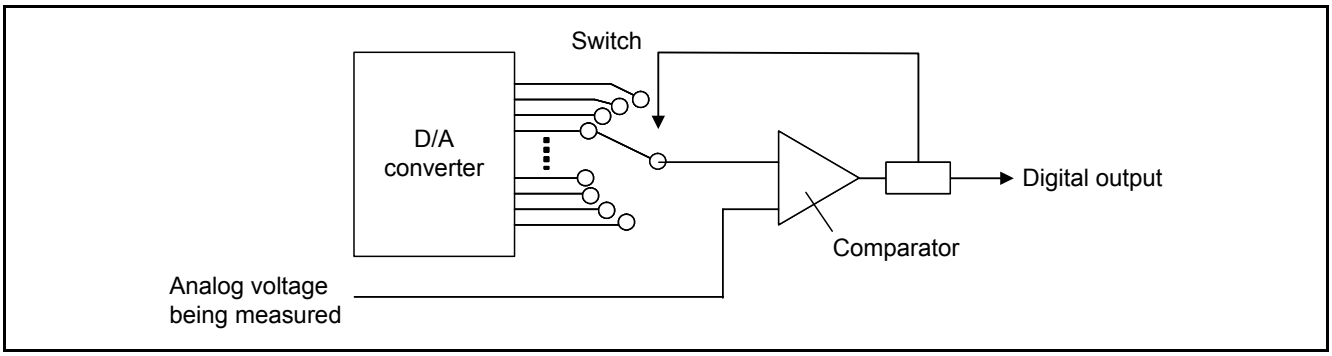


Figure 1.1 Internal Structure of Successive Approximation A/D Converter

1.4 Features of ΔΣ Modulation

- The conversion speed is slower than that of successive approximation. This is because noise processing (digital filtering) is performed in hardware, which contributes to improved noise tolerance and resolution.
- The size of the converter module is comparatively small relative to the resolution, making it possible to achieve high resolution in a smaller area when integrated into devices such as microcontrollers.
- The ΔΣ A/D converters integrated into microcontrollers typically have a resolution of 16 or 24 bits.

1.5 ΔΣ Modulation Conversion Method

In ΔΣ conversion the voltage being measured is converted to a digital value by sampling and integration, using a fixed reference voltage for comparison. A ΔΣ A/D converter comprises a ΔΣ modulator and a decimation filter (digital filter).

The ΔΣ modulator operates in the following manner:

1. The output from a 1-bit D/A converter is subtracted from the analog voltage to be measured, and the result is integrated by an integrator.
2. The comparison voltage and the integrator output are compared, and the result is output as 1-bit A/D conversion data.
3. The 1-bit D/A output is determined by the comparator output.

The decimation filter processes K units of data output by the ΔΣ modulator and produces output at the sampling frequency.

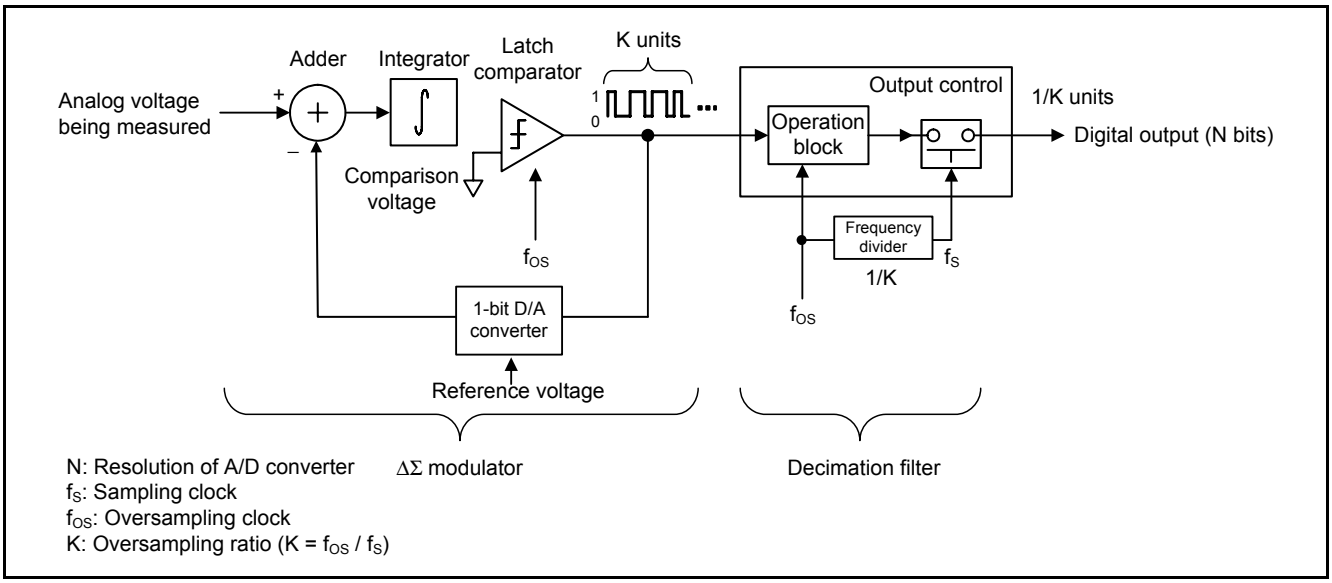


Figure 1.2 Internal Structure of ΔΣ A/D Converter

1.6 Outline of A/D Conversion by ΔΣ A/D Converter

Figure 1.3 is a block diagram of a ΔΣ A/D converter. As described in 1.5, ΔΣ Modulation Conversion Method, the ΔΣ A/D converter comprises a ΔΣ modulator and a decimation filter (digital filter).

The ΔΣ modulator converts the analog input to 1-bit digital values (a bit stream) that are output at the oversampling frequency.

The decimation filter processes the oversampled data by sub-sampling (decimation). This enables A/D conversion data to be obtained for each sampling period.

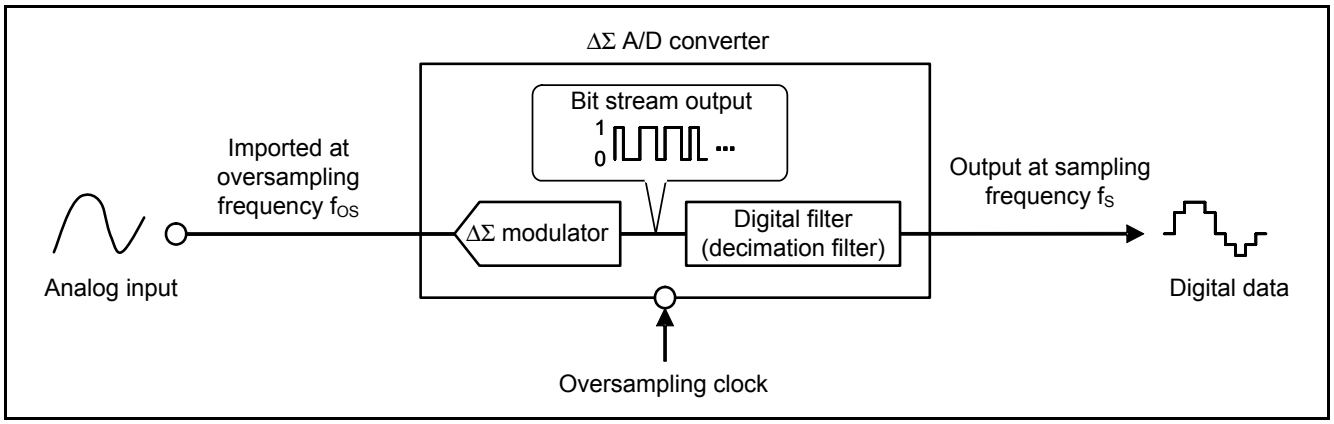


Figure 1.3 ΔΣ A/D Converter Block Diagram

(1) Oversampling

Oversampling consists of fetching data at a frequency higher than the normal sampling frequency.

Figure 1.4 shows an outline of oversampling. Usually, the A/D conversion data is output at the sampling frequency (f_S), but with oversampling A/D conversion is performed at a frequency (f_{OS}) that is higher than the sampling frequency. Generally, f_{OS} is called the oversampling frequency. The ratio of the oversampling frequency to the sampling frequency (f_{OS} / f_S) is called the oversampling ratio.

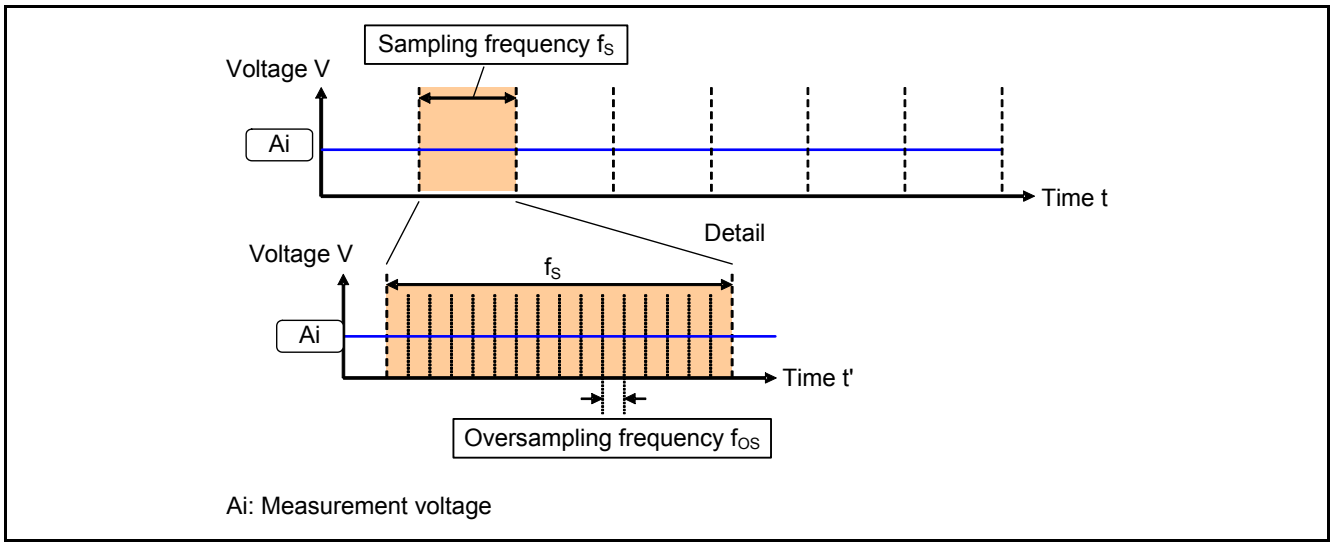


Figure 1.4 Outline of Oversampling

Figure 1.5 illustrates A/D conversion by the ΔΣ modulator. The measurement of direct current (DC) voltage is described in this example. The variables are Ai, the analog input voltage to be measured, Vf, the integral value of Ai, Vcomp, the comparison voltage (with an initial value of 0 V), Vref, the reference voltage, SC, the oversampling clock, and Dq, the comparison result.

Operations (a), (b), and (c), which occur each time SC elapses, are defined as follows:

(a) If Vf ≥ Vcomp, set Dq to 1 and add Vref to Vcomp.
(b) If Vf < Vcomp, set Dq to 0.
(c) Add Ai to Vf.

By performing operations (a), (b), and (c), the ΔΣ modulator obtains K instances of Dq within the f_S period. Dq is A/D conversion data, but each instance only contains 1 bit of information. Through processing by the decimation filter in the next stage this data is turned into high-resolution A/D conversion data.

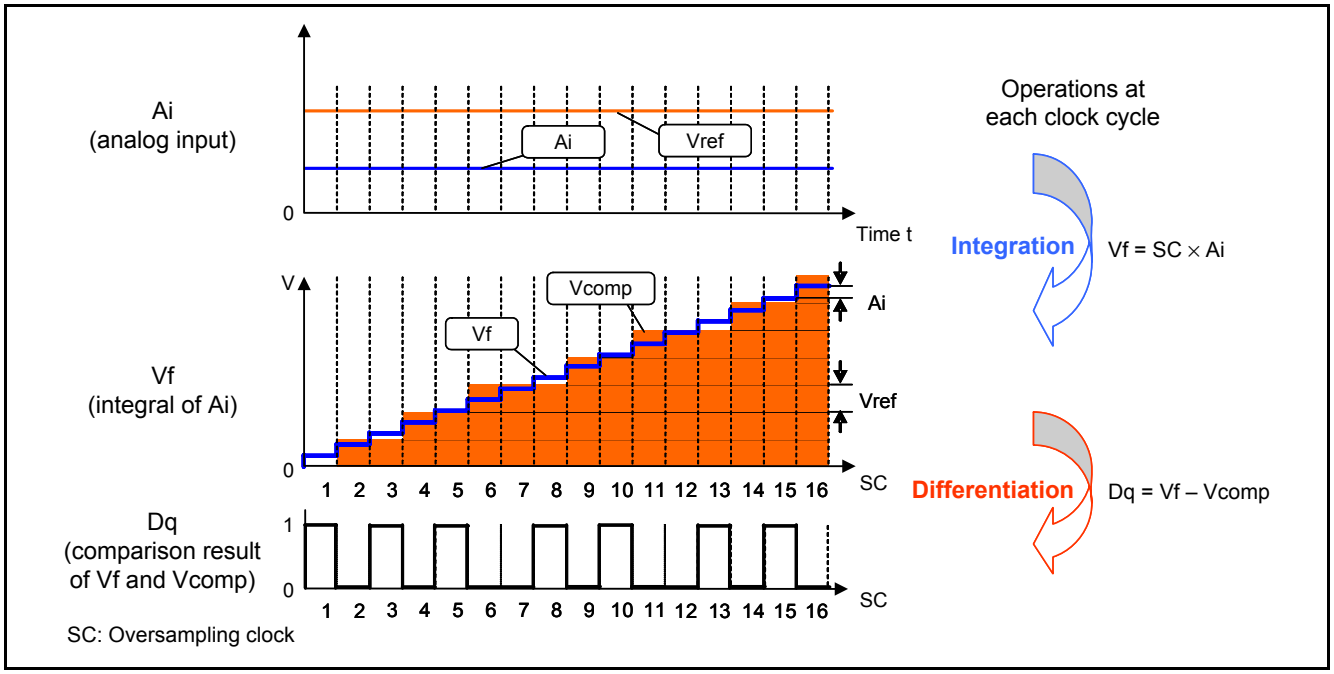


Figure 1.5 A/D Conversion by ΔΣ Modulator

(2) Decimation Filter (Digital Filter)

Figure 1.6 illustrates the processing performed by the decimation filter. The decimation filter processes the n units of Dq that have been obtained by oversampling within one cycle of the sampling frequency. This processing involves averaging the data stream consisting of n bits and multiplying the result by the A/D converter's maximum digital value (FS) to obtain Do. The decimation filter outputs this result once each sampling period.

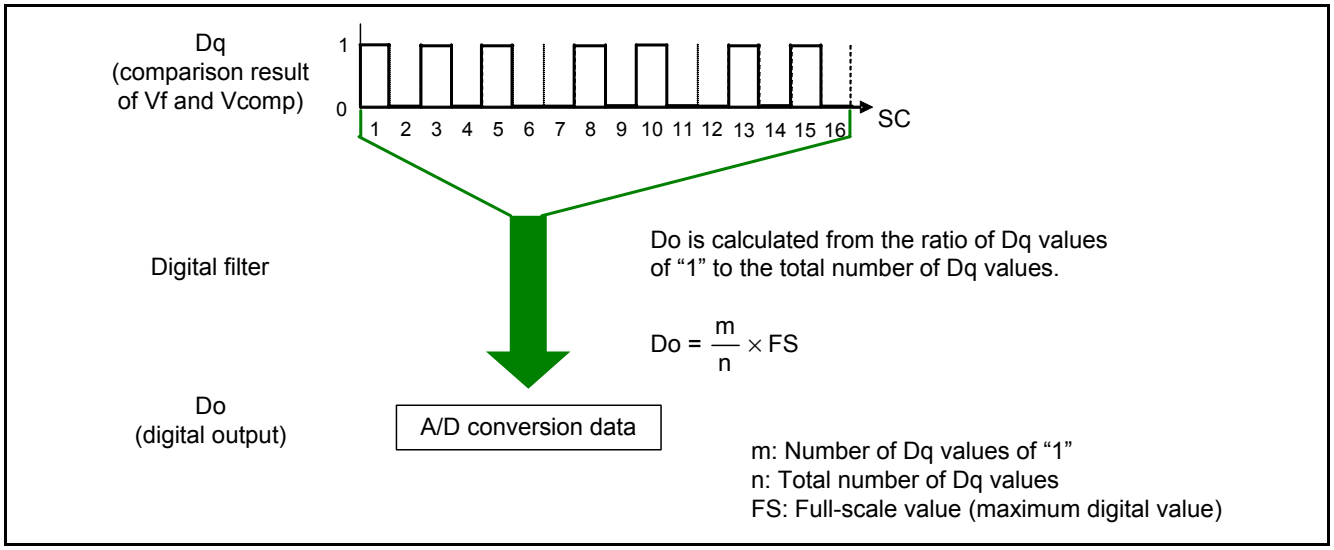


Figure 1.6 Processing by Digital Filter

2. Description of RX21A Group ΔΣ A/D Converter Function

The RX21A Group has an on-chip 24-bit A/D converter module that employs ΔΣ modulation to convert analog inputs from up to seven channels to digital values. Four of the seven channels support differential input and the remaining three channels support single-ended input. The initial stage of the A/D converter is equipped with a programmable gain amplifier (PGA) for amplifying the signal, and the gain can be set at up to 64 times for differential input and up to four times for single-ended input.

One PGA and ΔΣ A/D converter unit is allocated to each channel, so each channel is independent and controlled at a separate timing. An interrupt request can be generated for each channel at the completion of conversion. However, the clock supplied to the ΔΣ A/D converter module is common to all the channels. The A/D conversion clock frequency is 25 MHz. In addition, data register overwrite interrupt requests for all the channels are shared and operate as a single interrupt request.

The RX21A Group has an on-chip band gap reference (BGR) circuit. The reference voltage is generated based either on the BGR voltage or on the voltage applied externally to the BGR_BO pin.

Another feature is the ability to perform A/D conversion by applying input directly to the ΔΣ modulator. This enables evaluation of the characteristics of the individual ΔΣ modulator units. Use of the on-chip D/A converter allows evaluation of characteristics using the chip alone.

Table 2.1 outlines the functions of the ΔΣ A/D converter module.

Table 2.1 Outline of Functions of RX21A Group ΔΣ A/D Converter

Item	Description
Number of units	Max. 7 units
Input channels	• Max. 7 channels • Differential: 4 channels (ANDS0P/ ANDS0N, ANDS1P/ ANDS1N, ANDS2P/ ANDS2N, ANDS3P/ ANDS3N) • Single-ended: 3 channels (ANDS4, ANDS5, ANDS6)
A/D conversion method	2nd order ΔΣ modulation
Resolution	24 bits
Min. conversion time	81.92 µs (A/D conversion clock: DSADCLK = 25 MHz)
Gain	ANDS0P to ANDS3P, ANDS0N to ANDS3N: ×1, ×2, ×4, ×8, ×16, ×32, ×64 ANDS4 to ANDS6: ×1, ×2, ×4
A/D conversion clock	Supported frequency division ratio settings for peripheral module clock PCLKB*[1] and A/D conversion clock DSADCLK[1] are as follows: PCLK : DSADCLK frequency division ratio = N : 1 (N: 1, 2, 4, 8, 16, or 32) DSADCLK = 25 MHz (fixed)
Oversampling frequency	3.125 MHz (DSADCLK divided by 8)
Data registers	Conversion results have upper bits extended and are stored as signed 32-bit data.
A/D conversion start condition	Occurrence of event set by the event link controller (ELC). Events can be specified independently for each channel.
Reference voltage	Generated based on the on-chip BGR output voltage or voltage externally applied to BGR_BO pin.
Interrupt source	• An interrupt request (DSADI0 to DSADI6) is generated for each channel at the completion of A/D conversion, and the DMA controller (DMAC) or data transfer controller (DTC) can be activated by any of these interrupts. • A data register overwrite interrupt request (DSADORI) is generated when a conversion result overwrites the previous conversion result in a data register before the latter has been read.
Low power consumption function	• Enables the module stop state and stops supply of the clock. • Can be set to activate or stop the on-chip BGR and the PGA, and the ΔΣ modulator for each channel independently.
Operating modes	• Normal conversion: A/D conversion of input from the analog input pins • Single ΔΣ modulator conversion: A/D conversion of input from the on-chip D/A converter to the ΔΣ modulator

Note: 1. The frequency of peripheral module clock PCLKB is set by bits PCKB[3:0] in SCKCR, and the frequency of the A/D conversion clock ADCLK is set by bits PCLKC[3:0] in SCKCR.

Figure 2.1 is a block diagram of the ΔΣ A/D converter. The ΔΣ A/D converter of the RX21A Group uses the voltage between the VREFDSH and VREFDSL pins as the reference voltage when converting the analog input voltage to a digital value. The ΔΣ A/D converter comprises ΔΣ modulators, decimation filters (digital filters), and their associated control circuits.

The analog input signal is sampled at the oversampling frequency (A/D conversion clock divided by 8, operation guaranteed at 3.125 MHz) and converted into a digital signal by the ΔΣ modulator. This digital signal is processed by the decimation filter in the next stage, and the output of this filter is stored in a ΔΣ A/D data register.

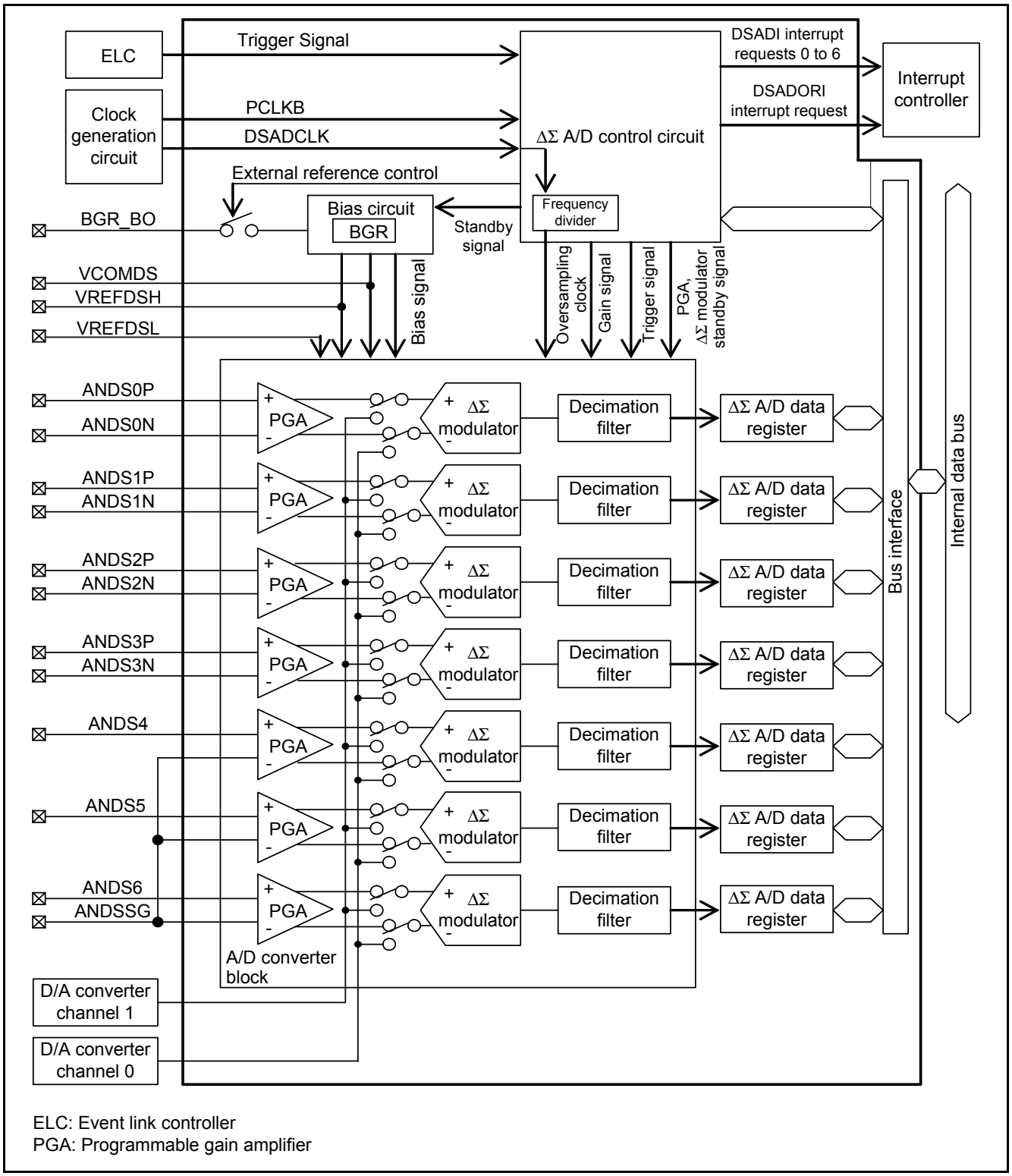


Figure 2.1 Block Diagram of RX21A Group ΔΣ A/D Converter

Table 2.2 lists the pins of the ΔΣ A/D converter.

Table 2.2 Pins of ΔΣ A/D Converter

Pin Name	I/O	Function
ANDS0P, ANDS0N	Input	Analog input, channel 0, differential input
ANDS1P, ANDS1N	Input	Analog input, channel 1, differential input
ANDS2P, ANDS2N	Input	Analog input, channel 2, differential input
ANDS3P, ANDS3N	Input	Analog input, channel 3, differential input
ANDS4	Input	Analog input, channel 4, single-ended input
ANDS5	Input	Analog input, channel 5, single-ended input
ANDS6	Input	Analog input, channel 6, single-ended input
VREFDSH	—	Reference voltage, high side; connects to analog ground via 1 μF capacitor.
VREFDSL	Input	Reference voltage, low side; connects to analog ground.
VCOMDS	—	Common mode voltage; connects to analog ground via 0.1 μF capacitor.
AVCCA	Input	Analog power supply
AVSSA	Input	Analog ground
ANDSSG	Input	Connects to signal ground (signal source ground).
BGR_BO	Input	Pin to which external reference voltage is applied; Hi-z (high impedance) when on-chip BGR selected as reference voltage.

2.1 Description of Basic Operation

2.1.1 A/D Conversion Trigger Signal

Figure 2.2 shows the A/D conversion trigger signal sequence. The RX21A Group's ΔΣ A/D converter uses event signals from a peripheral module linked via the ELC as the triggers for A/D conversion. The peripheral module uses a timer function (MTU2a, CMT, or TMR) to output events cyclically. The timer function is linked to the ΔΣ A/D converter via the ELC, allowing A/D conversion to start in synchronization with the generation of events and without taking over the CPU. This makes for effective utilization of resources. For details on the ELC and each of the timer functions, see RX21A Group User's Manual: Hardware.

A single event signal can be assigned to multiple ΔΣ A/D converter units, up to a maximum of seven, for simultaneous conversion timing. Alternately, separate event signals can be assigned to the various units, enabling A/D conversion on independent timings.

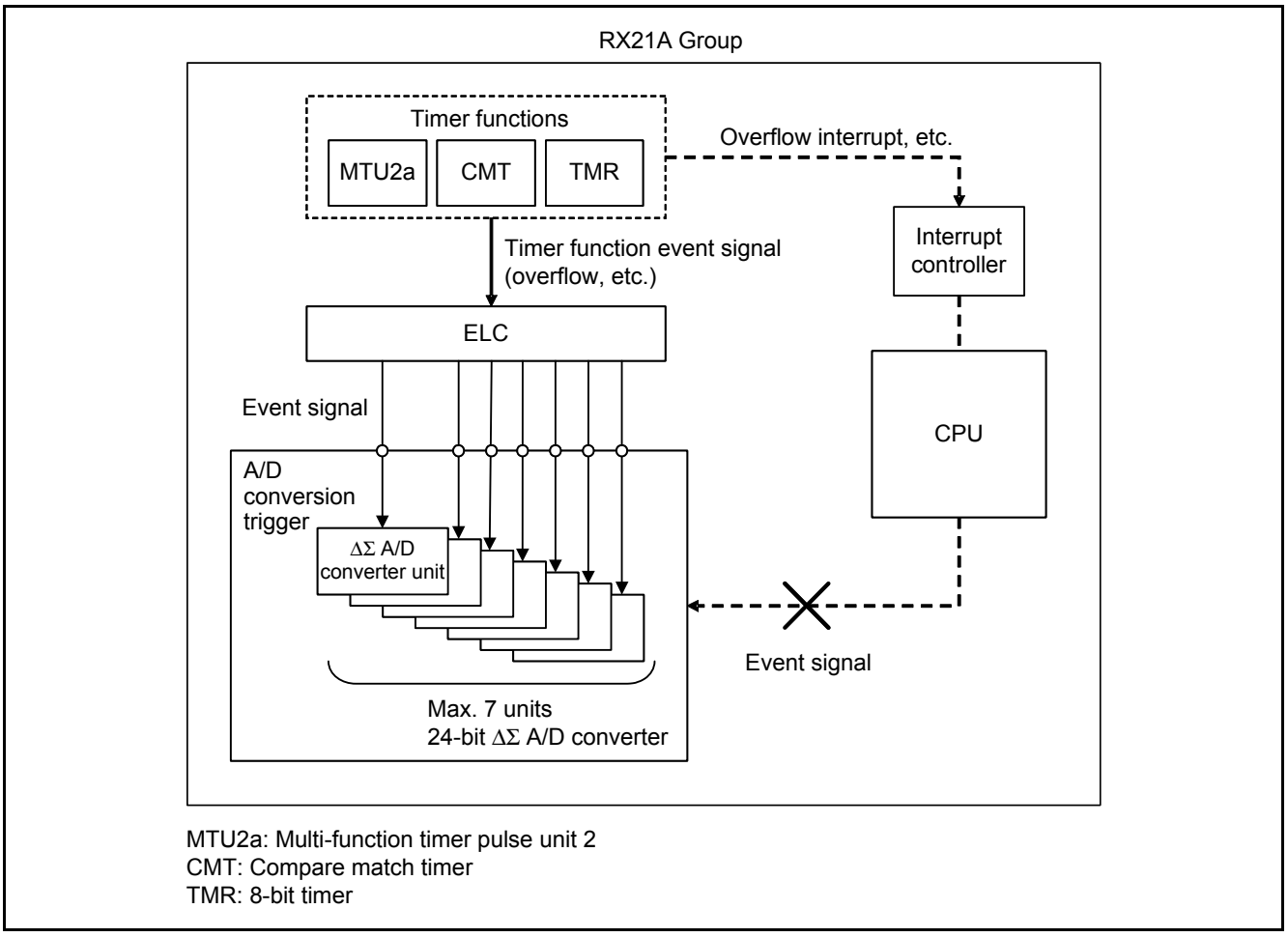
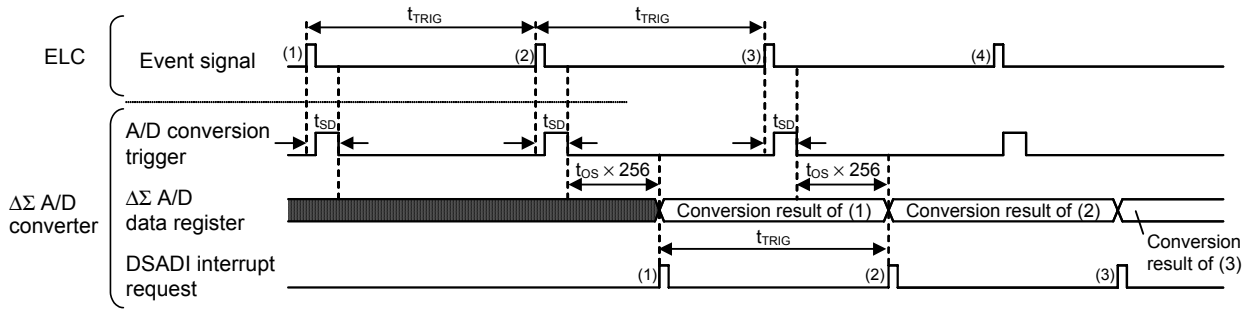


Figure 2.2 A/D Conversion Trigger Signal Sequence

2.1.2 A/D Converter Operation Timing

Figure 2.3 shows an example of A/D converter operation for a single channel.



t_{TRIG}: A/D conversion trigger period
t_{OS}: 1-cycle period of oversampling clock
t_{SD}: Conversion start delay time

Figure 2.3 Timing Chart

Description of Operation

1. Event signal (1), which is linked to the ΔΣ A/D converter via the ELC, operates as the A/D conversion trigger of the ΔΣ A/D converter.
2. After the conversion start delay time (t_{SD}) elapses, the A/D conversion trigger is recognized and A/D conversion (1) starts.
3. After the A/D conversion trigger period (t_{TRIG}) elapses following application of event signal (1), event signal (2) is applied, and after a period of t_{SD} + ($t_{OS} \times 256$) elapses, processing by the decimation filter finishes and the A/D conversion data from (1) is transferred to the ΔΣ A/D data register (DSADDRn, n = 0 to 6). Simultaneously, the second A/D conversion, associated with event signal (2), starts.
4. If the ADIE bit in the ΔΣ A/D control/status register (DSADCSRn, n = 0 to 6) is set to 1, a DSADI interrupt request is generated at the same time the conversion result is transferred to the ΔΣ A/D data register.

Thus, two event signals must be applied within the t_{TRIG} interval in order for the RX21A Group's ΔΣ A/D converter to perform a single A/D conversion. In addition, control of A/D conversion and A/D conversion end interrupt requests is performed each time an event signal is applied.

A/D conversion time is the total of the synchronous timing t_{SD}, the A/D conversion trigger period t_{TRIG}, and the decimation filter operation period of $t_{OS} \times 256$, as shown in the following expression:

$$\text{A/D conversion time} = t_{SD} + t_{TRIG} + t_{OS} \times 256$$

The duration from the start of event signal application to the output of the first A/D conversion result can be calculated with the above expression. The second and subsequent A/D conversion results are output at intervals of t_{TRIG}.

2.1.3 Notes on A/D Conversion Trigger Setting

The operation of the decimation filter requires 256 or more t_{OS} cycles, so t_{TRIG} should be set to a duration such that $t_{OS} \times 256 \leq t_{TRIG} \leq t_{OS} \times 768$, and the value should be an integral multiple of t_{OS}.

The synchronization timing of the event signals from the ELC, which operates on the peripheral module clock (PCLKB), and the oversampling frequency (DSADCLK / 8) determines t_{SD}. Thus, t_{SD} differs depending on the ratio between the two clock frequencies. For details of the allowable range for tSD, see the Electrical Characteristics section in RX21A Group User's Manual: Hardware.

Using a peripheral function that generates asynchronous event signals, such as port input, as the A/D conversion trigger can lead to errors in the A/D conversion trigger synchronization timing t_{SD} or decimation filter processing duration. This could have an adverse effect on the A/D conversion data, so such settings should not be used. Use a peripheral function capable of producing event signals at regular intervals as the A/D conversion trigger. Note that it is not possible to specify multiple event signals for a single channel. For details of the ELC registers and event signal settings, see RX21A Group User's Manual: Hardware.

2.1.4 Output Format of A/D Conversion Data

The A/D conversion data is the maximum value when the analog input voltage equals the reference voltage. Generally, the digital value corresponding to the analog input voltage can be obtained by multiplying the full-scale (FS) value of the A/D converter by the ratio of the analog input voltage to the reference voltage, as shown in the following expression:

A/D conversion value = analog input voltage / reference voltage × FS value of A/D converter

Figure 2.4 illustrates the relationship between the analog input and the digital output on the RX21A Group. The ΔΣ A/D data register value is stored as a two's complement. Under the conditions $t_{TRIG} = (t_{OS} \times 256)$ and a gain multiplier of 1, the highest-order bit of the 24-bit data is assigned as the sign bit indicating positive or negative, and the remaining 23 bits are assigned to the A/D conversion data.

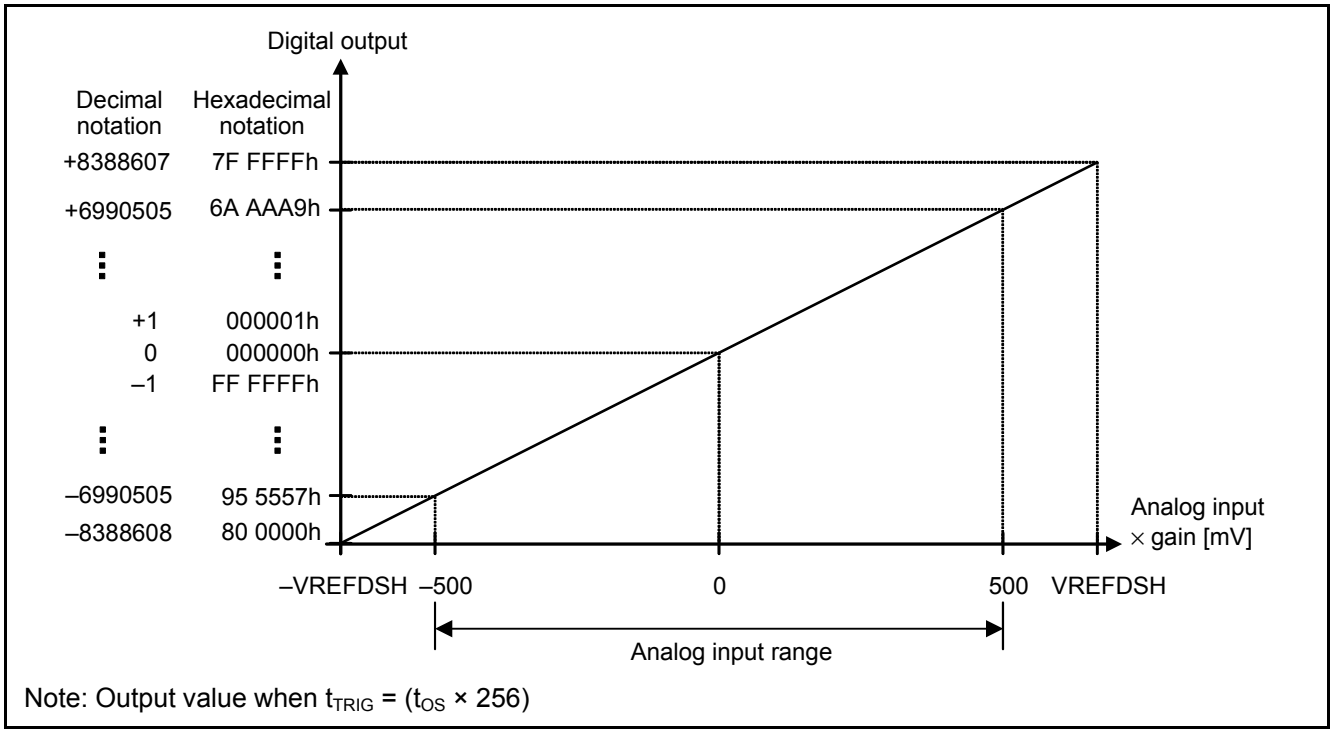


Figure 2.4 Relationship between Analog Input and Digital Output

The analog input range within which the conversion accuracy of the RX21A Group's ΔΣ A/D converter can be guaranteed is as follows:

$$-500\ \text{mV} \leq \text{analog input voltage} \times \text{gain} \leq 500\ \text{mV}$$

This is due to the offset error and full-scale error characteristics of the ΔΣ A/D converter. For more information on offset and full-scale error, see 4.2, Correction of Offset and Full-Scale Error. In addition, the analog input range varies according to the specified gain. Refer to the Electrical Characteristics section in RX21A Group User's Manual: Hardware, and use an analog signal within the range defined by these restrictions.

Reference: The analog input range of the RX21A Group's ΔΣ A/D converter is determined by the gain and the VREFDSH voltage. The maximum input must be within the following range:

$$-\text{VREFDSH} \leq \text{analog input voltage} \times \text{gain} \leq \text{VREFDSH}$$

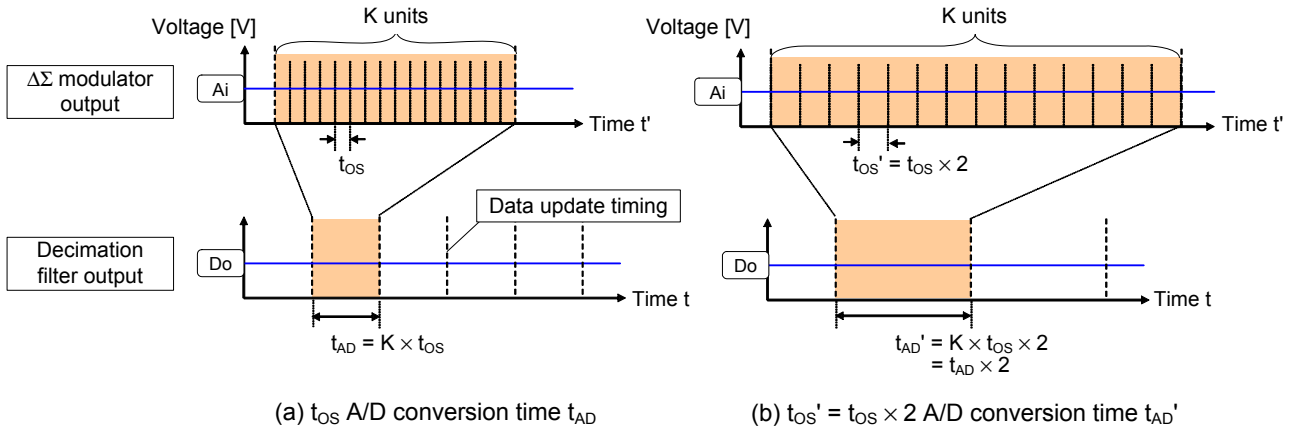
The output range of digital values is 00 0000h to 7F FFFFh (0 to + 8388607 in decimal notation) for positive voltages and FF FFFFh to 80 0000h (–1 to –8388608 in decimal notation) for negative voltages. Note that A/D conversion results are not guaranteed when the analog input is outside the voltage range defined by these restrictions.

2.1.5 A/D Conversion Time and Data Size

Generally, the ΔΣ A/D converter's A/D conversion time (t_{AD}) is determined by the 1-cycle period of the oversampling frequency (f_{OS}) ($t_{OS} = 1 / f_{OS}$) and the oversampling ratio (K), as shown in the following expression:

$$t_{AD} = K / f_{OS} = K \times t_{OS}$$

Thus, to change the A/D conversion time one adjusts the oversampling frequency or the oversampling ratio, as shown in figure 2.5.



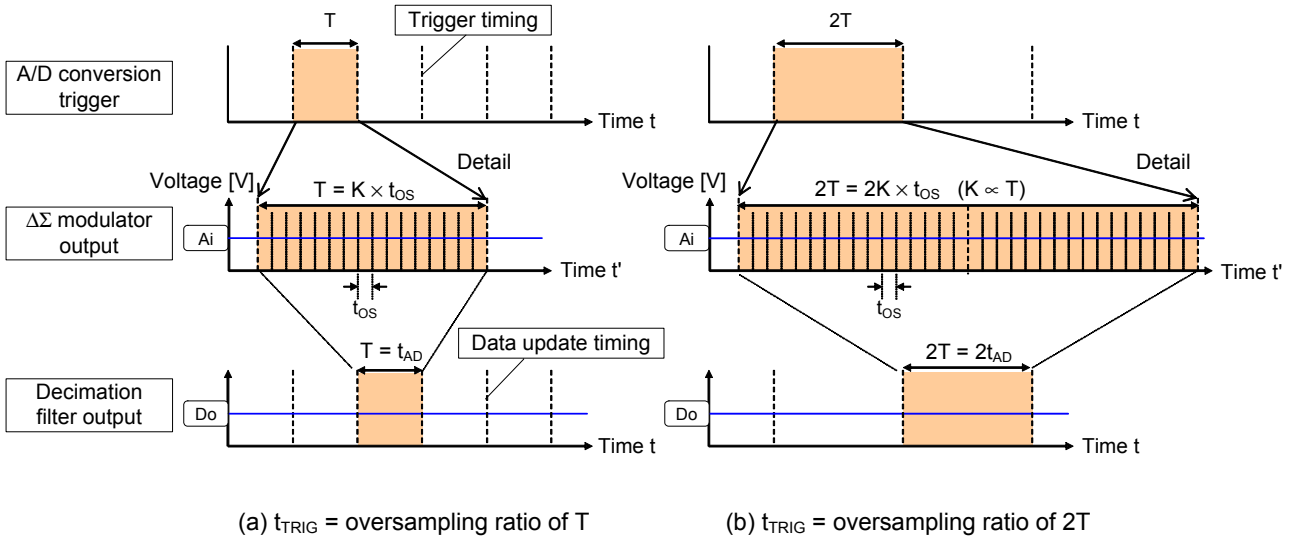
(a) t_{OS} A/D conversion time t_{AD} (b) $t_{OS}' = t_{OS} \times 2$ A/D conversion time t_{AD}'

Ai: Measurement voltage
Do: A/D conversion data
t_{AD}: A/D conversion time
t_{OS}: 1-cycle period of oversampling clock

Figure 2.5 Outline of A/D Conversion Time of ΔΣ A/D Converter

The A/D conversion time of the RX21A Group's ΔΣ A/D converter is equivalent to the A/D conversion trigger period (t_{TRIG}).

On the RX21A Group operation is guaranteed at an oversampling frequency of 3.125 MHz. Operation is not guaranteed if the oversampling frequency is changed. Therefore, the A/D conversion time can be changed by adjusting the A/D conversion trigger period to change the oversampling ratio, as shown in figure 2.6.



(a) t_{TRIG} = oversampling ratio of T (b) t_{TRIG} = oversampling ratio of 2T

Ai: Measurement voltage
Do: A/D conversion data
T: Setting value of A/D conversion trigger period
t_{OS}: 1-cycle period of oversampling clock
K: Oversampling ratio (K = f_{OS} / f_S)
t_{AD}: A/D conversion time

Figure 2.6 RX21A Group A/D Conversion Trigger Period and Oversampling Ratio

A/D conversion on the RX21A Group uses events generated by a peripheral function as the triggers for operation. In the example described here, a timer is used as the peripheral function, and the oversampling ratio is changed by means of the setting by which an event is generated at regular intervals. The procedure for calculating the count value N timer setting is described below.

1. The formula below is used to calculate the oversampling ratio K. Note that K must be an integer within the range $256 \leq K \leq 768$.
   K = trigger period / t_{OS}
   t_{OS} = (1 / oversampling frequency) = 0.32 µs, so the trigger period is set in increments of 0.32 µs.
2. The count value N is calculated as follows:
   N = counting frequency of timer × (t_{OS} × K) – 1
   For details of the timer functions, see RX21A Group User's Manual: Hardware.

On the RX21A Group, the data size changes according to the oversampling ratio. The maximum data size that can be stored in the ΔΣ A/D data register changes according to t_{TRIG}, and it can be calculated using the following formula:

$$\text{Max. data size} = \log_2\left(2^{24} \times \frac{t_{TRIG}}{t_{OS} \times 256}\right)$$

$$= 24 + \log_2\left(\frac{t_{TRIG}}{t_{OS} \times 256}\right)$$

When the minimum setting value of $t_{OS} \times 256 = 81.92$ µs is used for t_{TRIG}, the data length that can be stored in the data register is 24 bits, according to the formula above.

When the maximum setting value of $t_{OS} \times 768 = 245.76$ µs is used for t_{TRIG}, the data length that can be stored in the data register is 25.6 bits, according to the formula above, and a data area of 26 bits is required to accommodate it. Accordingly, the range of values that can be stored in the data register is FE00 0000h to 01FF FFFFh.

When handling A/D conversion data with larger data sizes, care should be taken to avoid problems such as calculation result overflows. To handle data extended to 26 bits or the like using the standard data size of 24 bits, convert the data in software and then apply correction by multiplying by ($t_{OS} \times 256$) / t_{TRIG}.

2.2 Gain Function

2.2.1 Outline of Function

The input range of the ΔΣ A/D converter can be utilized effectively by performing voltage amplification, allowing accurate A/D conversion of small-amplitude or low-voltage signals.

Figure 2.7 shows a usage example of the gain function. When performing A/D conversion of an analog voltage one-fourth the maximum limit of the input range, as in (a), the results are treated internally by the microcontroller as having a data range of 22 bits. However, when the analog voltage is amplified four times and then A/D conversion is performed, as in (b), the results are treated internally by the microcontroller as having a data range of 24 bits.

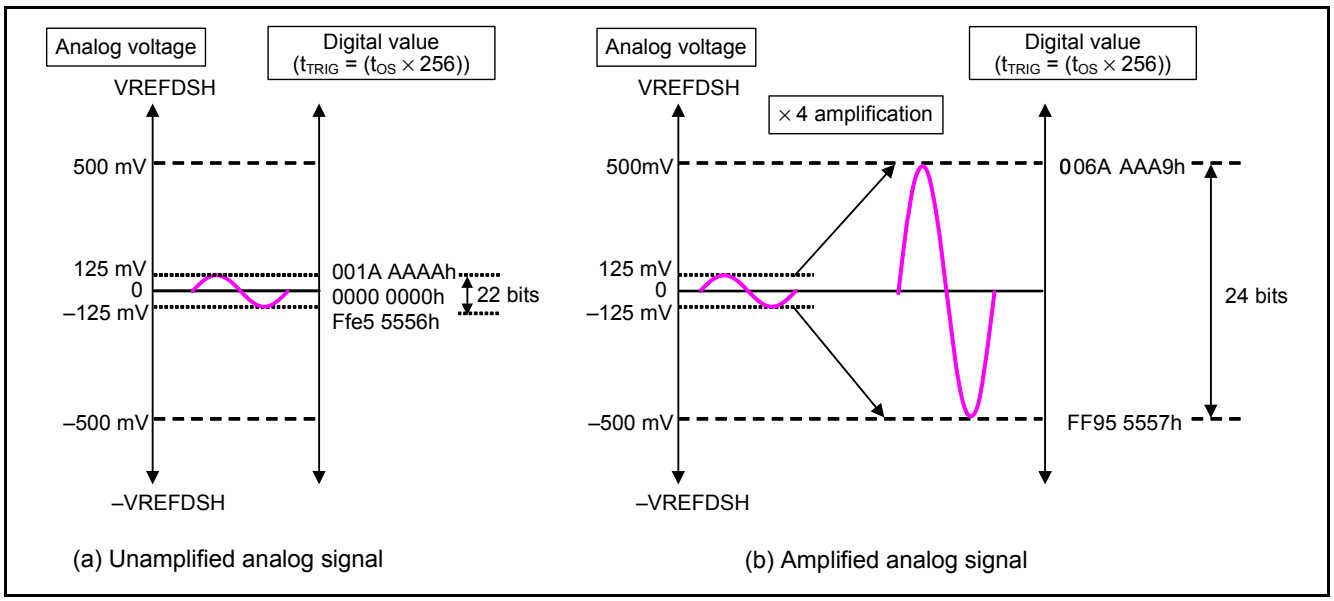


Figure 2.7 Usage Example of Gain Function

2.2.2 Setting Method and Input Range

The gain function setting is made by using of the GAIN bit field in the ΔΣ A/D gain select register DSADGSRn (n = 0 to 6). Table 2.3 lists the available gain settings.

For differential input, settings of ×1, ×2, ×4, ×8, ×16, ×32, and ×64 are supported. These settings are made by means of bits GAIN2, GAIN1, and GAIN0 in registers DSADGSR0 to DSADGSR3.

For single-ended input, settings of ×1, ×2, and ×4 are supported. These settings are made by means of bits GAIN1 and GAIN0 in registers DSADGSR4 to DSADGSR6.

Note that analog input range restrictions apply to each of the gain settings. Use settings within the analog input range listed in 2.1.4, Output Format of A/D Conversion Data.

Table 2.3 List of Gain Settings

Gain	DSADGSRn Register	
	GAIN[2:0] Bits (n = 0 to 3, differential input channels)	GAIN[2:0] Bits (n = 4 to 6, single-ended input channels)
1	000b	00b
2	001b	01b
4	010b	10b
8	011b	×
16	100b	×
32	101b	×
64	110b	×

×: Setting prohibited

2.3 Single-Ended Input Pins

2.3.1 Outline of Single-Ended Signals

For single-ended input, the single analog voltage *Vin* is used. If the single-ended signal picks up external noise along its transfer path, the noise components are also treated as part of the signal by the processing system. It may not be possible to measure the level of small-amplitude or low-voltage signals, particularly in environments prone to the generation of noise. Single-ended input is therefore used to handle comparatively large signals that allow the noise level to be ignored.

2.3.2 A/D Conversion of Single-Ended Signals

In the A/D converter block, first Vin is amplified by the specified gain setting (×1 to ×4). Next, the analog input voltage range determined by the VREFDSH and VREFDSL pins is converted to digital values at 24 bit resolution. Thus, the voltage range of the ΔΣ A/D converter's single-ended input pins is as follows:

$$-500\ \text{mV} \leq \text{Vin} \times \text{gain} \leq 500\ \text{mV}$$

When $t_{TRIG} = (t_{OS} \times 256)$, the range of A/D conversion results is 00 0000h to 7F FFFFh for positive voltages (Vin ≥ 0 (V)) and FF FFFFh to 80 0000h for negative voltages (Vin < 0 (V)).

The pins supporting single-ended input are ANDS4, ANDS5, and ANDS6. The ground level of the signal source is used as the center value for A/D conversion of single-ended signals, so the ANDSSG pin is connected to the signal ground (signal source ground). For more information on the handling of the ANDSSG pin, see 3.3, Notes on Countermeasures for Noise.

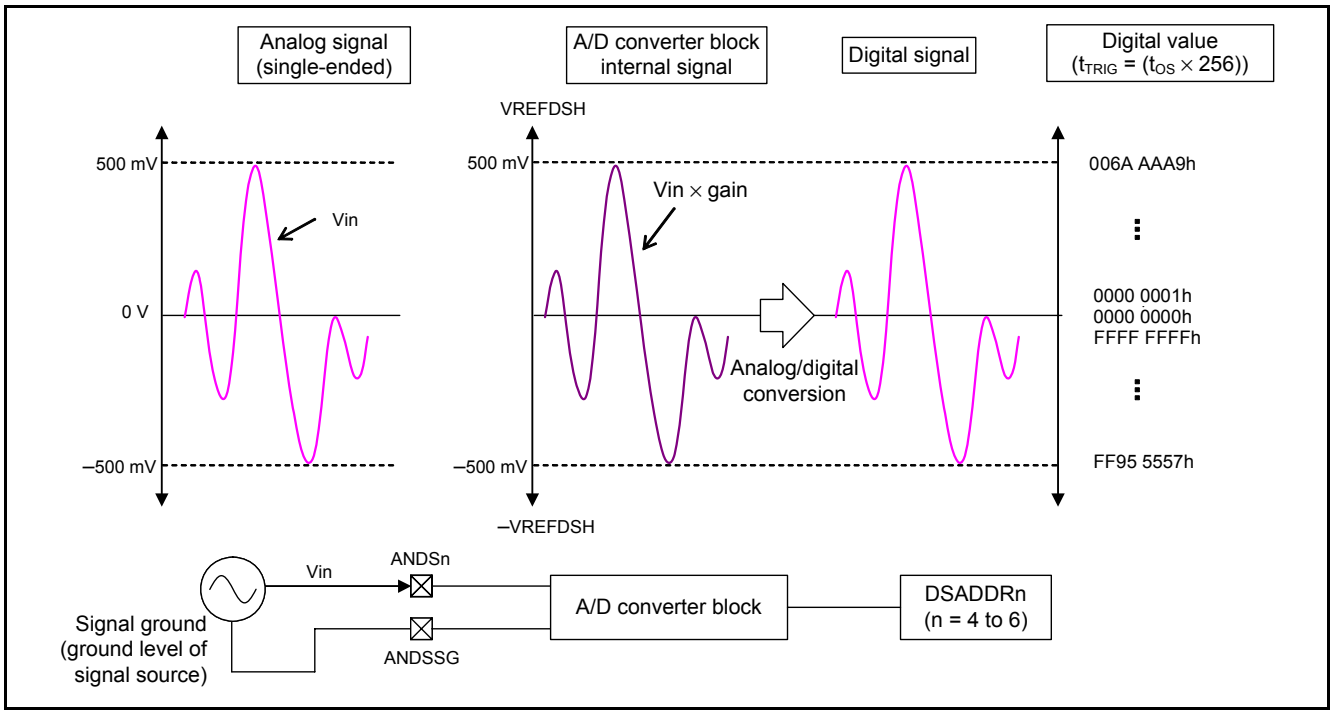


Figure 2.8 Example of Single-Ended Input

2.4 Differential Signal Input Pins

2.4.1 Outline of Differential Signals

A differential signal consists of a pair of two analog voltages, VinP and VinN, with a common mode voltage as the center. The advantage of using differential input is that common mode noise (overlapping noise components that are present on both of the signal lines) is eliminated by the processing system, which is effective in cases where it is necessary to transfer a comparatively small signal. Note that it is important to keep in mind that the signal level that is handled by the processing system is VinP – VinN.

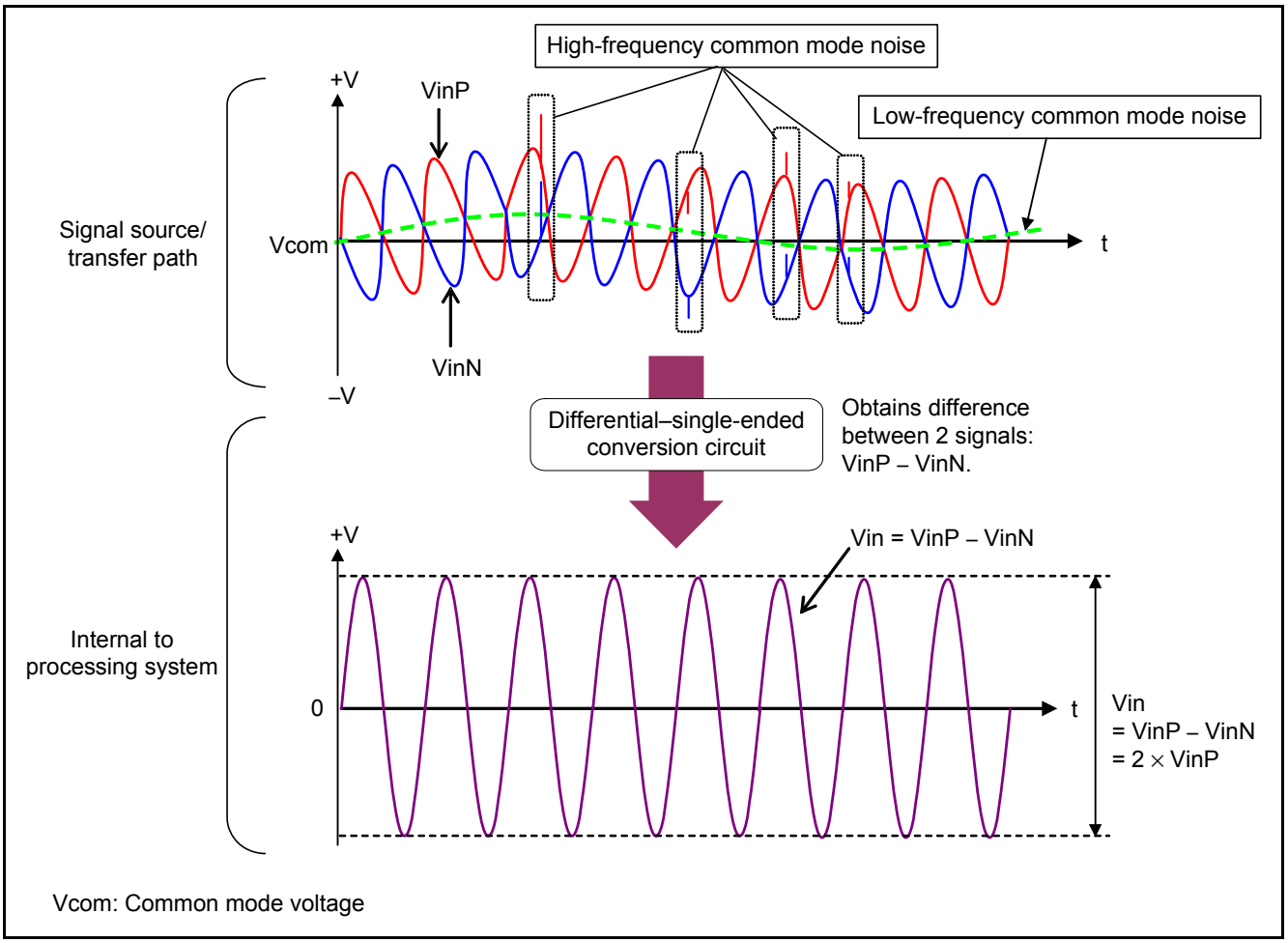


Figure 2.9 Conceptual View of Differential Signals

2.4.2 A/D Conversion of Differential Signals

In the A/D converter block, first VinP and VinN are amplified by the specified gain setting (×1 to ×64). Next, VinN is subtracted from VinP ((VinP – VinN) × gain), and the analog input voltage range determined by the VREFDSH and VREFDSL pins is converted to digital values at 24 bit resolution. Thus, the voltage range of the ΔΣ A/D converter's differential input pins is as follows:

$$-500\ \text{mV} \le (\text{VinP} - \text{VinN}) \times \text{gain} \le 500\ \text{mV}$$
$$(-250\ \text{mV} \le \text{VinP} \times \text{gain} \le 250\ \text{mV},\ -250\ \text{mV} \le \text{VinN} \times \text{gain} \le 250\ \text{mV})$$

When $t_{TRIG} = (t_{OS} \times 256)$, the range of A/D conversion results is 00 0000h to 7F FFFFh for positive voltages (VinP – VinN ≥ 0 (V)) and FF FFFFh to 80 0000h for negative voltages (VinP – VinN < 0 (V)).

The pins supporting differential input are ANDS0P and ANDS0N; ANDS1P and ANDS1N; ANDS2P and ANDS2N; and ANDS3P and ANDS3N. Input differential signals to these pins such that the analog ground level (0 V) is the common mode voltage.

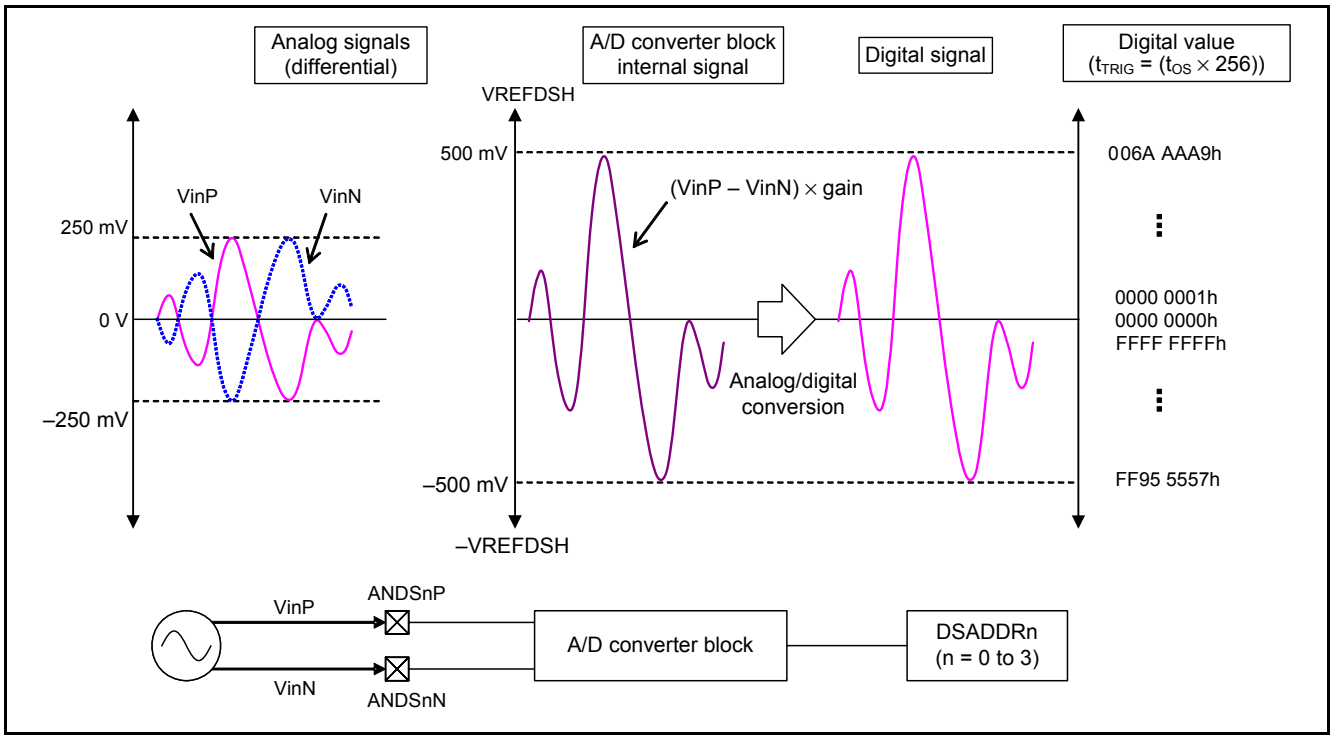


Figure 2.10 Example of Differential Input

2.5 On-Chip Reference Circuit

2.5.1 Outline of Function

The reference voltage serves as the basis when calculating A/D conversion results. The accuracy of the reference voltage therefore affects the A/D conversion accuracy.

Figure 2.11 illustrates A/D conversion results obtained when using a reference power supply with low accuracy. The A/D conversion results express the ratio of the measurement voltage to the reference voltage. However, when A/D conversion of a constant voltage is performed in an environment in which the reference voltage is unstable, the ratio of the measurement voltage to the reference voltage changes according to the conversion timing. Thus, ideal A/D conversion results cannot be obtained.

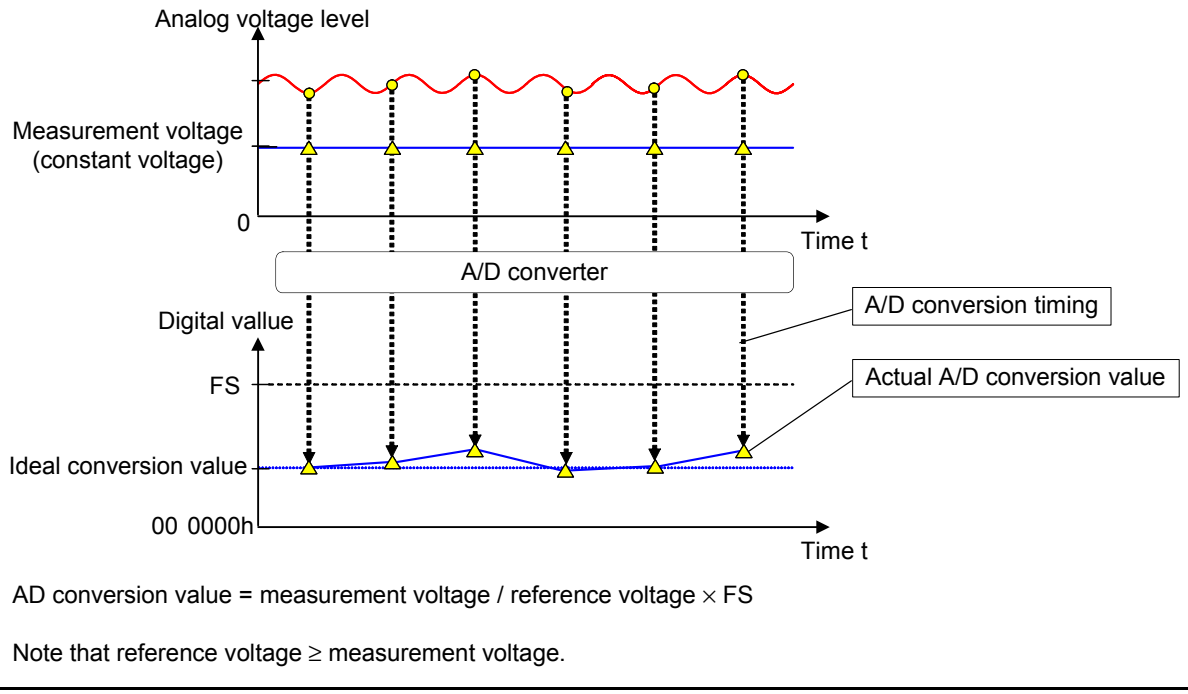


Figure 2.11 A/D Conversion Results with Low-Accuracy Reference Voltage

Figure 2.12 illustrates A/D conversion results obtained when using a reference power supply of high accuracy. When the reference voltage is stable, ideal A/D conversion results can be obtained regardless of the A/D conversion timing.

RX21A Group has an on-chip high-precision BGR for generating the reference voltage. It provides a stable reference power supply without the need for an additional external circuit, so highly accurate A/D conversion is possible.

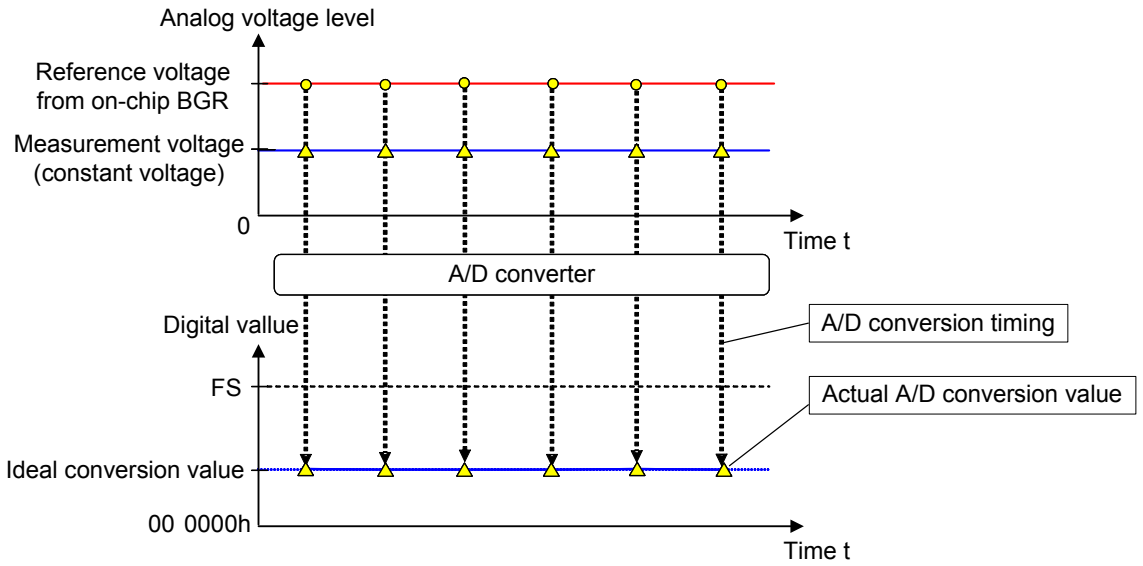


Figure 2.12 A/D Conversion Results with Highly Accuracy Reference Voltage

2.5.2 Internal Structure

Figure 2.13 is a block diagram of the on-chip reference circuit of the RX21A Group. The BGR incorporated into the reference circuit generates the A/D conversion reference voltage (high side, VREFDSH), PGA and ΔΣ modulator bias signals, and the common mode voltage for internal signals. A reference voltage can also be generated from a voltage supplied externally via the BGR_BO pin.

The VREFDSH and VCOMDS pins should be connected to capacitors to stabilize the voltages generated by the bias circuit. Note that operation is not guaranteed if an A/D conversion reference voltage and internal signal common mode voltage are input to these pins.

After selecting the on-chip BGR or the BGR_BO pin as the source of the reference voltage, the reference voltage should be allowed to stabilize before obtaining A/D conversion data. If the stabilization time is not sufficient, the accuracy of the A/D conversion data cannot be guaranteed during the settling period.

For more information on applying a voltage to the BGR_BO pin and reference voltage stabilization time, see the Electrical Characteristics section in RX21A Group User's Manual: Hardware.

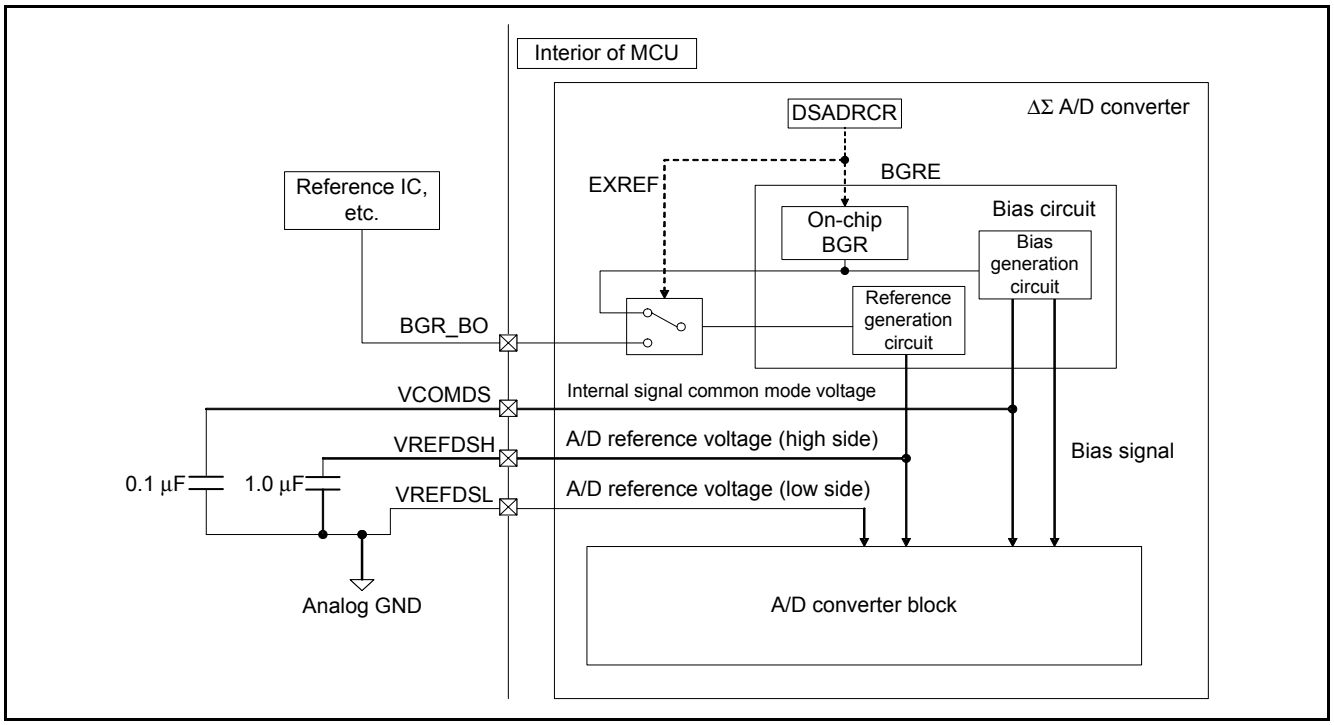


Figure 2.13 Block Diagram of On-Chip Reference Circuit

2.5.3 Selecting the Reference Supply Source

The ΔΣ A/D reference control register (DSADRCR) is used to select internal BGR control and the reference voltage supply source. To specify the on-chip BGR as the reference voltage supply source, clear the EXREF bit in DSADRCR to 0. This setting puts the BGR_BO pin into the Hi-z (high-impedance) state. To use an external reference voltage, set the EXREF bit to 1. For more information on applying a voltage for use as an external reference, see the Electrical Characteristics section in RX21A Group User's Manual: Hardware.

Note that the BGRE bit in DSADRCR should be set to 1 during A/D conversion, regardless of the setting of the EXREF bit.

Table 2.4 Selecting the Reference Supply Source

Reference Supply Source	DSADRCR Register		Remarks
	BGRE Bit	EXREF Bit	
On-chip BGR	1	0	
External reference	1	1	
×	0	×	A/D conversion not possible.

×: Any value
Set the BGRE bit in DSADRCR to 1 during A/D conversion, regardless of the setting of the EXREF bit.

2.6 Single ΔΣ Modulator Conversion Function

2.6.1 Outline of Function

It is possible to connect one or more of the ΔΣ modulators inside the ΔΣ A/D converter to D/A converter output to perform A/D conversion testing of individual ΔΣ modulators. This function enables use of the on-chip D/A converter to evaluate the performance of individual on-chip ΔΣ modulator units, and it also can be used for correction of offset error and full-scale error. For details of the method for offset error and full-scale error correction, see 4.2, Correction of Offset and Full-Scale Error.

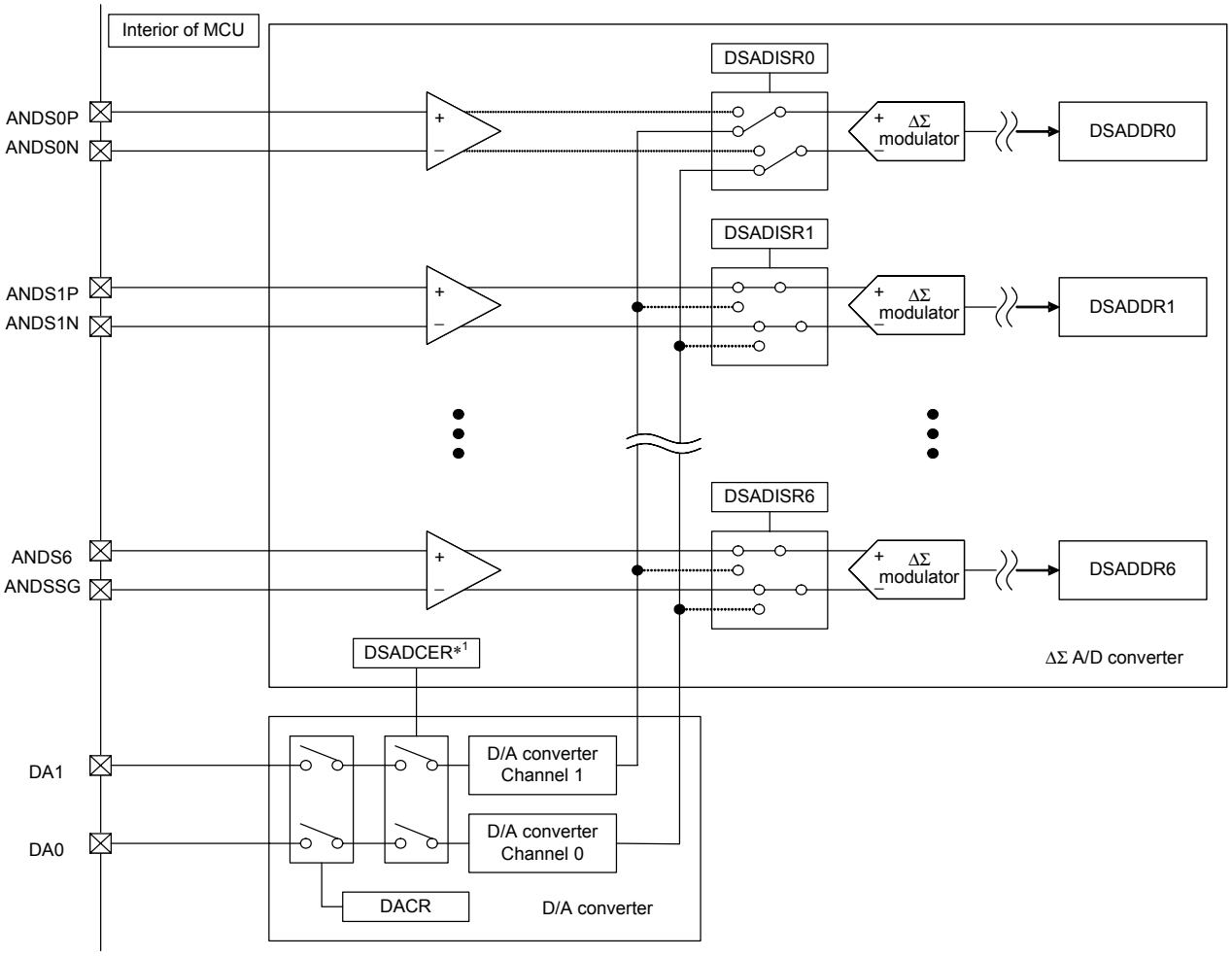
Note that this function cannot be used as an offset adjustment function for analog input signals.

2.6.2 Internal Structure

Figure 2.14 is a block diagram illustrating use of the single ΔΣ modulator conversion function. The ΔΣ A/D control expansion register (DSADCER) and ΔΣ A/D input select registers (DSADISRn: n = 0 to 6) are used connect one or more ΔΣ modulators to D/A converter output. In this case, the input on the analog input pins is ignored.

In order to use the single ΔΣ modulator conversion function, it is necessary to select D/A converter output for each ΔΣ modulator channel by setting the ISEL bit in the corresponding DSADISRn register to 1.

Once the ISEL bit in DSADISRn has been set to 1 for at least one channel, it is possible to control the analog output of the D/A converter. When output is enabled, do not use the port output function of ports that support selection of the analog function (ports 0 and 4). Control of the disabling of output takes precedence over the setting of the DAOEn (n = 0 and 1) bit in the D/A control register (DACR) of the D/A converter.



Note: 1. Enabled when ISEL bit in any DSADISRn register is set to 1.

Figure 2.14 Block Diagram of Use of Single ΔΣ Modulator Conversion Function

2.6.3 Voltage Input Range of ΔΣ Modulator Input

Figure 2.15 illustrates the internal signal processing performed by the ΔΣ A/D converter. When signals are input on the analog input pins, as in (a), differential voltages comprising VinP and VinN can be handled in a range from –500 mV to 500 mV. However, the voltage range from ground level (0 V) to the power supply voltage (VCC) cannot be handled internally by the microcontroller. Therefore, the voltage level is shifted by the microcontroller internally, as in (b), and the input signal is converted to a positive voltage for signal processing. The RX21A Group's ΔΣ A/D converter shifts the voltage level by approximately 700 mV (the VCOMDS pin voltage) internally, converting the analog input analog input signal to VinP' and VinN' for input to the ΔΣ modulator. During A/D conversion, as in (c), the voltage level of VinN' relative to VinP' (VinP' – VinN') is converted, and the voltage component from the VCOMDS pin is removed from the A/D conversion result.

To use the single ΔΣ modulator conversion function to input a signal from the D/A converter to the ΔΣ modulator, use two D/A converter channels and specify a differential voltage of –500 mV to +500 mV with a common mode voltage of 700 mV. D/A converter channel 1 can be used as the positive input and channel 0 as the negative input to input differential signals to all of the ΔΣ A/D modulator units. Note that when D/A conversion is disabled on one of the D/A converter units, the output of the channel for which D/A conversion is disabled is low level (0 V).

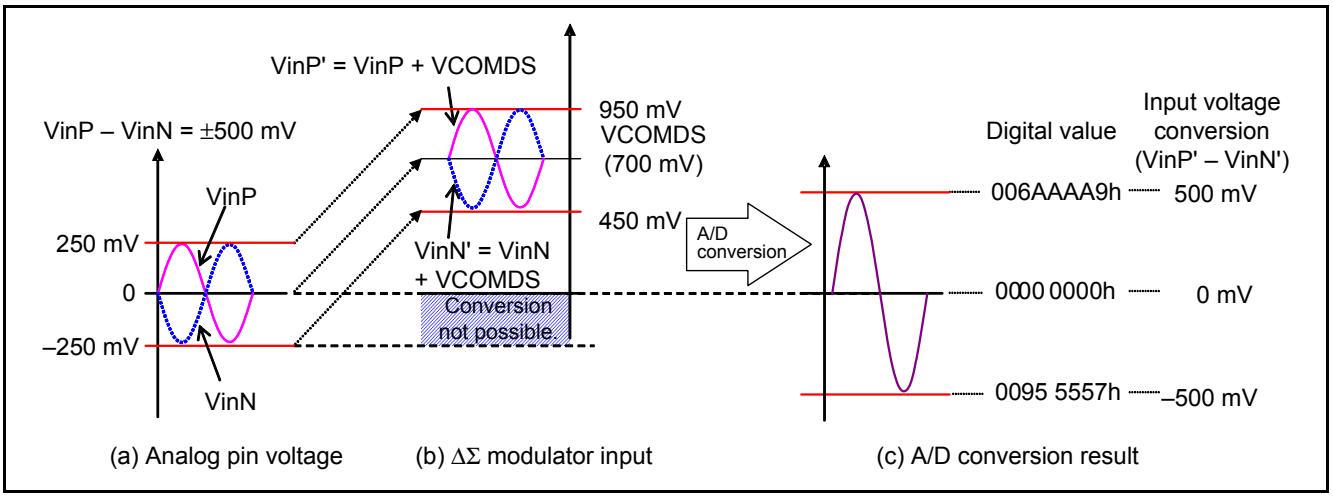


Figure 2.15 Internal Signal Processing by ΔΣ A/D Converter

2.6.4 ΔΣ Modulator Input Setting Examples

Table 2.5 lists the D/A converter output control register setting combinations that can be used with the single ΔΣ modulator conversion function.

To enable D/A converter output on two channels when using the single ΔΣ modulator conversion function, either set the D/A enable bit (DAE) in DACR to 1, or set to 1 both the D/A output enable 0 bit (DAOE0) and the D/A output enable 1 bit (DAOE1).

In addition, it is recommended when using the single ΔΣ modulator conversion function to clear the analog output control bit (AOC) in DSADCER to 0 to disable output to the D/A converter analog output pins.

Table 2.5 D/A Converter Output Control Register Setting Combinations Usable with Single ΔΣ Modulator Conversion Function

Peripheral Function	D/A Converter			Usability of Single ΔΣ Modulator Conversion Function
Register	DACR			
Bit	DAE	DAOE1	DAOE0	
Setting value	1	×	×	Usable
	0	1	1	Usable
	0	1	0	Not usable
	0	0	1	Not usable
	0	0	0	Not usable

×: Any value

Table 2.6 lists ΔΣ modulator gain settings and the corresponding differential input ranges. The ΔΣ modulator gain differs according to the setting in the DSADGSRn register, resulting in different differential input ranges. Make sure to select the D/A converter settings such that the differential input range is not exceeded.

Table 2.7 lists D/A converter setting examples. Figure 2.16 shows a differential input setting example where the ΔΣ modulator gain is ×1.

Table 2.6 ΔΣ Modulator Gain Settings and Differential Input Ranges

ΔΣ Modulator Gain	DSADGSRn Setting Values (Single ΔΣ Modulator Conversion)		Max. Differential Input Voltage of ΔΣ Modulator [mV]
	GAIN[2:0] Bits (n = 0 to 3, differential input channels)	GAIN[1:0] Bits (n = 4 to 6, single-ended input channels)	
×1	000b 001b 010b 011b 010b	00b 01b 10b	±500
×2	101b	—	±250
×4	110b	—	±125

—: Not applicable

Table 2.7 D/A Converter Setting Examples

ΔΣ Modulator Gain	DADR1 (Positive Input Side)	DA1 Output [mV]	DADR0 (Negative Input Side)	DA0 Output [mV]	A/D Conversion Voltage [mV]
×1	8Bh	447.8	126h	947.2	–499.4
	126h	947.2	8Bh	447.8	499.4
×2	B3h	576.7	100h	824.8	–248.1
	100h	824.8	B3h	576.7	248.1
×4	C7h	641.1	ECh	760.3	–119.2
	ECh	760.3	C7h	641.1	119.2

Note: Setting values under conditions where VCC = AVCC0 = AVCCA = VREFH = 3.3 V and VSS = AVSS0 = AVSSA = VREFL = 0 V

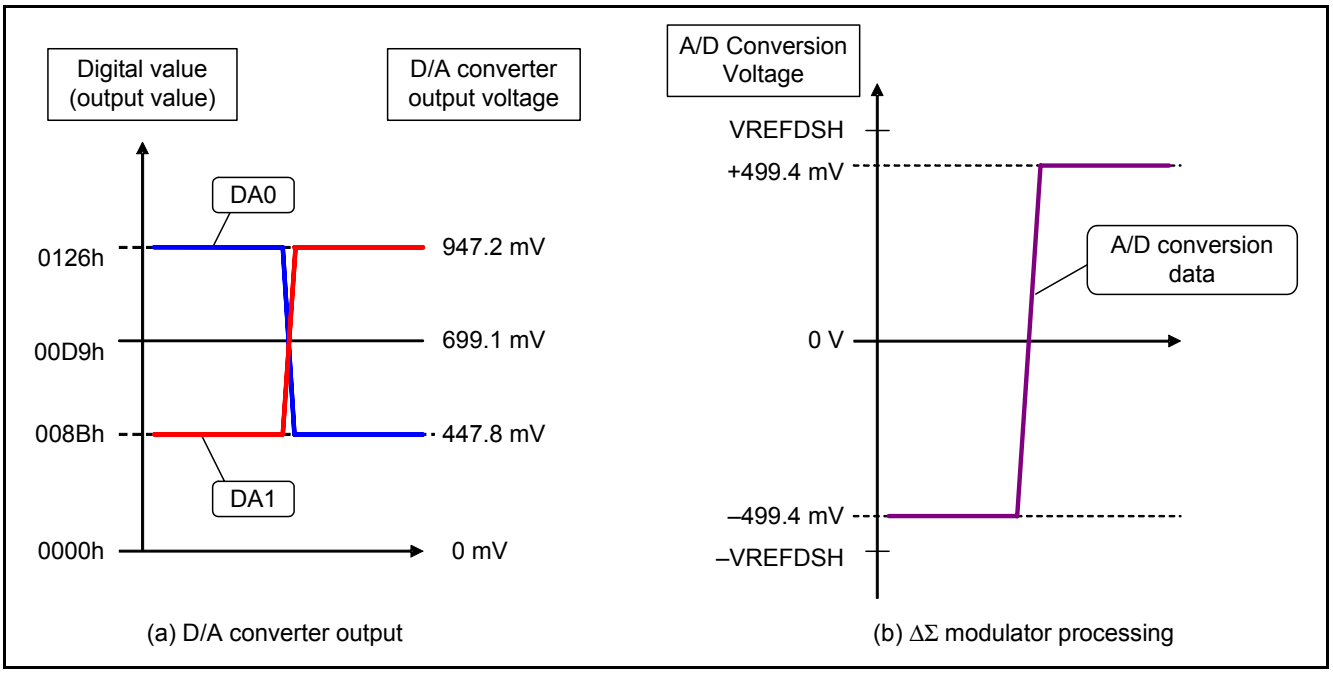


Figure 2.16 Differential Input Setting Example with ΔΣ Modulator Gain of ×1

3. Recommended External Circuits and Usage Notes

3.1 ΔΣ A/D Converter Usage Notes

For usage notes on the ΔΣ A/D converter, see RX21A Group User's Manual: Hardware.

3.2 Selection of Main Clock Source

Use of a crystal oscillator device is recommended to improve A/D conversion accuracy. A crystal oscillator device with a guaranteed temperature rating should be used if necessitated by the thermal characteristics of the system.

3.3 Notes on Countermeasures for Noise

For notes on noise countermeasures involving the analog input pins of the ΔΣ A/D converter, see RX21A Group User's Manual: Hardware.

3.4 Design of Power Supply Circuit

To improve A/D conversion accuracy, follow the recommendations below when designing the power supply circuit.

- Provide separate voltage sources for the system power supplies (VCC and AVCC0) and the analog power supply of the ΔΣ A/D converter (AVCCA). Note that there is no specified power rise sequence for VCC, AVCC0, and AVCCA, but that supplying power on VCC, AVCC0, or AVCCA alone for an extended period of time can damage the microcontroller. Rather, the power supply to these three pins should rise and fall at the same time as far as possible. Note that if possible the supply to both VCC and AVCCA should have the same potential.
- When using a single voltage supply source, it should be branched close to the output pins of the supply source and the two branches used to supply the system power supply and the analog power supply of the ΔΣ A/D converter, respectively.
- The digital power supply patterns (VCC and VSS) and the analog power supply patterns (AVCCA and AVSSA) should be isolated from each other.
- The analog ground (AVSSA) pattern should be connected at a single point to the digital ground (VSS) pattern that is stabilized on the board to ensure that the electrical potential of the analog and digital grounds is equivalent and prevent the entry of noise via the digital ground.
- The wiring patterns of the analog power supply (AVCCA), the external reference input pin (BGR_BO), the reference voltage pins (VREFDSH and VREFDSL), and the common mode voltage pin (VCOMDS) should be shielded by the analog ground (AVSSA).
- The 1.0 μF capacitor connected to the VREFDSH pin and the 0.1 μF capacitor connected to the pin should be located as close to the pins as possible.
- Connect the AVCC0 and VREFH pins to capacitors when using the single ΔΣ modulator conversion function.

Figure 3.1 shows an example power supply circuit for use with the ΔΣ A/D converter of the RX21A Group.

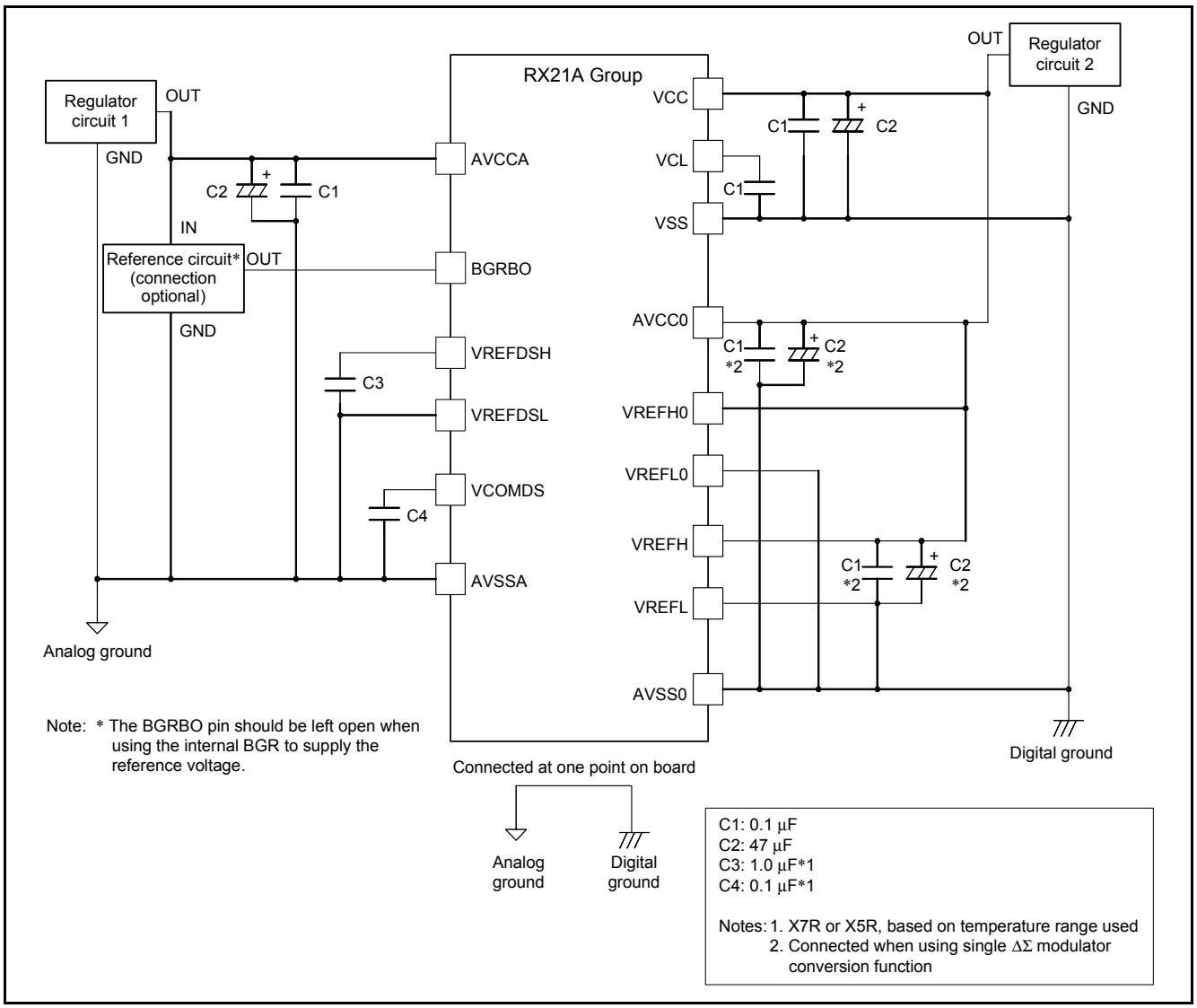


Figure 3.1 Example Power Supply Circuit for Use with ΔΣ A/D Converter of RX21A Group

3.5 Electrical Characteristics

3.5.1 ΔΣ A/D Conversion Characteristics

For the conversion characteristics of the RX21A Group's ΔΣ A/D converter, see RX21A Group User's Manual: Hardware.

The sampling period of the RX21A Group's ΔΣ A/D converter is the A/D conversion trigger period. In addition, the A/D conversion time is dependent on the A/D conversion trigger period. Restrictions apply to the A/D conversion trigger period setting value. Refer to 2.1.3, Notes on A/D Conversion Trigger Setting, and select an appropriate trigger period setting. The sampling frequency of the ΔΣ A/D converter can be calculated from the reciprocal of the A/D conversion trigger period. In addition, the upper limit signal frequency at which A/D conversion is possible is one-half the sampling frequency, according to the Nyquist theorem.

For details of SNDR sampling period dependency and input frequency dependency, band dependency, and PGA gain dependency, see the Electrical Characteristics section in RX21A Group User's Manual: Hardware.

4. Utilizing the ΔΣ A/D Converter

4.1 Improving SNDR

Depending on the SNDR properties, it may be possible to achieve improvements by boosting signal components or reducing noise components.

A PGA is used to boost signal components. However, analog circuits such as a PGA have associated noise, which is also amplified, so the larger the gain the lower the improvement in SNDR. Caution is required when using the PGA at a high-gain setting.

Limiting the frequency band of the A/D converter is a way to reduce noise components. The frequency band can be changed by means of the sampling frequency setting of the A/D converter. To narrow the frequency band, lower the sampling frequency. Alternately, a digital filter implemented in software can be used to restrict the frequency band to a user-defined range of frequencies.

4.2 Correction of Offset and Full-Scale Error

4.2.1 Error Specific to ΔΣ A/D Converters

Figure 4.1 shows an example of ΔΣ A/D converter input and output characteristics. The I/O characteristics of an ideal A/D converter would appear as a straight line from the origin to the full-scale value, as shown in figure 4.1. An actual ΔΣ A/D converter, in contrast, generates offset error and gain error, so the measurement range extends from OS to FS. Therefore, it is necessary to correct for the offset error and full-scale error in order to obtain the target value being measured from the digital value with a high degree of accuracy. When offset and gain have been corrected for, highly linear output characteristics can be obtained.

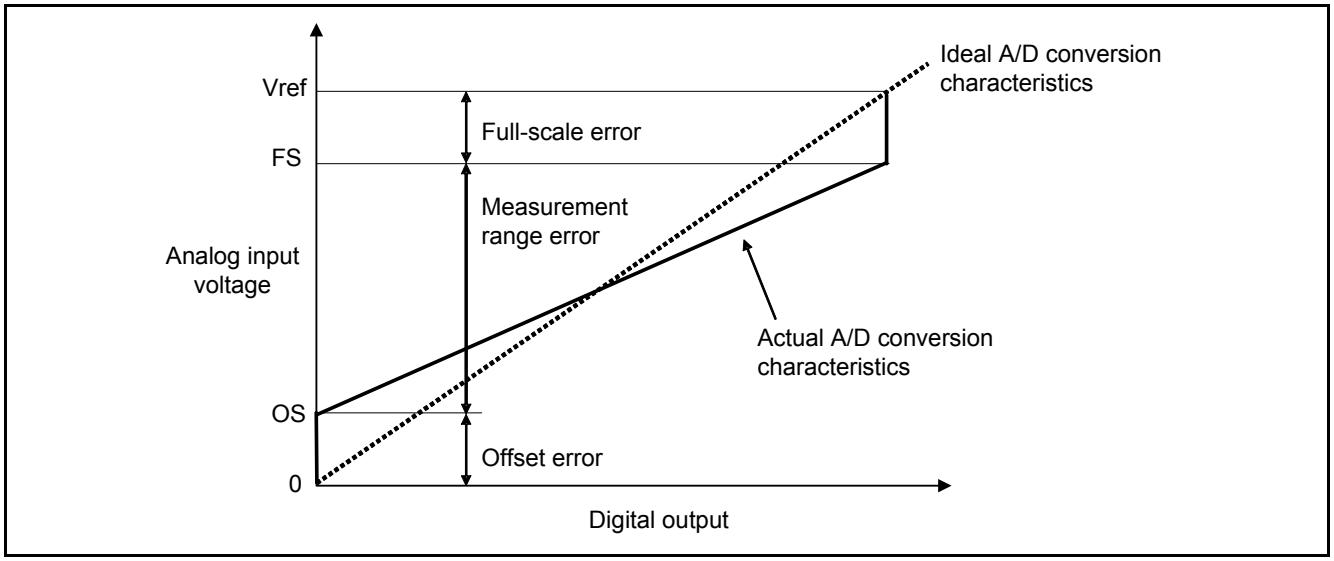


Figure 4.1 Example of ΔΣ Converter I/O Characteristics

4.2.2 Correction Concept

The relationship between the *x* and *y* coordinates in the example ΔΣ converter I/O characteristics, as shown in figure 4.2, can be expressed as follows:

$$lsb = (xC - xB) / (yC - yB) \quad (1)$$

$$x = (xC - xB) / (yC - yB) * y + OS \quad (2)$$

$$OS = xB - (xC - xB) / (yC - yB) * yB \quad (3)$$

Combining expressions (1), (2), and (3) yields the following expression:

$$x = lsb * y + xB - lsb * yB = lsb * (y - yB) + xB$$

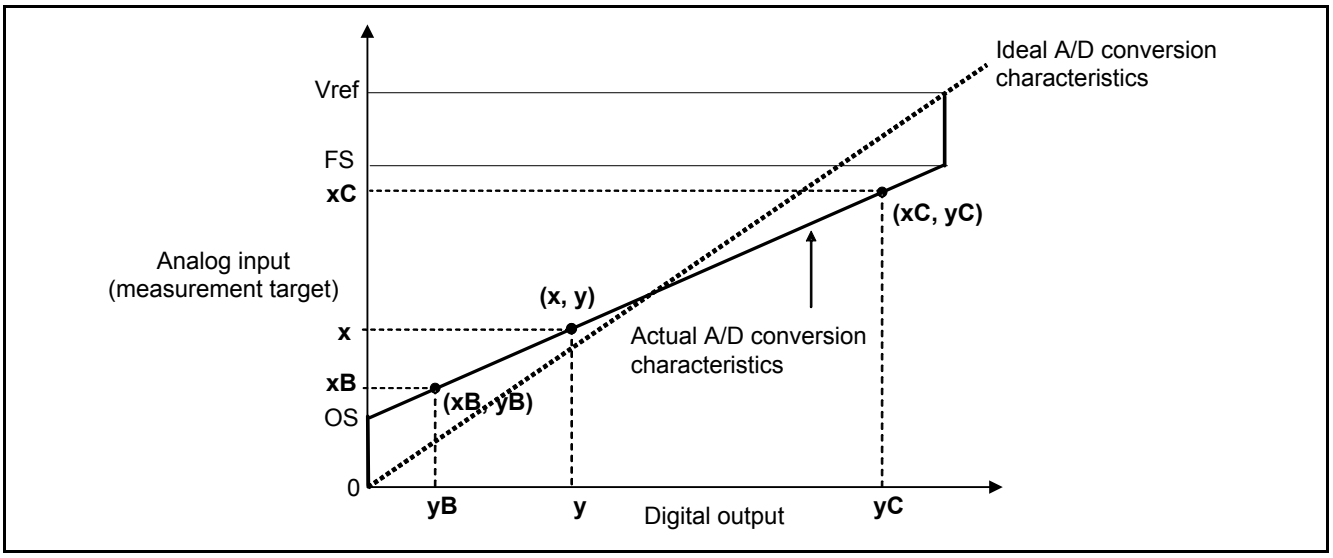


Figure 4.2 Error Correction Concept

4.2.3 Offset/Full-Scale Error Correction Method

The procedure for actually applying offset and full-scale error correction is as follows:

1. Measure the two points, (xB, yB) and (xC, yC), shown in figure 4.2.
2. From the two measured points, (xB, yB) and (xC, yC), calculate the slope (lsb).
3. Calculate the target value being measured from the digital value (the value of DSADDR).

$$\text{Target value being measured} = \text{slope (lsb)} \times (\text{DSADDR value} - yB) + xB$$

5. Reference Document

Obtain the latest version of the following document from the Renesas Electronics Web site:

[1] RX21A Group User's Manual: Hardware

6. Glossary

6.1 SNDR

The signal-to-noise and distortion ratio (SNDR) is an index of the conversion accuracy of an A/D converter. It is generally used as an index of A/D converter AC characteristics, and due to the manner in which it is calculated it constitutes the most demanding such index. The measurement frequency is considered the *signal*, signal components at other than the measurement frequency, including harmonics, are considered *noise and distortion*, and the ratio of the signal to total noise and distortion is calculated. A higher numeric value for SNDR indicates more accurate A/D conversion capability. Note that the SNDR listed in the conversion characteristics of a ΔΣ A/D converter represents the performance that can be obtained when the SNDR of the input signal itself is sufficiently assured.

6.2 ENOB (Effective Resolution)

The effective number of bits (ENOB) indicates the resolution that can be detected by an A/D converter. Sometimes the term "effective resolution" is used to express the same thing. The ENOB can be calculated from the SNDR as follows:

ENOB (bits) = (SNDR (dB) – 1.76) ÷ 6.02

6.3 Gain Error

(1) Gain Error of A/D Converter

The gain error of an A/D converter is the deviation from ideal A/D conversion characteristics when the digital output changes from the full-scale value – 1 (11 … 10b) to the full-scale value (11 … 11b) (figure 6.1). Note that it does not include quantization error. This type of gain error is sometimes referred to as "full-scale error." In an A/D converter with a built-in PGA, the gain error notation is for the gain error characteristics including the gain error of the PGA.

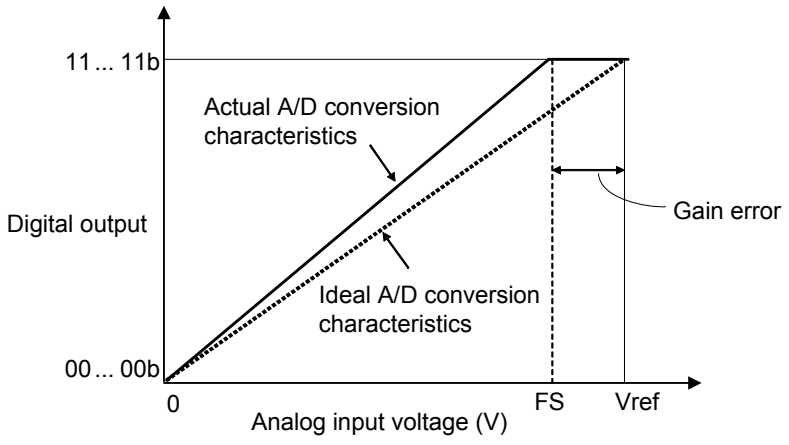


Figure 6.1 Gain Error of A/D Converter

(2) Gain Error of PGA

The gain error of a PGA indicates the deviation between the gain setting value and the actual gain. The gain error of a PGA is the result of variations among individual elements.

6.4 Offset Error

The offset error is the deviation from ideal A/D conversion characteristics when the digital output changes from all zeros (00 … 00b) to a value in which only the LSB*[1] is 1 (00 … 01b) (figure 6.2). Note that it does not include quantization error. This type of error is sometimes referred to as "zero error."

Note: 1. LSB: Least significant bit, the lowest-order bit of the digital data. This term is also used to refer to the minimum unit that can be expressed by the digital data.

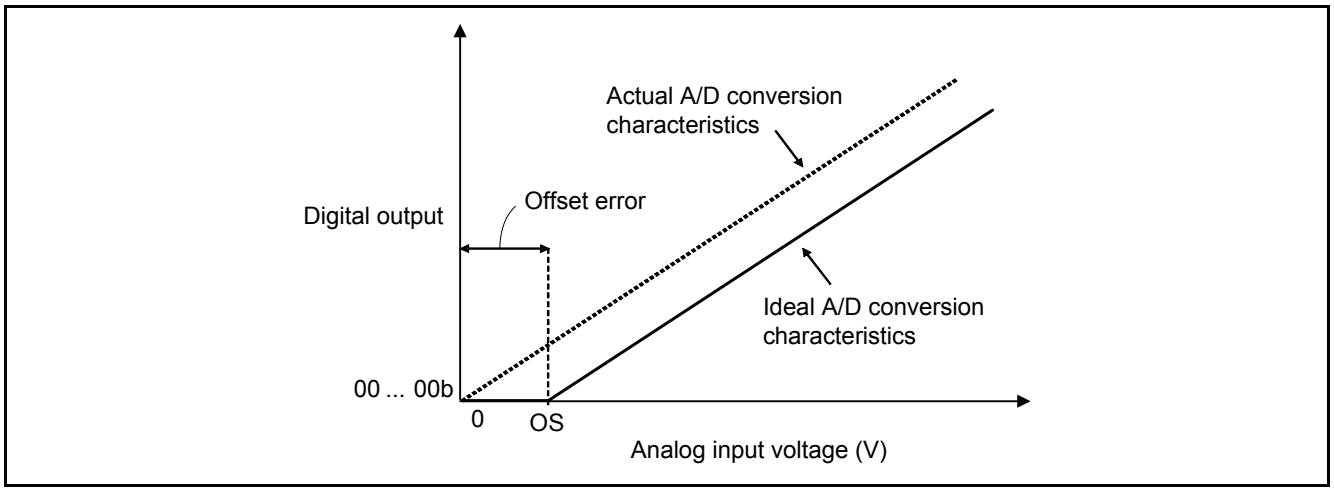


Figure 6.2 Offset Error of A/D Converter

6.5 Quantization Error

This is the error intrinsic to an A/D converter, and it is given as 1/2 LSB.

Analog voltage has a continuous range of values, but digital values are expressed as discrete units of data. The smallest discrete data unit is expressed by the LSB. However, when an analog voltage somewhere between two levels one LSB apart is A/D converted, it does not correspond to a unique value and error arises in the conversion result. Since the largest error possible occurs when A/D converting an analog voltage corresponding to 1/2 LSB, the maximum quantization error is specified as 1/2 LSB.

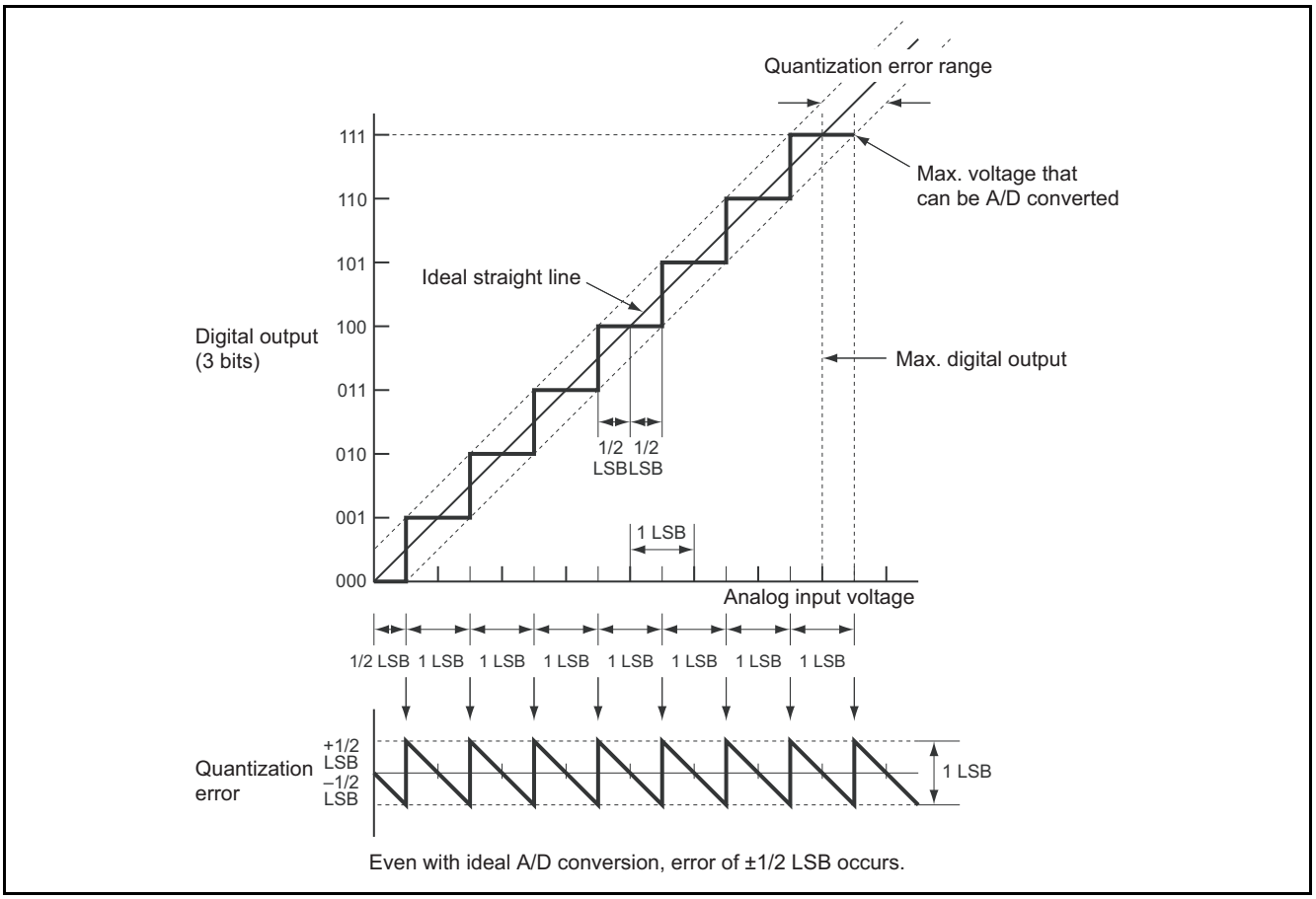


Figure 6.3 Quantization Error

6.6 Differential Nonlinearity Error

Differential nonlinearity error is the difference between the ideal value corresponding to one LSB and the actual step width (figure 6.4). The differential nonlinearity error is 0 when the step width is exactly equivalent to one LSB. If the differential nonlinearity error exceeds 1 LSB, the output will increase by a smaller amount when input increases. Furthermore, code loss may occur. That is, the converter may become incapable of outputting one or more of the 2n codes.

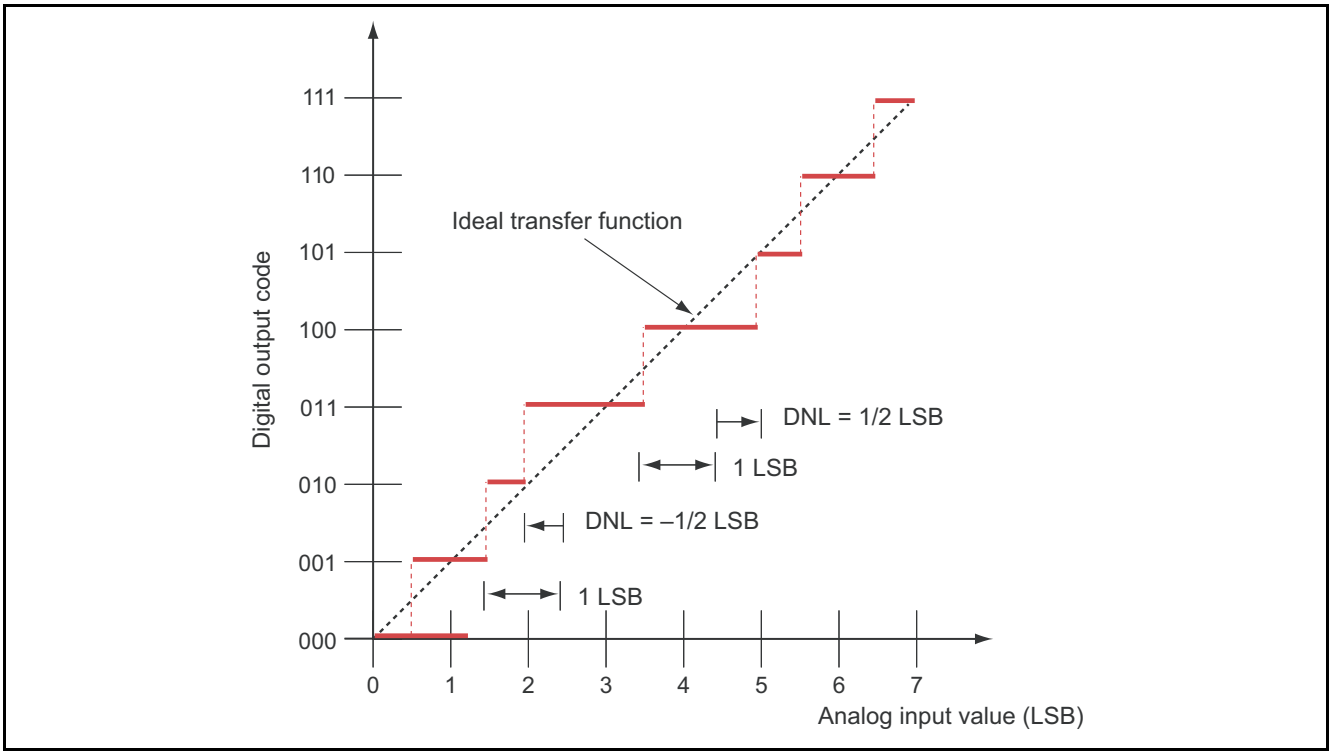


Figure 6.4 Differential Nonlinearity Error

6.7 Integral Nonlinearity Error

The deviation of the actual conversion value from ideal value (straight line) is called the integral nonlinearity error (figure 6.5). This deviation is measured as the width of the change per step.

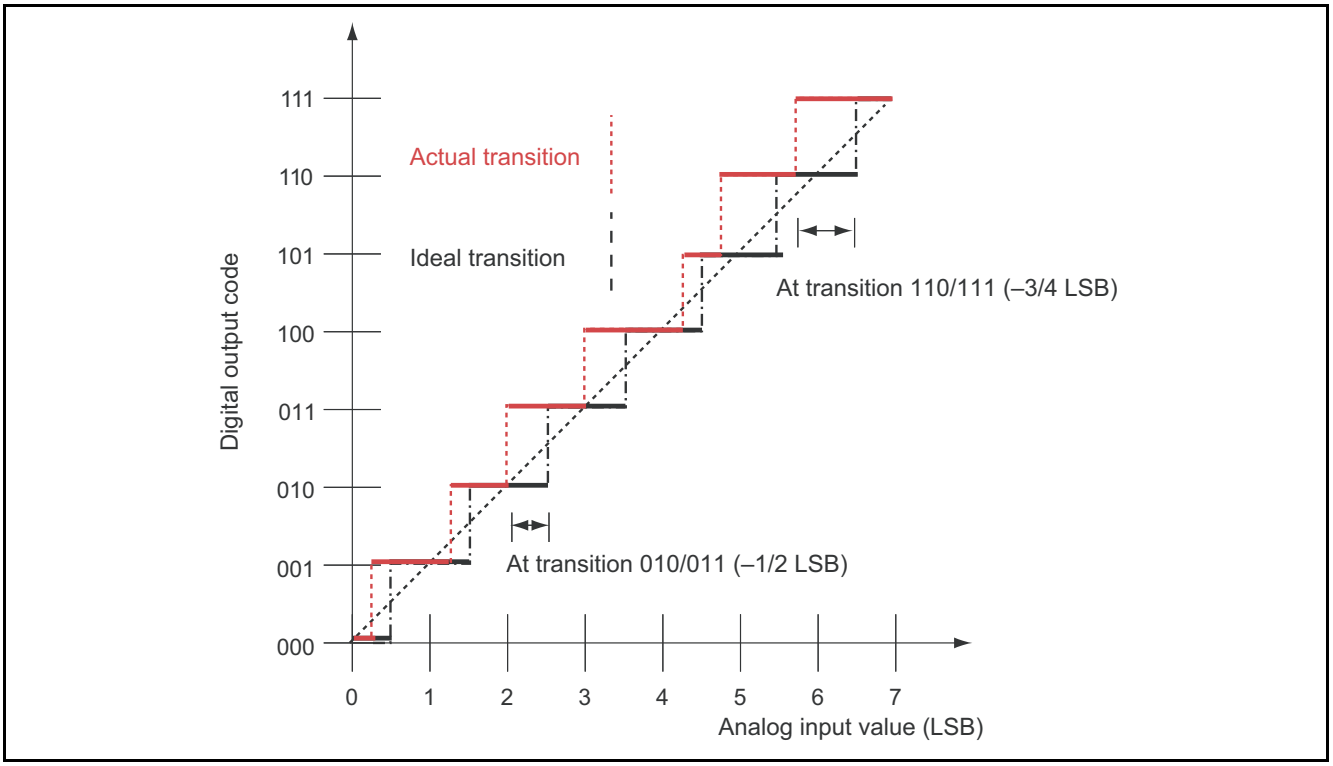


Figure 6.5 Integral Nonlinearity Error

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REVISION HISTORY	RX21A Group Application Note ΔΣ A/D Converter User's Guide

Rev.	Date	Description	
		Page	Summary
1.00	Mar. 04, 2013	—	First edition issued

General Precautions in the Handling of MPU/MCU Products

The following usage notes are applicable to all MPU/MCU products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Handling of Unused Pins

   Handle unused pins in accord with the directions given under Handling of Unused Pins in the manual.

   — The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible. Unused pins should be handled as described under Handling of Unused Pins in the manual.

2. Processing at Power-on

   The state of the product is undefined at the moment when power is supplied.

   — The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the moment when power is supplied.
   In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the moment when power is supplied until the reset process is completed.
   In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the moment when power is supplied until the power reaches the level at which resetting has been specified.

3. Prohibition of Access to Reserved Addresses

   Access to reserved addresses is prohibited.

   — The reserved addresses are provided for the possible future expansion of functions. Do not access these addresses; the correct operation of LSI is not guaranteed if they are accessed.

4. Clock Signals

   After applying a reset, only release the reset line after the operating clock signal has become stable. When switching the clock signal during program execution, wait until the target clock signal has stabilized.

   — When the clock signal is generated with an external resonator (or from an external oscillator) during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Moreover, when switching to a clock signal produced with an external resonator (or by an external oscillator) while program execution is in progress, wait until the target clock signal is stable.

5. Differences between Products

   Before changing from one product to another, i.e. to a product with a different part number, confirm that the change will not lead to problems.

   — The characteristics of an MPU or MCU in the same group but having a different part number may differ in terms of the internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

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