RL78/G14, R8C/36M Group

Migration Guide from R8C to RL78: Timer RB to Timer Array Unit

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Introduction

This document describes how to migrate from timer RB in R8C/36M Group to the timer array unit (TAU) in RL78/G14 (This document is described in 64-pin package as an example).

Target Device

RL78/G14, R8C/36M Group

When using this application note with other Renesas MCUs, careful evaluation is recommended after making modifications to comply with the alternate MCU.

Contents

1. Migration Method from R8C Family to RL78 Family

This application note explains how to achieve each mode (timer mode, programmable waveform generation mode, programmable one-shot generation mode and programmable wait one-shot generation mode) in Timer RB of R8C/36M using RL78/G14.
Table 1.1 shows the mode in Timer RB of R8C/36M group, and Table 1.2 shows the mode in Timer Array Unit of RL78/G14.

In R8C/36M Group, Timer RB is an 8-bit timer with an 8-bit prescaler. The prescaler and timer each consist of a reload register and counter. An internal or external count source is counted by the TRBPRE register. TRBPR register counts the underflows of the TRBPRE register. (In programmable waveform generation mode or programmable wait one-shot generation mode, TRBSC register counts the underflows of the TRBPRE register.)

In RL78/G14, the timer array unit has four 16-bit timers. Each 16-bit timer is called a channel and can be used as an independent timer. In addition, two or more "channels" can be used to create a high-accuracy timer. A count clock is counted by the TCRmn register. Set the count value in the TDRmn register.

The same operation as that in timer mode of R8C/36M can be realized by using interval timer function in TAU of RL78/G14. In RL78/G14, each timer of a unit can be used as a reference timer that generates an interrupt (INTTMmn) at fixed intervals.

The same operation as that in programmable waveform generation mode of R8C/36M can be realized by using PWM (Pulse Width Modulation) output function in TAU of RL78/G14. In RL78/G14, two channels are used as a set to generate a pulse with a specified period and a specified duty factor.

The same operation as that in programmable one-shot generation mode and programmable wait one-shot generation mode of R8C/36M can be realized by using one-shot pulse output function in TAU of RL78/G14. In RL78/G14, two channels are used as a set to generate a one-shot pulse with a specified output timing and a specified pulse width. When there is a specified output timing, one-shot pulse output in RL78/G14 corresponds to programmable wait one-shot generation mode in R8C/36M Group. On the contrary, when there is no specified output timing, one-shot pulse output in RL78/G14 corresponds to programmable one-shot generation mode in R8C/36M Group.

Table 1.1 Operation Mode of Timer RB in R8C/36M

Timer RB in R8C/36M	
Mode	**Function**
Timer mode	The timer counts an internal count source (peripheral function clock or timer RA underflows).
Programmable waveform generation mode	The timer outputs pulses of a given width successively.
Programmable one-shot generation mode	The timer outputs a one-shot pulse.
Programmable wait one-shot generation mode	The timer outputs a delayed one-shot pulse.

Table 1.2 Operation Mode of TAU in RL78/G14

TAU in RL78/G14	
Mode	**Function**
Interval timer	**The timer array unit can be used as a reference timer that generates INTTMmn (timer interrupt) at fixed intervals.**
Square wave output	TOmn performs a toggle operation as soon as INTTMmn has been generated, and outputs a square wave with a duty factor of 50%.
External event counter	The timer array unit can be used as an external event counter that counts the number of times the valid input edge (external event) is detected in the TImn pin.
Divider	A clock input from a timer input pin (TI00) is divided and output from an output pin (TOm0).
Input pulse interval measurement	The count value can be captured at the TImn valid edge and the interval of the pulse input to TImn can be measured.
Measurement of high-/low-level width of input signal	By starting counting at one edge of the TImn pin input and capturing the number of counts at another edge, the signal width (high-level width/low-level width) of TImn can be measured.
Delay counter	It is possible to start counting down when the valid edge of the TImn pin input is detected (an external event), and then generate INTTMmn (a timer interrupt) after any specified interval.
One-shot pulse output	**By using two channels as a set, a one-shot pulse having any delay pulse width can be generated from the signal input to the TImn pin.**
PWM output	**Two channels can be used as a set to generate a pulse of any period and duty factor.**
Multiple PWM output	By extending the PWM function and using multiple slave channels, many PWM waveforms with different duty values can be output.

2. Differences between RL78/G14 and R8C/36M Group

2.1 Differences in Function Overview

Table 2.1 lists the differences between timer RB in R8C/36M Group and the TAU in RL78/G14.

Table 2.1 Differences

Item	R8C/36M Group Timer RB	RL78/G14 TAU
Configuration	8-bit timer with an 8-bit prescaler	16-bit timer Note 1
Count clock	f1, f2, f8, timer RA underflow	f_{TCLK} (between f_{CLK} to $f_{CLK}/2^{15}$)
Counters	• TRBPRE register • TRBPR register • TRBSC register	TCRmn register
Count value setting	• TRBPRE register • TRBPR register • TRBSC register	TDRmn register
Modes	• Timer mode • Programmable waveform generation mode • Programmable one-shot generation mode • Programmable wait one-shot generation mode	• Interval timer • Square wave output • External event counter • Divider (channel 0 in unit 0 only) • Input pulse interval measurement • Measurement of high-/low-level width of input signal • Delay counter • one-shot pulse output Note 2 • PWM output Note 2 • Multiple PWM output Note 2
Count operations	Decrement	• Count up Note 3 • Count down Note 3
Timer input	INT0 pin	• Channel 0 - Input from the TI00 pin - Event input signal from the ELC • Channel 1 - Input from the TI01 pin - Event input signal from the ELC - Low-speed on-chip oscillator clock (f_{IL}) - Subsystem clock (f_{SUB}) • Channel 2 - Input from the TI02 pin • Channel 3 - Input from the TI03 pin - RxD0 (Serial input pin)
I/O pin selection (output port)	Yes	No
Simultaneous channel operation function	No	Yes Note 2
Coordination with event link controller (ELC)	No	Yes

Notes: 1. Channels 1 and 3 can operate as 8-bit timers.
2. These modes are available by using a master channel to link with slave channels.
3. Count operations depend on modes specified.

2.2 Differences in Timer Mode

The interval timer in RL78/G14 corresponds to timer mode in R8C/36M Group.
Table 2.2 lists the differences between timer mode in R8C/36M Group and interval timer in RL78/G14.

Table 2.2 Differences between Timer Mode and Interval Timer

Item	R8C/36M Group (Timer Mode)	RL78/G14 (Interval Timer)
Count clock	f1, f2, f8, timer RA underflow	f_{TCLK} (between f_{CLK} to $f_{CLK}/2^{15}$)
Count operations	• Decrement • When the timer underflows, it reloads the reload register contents before the count continues (when timer RB underflows, the contents of timer RB primary reload register is reloaded).	No operation is carried out from start trigger detection (TSmn = 1) until count clock generation. The first count clock loads the value of the TDRmn register to the TCRmn register and the subsequent count clock performs count down operation.
Divide ratio	1/(n+1)(m+1) n: setting value in TRBPRE register, m: setting value in TRBPR register	Generation period of INTTMmn (timer interrupt) = Period of count clock × (Set value of TDRmn + 1)
Count start condition	1 (count starts) is written to the TSTART bit in the TRBCR register.	1 is written to the TSmn, TSHm1, or TSHm3 bit in the TSm register
Count stop conditions	• 0 (count stops) is written to the TSTART bit in the TRBCR register. • 1 (count forcibly stop) is written to the TSTOP bit in the TRBCR register.	1 is written to the TTmn, TTHm1, or TTHm3 bit in the TTm register
Read from timer	Read registers TRBPR and TRBPRE	Read the TCRmn register
Write to timer	Write to registers TRBPR and TRBPRE	Write to the TDRmn register

2.3 Differences in Programmable Waveform Generation Mode

Operation as PWM function in RL78/G14 corresponds to programmable waveform generation mode in R8C/36M Group.
Table 2.3 lists the differences between programmable waveform generation mode in R8C/36M Group and operation as PWM function in RL78/G14.

Table 2.3 Differences between Programmable Waveform Generation Mode and Operation as PWM Function

Item	R8C/36M Group (Programmable Waveform Generation Mode)	RL78/G14 (Operation as PWM Function)
Count clock	f1, f2, f8, timer RA underflow	f_{TCLK} (between f_{CLK} to $f_{CLK}/2^{15}$)
Count operations	• Decrement • When the timer underflows, it reloads the contents of the primary reload and secondary reload registers alternately before the count continues.	Two channels can be used as a set to generate a pulse of any period and duty factor. The master channel operates in the interval timer mode. The slave channel operates in one-count mode.
Width and period of output waveform	Primary period: (n+1)(m+1)/fi Secondary period: (n+1)(p+1)/fi Period: (n+1){(m+1)+(p+1)}/fi fi: Count source frequency n: Value set in TRBPRE register m: Value set in TRBPR register p: Value set in TRBSC register	Pulse period = {Set value of TDRmn (master) + 1} × Count clock period Duty factor [%] = {Set value of TDRmp (slave)}/{Set value of TDRmn (master) + 1} × 100
Count start condition	1 (count start) is written to the TSTART bit in the TRBCR register.	1 is written to the TSmn, TSHm1, or TSHm3 bit in the TSm register
Count stop conditions	• 0 (count stop) is written to the TSTART bit in the TRBCR register. • 1 (count forcibly stop) is written to the TSTOP bit in the TRBCR register.	1 is written to the TTmn, TTHm1, or TTHm3 bit in the TTm register
Interrupt request generation timing	In half a cycle of the count source, after timer RB underflows during the secondary period (at the same time as the TRBO output change) [timer RB interrupt]	Master channel: If the channel start trigger bit (TSmn) of timer channel start register m (TSm) is set to 1, an interrupt (INTTMmn) is output. Slave channel: By using INTTMmn from the master channel as a start trigger, the TCRmp register loads the value of the TDRmp register and the counter counts down to 0000H. When the counter reaches 0000H, it outputs INTTMmp.
Read from timer	Read registers TRBPR and TRBPRE	Read the registers TCRmn and TCRmp
Write to timer	Write to registers TRBPRE, TRBSC, and TRBPR	Write to the register TDRmn and TDRmp
Selectable functions	• Output level select function The output level during primary and secondary periods is selected by the TOPL bit in the TRBIOC register. • TRBO pin output switch function Timer RB pulse output or P3_1 (P1_3) latch output is selected by the TOCNT bit in the TRBIOC register.	• Whether the timer interrupt is generated when counting is started • Output pin level when pulse output is started

2.4 Differences in Programmable One-shot Generation Mode

Operation as one-shot pulse output function in RL78/G14 corresponds to programmable one-shot generation mode in R8C/36M Group.
Table 2.4 lists the differences between programmable one-shot generation mode in R8C/36M Group and operation as one-shot pulse output function in RL78/G14.

Table 2.4 Differences between Programmable One-shot Generation Mode and Operation as One-shot Pulse Output Function

Item	R8C/36M Group (Programmable One-shot Generation Mode)	RL78/G14 (Operation as One-shot Pulse Output Function)
Count clock	f1, f2, f8, timer RA underflow	f_{TCLK} (between f_{CLK} to $f_{CLK}/2^{15}$)
Count operations	• Decrement the setting value in the TRBPR register • When the timer underflows, it reloads the contents of the reload register before the count completes and the TOSSTF bit is set to 0 (one-shot stops). • When the count stops, the timer reloads the contents of the reload register before it stops.	By using two channels as a set, a one-shot pulse having any delay pulse width can be generated from the signal input to the TImn pin. The master channel operates in the one-count mode and counts the delays. The slave channel operates in the one-count mode and counts the pulse width.
One-shot pulse output time	(n+1)(m+1)/fi fi: Count source frequency n: Setting value in TRBPRE register m: Setting value in TRBPR register	Pulse width = {Set value of TDRmp (slave)} × Count clock period
Count start condition	• The TSTART bit in the TRBCR register is set to 1 (count starts) and the next trigger is generated • Set the TOSST bit in the TRBOCR register to 1 (one-shot starts) • Input trigger to the INT0 pin	Master channel: Timer count register mn (TCRmn) of the master channel starts operating upon start trigger detection. Slave channel: The TCRmp register of the slave channel starts operation using INTTMmn of the master channel as a start trigger.
Count stop conditions	• When reloading completes after timer RB underflows during primary period • When the TOSSP bit in the TRBOCR register is set to 1 (one-shot stops) • When the TSTART bit in the TRBCR register is set to 0 (stops counting) • When the TSTOP bit in the TRBCR register is set to 1 (forcibly stops counting)	Master channel: When TCRmn = 0000H, it outputs INTTMmn and stops counting until the next start trigger is detected. Slave channel: When count value = 0000H, it outputs INTTMmp and stops counting until the next start trigger (INTTMmn of the master channel) is detected.
Interrupt request generation timing	In half a cycle of the count source, after the timer underflows (at the same time as the TRBO output ends) [timer RB interrupt]	Master channel: When TCRmn = 0000H, it outputs INTTMmn. Slave channel: When count value = 0000H, it outputs INTTMmp.
Read from timer	Read registers TRBPR and TRBPRE	Read the registers TCRmn and TCRmp
Write to timer	Write registers TRBPRE and TRBPR	Write to the register TDRmn and TDRmp
Selectable functions	• Output level select function The output level of the one-shot pulse waveform is selected by the TOPL bit in the TRBIOC register. • One-shot trigger select function	• Output pin level when pulse output is started

2.5 Differences in Programmable Wait One-shot Generation Mode

Operation as one-shot pulse output function in RL78/G14 corresponds to programmable wait one-shot generation Mode in R8C/36M Group.
Table 2.5 and Table 2.6 list the differences between programmable wait one-shot generation mode in R8C/36M Group and operation as one-shot pulse output function in RL78/G14.

Table 2.5 Differences between Programmable Wait One-shot Generation Mode and Operation as One-shot Pulse Output Function (1/2)

Item	R8C/36M Group (Programmable Wait One-shot Generation Mode)	RL78/G14 (Operation as One-shot Pulse Output Function)
Count clock	f1, f2, f8, timer RA underflow	f_{TCLK} (between f_{CLK} to $f_{CLK}/2^{15}$)
Count operations	• Decrement the timer RB primary setting value. • When a count of the timer RB primary underflows, the timer reloads the contents of timer RB secondary before the count continues. • When a count of the timer RB secondary underflows, the timer reloads the contents of timer RB primary before the count completes and the TOSSTF bit is set to 0 (one-shot stops). • When the count stops, the timer reloads the contents of the reload register before it stops.	By using two channels as a set, a one-shot pulse having any delay pulse width can be generated from the signal input to the TImn pin. The master channel operates in the one-count mode and counts the delays. The slave channel operates in the one-count mode and counts the pulse width.
Wait time	(n+1)(m+1)/fi fi: Count source frequency n: Value set in the TRBPRE register m: Value set in the TRBPR register	Delay time = {Set value of TDRmn (master) + 2} × Count clock period
One-shot pulse output time	(n+1)(p+1)/fi fi: Count source frequency n: Value set in the TRBPRE register, p: Value set in the TRBSC register	Pulse width = {Set value of TDRmp (slave)} × Count clock period
Count start condition	• The TSTART bit in the TRBCR register is set to 1 (count starts) and the next trigger is generated • Set the TOSST bit in the TRBOCR register to 1 (one-shot starts) • Input trigger to the INT0 pin	Master channel: Timer count register mn (TCRmn) of the master channel starts operating upon start trigger detection. Slave channel: The TCRmp register of the slave channel starts operation using INTTMmn of the master channel as a start trigger.
Count stop conditions	• When reloading completes after timer RB underflows during secondary period. • When the TOSSP bit in the TRBOCR register is set to 1 (one-shot stops). • When the TSTART bit in the TRBCR register is set to 0 (starts counting). • When the TSTOP bit in the TRBCR register is set to 1 (forcibly stops counting).	Master channel: When TCRmn = 0000H, it outputs INTTMmn and stops counting until the next start trigger is detected. Slave channel: When count value = 0000H, it outputs INTTMmp and stops counting until the next start trigger (INTTMmn of the master channel) is detected.

Table 2.6 Differences between Programmable Wait One-shot Generation Mode and Operation as One-shot Pulse Output Function (2/2)

Item	R8C/36M Group (Programmable Wait One-shot Generation Mode)	RL78/G14 (Operation as One-shot Pulse Output Function)
Interrupt request generation timing	In half a cycle of the count source after timer RB underflows during secondary period (complete at the same time as waveform output from the TRBO pin) [timer RB interrupt]	Master channel: When TCRmn = 0000H, it outputs INTTMmn. Slave channel: When count value = 0000H, it outputs INTTMmp.
Read from timer	Read registers TRBPR and TRBPRE	Read the registers TCRmn and TCRmp
Write to timer	Write registers TRBPRE, TRBSC, and TRBPR	Write to the register TDRmn and TDRmp
Selectable functions	• Output level select function The output level of the one-shot pulse waveform is selected by the TOPL bit in the TRBIOC register. • One-shot trigger select function	• Output pin level when pulse output is started

2.6 Assigned I/O Pins

Table 2.7 lists the I/O pins assigned for use in R8C/36M Group.

Table 2.7 R8C/36M Group I/O Pins

Pin Name	Assigned Pins	I/O
TRBO	P1_3 or P3_1	output

Table 2.8 lists the I/O pins assigned for use in RL78/G14.

Table 2.8 RL78/G14 I/O Pins (64-pin products)

Unit Number	Target Channel	Pin Name	Assigned Pins	I/O
Unit 0	Channel 0	TI00	P00	Input
		TO00	P01	Output
	Channel 1	TI01	P16	Input
		TO01	P16	Output
	Channel 2	TI02	P17	Input
		TO02	P17	Output
	Channel 3	TI03	P31	Input
		TO03	P31	Output

2.7 Register Compatibility

Register compatibilities between timer RB in R8C/36M Group and TAU in RL78/G14 are listed in Table 2.9 and Table 2.10.

Table 2.9 Register Compatibility (1/2)

Item	R8C/36M Group	RL78/G14
Count start	• TRBCR register TSTART bit	• TSm register Bits TSmn, TSHm1, TSHm3 Note 1
Count status flag	• TRBCR register TCSTF bit	• TEm register Bits TEmn, TEHm1, TEHm3 Note 2
Count stop	• TRBCR register TSTART bit	• TTm register Bits TTmn, TTHm1, TTHm3 Note 3
Count forcible stop	• TRBCR register TSTOP bit	N/A
Pin Select	• TRBRCSR register TRBOSEL0 bit	• PMCxx register • PMxx register • Pxx register
One-shot trigger control	• TRBIOC register INOSTG bit	• TMRmn register Bits STSmn0 to STSmn2
One-shot trigger polarity select	• TRBIOC register INOSEG bit	• TMRmn register Bits STSmn0 to STSmn2
Operating mode select	• TRBMR register Bits TMOD0 and TMOD1	• TMRmn register Bits MDmn1 to MDmn3
Count clock select	• TRBMR register Bits TCK0 and TCK1	• TPSm register • TMRmn register Bits CKSmn0, CKSmn1, CCSmn
Count clock cutoff	• TRBMR register TCKCUT bit	N/A
Prescaler	• TRBPRE register	N/A
Timer	• TRBPR register (primary) • TRBSC register (secondary)	• Registers TCRmn, TDRmn (TCRmn: read-only, TDRmn: read/write)
Independent channel operation/simultaneous channel operation (slave/master) select	N/A	• TMRmn register Bits MASTERmn, SPLITmn Notes 4, 5
8-bit timer/16-bit timer select on channels 1 and 3	N/A	• TMRmn register SPLITmn bit Note 5
Count start and interrupt setting	N/A	• TMRmn register MDmn0 bit
Counter overflow status	N/A	• TSRmn register OVF bit
Timer input select on channels 1 and 3	N/A	• TIS0 register Bits TIS00 to TIS02, TIS04

Notes: 1. When channels 1 and 3 are in 8-bit timer mode, bits TSHm1 and TSHm3 are triggers to enable operation of (start) the higher 8-bit timer.
2. When channels 1 and 3 are in 8-bit timer mode, bits TEHm1 and TEHm3 indicate whether the higher 8-bit timer is enabled or stopped.
3. When channels 1 and 3 are in 8-bit timer mode, bits TTHm1 and TTHm3 are triggers to stop the higher 8-bit timer.
4. MASTERmn bit: n = 2
5. SPLITmn bit: n = 1, 3

Table 2.10 Register Compatibility (2/2)

Item	R8C/36M Group	RL78/G14
Timer output buffer	N/A	• TOm register TOmn bit
Timer output enable	• TRBIOC register TOCNT bit	• TOEm register TOEmn bit
Timer output level control	• TRBIOC register TOPL bit	• TOLm register TOLmn bit
Timer output mode control	N/A	• TOMm register TOMmn bit

3. How to migrate Timer RB in this sample code

In this sample program, the operation of Timer RB of R8C/36M group is realized with RL78/G14 by the method shown in Table 3.1.
For detailed contents of the sample program, please refer to "4. Example of Migration from Timer Mode" ~ "6. Example of Migration from Programmable Wait One-shot Generation mode".

Table 3.1 How to migrate from R8C/36M group to RL78/G14 in this sample program

Timer RB in R8C/36M	TAU in RL78/G14
Mode	Mode
Timer mode	Interval timer
Programmable waveform generation mode	PWM function
Programmable one-shot generation mode	One-shot pulse output function
Programmable wait one-shot generation mode	

4. Example of Migration from Timer Mode

4.1 Specifications

When implementing timer mode of Timer RB in R8C/36M, RL78/G14 can use interval timer of TAU.
Timer interrupt (INTTMmn) is generated at fixed intervals.

Table 4.1 lists the peripheral functions to be used and their uses (example of migration from timer mode), and Figure 4.1 shows the operation overview (example of migration from timer mode).

Table 4.1 Peripheral Functions to be Used and Their Uses (Example of Migration from Timer Mode)

Peripheral Function	Use
Timer array unit (interval timer)	Timer interrupt (INTTMmn) is generated at fixed intervals

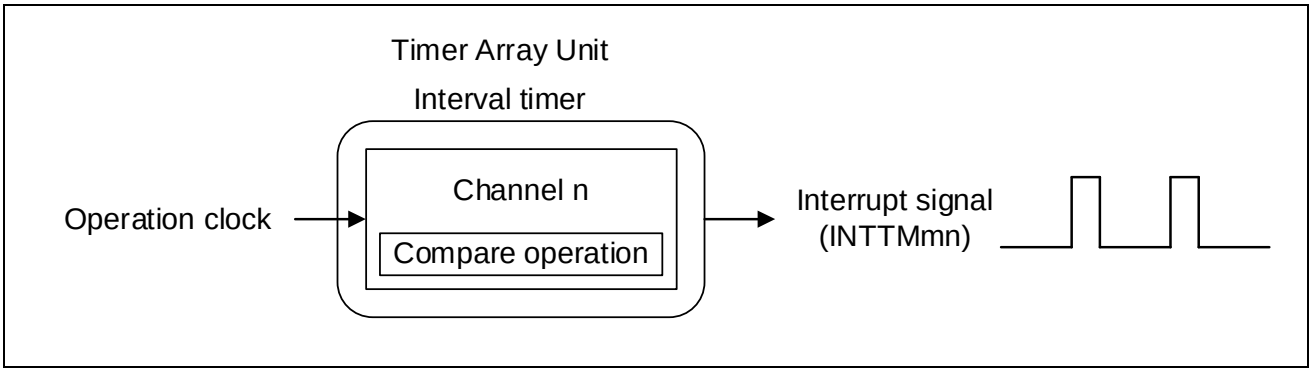

Figure 4.1 Operation Overview (Example of Migration from Timer Mode)

4.2 Operation Check Conditions

The sample code described in this application note has been checked under the conditions listed in the table below.

Table 4.2 Operation Check Conditions

Item	Description
Microcontroller used	RL78/G14 (R5F104LEAFB)
Operating frequency	High-speed on-chip oscillator (HOCO) clock: 32 MHz CPU/peripheral hardware clock: 32 MHz
Operating voltage	5.0V (can run on a voltage range of 2.9 V to 5.5 V.) LVD operation (V_{LVD}): Reset mode 2.81 V (2.76 V to 2.87 V)
Integrated development environment (CS+)	CS+ V4.01.00 from Renesas Electronics Corp.
C compiler (CS+)	CC-RL V1.03.00 from Renesas Electronics Corp.
Integrated development environment (e^2 studio)	e^2 studio V5.2.0.020 from Renesas Electronics Corp.
C compiler (e^2 studio)	CC-RL V1.03.00 from Renesas Electronics Corp.

4.3 Description of Hardware

4.3.1 Hardware Configuration Example

Figure 4.2 shows an example of hardware configuration that is used for this application note.

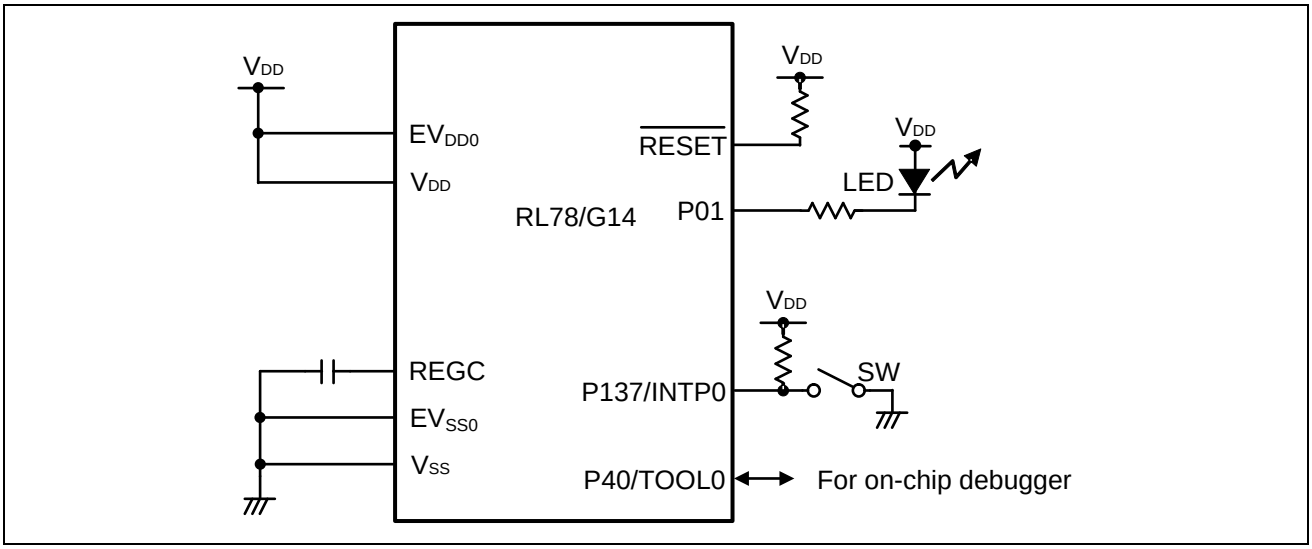

Figure 4.2 Hardware Configuration

Cautions: 1. The purpose of this circuit is only to provide the connection outline and the circuit is simplified accordingly. When designing and implementing an actual circuit, provide proper pin treatment and make sure that the hardware's electrical specifications are met (connect the input-only ports separately to V_{DD} or V_{SS} via a resistor).

2. Connect any pins whose name begins with EV_{SS} to V_{SS} and any pins whose name begins with EV_{DD} to V_{DD}, respectively.
3. V_{DD} must be held at not lower than the reset release voltage (V_{LVD}) that is specified as LVD.

4.3.2 List of Pins to be used

Table 4.3 lists the pins to be used and their functions.

Table 4.3 Pins to be Used and Their Functions

Pin Name	I/O	Description
P01	Output	Output port for LED indications
P137/INTP0	Input	Switch (SW) input pin (external interrupt request input pin)

4.4 Description of Software

4.4.1 Operation Outline

This chapter describes how to set up the interval timer function of TAU0.
This setup is followed by operation for counting the number of timer interrupts (INTTM00) generated by the interval timer. Each time the count reaches 250, the LED indication is inverted. The timer interrupt (INTTM00) cycle time is changed according to the number of times the switch is pressed. The LED on/off cycle time is changed as follows.
500 ms → 250 ms → 125 ms → 62.5 ms → 500 ms → …

Table 4.4 lists the peripheral functions to be used and their uses. Figure 4.3 shows the timer and its interrupt operation.

(1) Initialize the TAU.
Use the interval timer mode as the timer operation mode.
Initialize timer data register 00 (TDR00) to 2 ms.
Set the timer output enable register to disable operation.
Use timer interrupts (INTTM00) from timer channel 0.

(2) Initialize the external edge detection interrupt.
Select a falling edge as the valid edge for INTP0.
Use INTP0 interrupts.

(3) Execute a HALT instruction to wait for timer interrupts (INTTM00).

(4) After the HALT mode is cancelled by a timer interrupt (INTTM00), the number of INTTM00 interrupts generated is counted.

(5) When the timer interrupt count reaches 250, the LED indication is inverted. The value (g_TDR00_Work) in RAM for the timer data register is set in the timer data register (TDR00).

(6) INTP0 interrupt processing changes the switch input count (INTP0 interrupt count) and g_TDR00_Work value.

Table 4.4 Peripheral Functions to be Used and Their Uses

Peripheral Function	Use
Timer array unit (channel 0)	Time interval control for inversion of the P01 pin output (LED indication)

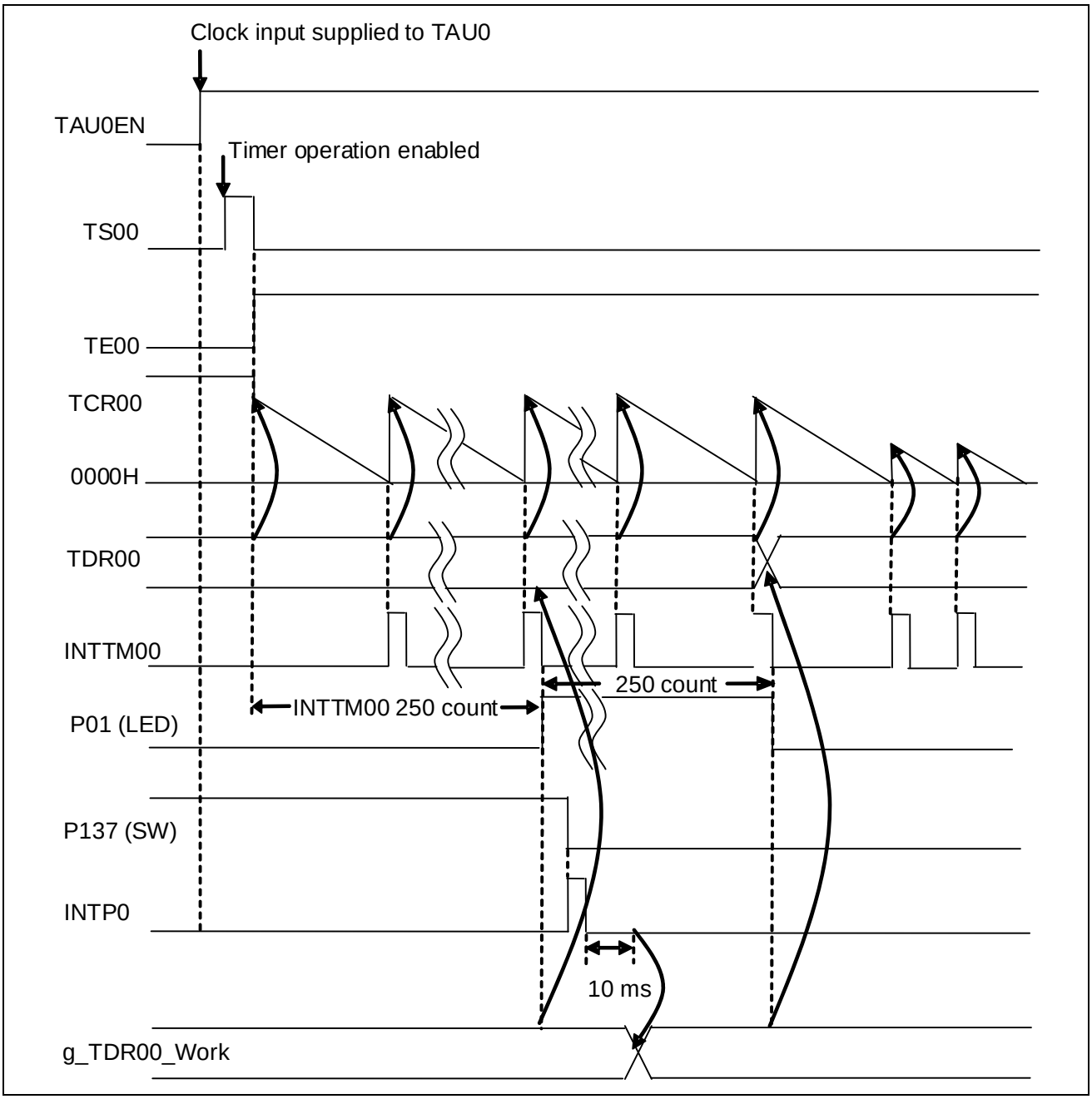

Figure 4.3 Overview of Timer Operation and Interrupts

4.4.2 List of Option Byte Setting

Table 4.5 summarizes the settings of the option bytes.

Table 4.5 Option Byte Settings

Address	Value	Description
000C0H/010C0H	01101110B	Disables the watchdog timer. (Stops counting after the release from the reset state.)
000C1H/010C1H	01111111B	LVD reset mode, 2.81 V (2.76 V to 2.87 V)
000C2H/010C2H	11101000B	HS mode, HOCO: 32 MHz
000C3H/010C3H	10000100B	Enables the on-chip debugger.

4.4.3 List of Constant

Table 4.6 lists the constants that are used in this sample program.

Table 4.6 Constants for the Sample Program

Constant	Setting	Description
_01_INTP0_EDGE_FALLING_SEL	01h	Selects a falling edge as the valid edge of INTP0.
g_TDR00_Data[]	(64000-1) (32000-1) (16000-1) (8000-1)}	TDR00 settings by number of times the switch is pressed
g_10msCount[]	(5+1) (10+1) (20+1) (40+1)	10 ms timer count values by number of times the switch is pressed

4.4.4 List of Variables

Table 4.7 lists the global variables that are used in this sample program.

Table 4.7 Global Variables for the Sample Program

Type	Variable Name	Contents	Function Used
uint8_t	g_SW_Counter	Switch press count	r_intc0_interrupt() main() R_InvertLED_interrupt()
uint16_t	g_TDR00_Work	Value which is set in TDR00 each time the timer interrupt count reaches 250.	r_intc0_interrupt() main() R_InvertLED_interrupt()
uint8_t	g_inttm00counter	Variable for counter of INTTM00	r_intc0_interrupt() main() R_InvertLED_interrupt()

4.4.5 List of Functions

Table 4.8 lists the functions that are used in this sample program.

Table 4.8 Functions

Function Name	Outline
R_TAU0_Channel0_Start()	Starts operation of TAU0 channel 0.
r_tau0_channel0_interrupt()	Processes timer interrupts on TAU0 channel 0.
R_InvertLED_interrupt()	Counts the number of INTTM00 interrupts generated. Inverts the LED indication each time the interrupt count reaches 250.
R_INTC0_Start()	Enables INTP0 interrupts.
r_intc0_interrupt()	Processes INTP0 interrupts.

4.4.6 Function Specification

The followings are the functions that are used in this sample program.

[Function Name] R_TAU0_Channel0_Start()

Synopsis	TAU0 channel 0 operation start
Header	r_cg_macrodriver.h r_cg_timer.h r_cg_userdefine.h
Declaration	void R_TAU0_Channel0_Start(void)
Explanation	This function unmasks TAU0 channel 0 interrupts and starts count operation.
Arguments	None
Return value	None
Remarks	None

[Function Name] r_tau0_channel0_interrupt()

Synopsis	TAU0 channel 0 timer interrupt processing
Header	r_cg_macrodriver.h r_cg_timer.h r_cg_userdefine.h
Declaration	static void __near r_tau0_channel0_interrupt(void)
Explanation	This function calls the function which will invert the LED indication.
Arguments	None
Return value	None
Remarks	None

[Function Name] R_InvertLED_interrupt()

Synopsis	LED indication inversion processing
Header	r_cg_macrodriver.h r_cg_cgc.h r_cg_port.h r_cg_intc.h r_cg_timer.h r_cg_userdefine.h
Declaration	void R_InvertLED_interrupt(void)
Explanation	This function counts 250 timer interrupts (INTTM00) and then inverts the LED indication (for port latch inversion). It also changes the TDR00 setting to the value specified with g_TDR00_Work.
Arguments	None
Return value	None
Remarks	None

[Function Name] R_INTC0_Start()

Synopsis	INTP0 interrupt enable
Header	r_cg_intc.h
Declaration	void R_INTC0_Start(void)
Explanation	This function clears the interrupt request flag. It enables INTP0 interrupts and starts taking in the switch input.
Arguments	None
Return value	None
Remarks	None

[Function Name] r_intc0_interrupt()

Synopsis	INTP0 interrupt processing
Header	r_cg_macrodriver.h r_cg_intc.h r_cg_userdefine.h
Declaration	static void __near r_intc0_interrupt(void)
Explanation	This function processes INTP0 interrupts as they occur. It waits 10 ms and then scans P137 (SW input pin). When the switch is pressed, this function changes the g_TDR00_Work value.
Arguments	None
Return value	None
Remarks	None

4.4.7 Flow Chart

4.4.7.1 Overall Flow

Figure 4.4 shows the overall flow of the sample program described in this chapter.

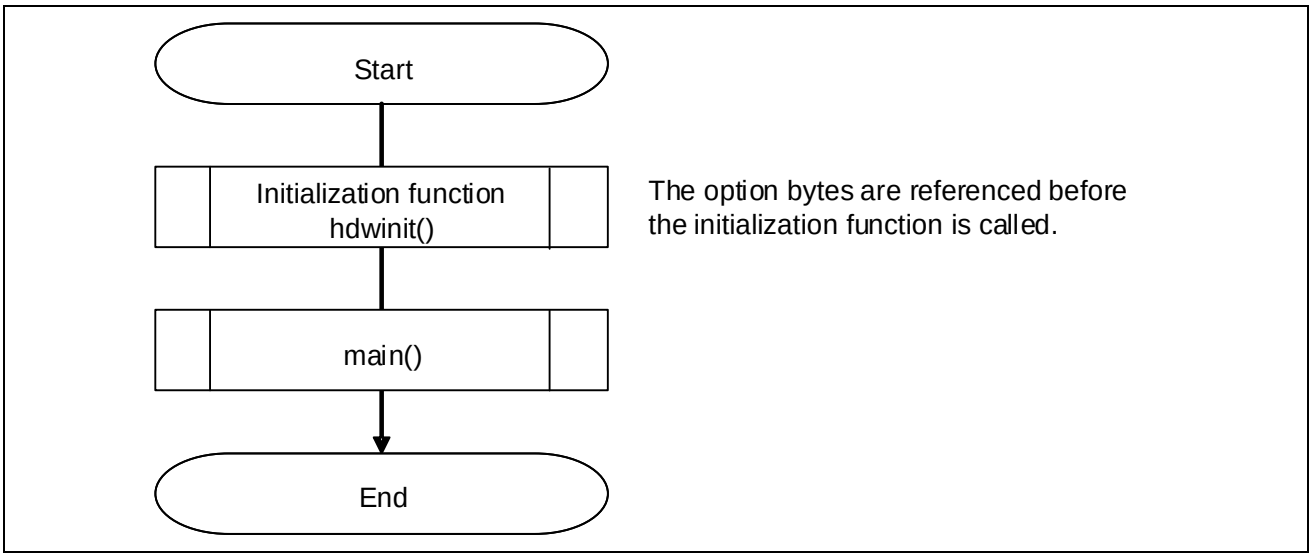

Figure 4.4 Overall Flow

4.4.7.2 Initialization Function

Figure 4.5 shows the flowchart for the initialization function.

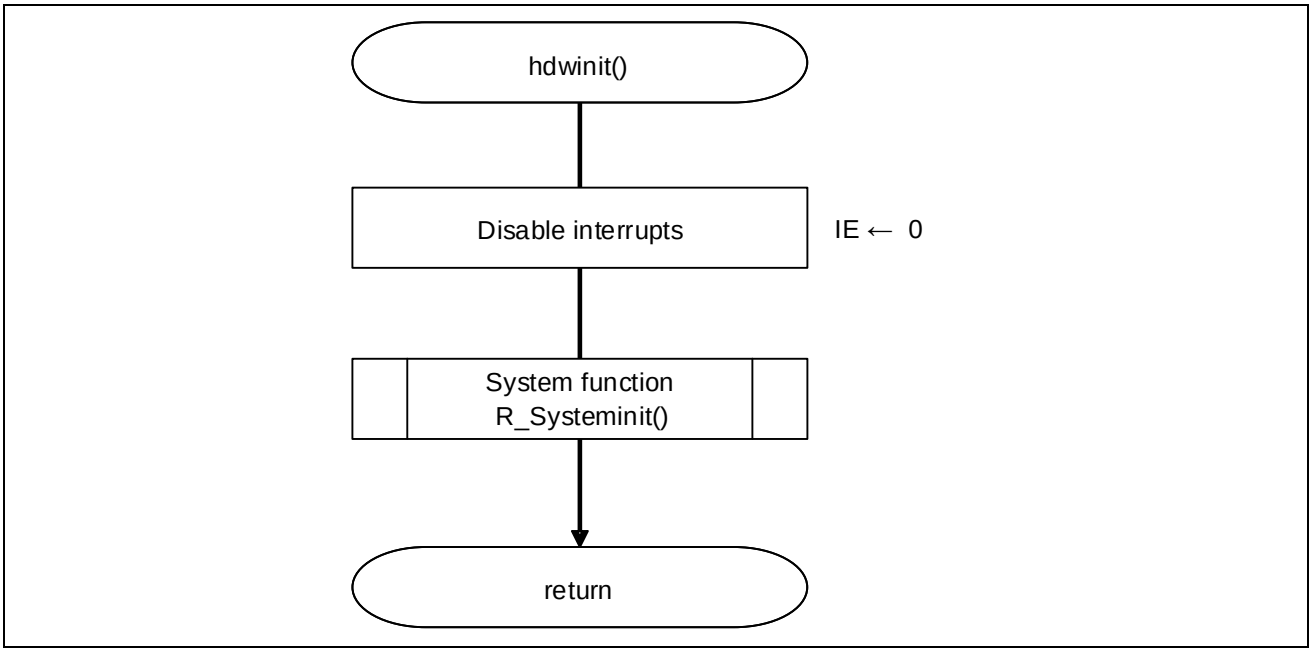

Figure 4.5 Initialization Function

4.4.7.3 System Function

Figure 4.6 shows the flowchart for the system function.

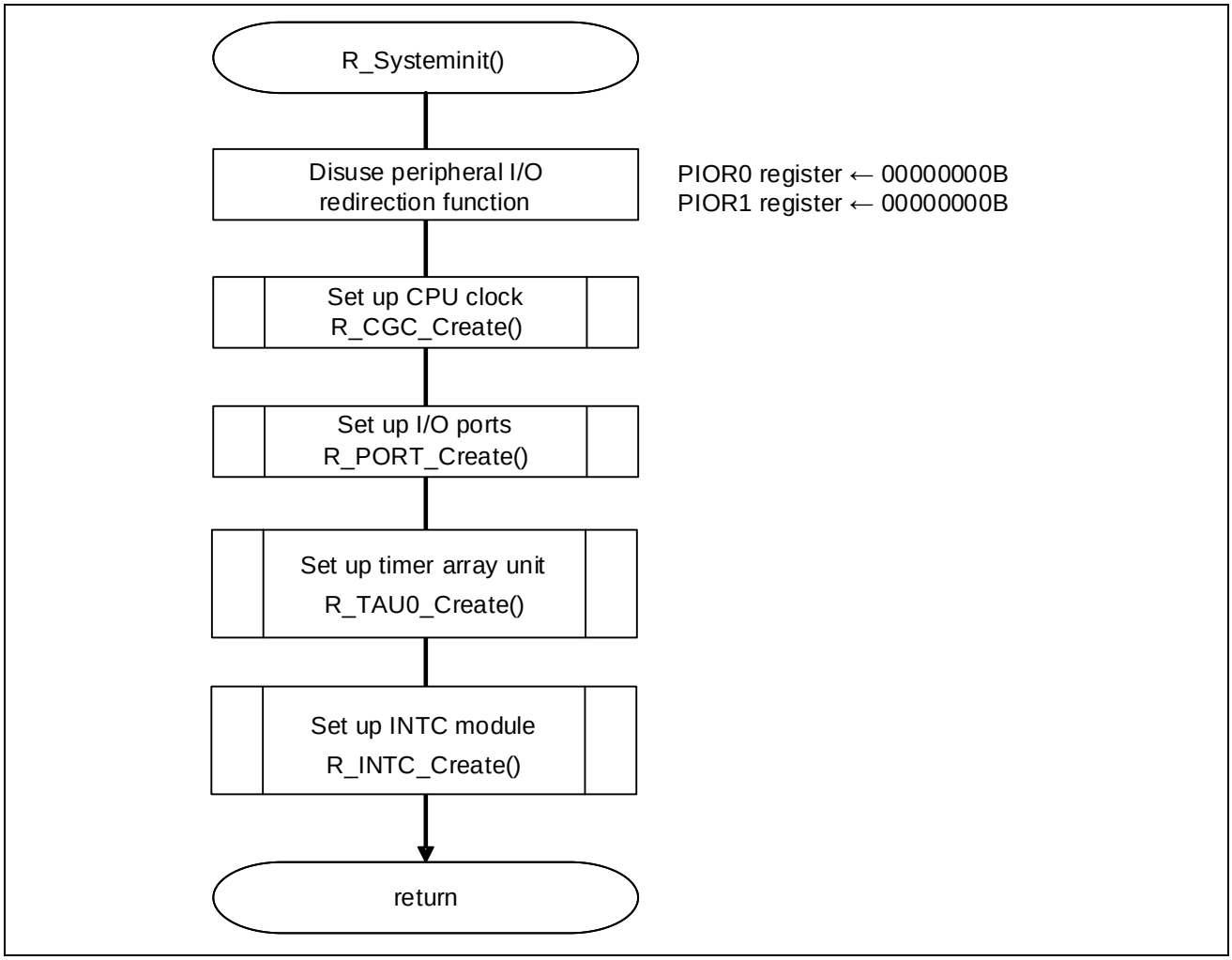

Figure 4.6 System Function

4.4.7.4 CPU Clock Setup

Figure 4.7 shows the flowchart for setting up the CPU clock.

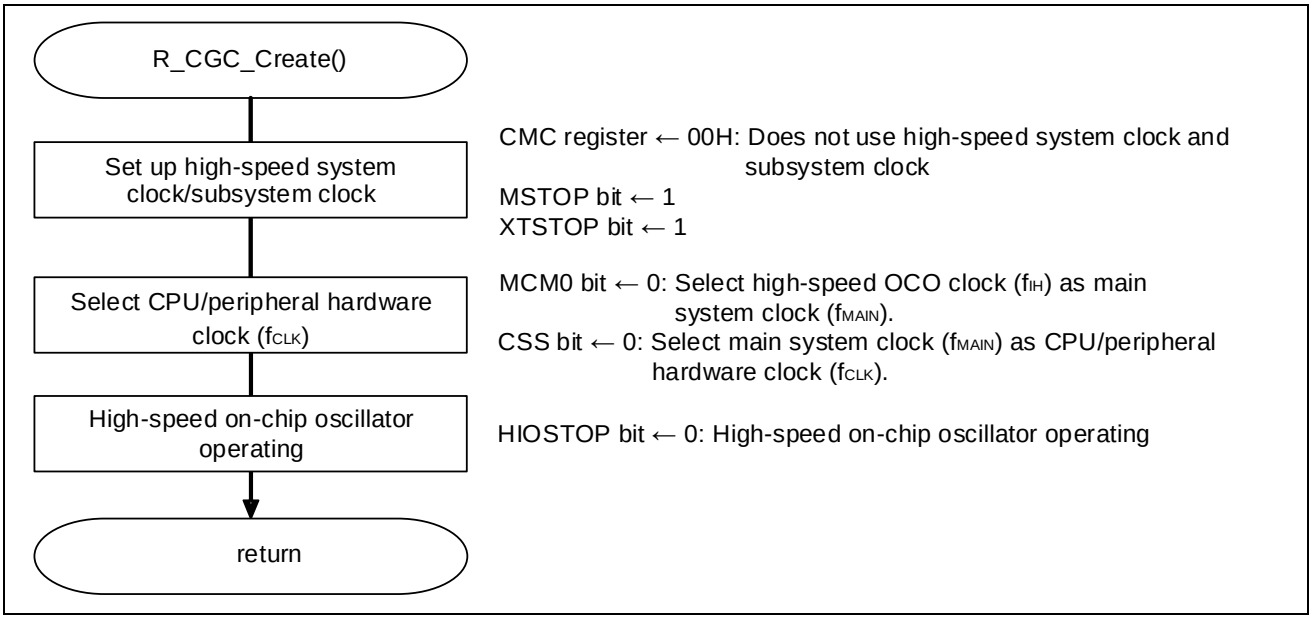

Figure 4.7 CPU Clock Setup

4.4.7.5 I/O Port Setup

Figure 4.8 shows the flowchart for setting up the I/O ports.

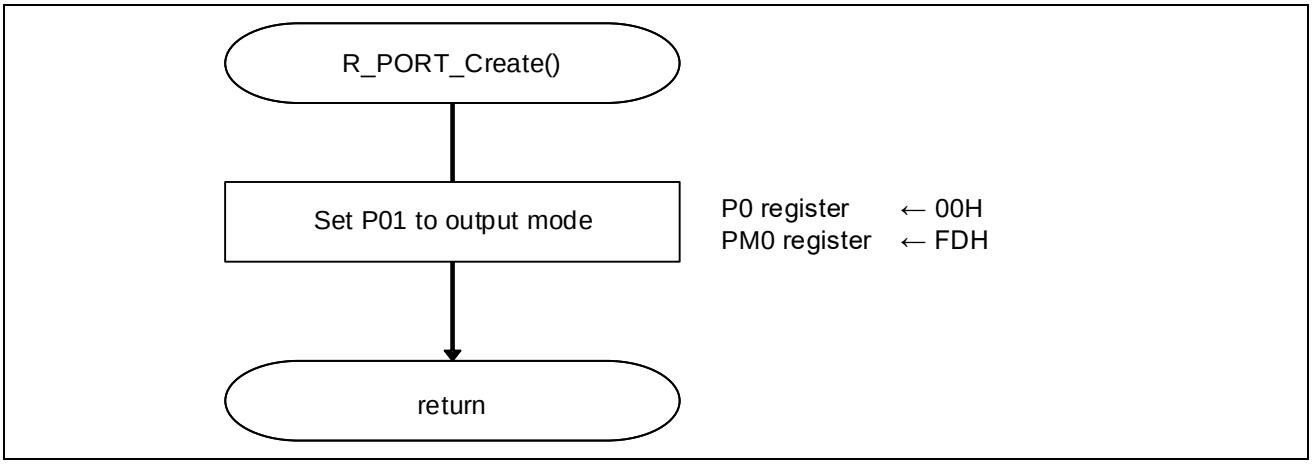

Figure 4.8 I/O Port Setup

Caution: Provide proper treatment for unused pins so that their electrical specifications are observed. Connect each of any unused input-only ports to V_{DD} or V_{SS} via a separate resistor.

Setting up the LED port

• Port register 0 (P0)
Set the output latch value.

Symbol: P0

7	6	5	4	3	2	1	0
0	**P06**	**P05**	**P04**	**P03**	**P02**	**P01**	**P00**
0	x	x	x	x	x	**0**	x

Bit 1

P01	Output data control (in output mode)
0	**Output 0**
1	Output 1

• Port mode register 0 (PM0)
Select I/O mode for the port.

Symbol: PM0

7	6	5	4	3	2	1	0
1	**PM06**	**PM05**	**PM04**	**PM03**	**PM02**	**PM01**	**PM00**
1	x	x	x	x	x	**0**	x

Bit 1

PM01	P01 pin I/O mode selection
0	**Output mode (output buffer on)**
1	Input mode (output buffer off)

Caution: For details on the register setup procedures, refer to RL78/G14 User's Manual: Hardware.

x: Bits not used in this setting item

4.4.7.6 Timer Array Unit Setup

Figure 4.9 shows the flowchart for setting up the timer array unit.

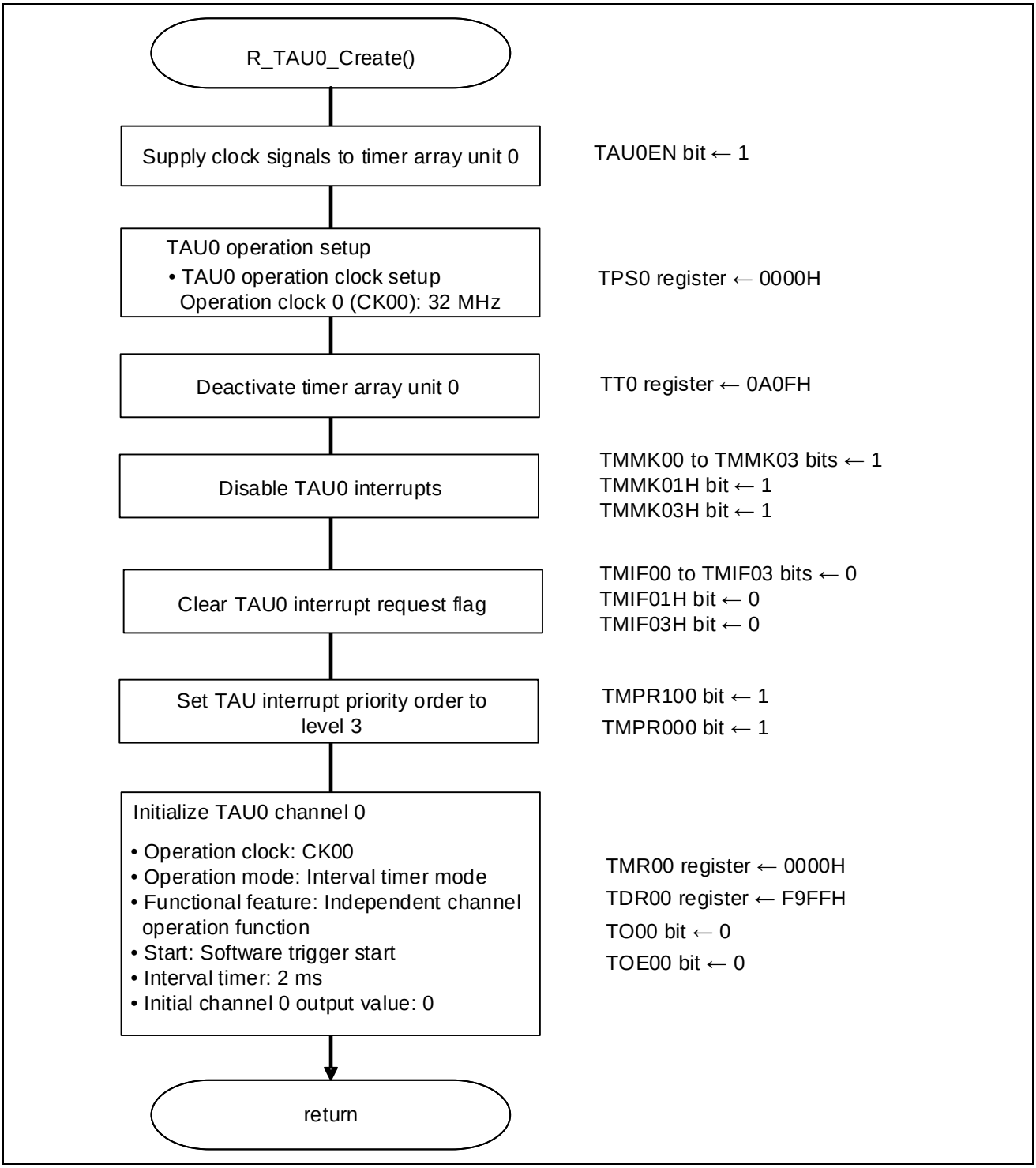

Figure 4.9 Timer Array Unit Setup

Starting clock signal supply to the timer array unit 0

• Peripheral enable register 0 (PER0)

Start supplying clock signals to the timer array unit 0.

Symbol: PER0

7	6	5	4	3	2	1	0
RTCEN	IICA1EN	ADCEN	IICA0EN	SAU1EN	SAU0EN	TAU1EN	TAU0EN
x	x	x	x	x	x	x	**1**

Bit 0

TAU0EN	Control of timer array unit 0 input clock supply
0	Stops input clock supply.
1	**Enables input clock supply.**

Caution: For details on the register setup procedures, refer to RL78/G14 User's Manual: Hardware.

x: Bits not used in this setting item

Configuring the timer clock frequency

• Timer clock select register 0 (TPS0)

Select an operation clock for timer array unit 0.

Symbol: TPS0

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	PRS 031	PRS 030	0	0	PRS 021	PRS 020	PRS 013	PRS 012	PRS 011	PRS 010	PRS 003	PRS 002	PRS 001	PRS 000
0	0	x	x	0	0	x	x	x	x	x	x	0	0	0	0

Bits 3 to 0

PRS 003	PRS 002	PRS 001	PRS 000	Operation clock (CK00) selection					
					f_{CLK}= 2 MHz	f_{CLK}= 4 MHz	f_{CLK}= 8 MHz	f_{CLK}= 20 MHz	f_{CLK}= 32 MHz
0	0	0	0	f_{CLK}	2 MHz	4 MHz	8 MHz	20 MHz	32 MHz
0	0	0	1	$f_{CLK}/2$	1 MHz	2 MHz	4 MHz	10 MHz	16 MHz
0	0	1	0	$f_{CLK}/2^2$	500 kHz	1 MHz	2 MHz	5 MHz	8 MHz
0	0	1	1	$f_{CLK}/2^3$	250 kHz	500 kHz	1 MHz	2.5 MHz	4 MHz
0	1	0	0	$f_{CLK}/2^4$	125 kHz	250 kHz	500 kHz	1.25 MHz	2 MHz
0	1	0	1	$f_{CLK}/2^5$	62.5 kHz	125 kHz	250 kHz	625 kHz	1 MHz
0	1	1	0	$f_{CLK}/2^6$	31.3 kHz	62.5 kHz	125 kHz	313 kHz	500 kHz
0	1	1	1	$f_{CLK}/2^7$	15.6 kHz	31.3 kHz	62.5 kHz	156 kHz	250 kHz
1	0	0	0	$f_{CLK}/2^8$	7.81 kHz	15.6 kHz	31.3 kHz	78.1 kHz	125 kHz
1	0	0	1	$f_{CLK}/2^9$	3.91 kHz	7.81 kHz	15.6 kHz	39.1 kHz	62.5 kHz
1	0	1	0	$f_{CLK}/2^{10}$	1.95 kHz	3.91 kHz	7.81 kHz	19.5 kHz	31.25 kHz
1	0	1	1	$f_{CLK}/2^{11}$	977 Hz	1.95 kHz	3.91 kHz	9.77 kHz	15.6 kHz
1	1	0	0	$f_{CLK}/2^{12}$	488 Hz	977 Hz	1.95 kHz	4.88 kHz	7.81 kHz
1	1	0	1	$f_{CLK}/2^{13}$	244 Hz	488 Hz	977 Hz	2.44 kHz	3.91 kHz
1	1	1	0	$f_{CLK}/2^{14}$	122 Hz	244 Hz	488 Hz	1.22 kHz	1.95 kHz
1	1	1	1	$f_{CLK}/2^{15}$	61.0 Hz	122 Hz	244 Hz	610 Hz	977 Hz

Caution: For details on the register setup procedures, refer to RL78/G14 User's Manual: Hardware

x: Bits not used in this setting item

Setting up the channel 0 operation mode

• Timer mode register 00 (TMR00)
Select an operation clock (f_{MCK}).
Select a count clock.
Select a start trigger and capture trigger.
Select a valid edge for timer input.
Set up the operation mode.

Symbol: TMR00

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CKS 001	CKS 000	0	CCS 00	0	STS 002	STS 001	STS 000	CIS 001	CIS 000	0	0	MD 003	MD 002	MD 001	MD 000
0	0	0	0	0	x	x	x	x	x	0	0	0	0	0	0

Bits 15 and 14

CKS001	CKS000	Selection of operation clock (f_{MCK}) of channel 0
0	0	Operation clock CK00 set by timer clock select register 0 (TPS0)
0	1	Operation clock CK02 set by timer clock select register 0 (TPS0)
1	0	Operation clock CK01 set by timer clock select register 0 (TPS0)
1	1	Operation clock CK03 set by timer clock select register 0 (TPS0)

Bit 12

CCS00	Selection of count clock (f_{TCLK}) of channel 0
0	Operation clock (f_{MCK}) specified by the CKS000 and CKS001 bits
1	Valid edge of input signal input from the TI00 pin

Caution: For details on the register setup procedures, refer to RL78/G14 User's Manual: Hardware.
x: Bits not used in this setting item

Symbol: TMR00

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CKS001	CKS000	0	CCS00	0	STS002	STS001	STS000	CIS001	CIS000	0	0	MD003	MD002	MD001	MD000
0	0	0	0	0	x	x	x	x	x	0	0	0	0	0	0

Bits 3 to 0

MD003	MD002	MD001	MD000	Operation mode of channel 0	Corresponding function	Count operation of TCR
0	0	0	1/0	Interval timer mode	Interval timer / Square wave output / Divider function / PWM output (master)	Counting down
0	1	0	1/0	Capture mode	Input pulse interval measurement	Counting up
0	1	1	0	Event counter mode	External event counter	Counting down
1	0	0	1/0	One-count mode	Delay counter / One-shot pulse output / PWM output (slave)	Counting down
1	1	0	0	Capture & one-count mode	Measurement of high-/low-level width of input signal	Counting up
Other than above				Setting prohibited		

The operation of each mode varies depending on MD000 bit (see table below).

Operation mode (Value set by the MD003 to MD001 bits (see table above))	MD000	Setting of starting counting and interrupt
• Interval timer mode (0, 0, 0) • Capture mode (0, 1, 0)	0	Timer interrupt is not generated when counting is started (timer output does not change, either).
	1	Timer interrupt is generated when counting is started (timer output also changes).
• Event counter mode (0, 1, 1)	0	Timer interrupt is not generated when counting is started (timer output does not change, either).
• One-count mode (1, 0, 0)	0	Start trigger is invalid during counting operation. At that time, interrupt is not generated.
	1	Start trigger is valid during counting operation. At that time, interrupt is not generated.
• Capture & one-count mode (1, 1, 0)	0	Timer interrupt is not generated when counting is started (timer output does not change, either). Start trigger is invalid during counting operation. At that time, interrupt is not generated.
Other than above		Setting prohibited

Caution: For details on the register setup procedures, refer to RL78/G14 User's Manual: Hardware.
x: Bits not used in this setting item

Configuring the interval timer cycle time
• Timer data register 00 (TDR00)
Configure the interval timer compare value.

Symbol: TDR00

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Timer interrupt (INTTM00) occurrence = (TDR00 setting + 1) × Count clock cycle time

Configuring the output value for the timer output pin
• Timer output register 0 (TO0)
Configure the output value for the timer output pin for each channel.

Symbol: TO0

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**TO03**	**TO02**	**TO01**	**TO00**
0	0	0	0	0	0	0	0	0	0	0	0	x	x	x	**0**

Bit 0

TO00	Timer output of channel 0
0	**Timer output value is “0”**
1	Timer output value is “1”

Enabling the timer output
• Timer output enable register 0 (TOE0)
Enable/disable the timer output for each channel.

Symbol: TOE0

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**TOE03**	**TOE02**	**TOE01**	**TOE00**
0	0	0	0	0	0	0	0	0	0	0	0	x	x	x	**0**

Bit 0

TOE00	Timer output enable/disable of channel 0
0	**Timer output is disabled.** **Timer operation is not applied to the TO00 bit and the output is fixed.** **Writing to the TO00 bit is enabled and the level set in the TO00 bit is output from the TO00 pin.**
1	Timer output is enabled. Timer operation is applied to the TO00 bit and an output waveform is generated. Writing to the TO00 bit is ignored.

Caution: For details on the register setup procedures, refer to RL78/G14 User's Manual: Hardware.
x: Bits not used in this setting item

4.4.7.7 INTP0 Initialization

Figure 4.10 shows the flowchart for INTP0 initialization.

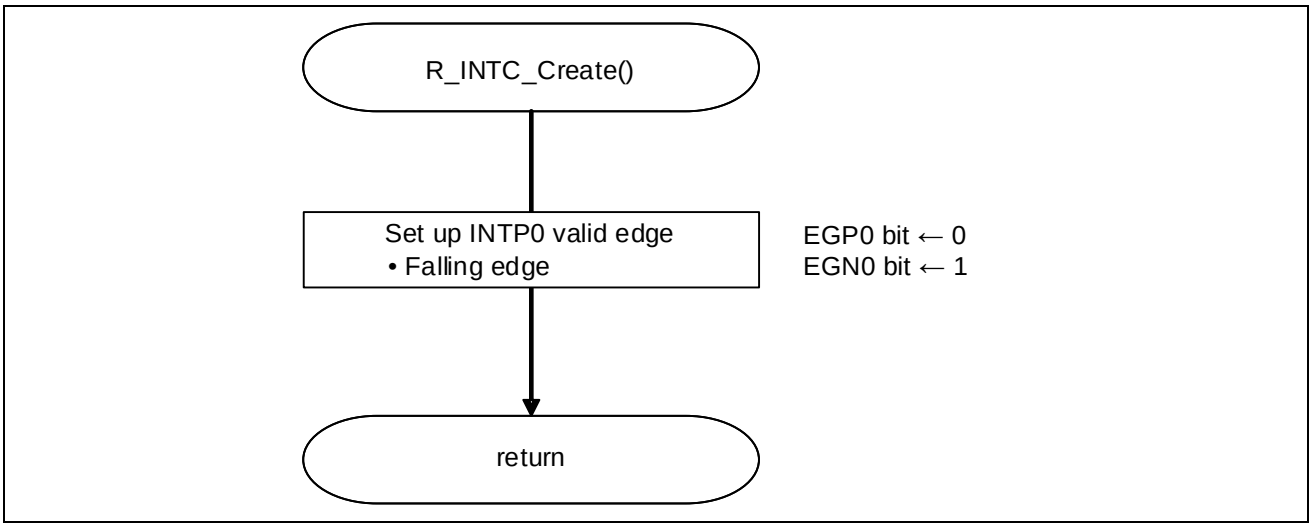

Figure 4.10 INTP0 Initialization

Setup for INTP0 pin edge detection
- External interrupt rising edge enable register (EGP0)
- External interrupt falling edge enable register (EGN0)

Select a valid edge for INTP0

Symbol: EGP0

7	6	5	4	3	2	1	0
EGP7	**EGP6**	**EGP5**	**EGP4**	**EGP3**	**EGP2**	**EGP1**	**EGP0**
x	x	x	x	x	x	x	**0**

Symbol: EGN0

7	6	5	4	3	2	1	0
EGN7	**EGN6**	**EGN5**	**EGN4**	**EGN3**	**EGN2**	**EGN1**	**EGN0**
x	x	x	x	x	x	x	**1**

Bit 0

EGP0	EGN0	INTP0 pin valid edge selection
0	0	Edge detection disabled
0	**1**	**Falling edge**
1	0	Rising edge
1	1	Both rising and falling edges

Caution: For details on the register setup procedures, refer to RL78/G14 User's Manual: Hardware.
x: Bits not used in this setting item

4.4.7.8 Main Processing

Figure 4.11 shows the flowchart for main processing.

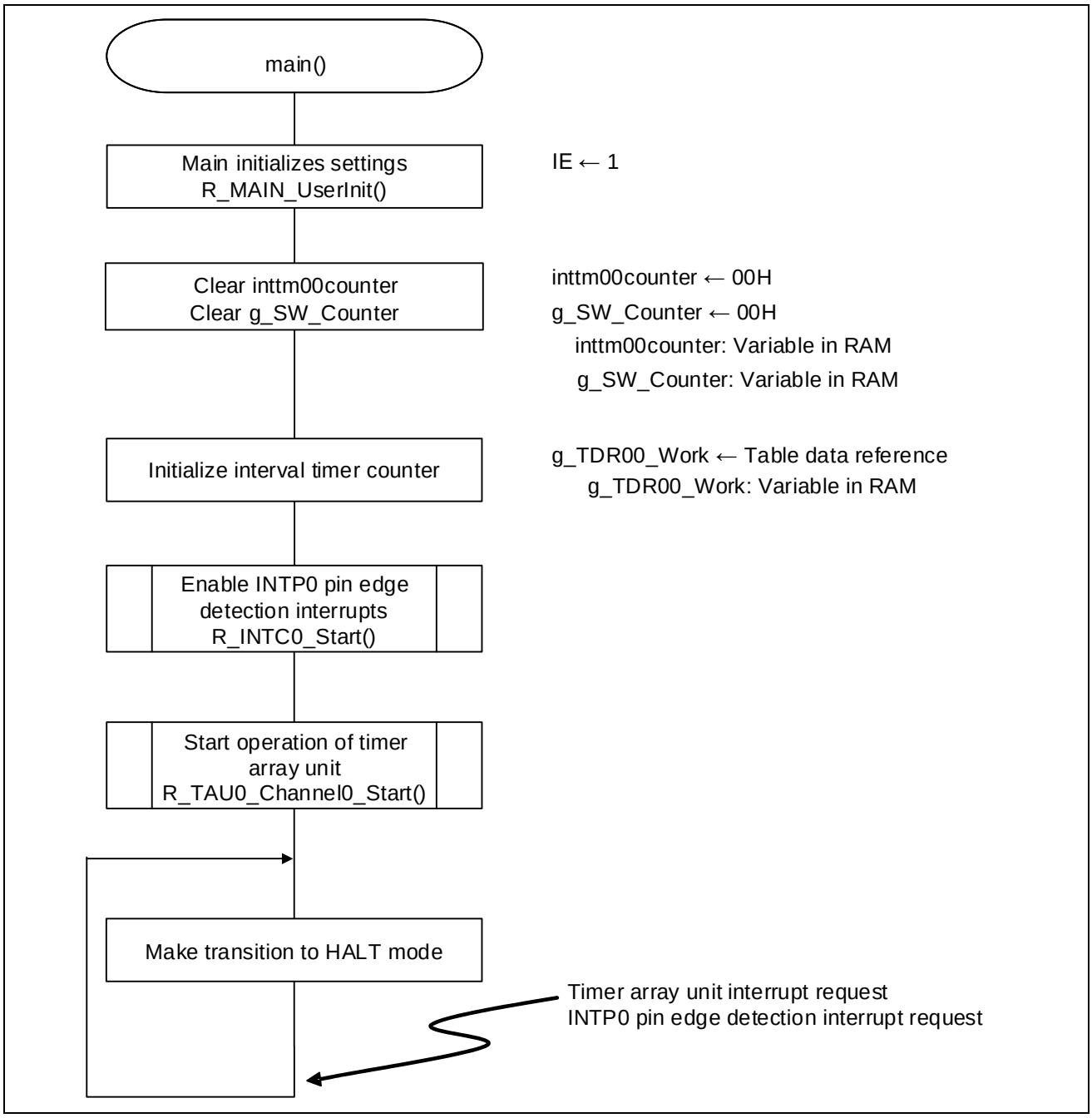

Figure 4.11 Main Processing

4.4.7.9 INTP0 Operation Start

Figure 4.12 shows the flowchart for starting INTP0 operation.

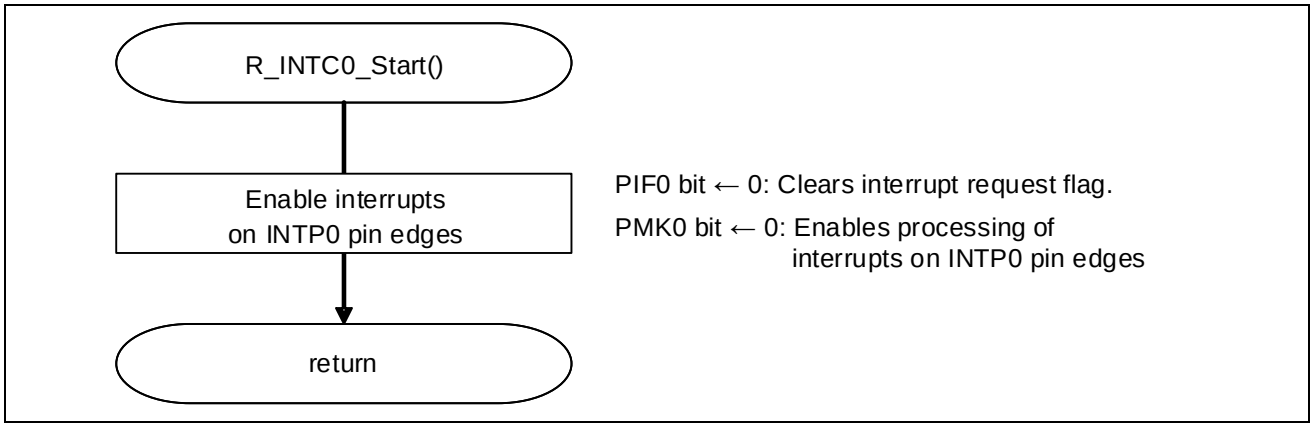

Figure 4.12 INTP0 Operation Start

Setup for INTP0 Interrupts
- Interrupt request flag register (IF0L)
  Clear interrupt request flag.
- Interrupt mask flag register (MK0L)
  Clear interrupt mask.

Symbol: IF0L

7	6	5	4	3	2	1	0
PIF5	PIF4	PIF3	PIF2	PIF1	PIF0	LVIIF	WDTIIF
x	x	x	x	x	0	x	x

Bit 2

PIF0	Interrupt request flag
0	No interrupt request signal is generated
1	Interrupt request is generated, interrupt request status

Symbol: MK0L

7	6	5	4	3	2	1	0
PMK5	PMK4	PMK3	PMK2	PMK1	PMK0	LVIMK	WDTIMK
x	x	x	x	x	0	x	x

Bit 2

PMK0	Interrupt servicing control
0	Interrupt servicing enabled
1	Interrupt servicing disabled

Caution: For detailed information about setting the registers, see RL78/G14 User's Manual: Hardware.
x: Bits not used in this setting item

4.4.7.10 Timer Array Unit 0 Operation Start

Figure 4.13 shows the flowchart for starting timer array unit operation.

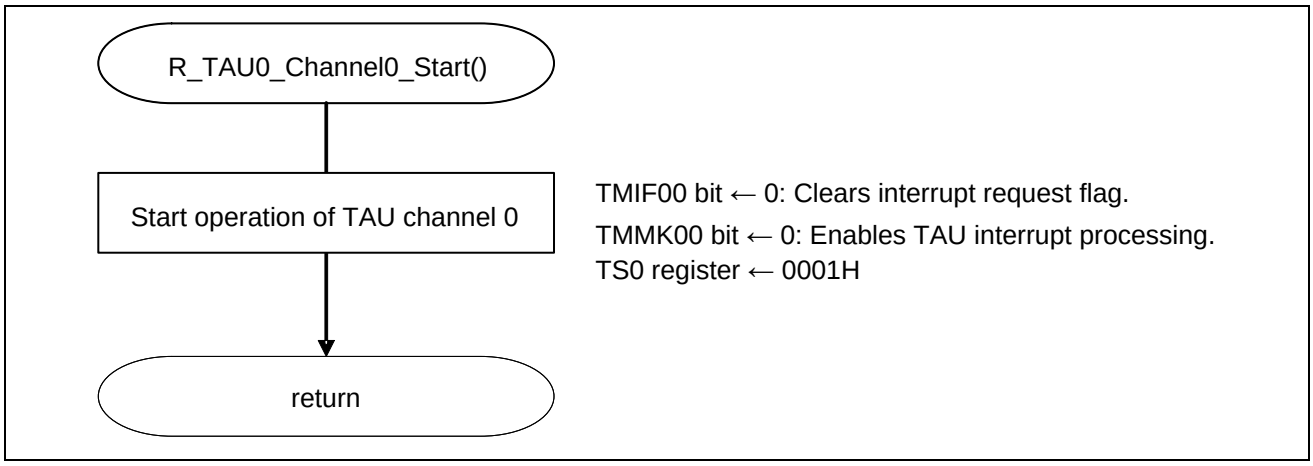

Figure 4.13 Timer Array Unit 0 Operation Start

Configuring the timer interrupt
- Interrupt request flag register (IF1L)
  Clear the interrupt request flag.
- Interrupt mask flag register (MK1L)
  Enable interrupt processing.

Symbol: IF1L

7	6	5	4	3	2	1	0
TMIF03	TMIF02	TMIF01	TMIF00	IICAIF0	SREIF1 TMIF03H	SRIF1 CSIIF11 IICIF11	STIF1 CSIIF10 IICIF10
x	x	x	0	x	x	x	x

Bit 4

TMIF00	Interrupt request flag
0	No interrupt request signal is generated
1	Interrupt request is generated, interrupt request status

Symbol: MK1L

7	6	5	4	3	2	1	0
TMMK03	TMMK02	TMMK01	TMMK00	IICAMK0	SREMK1 TMMK03H	SRMK1 CSIMK11 IICMK11	STMK1 CSIMK10 IICMK10
x	x	x	0	x	x	x	x

Bit 4

TMMK00	Interrupt servicing control
0	Interrupt servicing enabled
1	Interrupt servicing disabled

Configuring the timer startup
- Timer channel start register 0 (TS0)
  Enable count operation of channel 0.

Symbol: TS0

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	TSH03	0	TSH01	0	0	0	0	0	TS03	TS02	TS01	TS00
0	0	0	0	x	0	x	0	0	0	0	0	x	x	x	1

Bit 0

TS00	Operation enable (start) trigger of channel 0
0	No trigger operation
1	The TE00 bit is set to 1 and the count operation becomes enabled. The TCR00 register count operation start in the count operation enabled state varies depending on each operation mode.

Caution: For details on the register setup procedures, refer to RL78/G14 User's Manual: Hardware.
x: Bits not used in this setting item

4.4.7.11 INTTM00 Interrupt Processing

Figure 4.14 shows the flowchart for INTTM00 interrupt processing.

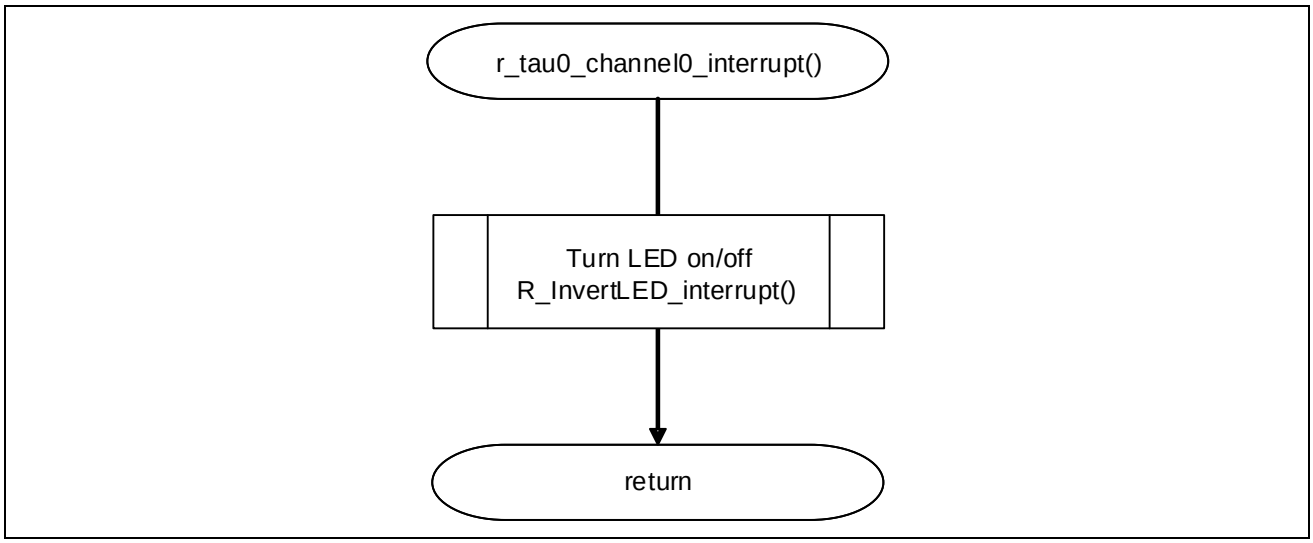

Figure 4.14 INTTM00 Interrupt Processing

4.4.7.12 LED Turn-On/Off Processing

Figure 4.15 shows the flowchart for LED turn-on/off processing.

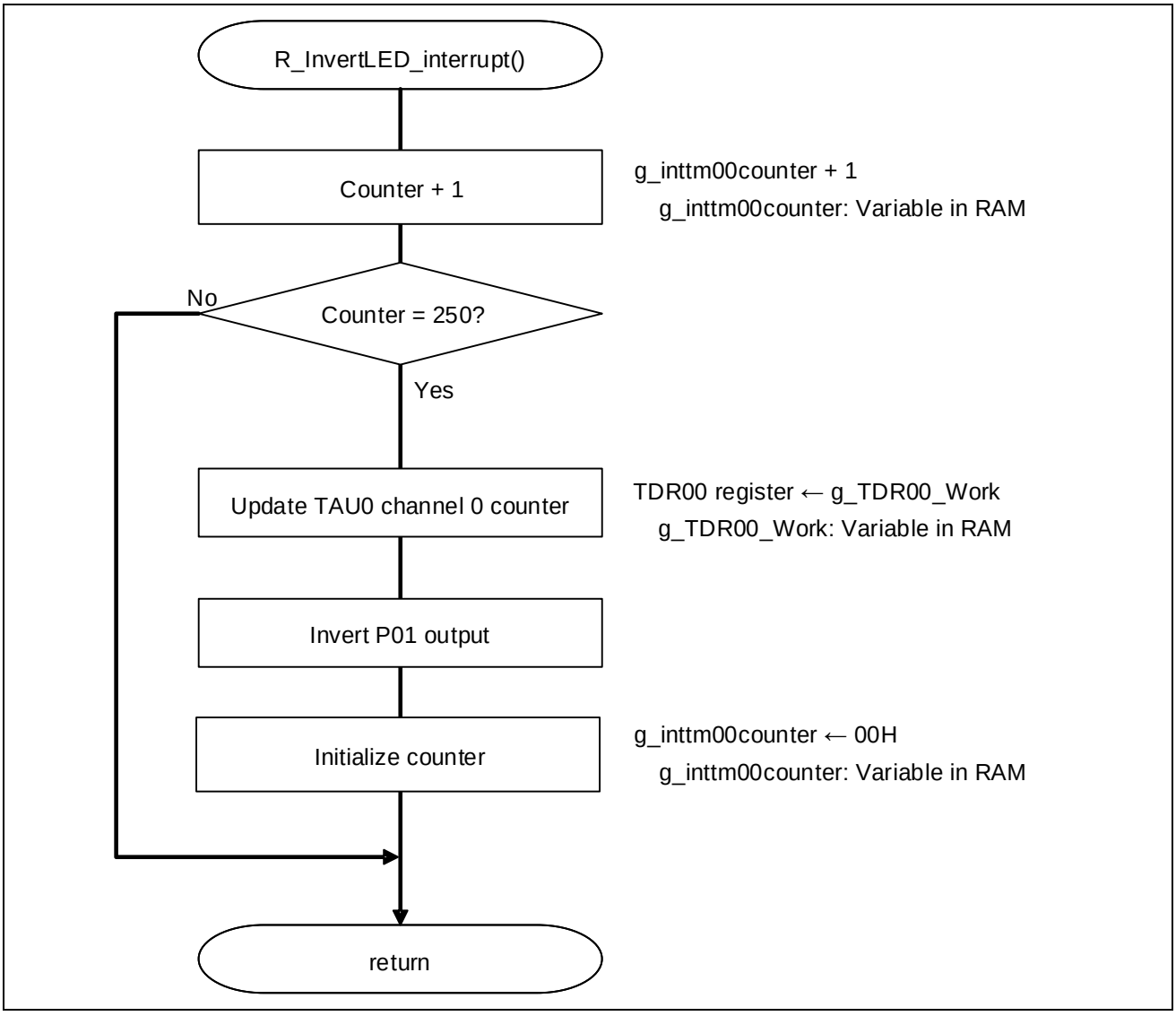

Figure 4.15 LED turn-on/off processing

4.4.7.13 INTP0 Interrupt Processing

Figures 4.16 and 4.17 show the flowchart for INTP0 interrupt processing.

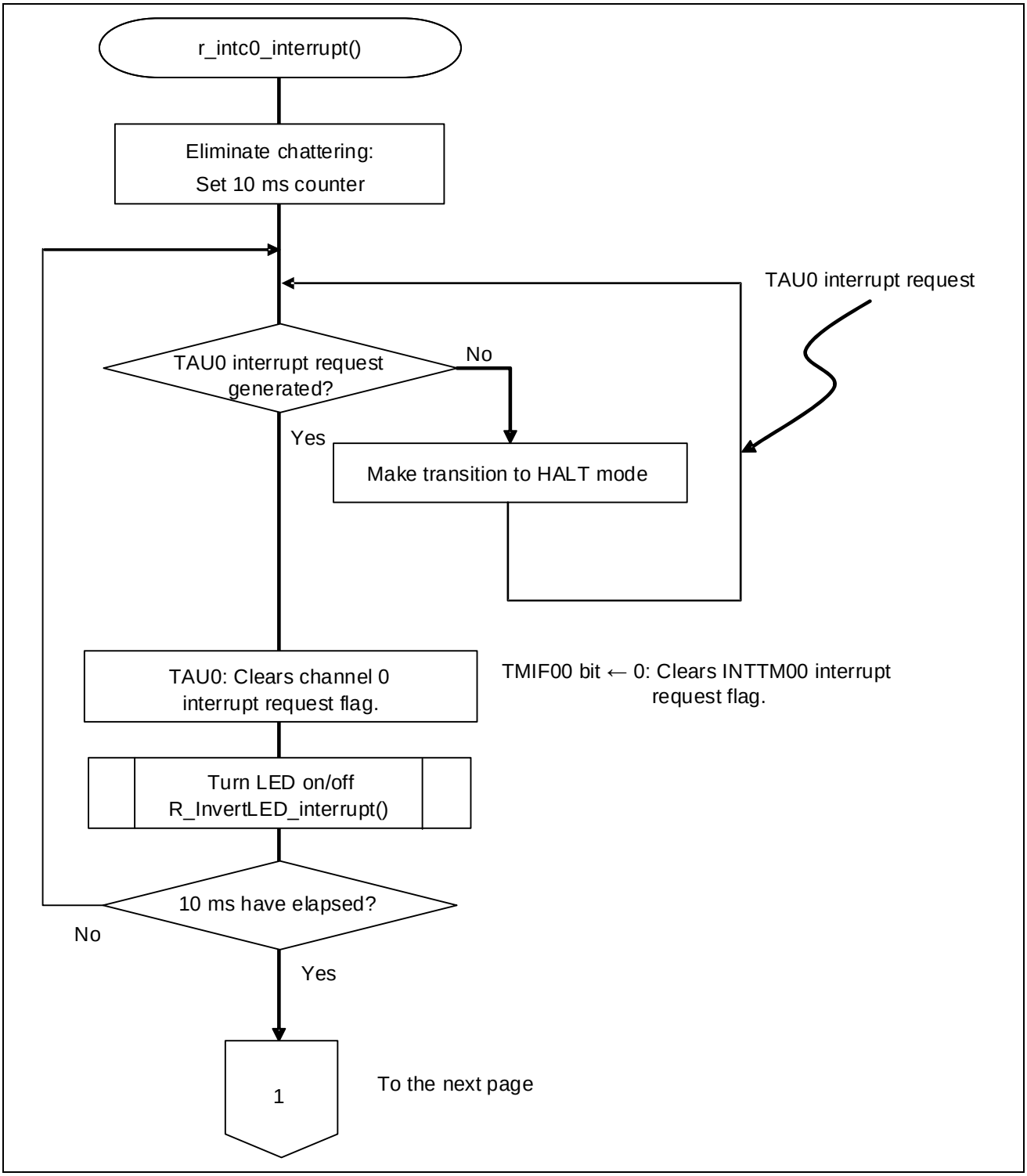

Figure 4.16 INTP0 Interrupt Processing (1/2)

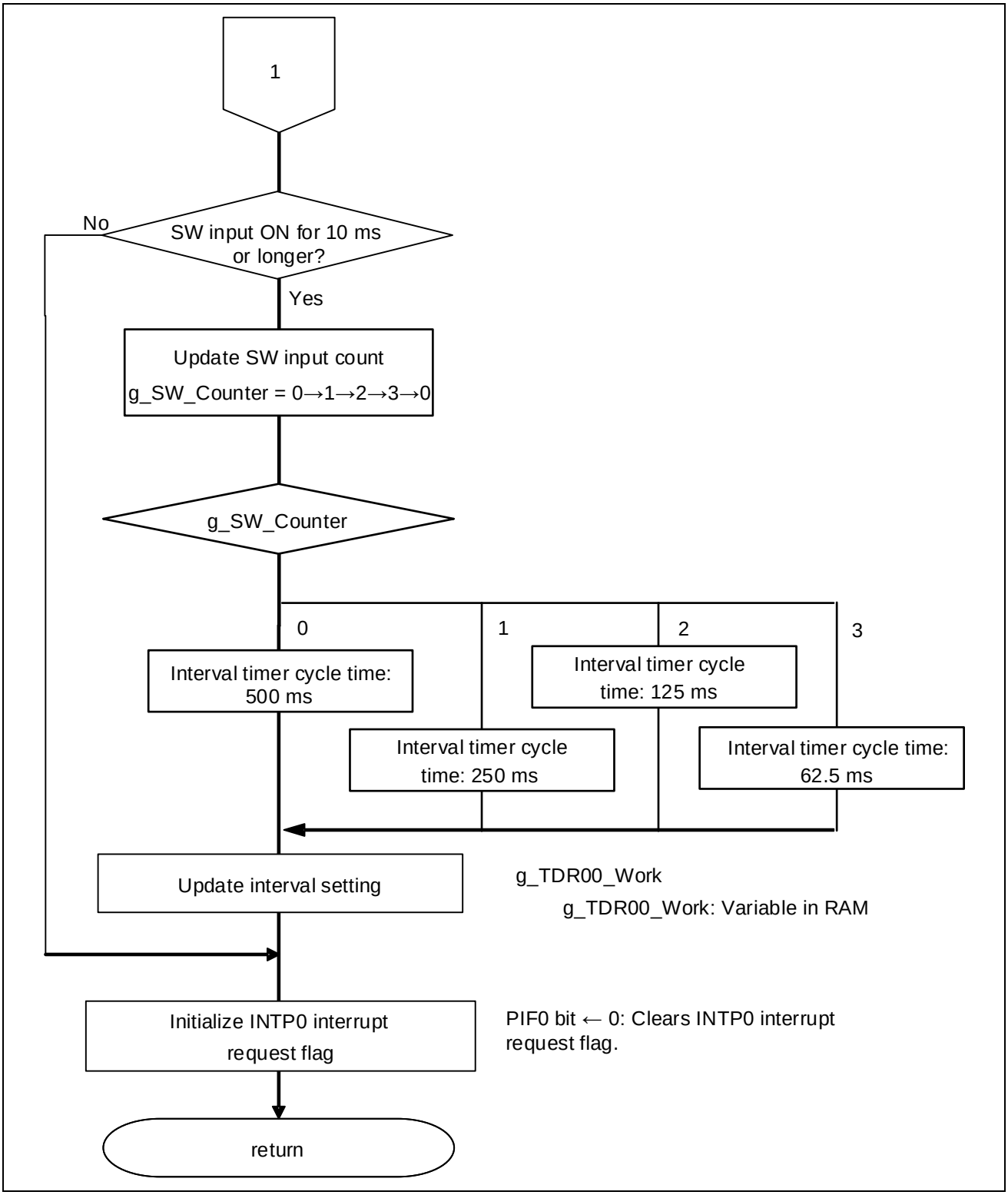

Figure 4.17 INTP0 Interrupt Processing (2/2)

5. Example of Migration from Programmable Waveform Generation Mode

5.1 Specifications

When implementing programmable waveform generation mode of Timer RB in R8C/36M, RL78/G14 can use PWM (Pulse Width Modulation) output of TAU.
Two channels are used as a set to generate a pulse with a specified period and a specified duty factor.

Table 5.1 lists the peripheral functions to be used and their uses (example of migration from programmable waveform generation mode), and Figure 5.1 shows operation overview (example of migration from programmable waveform generation mode).

Table 5.1 Peripheral Functions to be Used and Their Uses (Example of Migration from Programmable Waveform Generation Mode)

Peripheral Function	Use
Timer array unit (PWM (Pulse Width Modulation) output)	Generate a pulse with a specified period and a specified duty factor

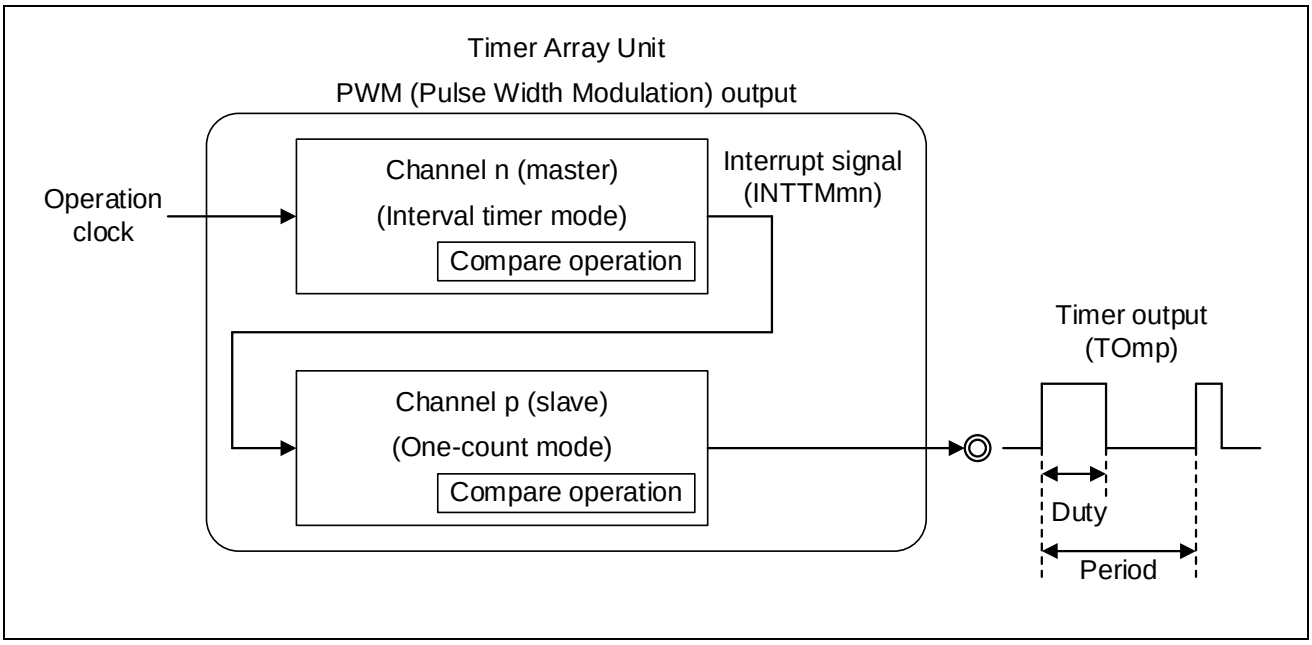

Figure 5.1 Operation Overview (Example of Migration from Programmable Waveform Generation Mode)

5.2 Operation Check Conditions

The sample code described in this application note has been checked under the conditions listed in the table below.

Table 5.2 Operation Check Conditions

Item	Description
Microcontroller used	RL78/G14 (R5F104LEAFB)
Operating frequency	High-speed on-chip oscillator (HOCO) clock: 32 MHz CPU/peripheral hardware clock: 32 MHz
Operating voltage	5.0V (can run on a voltage range of 2.9 V to 5.5 V.) LVD operation (V_{LVD}): Reset mode 2.81 V (2.76 V to 2.87 V)
Integrated development environment (CS+)	CS+ V4.01.00 from Renesas Electronics Corp.
C compiler (CS+)	CC-RL V1.03.00 from Renesas Electronics Corp.
Integrated development environment (e^2 studio)	e^2 studio V5.2.0.020 from Renesas Electronics Corp.
C compiler (e^2 studio)	CC-RL V1.03.00 from Renesas Electronics Corp.

5.3 Description of Hardware

5.3.1 Hardware Configuration Example

Figure 5.2 shows an example of the hardware configuration used for this application note.

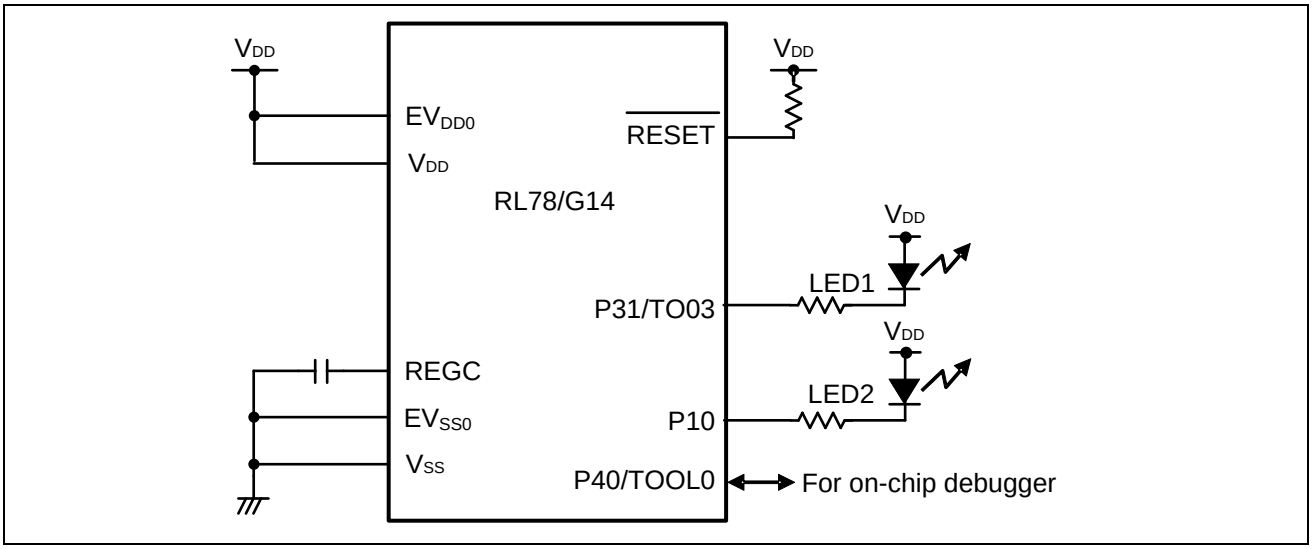

Figure 5.2 Hardware Configuration

Cautions: 1. The purpose of this circuit is only to provide the connection outline and the circuit is simplified accordingly. When designing and implementing an actual circuit, provide proper pin treatment and make sure that the hardware's electrical specifications are met (connect the input-only ports separately to V_{DD} or V_{SS} via a resistor).

2. Connect any pins whose name begins with EV_{SS} to V_{SS} and any pins whose name begins with EV_{DD} to V_{DD}, respectively.
3. V_{DD} must be held at not lower than the reset release voltage (V_{LVD}) that is specified as LVD.

5.3.2 List of Pins to be used

Table 5.3 lists the pins to be used and their functions.

Table 5.3 Pins to be Used and Their Functions

Pin Name	I/O	Description
P31/TO03	Output	PWM output port
P10	Output	Output port for LED indications

5.4 Description of Software

5.4.1 Operation Outline

The sample program covered in this chapter implements PWM by operating channel 0 and channel 3 together, and delivers a PWM output from P31/TO03.
Also, this program detects 250 timer interrupts (INTTM00) with 2 ms cycle time which is generated by channel 0. Then, it changes the PWM output duty ratio and inverts the LED indication at 500 ms intervals.

Table 5.4 shows the required peripheral function and its use. Figure 5.3 presents an overview of the PWM output operation. Table 5.5 shows the relation between PWM output duty ratios and LED brightness. Figure 5.4 is a simplified timing chart which summarizes the PWM output operation.

(1) Initialize the TAU.
<Conditions for setting>
Set the P31/TO03 pin to a PWM output.
Set TAU0 channel 0 to 2 ms cycle interval timer mode.
Set TAU0 channel 3 to one-count mode.
Initialize the duty ratio of the PWM output to 10 %.
Use timer interrupts (INTTM00) from TAU0 channel 0.

(2) Operation starts when both the operation enable trigger bits for TAU0's channel 0 and channel 3 are set to 1 simultaneously. The sample program executes a HALT instruction to wait for a timer interrupt (INTTM00) from channel 0.

(3) After the start of timer operation, channel 0 generates a timer interrupt (INTTM00) at 2 ms intervals.

(4) When the HALT mode is canceled by a timer interrupt (INTTM00) from channel 0, the sample program starts counting the number of INTTM00 interrupts generated. After channel 0 has generated 250 timer interrupts (i.e., after 500 ms), the sample program updates the channel 3 count value and changes the duty ratio. This duty ratio is increased from 10% to 90% (10% → 30% → 50% → 70% → 90%). It is incremented by 20% each time the number of channel 0 timer interrupts (INTTM00) generated reaches 250. (Thus, it is incremented at 500 ms intervals). It is reset to 10% after it becomes 90%.

(5) After processing timer interrupts (INTTM00) from channel 0, the sample program executes another HALT instruction and waits for the next timer interrupt (INTTM00) from channel 0.

Table 5.4 Required Peripheral Function and Its Use

Peripheral function	Use
Timer array unit 0	This unit is used to realize the PWM function by operating channel 0 and channel 3 together and deliver a PWM output from the TO03 pin.

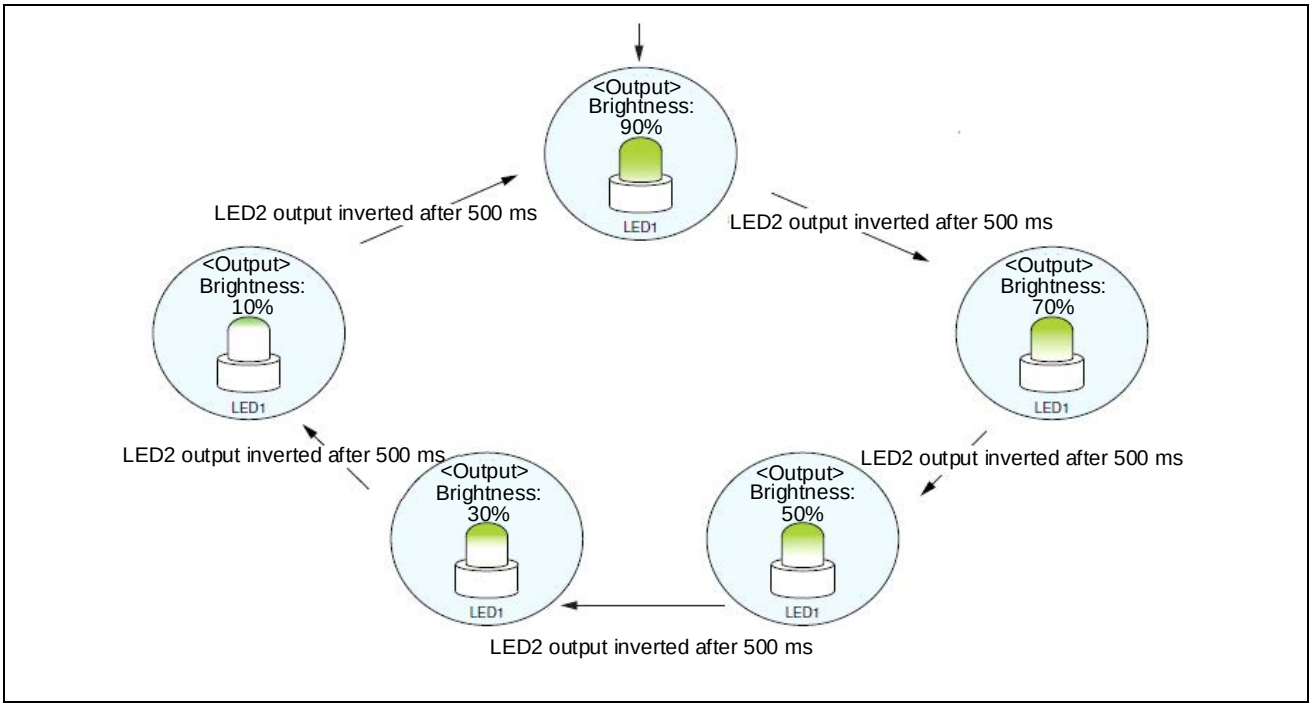

Figure 5.3 Overview of PWM Output Operation

Table 5.5 Relation between PWM Output Duty Ratios and LED Brightness

Duty ratio	LED1 brightness
10%	90%
30%	70%
50%	50%
70%	30%
90%	10%

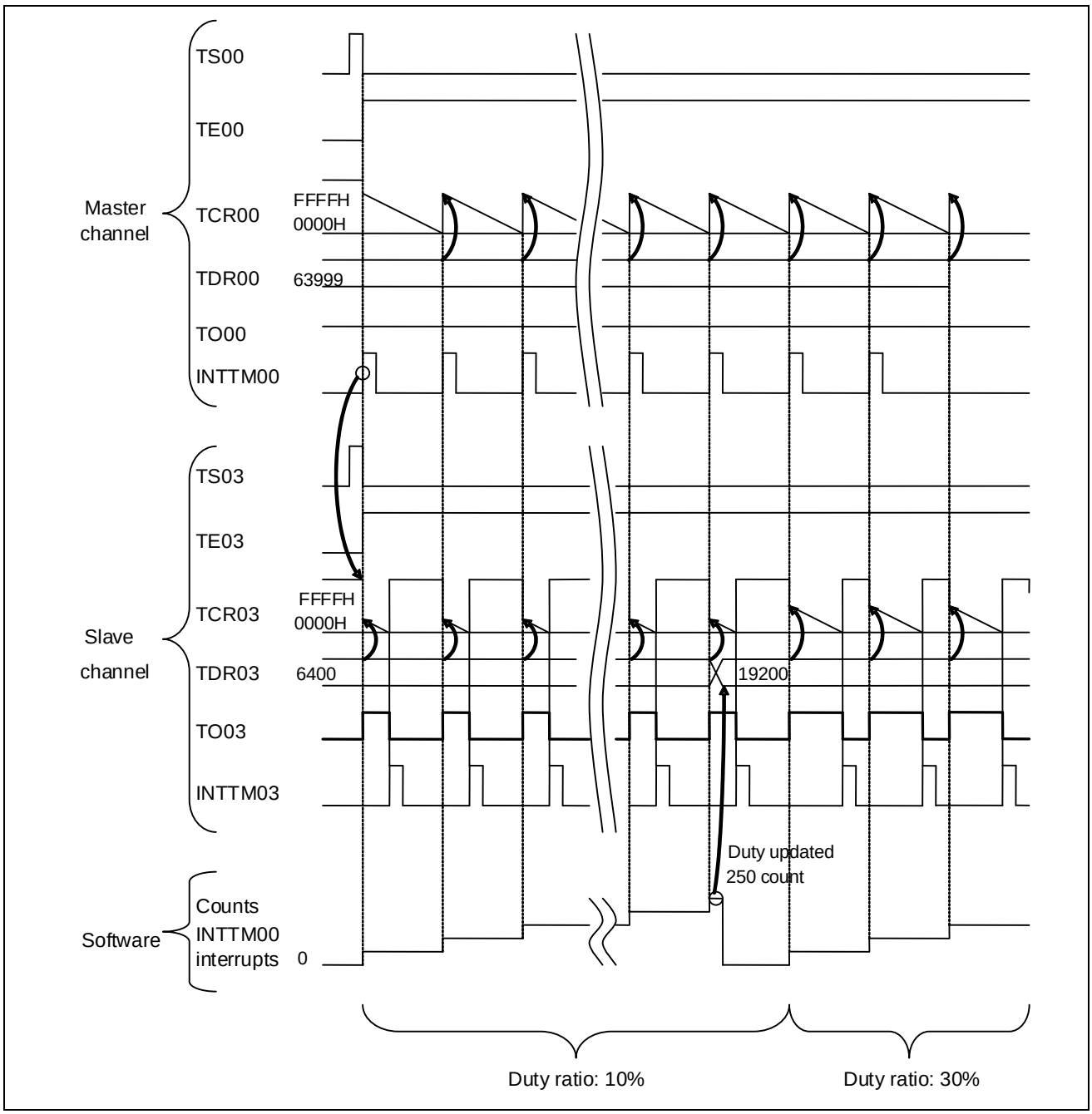

Figure 5.4 Simplified Timing Chart for PWM Output Operation

5.4.2 List of Option Byte Setting

Table 5.6 summarizes the settings of the option bytes.

Table 5.6 Option Byte Settings

Address	Value	Description
000C0H/010C0H	01101110B	Disables the watchdog timer. (Stops counting after the release from the reset state.)
000C1H/010C1H	01111111B	LVD reset mode which uses 2.81 V (2.76 V to 2.87 V)
000C2H/010C2H	11101000B	HS mode, HOCO: 32 MHz
000C3H/010C3H	10000100B	Enables the on-chip debugger.

5.4.3 List of Constant

Table 5.7 lists the constant that is used in this sample program.

Table 5.7 Constant for the Sample Program

Constant	Setting	Description
_1900_TAU_TDR03_VALUE	0x1900U	TDR03 setting for a 10% duty ratio

5.4.4 List of Functions

Table 5.8 lists the functions that are used in this sample program.

Table 5.8 Functions

Function	Outline
R_TAU0_Channel0_Start	TAU0 channel 0 start processing
r_tau0_channel0_interrupt	TAU0 channel 0 timer interrupt processing

5.4.5 Function Specification

The followings are the functions that are used in this sample program.

[Function Name] R_TAU0_Channel0_Start

Synopsis	TAU0 channel 0 start processing
Header	r_cg_macrodriver.h r_cg_timer.h r_cg_userdefine.h
Declaration	void R_TAU0_Channel0_Start(void)
Explanation	This function unmasks TAU0 channel 0 interrupts and starts count operation.
Arguments	None
Return value	None
Remarks	None

[Function Name] r_tau0_channel0_interrupt

Synopsis	Channel 0 timer interrupt processing
Header	r_cg_timer.h
Declaration	static void __near r_tau0_channel0_interrupt (void)
Explanation	This function counts the number of INTTM00 interrupts generated. Each time the count reaches 250, it updates the duty ratio of a PWM output. (Thus, it updates the duty ratio at 500 ms intervals.)
Arguments	None
Return value	None
Remarks	None

5.4.6 Flow Chart

5.4.6.1 Overall Flow

Figure 5.5 shows the overall flow of the sample program described in this chapter.

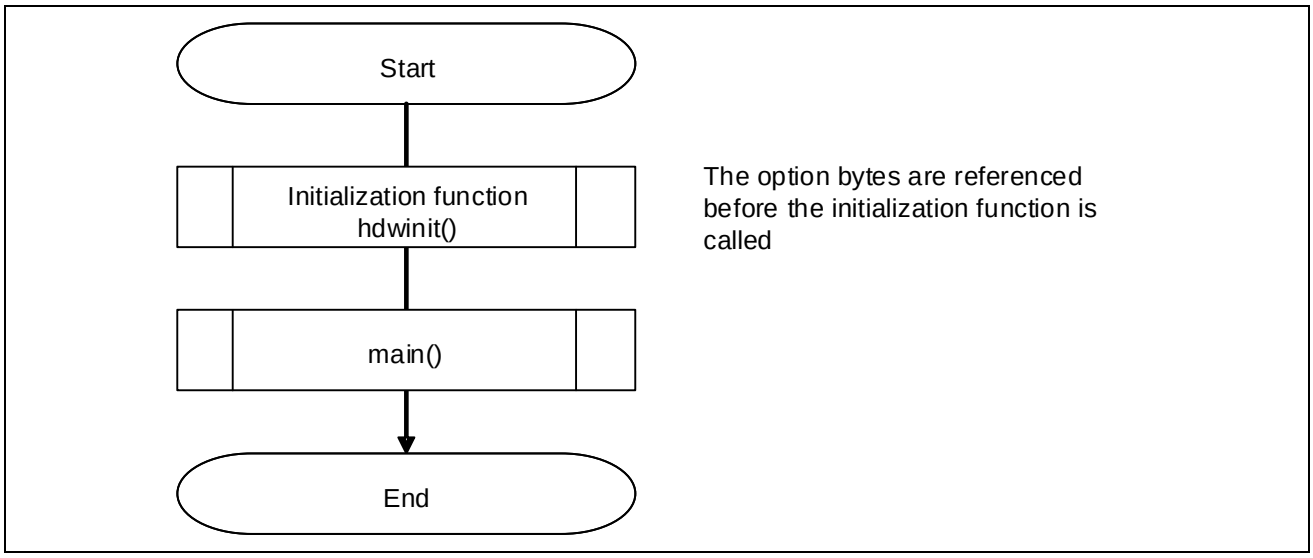

Figure 5.5 Overall Flow

5.4.6.2 Initialization Function

Figure 5.6 shows the flowchart for the initialization function.

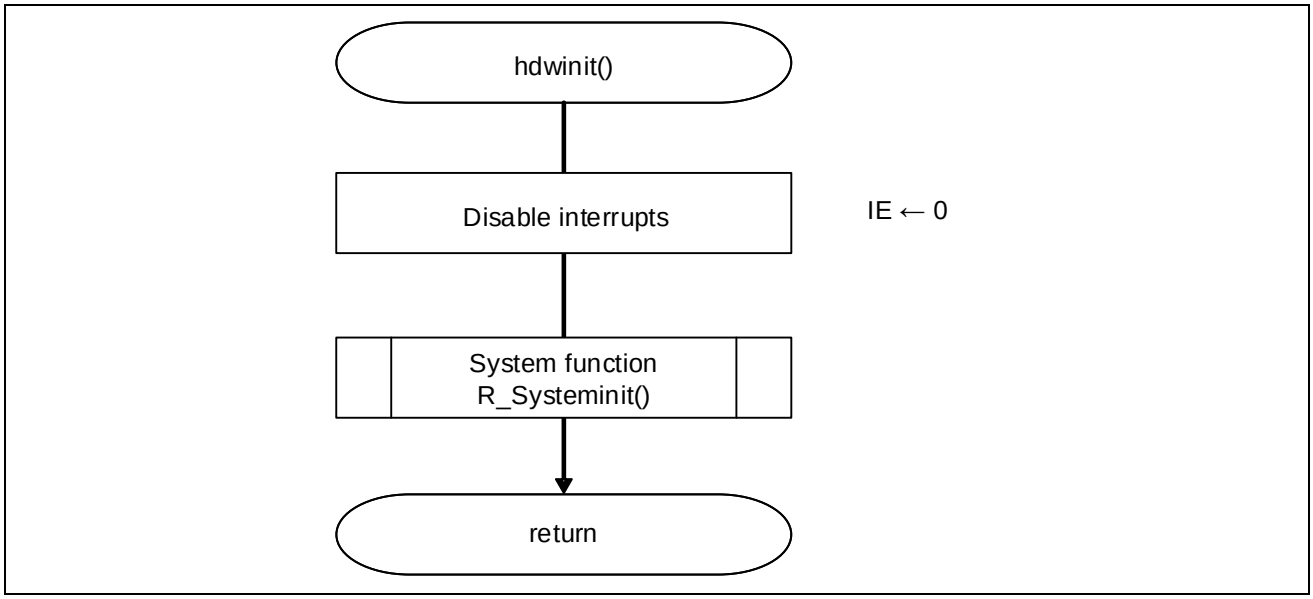

Figure 5.6 Initialization Function

5.4.6.3 System Function

Figure 5.7 shows the flowchart for the system function.

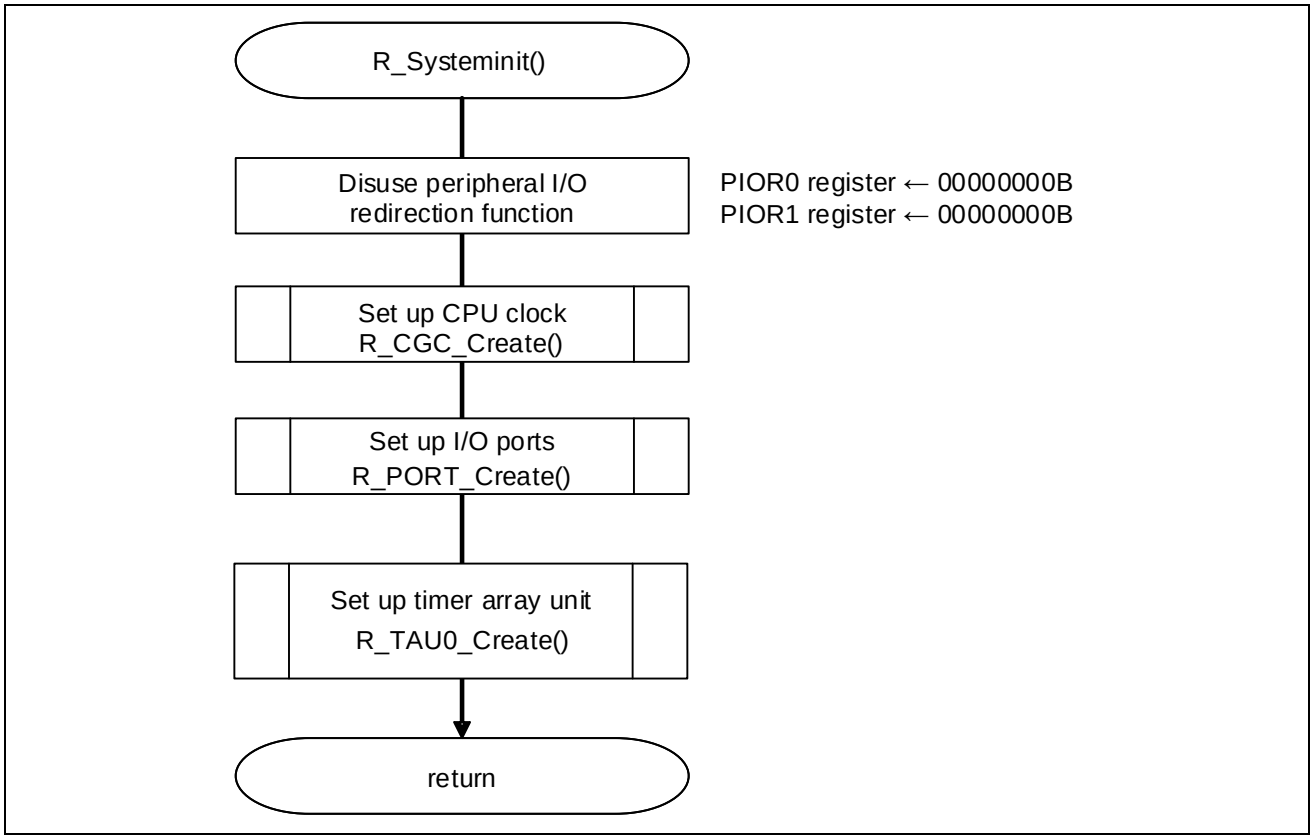

Figure 5.7 System Function

5.4.6.4 CPU Clock Setup

Figure 5.8 shows the flowchart for setting up the CPU clock.

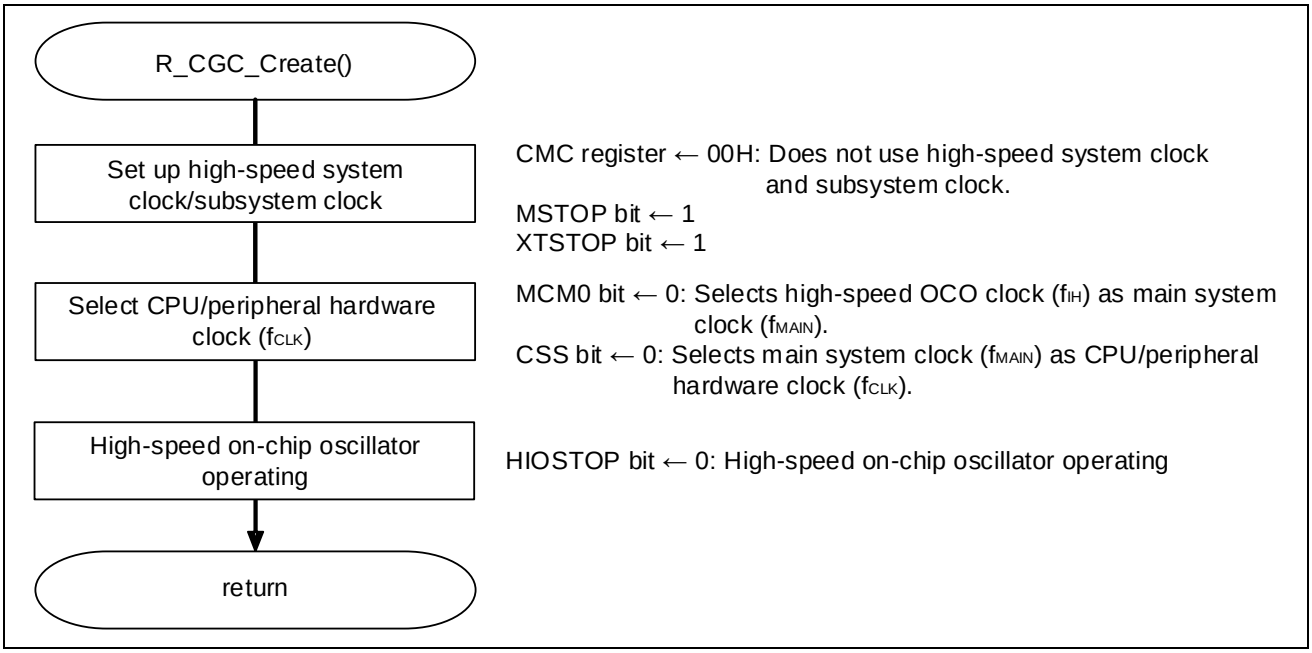

Figure 5.8 CPU Clock Setup

5.4.6.5 I/O Port Setup

Figure 5.9 shows the flowchart for setting up the I/O ports.

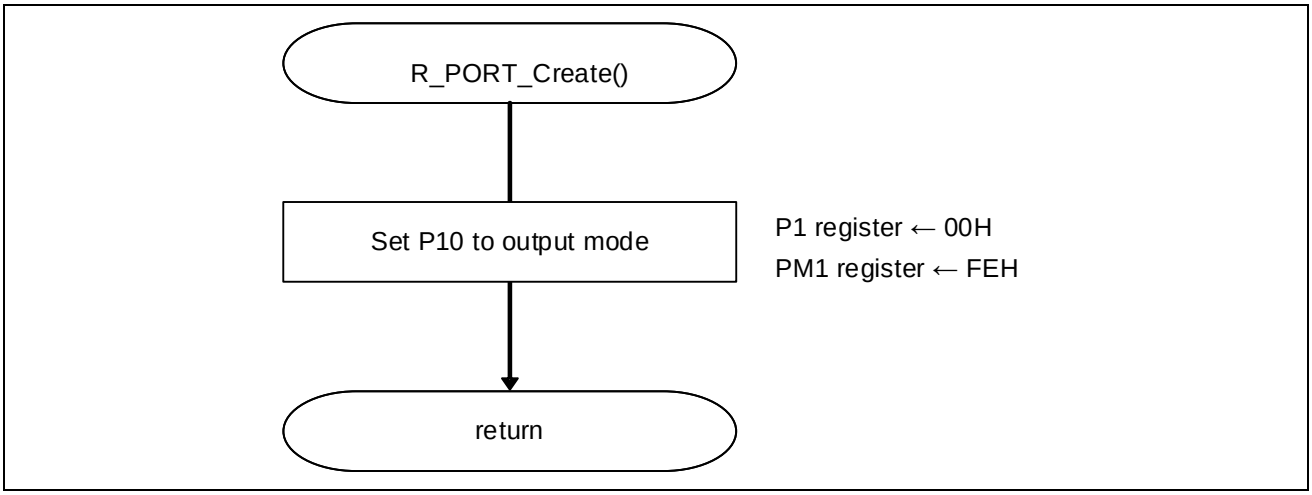

Figure 5.9 I/O Port Setup

Caution: Provide proper treatment for unused pins so that their electrical specifications are observed. Connect each of any unused input-only ports to V_{DD} or V_{SS} via a separate resistor.

Setting up the LED pin to indicate updating of the duty ratio

- Port register (P1)

  Set the output latch value.

Symbol: P1

7	6	5	4	3	2	1	0
P17	P16	P15	P14	P13	P12	P11	P10
x	x	x	x	x	x	x	0

Bit 0

P10	Output data control (in output mode)
0	Output 0
1	Output 1

- Port mode register (PM1)

  Select I/O mode for the port.

Symbol: PM1

7	6	5	4	3	2	1	0
PM17	PM16	PM15	PM14	PM13	PM12	PM11	PM10
x	x	x	x	x	x	x	0

Bit 0

PM10	PM10 I/O mode selection
0	Output mode (output buffer on)
1	Input mode (output buffer off)

Caution: For details on the register setup procedures, refer to RL78/G14 User's Manual: Hardware.

x: Bits not used in this setting item

5.4.6.6 Timer Array Unit Setup

Figures 5.10 and 5.11 show the flowchart for setting up the timer array unit.

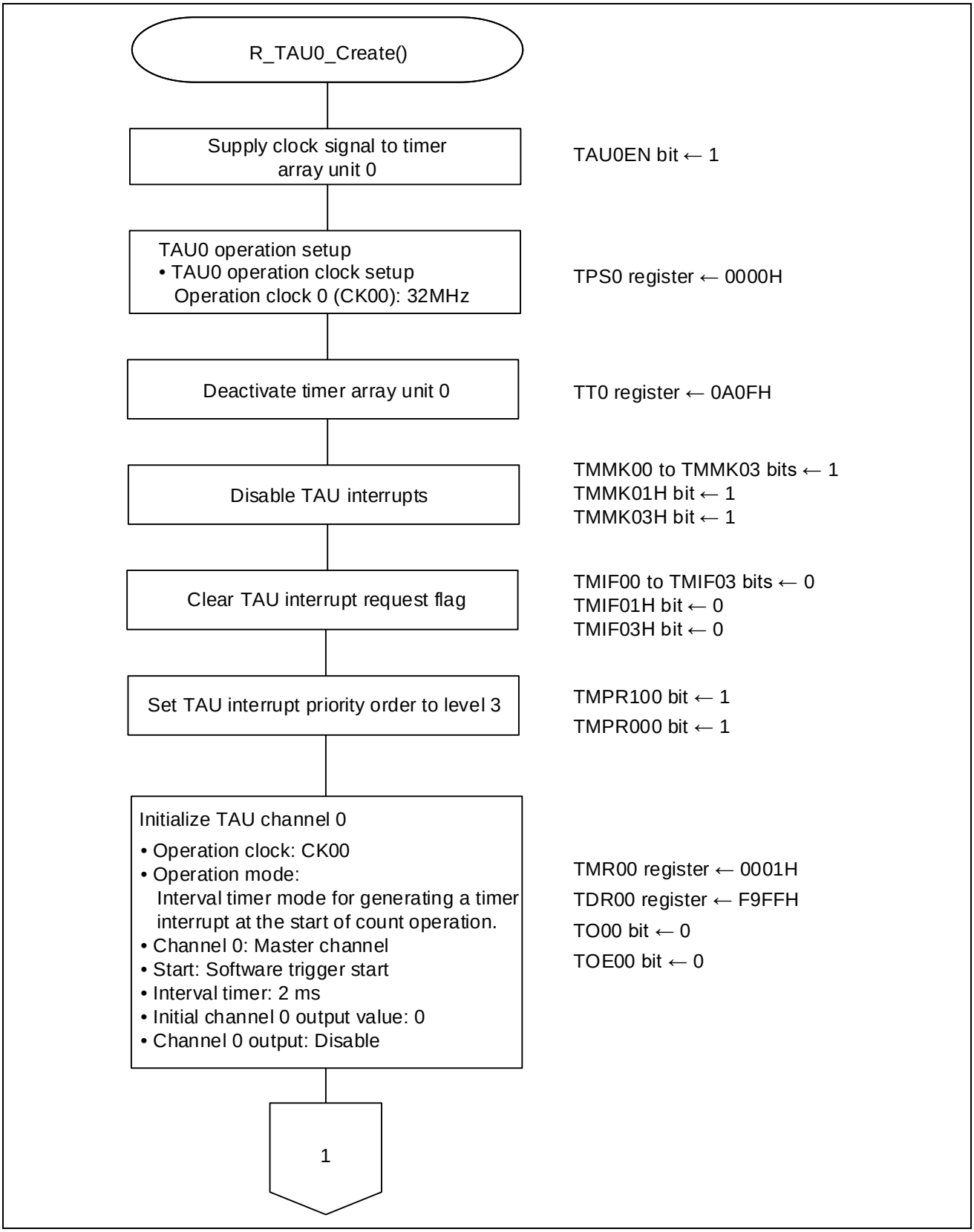

Figure 5.10 Timer Array Unit Setup (1/2)

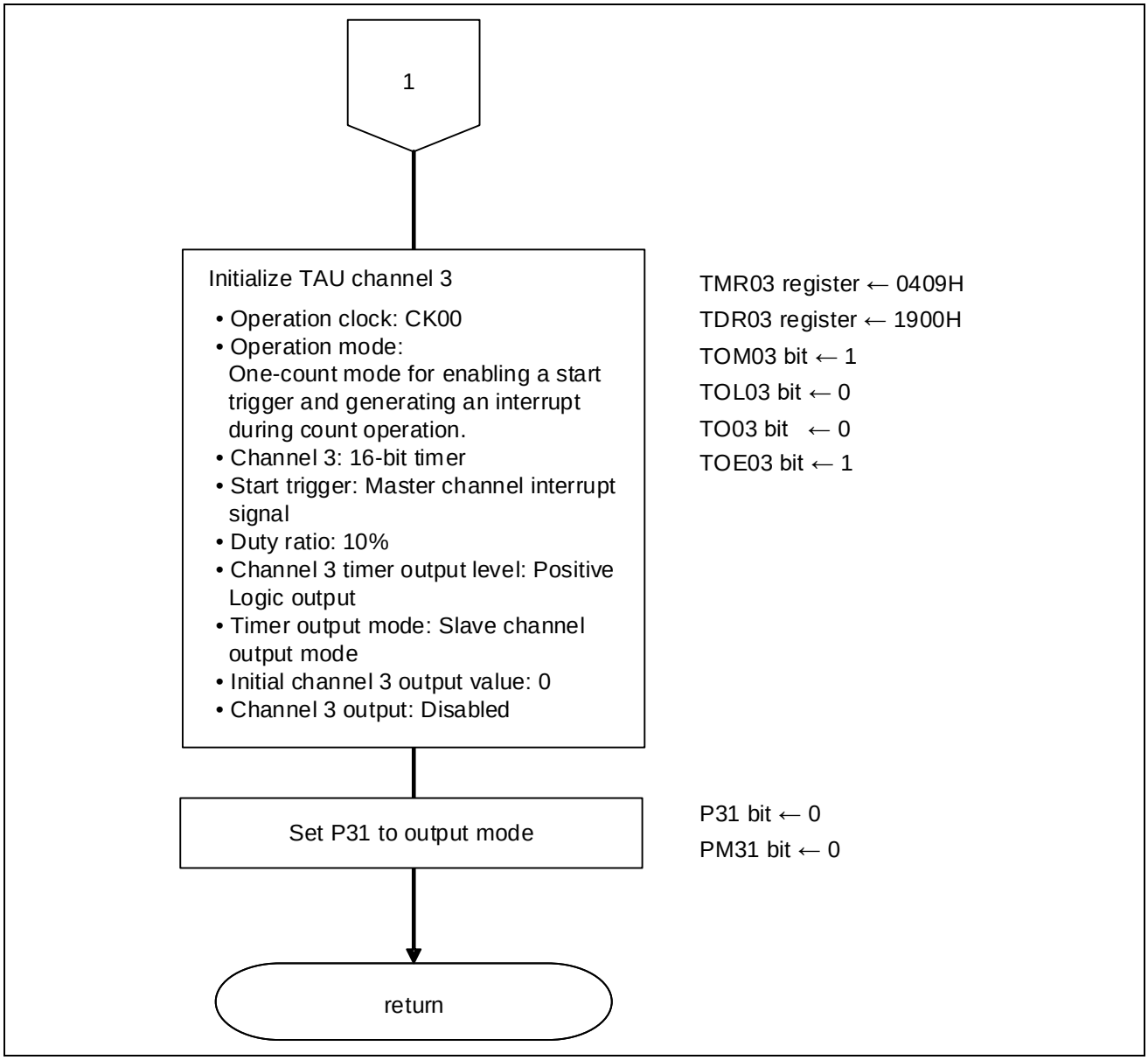

Figure 5.11 Timer Array Unit Setup (2/2)

Starting clock signal supply to the timer array unit 0

- Peripheral enable register 0 (PER0)

Start clock signal supply to the timer array unit 0.

Symbol: PER0

7	6	5	4	3	2	1	0
RTCEN	IICA1EN	ADCEN	IICA0EN	SAU1EN	SAU0EN	TAU1EN	TAU0EN
x	x	x	x	x	x	x	**1**

Bit 0

TAU0EN	Control of timer array unit 0 input clock supply
0	Stops input clock supply
1	**Enables input clock supply**

Caution: For details on the register setup procedures, refer to RL78/G14 User's Manual: Hardware.

x: Bits not used in this setting item

Configuring the timer clock frequency

- Timer clock select register 0 (TPS0)

  Select an operation clock for timer array unit 0.

Symbol: TPS0

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	PRS 031	PRS 030	0	0	PRS 021	PRS 020	PRS 013	PRS 012	PRS 011	PRS 010	PRS 003	PRS 002	PRS 001	PRS 000
0	0	x	x	0	0	x	x	x	x	x	x	0	0	0	0

Bits 3 to 0

PRS 003	PRS 002	PRS 001	PRS 000	Operation clock (CK00) selection					
					f_{CLK}= 2 MHz	f_{CLK}= 4 MHz	f_{CLK}= 8 MHz	f_{CLK}= 20 MHz	f_{CLK}= 32 MHz
0	0	0	0	f_{CLK}	2 MHz	4 MHz	8 MHz	20 MHz	32 MHz
0	0	0	1	$f_{CLK}/2$	1 MHz	2 MHz	4 MHz	10 MHz	16 MHz
0	0	1	0	$f_{CLK}/2^2$	500 kHz	1 MHz	2 MHz	5 MHz	8 MHz
0	0	1	1	$f_{CLK}/2^3$	250 kHz	500 kHz	1 MHz	2.5 MHz	4 MHz
0	1	0	0	$f_{CLK}/2^4$	125 kHz	250 kHz	500 kHz	1.25 MHz	2 MHz
0	1	0	1	$f_{CLK}/2^5$	62.5 kHz	125 kHz	250 kHz	625 kHz	1 MHz
0	1	1	0	$f_{CLK}/2^6$	31.3 kHz	62.5 kHz	125 kHz	313 kHz	500 kHz
0	1	1	1	$f_{CLK}/2^7$	15.6 kHz	31.3 kHz	62.5 kHz	156 kHz	250 kHz
1	0	0	0	$f_{CLK}/2^8$	7.81 kHz	15.6 kHz	31.3 kHz	78.1 kHz	125 kHz
1	0	0	1	$f_{CLK}/2^9$	3.91 kHz	7.81 kHz	15.6 kHz	39.1 kHz	62.5 kHz
1	0	1	0	$f_{CLK}/2^{10}$	1.95 kHz	3.91 kHz	7.81 kHz	19.5 kHz	31.25 kHz
1	0	1	1	$f_{CLK}/2^{11}$	977 Hz	1.95 kHz	3.91 kHz	9.77 kHz	15.6 kHz
1	1	0	0	$f_{CLK}/2^{12}$	488 Hz	977 Hz	1.95 kHz	4.88 kHz	7.81 kHz
1	1	0	1	$f_{CLK}/2^{13}$	244 Hz	488 Hz	977 Hz	2.44 kHz	3.91 kHz
1	1	1	0	$f_{CLK}/2^{14}$	122 Hz	244 Hz	488 Hz	1.22 kHz	1.95 kHz
1	1	1	1	$f_{CLK}/2^{15}$	61.0 Hz	122 Hz	244 Hz	610 Hz	977 Hz

Caution: For details on the register setup procedures, refer to RL78/G14 User's Manual: Hardware.

x: Bits not used in this setting item

Setting up the channel 0 operation mode

- Timer mode register 00 (TMR00)

Select an operation clock (f_{MCK}).
Select a count clock.
Select a start trigger and capture trigger.
Select a valid edge for timer input.
Set up the operation mode.

Symbol: TMR00

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CKS001	CKS000	0	CCS00	0	STS002	STS001	STS000	CIS001	CIS000	0	0	MD003	MD002	MD001	MD000
0	0	0	0	0	0	0	0	x	x	0	0	0	0	0	1

Bits 15 and 14

CKS001	CKS000	Selection of operation clock (f_{MCK}) of channel 0
0	0	Operation clock CK00 set by timer clock select register 0 (TPS0)
0	1	Operation clock CK02 set by timer clock select register 0 (TPS0)
1	0	Operation clock CK01 set by timer clock select register 0 (TPS0)
1	1	Operation clock CK03 set by timer clock select register 0 (TPS0)

Bit 12

CCS00	Selection of count clock (f_{TCLK}) of channel 0
0	Operation clock (f_{MCK}) specified by the CKS000 and CKS001 bits
1	Valid edge of input signal input from the TI00 pin

Bits 10 to 8

STS002	STS001	STS000	Setting of start trigger or capture trigger of channel 0
0	0	0	Only software trigger start is valid (other trigger sources are unselected).
0	0	1	Valid edge of the TI00 pin input is used as both the start trigger and capture trigger.
0	1	0	Both the edges of the TI00 pin input are used as a start trigger and a capture trigger.
1	0	0	Interrupt signal of the master channel is used (when the channel is used as a slave channel with the simultaneous channel operation function).
Other than above			Setting prohibited

Caution: For details on the register setup procedures, refer to RL78/G14 User's Manual: Hardware.
x: Bits not used in this setting item

Symbol: TMR00

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CKS 001	CKS 000	0	CCS 00	0	STS 002	STS 001	STS 000	CIS 001	CIS 000	0	0	MD 003	MD 002	MD 001	MD 000
0	0	0	0	0	0	0	0	x	x	0	0	0	0	0	1

Bits 3 to 0

MD003	MD002	MD001	MD000	Operation mode of channel 0	Corresponding function	Count operation of TCR
0	**0**	**0**	**1**/0	**Interval timer mode**	**Interval timer** / Square wave output / Divider function / PWM output (master)	**Counting down**
0	1	0	1/0	Capture mode	Input pulse interval measurement	Counting up
0	1	1	0	Event counter mode	External event counter	Counting down
1	0	0	1/0	One-count mode	Delay counter / One-shot pulse output / PWM output (slave)	Counting down
1	1	0	0	Capture & one-count mode	Measurement of high-/low-level width of input signal	Counting up
Other than above				Setting prohibited		

The operation of each mode varies depending on MD000 bit (see table below).

Operation mode (Value set by the MD003 to MD001 bits (see table above))	MD000	Setting of starting counting and interrupt
• **Interval timer mode (0, 0, 0)** • Capture mode (0, 1, 0)	0	Timer interrupt is not generated when counting is started (timer output does not change, either).
	1	**Timer interrupt is generated when counting is started (timer output also changes).**
• Event counter mode (0, 1, 1)	0	Timer interrupt is not generated when counting is started (timer output does not change, either).
• One-count mode (1, 0, 0)	0	Start trigger is invalid during counting operation. At that time, interrupt is not generated.
	1	Start trigger is valid during counting operation. At that time, interrupt is also generated.
• Capture & one-count mode (1, 1, 0)	0	Timer interrupt is not generated when counting is started (timer output does not change, either). Start trigger is invalid during counting operation. At that time interrupt is not generated.
Other than above		Setting prohibited

Caution: For details on the register setup procedures, refer to RL78/G14 User's Manual: Hardware.
x: Bits not used in this setting item

Setting up the channel 3 operation mode

- Timer mode register 03 (TMR03)

Select an operation clock (f_{MCK}).
Select a count clock.
Select the 16/8-bit timer.
Select a start trigger and capture trigger.
Select a valid edge for timer input.
Set up the operation mode.

Symbol: TMR03

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CKS031	CKS030	0	CCS03	SPLIT03	STS032	STS031	STS030	CIS031	CIS030	0	0	MD033	MD032	MD031	MD030
0	0	0	0	0	1	0	0	x	x	0	0	1	0	0	1

Bits 15 and 14

CKS031	CKS030	Selection of operation clock (f_{MCK}) of channel 3
0	**0**	**Operation clock CK00 set by timer clock select register 0 (TPS0)**
0	1	Operation clock CK02 set by timer clock select register 0 (TPS0)
1	0	Operation clock CK01 set by timer clock select register 0 (TPS0)
1	1	Operation clock CK03 set by timer clock select register 0 (TPS0)

Bit 12

CCS03	Selection of count clock (f_{TCLK}) of channel 3
0	**Operation clock (f_{MCK}) specified with the CKS030 and CKS031 bits**
1	Valid edge of input signal input from the TI03 pin

Bit 11

SPLIT03	Selection of 8 or 16-bit timer operation for channel 3
0	**Operates as 16-bit timer (Operates in independent channel operation function or as slave channel in simultaneous channel operation function.)**
1	Operates as 8-bit timer

Bits 10 to 8

STS032	STS031	STS030	Setting of start trigger or capture trigger of channel 3
0	0	0	Only software trigger start is valid (other trigger sources are unselected).
0	0	1	Valid edge of the TI03 pin input is used as both the start trigger and capture trigger.
0	1	0	Both the edges of the TI03 pin input are used as a start trigger and a capture trigger.
1	**0**	**0**	**Interrupt signal of the master channel is used (when the channel is used as a slave channel with the simultaneous channel operation function).**
Others than above			Setting prohibited

Caution: For details on the register setup procedures, refer to RL78/G14 User's Manual: Hardware.
x: Bits not used in this setting item

Symbol: TMR03

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CKS 031	CKS 030	0	CCS 03	SPLIT 03	STS 032	STS 031	STS 030	CIS 031	CIS 030	0	0	MD 033	MD 032	MD 031	MD 030
0	0	0	0	0	1	0	0	x	x	0	0	1	0	0	1

Bits 3 to 0

MD033	MD032	MD031	MD030	Operation mode of channel 3	Corresponding function	Count operation of TCR
0	0	0	1/0	Interval timer mode	Interval timer / Square wave output / Divider function / PWM output (master)	Counting down
0	1	0	1/0	Capture mode	Input pulse interval measurement	Counting up
0	1	1	0	Event counter mode	External event counter	Counting down
1	**0**	**0**	**1**/0	**One-count mode**	Delay counter / One-shot pulse output / **PWM output (slave)**	**Counting down**
1	1	0	0	Capture & one-count mode	Measurement of high-/low-level width of input signal	Counting up
Other than above				Setting prohibited		

The operation of each mode varies depending on MD030 bit (see table below).

Operation mode (Value set by the MD033 to MD031 bits (see table above))	MD030	Setting of starting counting and interrupt
• Interval timer mode (0, 0, 0) • Capture mode (0, 1, 0)	0	Timer interrupt is not generated when counting is started (timer output does not change, either).
	1	Timer interrupt is generated when counting is started (timer output also changes).
• Event counter mode (0, 1, 1)	0	Timer interrupt is not generated when counting is started (timer output does not change, either).
• One-count mode (1, 0, 0)	0	Start trigger is invalid during counting operation. At that time, interrupt is not generated.
	1	**Start trigger is valid during counting operation. At that time, interrupt is also generated.**
• Capture & one-count mode (1, 1, 0)	0	Timer interrupt is not generated when counting is started (timer output does not change, either). Start trigger is invalid during counting operation. At that time interrupt is not generated.
Other than above		Setting prohibited

Caution: For details on the register setup procedures, refer to RL78/G14 User's Manual: Hardware.
x: Bits not used in this setting item

Configuring the PWM output pulse cycle time
- Timer data register 00 (TDR00)

Configure the PWM output pulse cycle time.

Symbol: TDR00

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Pulse cycle time = (TDR00 setting + 1) × Count clock cycle time
2 [ms] = (1/32[MHz]) × (TDR00 setting + 1)

⇒ TDR00 setting = 63999

Configuring the PWM output duty ratio
- Timer data register 03 (TDR03)

Configure the PWM output duty ratio.

Symbol: TDR03

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Duty ratio = (TDR03 setting)/(TDR00 setting + 1) × 100
10 [%] = (TDR03 setting)/(63999 + 1) × 100

⇒ TDR03 setting = 6400

Setting up the timer output mode
- Timer output mode register 0 (TOM0)

Set up the timer output mode for each channel.

Symbol: TOM0

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	TOM03	TOM02	TOM01	0
0	0	0	0	0	0	0	0	0	0	0	0	1	x	x	0

Bit 3

TOM03	Control of timer output mode of channel 3
0	Master channel output mode (to produce toggle output by timer interrupt request signal (INTTM03))
1	**Slave channel output mode (output is set by the timer interrupt request signal (INTTM03) of the master channel, and reset by the timer interrupt request signal (INTTM0p) of the slave channel)**

Caution: For details on the register setup procedures, refer to RL78/G14 User's Manual: Hardware.
x: Bits not used in this setting item

Configuring the output level for the timer output pin

- Timer output level register 0 (TOL0)

Configure the output level for the timer output pin for each channel.

Symbol: TOL0

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**TOL03**	**TOL02**	**TOL01**	**0**
0	0	0	0	0	0	0	0	0	0	0	0	**0**	x	x	0

Bit 3

TOL03	Control of timer output level of channel 3
0	**Positive logic output (active-high)**
1	Negative logic output (active-low)

Configuring the output value for the timer output pin

- Timer output register 0 (TO0)

Configure the output value for the timer output pin for each channel.

Symbol: TO0

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**TO03**	**TO02**	**TO01**	**TO00**
0	0	0	0	0	0	0	0	0	0	0	0	**0**	x	x	**0**

Bit 3

TO03	Timer output of channel 3
0	**Timer output value is “0”**
1	Timer output value is “1”

Bit 0

TO00	Timer output of channel 0
0	**Timer output value is “0”**
1	Timer output value is “1”

Caution: For details on the register setup procedures, refer to RL78/G14 User's Manual: Hardware.

x: Bits not used in this setting item

Enabling the timer output

- Timer output enable register 0 (TOE0)

Enable/disable the timer output for each channel.

Symbol: TOE0

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	TOE03	TOE02	TOE01	TOE00
0	0	0	0	0	0	0	0	0	0	0	0	1	x	x	0

Bit 3

TOE03	Timer output enable/disable of channel 3
0	Timer output is disabled. Timer operation is not applied to the TO03 bit and the output is fixed. Writing to the TO03 bit is enabled and the level set in the TO03 bit is output from the TO03 pin.
1	**Timer output is enabled.** **Timer operation is applied to the TO03 bit and an output waveform is generated.** **Writing to the TO03 bit is ignored.**

Bit 0

TOE00	Timer output enable/disable of channel 0
0	**Timer output is disabled.** **Timer operation is not applied to the TO00 bit and the output is fixed.** **Writing to the TO00 bit is enabled and the level set in the TO00 bit is output from the TO00 pin.**
1	Timer output is enabled. Timer operation is applied to the TO00 bit and an output waveform is generated. Writing to the TO00 bit is ignored.

Caution: For details on the register setup procedures, refer to RL78/G14 User's Manual: Hardware.

x: Bits not used in this setting item

Setting up the PWM output pin

- Port register (P3)

  Set the output latch.

Symbol: P3

7	6	5	4	3	2	1	0
0	**0**	**0**	**0**	**0**	**0**	**P31**	**P30**
0	0	0	0	0	0	**0**	x

Bit 1

P31	Output data control
0	**Output 0**
1	Output 1

- Port mode register (PM3)

  Select the PM31 I/O mode.

Symbol: PM3

7	6	5	4	3	2	1	0
1	**1**	**1**	**1**	**1**	**1**	**PM31**	**PM30**
1	1	1	1	1	1	**0**	x

Bit 1

PM31	P31 pin I/O mode selection
0	**Output mode (the pin functions as an output port (output buffer on))**
1	Input mode (the pin functions as an input port (output buffer off))

Caution: For details on the register setup procedures, refer to RL78/G14 User's Manual: Hardware.

x: Bits not used in this setting item

5.4.6.7 Main Processing

Figure 5.12 shows the flowchart for main processing.

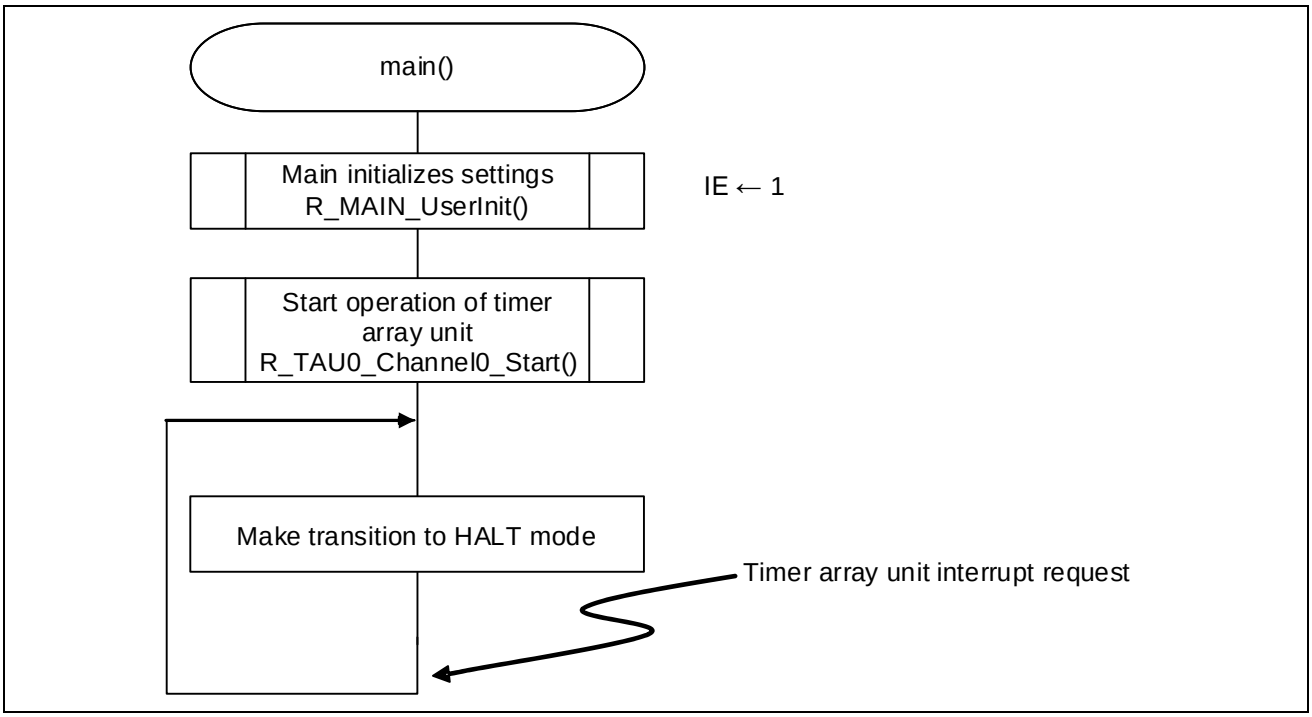

Figure 5.12 Main Processing

5.4.6.8 Timer Array Unit Startup

Figure 5.13 shows the flowchart for starting the operation of the timer array unit.

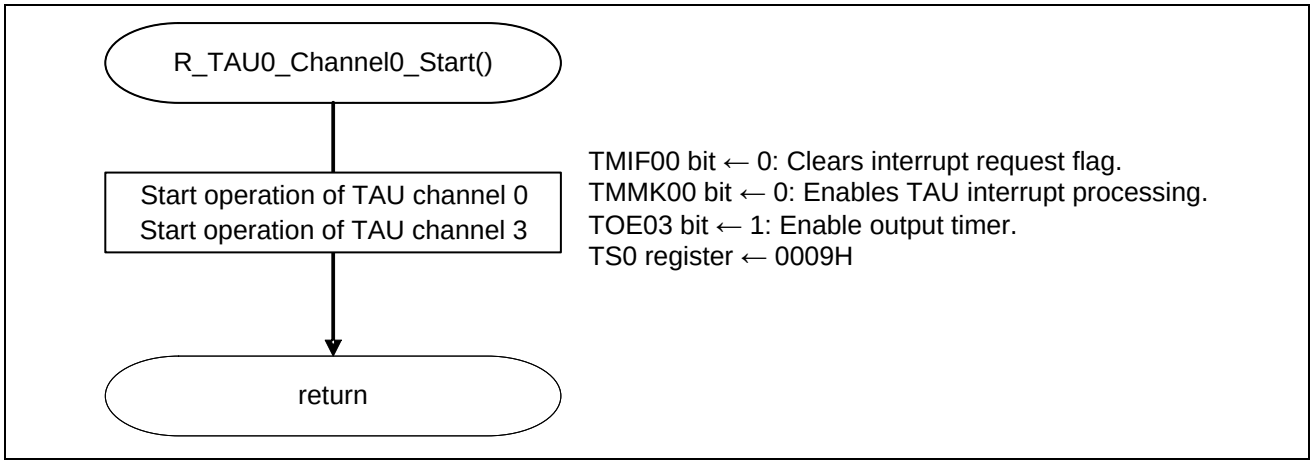

Figure 5.13 Timer Array Unit Startup

Configuring the timer interrupt
- Interrupt request flag register (IF1L)
  Clear the interrupt request flag.
- Interrupt mask flag register (MK1L)
  Enable interrupt processing.

Symbol: IF1L

7	6	5	4	3	2	1	0
TMIF03	TMIF02	TMIF01	TMIF00	IICAIF0	SREIF1 TMIF03H	SRIF1 CSIIF11 IICIF11	STIF1 CSIIF10 IICIF10
x	x	x	**0**	x	x	x	x

Bit 4

TMIF00	Interrupt request flag
0	**No interrupt request signal is generated**
1	Interrupt request is generated, interrupt request status

Symbol: MK1L

7	6	5	4	3	2	1	0
TMMK03	TMMK02	TMMK01	TMMK00	IICAMK0	SREMK1 TMMK03H	SRMK1 CSIMK11 IICMK11	STMK1 CSIMK10 IICMK10
x	x	x	**0**	x	x	x	x

Bit 4

TMMK00	Interrupt servicing control
0	**Interrupt servicing enabled**
1	Interrupt servicing disabled

Enabling the timer output
- Timer output enable register 0 (TOE0)
  Enable/disable the timer output for each channel.

Symbol: TOE0

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	TOE03	TOE02	TOE01	TOE00
0	0	0	0	0	0	0	0	0	0	0	0	**1**	x	x	x

Bit 3

TOE03	Timer output enable/disable of channel 3
0	Timer output is disabled. Timer operation is not applied to the TO03 bit and the output is fixed. Writing to the TO03 bit is enabled and the level set in the TO03 bit is output from the TO03 pin.
1	**Timer output is enabled.** **Timer operation is applied to the TO03 bit and an output waveform is generated.** **Writing to the TO03 bit is ignored.**

Caution: For details on the register setup procedures, refer to RL78/G14 User's Manual: Hardware.
x: Bits not used in this setting item

Configuring the timer startup

- Timer channel start register 0 (TS0)

  Enable count operation of channel 0 and channel 3.

Symbol: TS0

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	TSH03	0	TSH01	0	0	0	0	0	TS03	TS02	TS01	TS00
0	0	0	0	x	0	x	0	0	0	0	0	1	x	x	1

Bit 3

TS03	Operation enable (start) trigger of channel 3
0	No trigger operation
1	The TE03 bit is set to 1 and the count operation becomes enabled. The TCR03 register count operation start in the count operation enabled state varies depending on each operation mode.

Bit 0

TS00	Operation enable (start) trigger of channel 0
0	No trigger operation
1	The TE00 bit is set to 1 and the count operation becomes enabled. The TCR00 register count operation start in the count operation enabled state varies depending on each operation mode.

Caution: For details on the register setup procedures, refer to RL78/G14 User's Manual: Hardware.

x: Bits not used in this setting item

5.4.6.9 INTTM0 Interrupt Processing

Figure 5.14 shows the flowchart for INTTM0 interrupt processing.

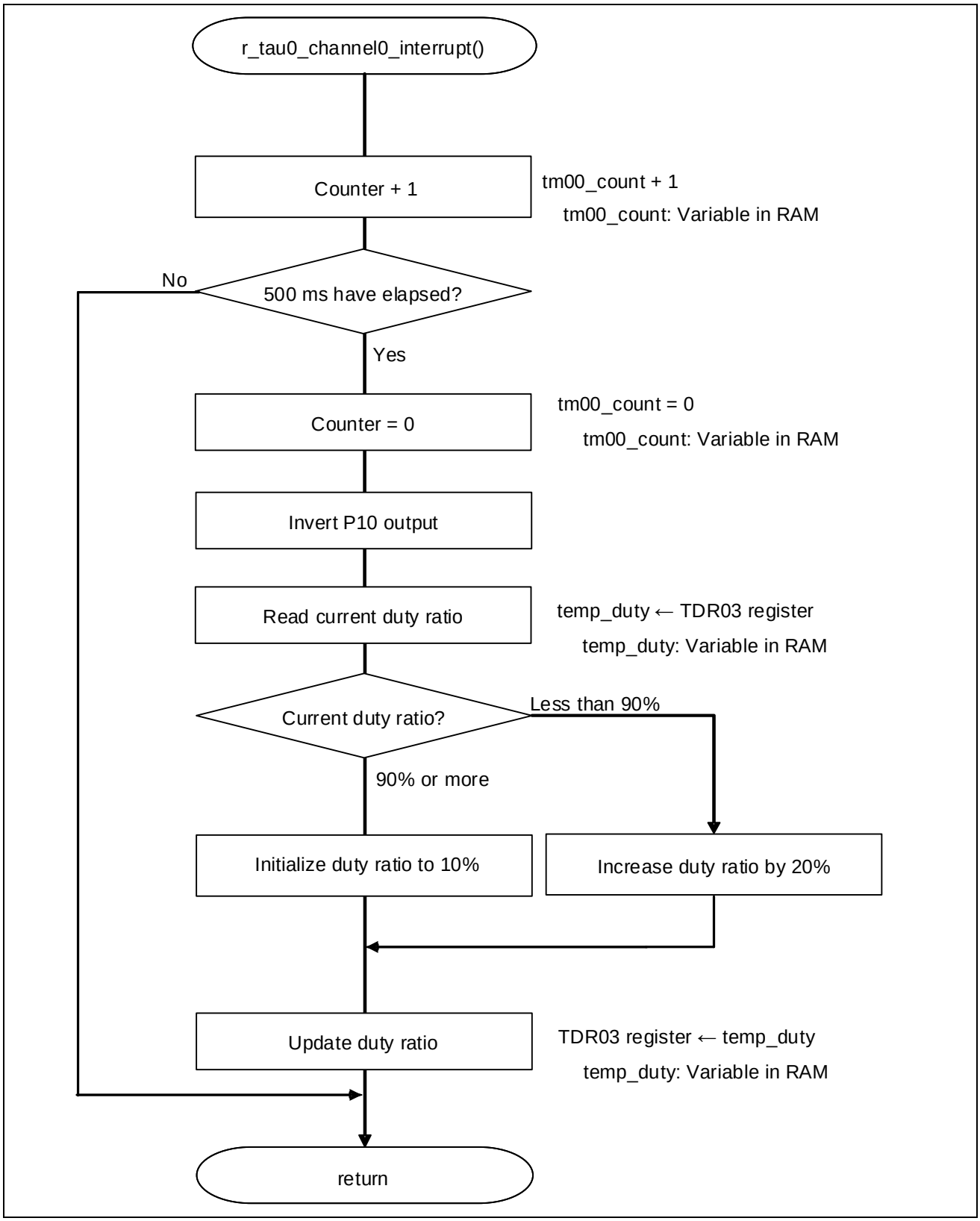

Figure 5.14 INTTM0 Interrupt Service Routine

6. Example of Migration from Programmable One-shot Generation Mode

6.1 Specifications

When implementing programmable one-shot generation mode of Timer RB in R8C/36M, RL78/G14 can use one-shot pulse output of TAU.
Two channels are used as a set to generate a one-shot pulse with a specified output timing and a specified pulse width.
When RL78/G14 uses one-shot pulse output of TAU replace of programmable one-shot generation mode of Timer RB in R8C/36M, specified output timing should be set to 0.

Table 6.1 lists the peripheral functions to be used and their uses (example of migration from programmable one-shot generation mode), and Figure 6.1 shows operation overview (example of migration from programmable one-shot generation mode).

Table 6.1 Peripheral Functions to be Used and Their Uses (Example of Migration from Programmable One-shot Generation Mode)

Peripheral Function	Use
Timer array unit (One-shot pulse output)	Generate a one-shot pulse with a specified output timing and a specified pulse width

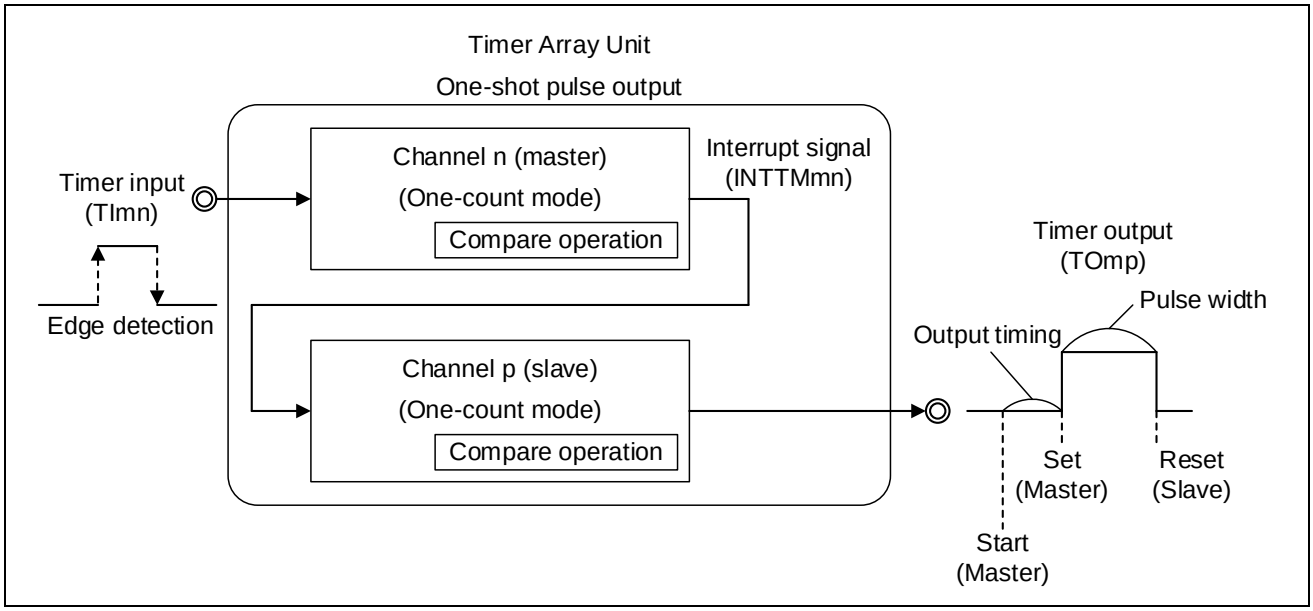

Figure 6.1 Operation Overview (Example of Migration from Programmable One-shot Generation Mode)

6.2 Operation Check Conditions

The sample code described in this application note has been checked under the conditions listed in the table below.

Table 6.2 Operation Check Conditions

Item	Description
Microcontroller used	RL78/G14 (R5F104LEAFB)
Operating frequency	High-speed on-chip oscillator (HOCO) clock: 32 MHz CPU/peripheral hardware clock: 32 MHz
Operating voltage	5.0V (can run on a voltage range of 2.9 V to 5.5 V.) LVD operation (V_{LVD}): Reset mode 2.81 V (2.76 V to 2.87 V)
Integrated development environment (CS+)	CS+ V4.01.00 from Renesas Electronics Corp.
C compiler (CS+)	CC-RL V1.03.00 from Renesas Electronics Corp.
Integrated development environment (e^2 studio)	e^2 studio V5.2.0.020 from Renesas Electronics Corp.
C compiler (e^2 studio)	CC-RL V1.03.00 from Renesas Electronics Corp.

6.3 Description of Hardware

6.3.1 Hardware Configuration Example

Figure 6.2 shows an example of the hardware configuration used for this application note.

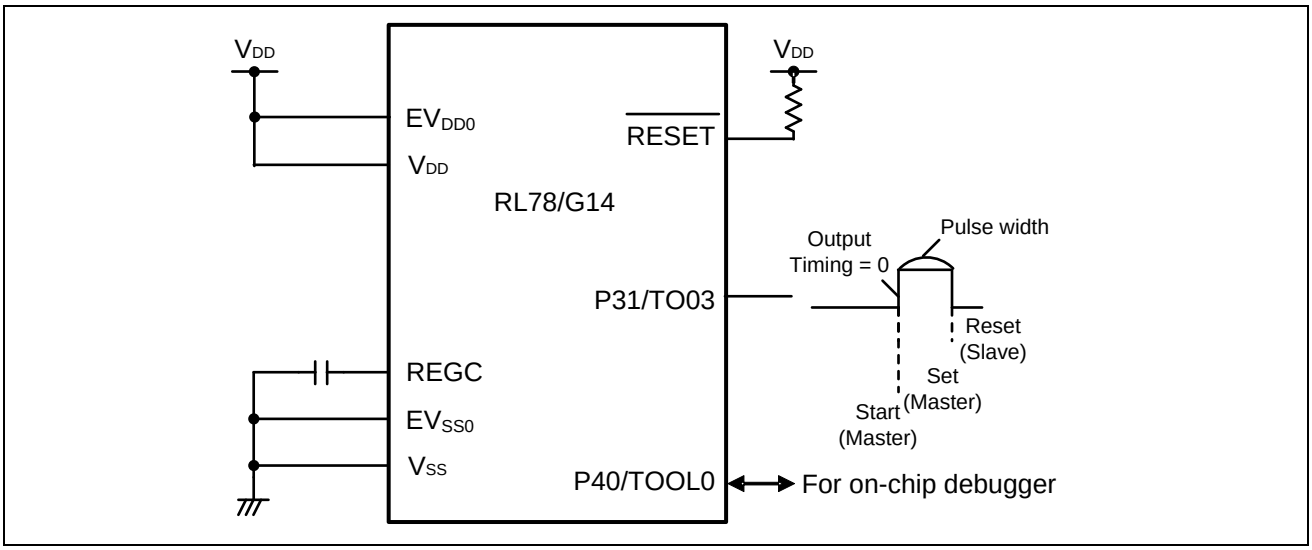

Figure 6.2 Hardware Configuration

Cautions: 1. The purpose of this circuit is only to provide the connection outline and the circuit is simplified accordingly. When designing and implementing an actual circuit, provide proper pin treatment and make sure that the hardware's electrical specifications are met (connect the input-only ports separately to V_{DD} or V_{SS} via a resistor).

2. Connect any pins whose name begins with EV_{SS} to V_{SS} and any pins whose name begins with EV_{DD} to V_{DD}, respectively.
3. V_{DD} must be held at not lower than the reset release voltage (V_{LVD}) that is specified as LVD.

6.3.2 List of Pins to be used

Table 6.3 lists the pins to be used and their functions.

Table 6.3 Pins to be Used and Their Functions

Pin Name	I/O	Description
P31/TO03	Output	One-shot pulse output port

6.4 Description of Software

6.4.1 Operation Outline

The sample program covered in this chapter implements one-shot pulse output by operating channel 0 and channel 3 together, and delivers an one-shot pulse output from P31/TO03.

Table 6.4 shows the required peripheral function and its use. Figure 6.3 is a simplified timing chart which summarizes the one-shot pulse output operation.

(1) Initialize the TAU.
<Conditions for setting>
Set the P31/TO03 pin to an one-shot pulse output.
Set TAU0 channel 0 to one-count mode and no delays.
Set TAU0 channel 3 to one-count mode and counts the 0.2 ms pulse width.

(2) Operation starts when both the operation enable trigger bits for TAU0's channel 0 and channel 3 are set to 1 simultaneously. The sample program executes a HALT instruction to wait for a timer interrupt (INTTM00) from channel 0.

(3) After the start of timer operation, channel 0 generates a timer interrupt (INTTM00) at once (no delays).

(4) When the HALT mode is canceled by a timer interrupt (INTTM00) from channel 0, and channel 0 stops counting until the next start trigger is detected.

(5) Channel 3 starts operation using INTTM00 of channel 0 as a start trigger, and the output level of TO03 becomes active ("H" level).

(6) After the start of timer operation, channel 3 generates a timer interrupt (INTTM03) at 0.2 ms pulse width, and the output level of TO03 becomes inactive ("L" level) until the next start trigger (INTTM00 of channel 0) is detected.

Table 6.4 Required Peripheral Function and Its Use

Peripheral function	Use
Timer array unit 0	This unit is used to realize the one-shot pulse output function by operating channel 0 and channel 3 together and deliver a one-shot pulse output from the TO03 pin. (At this sample code, there is no specified output timing.)

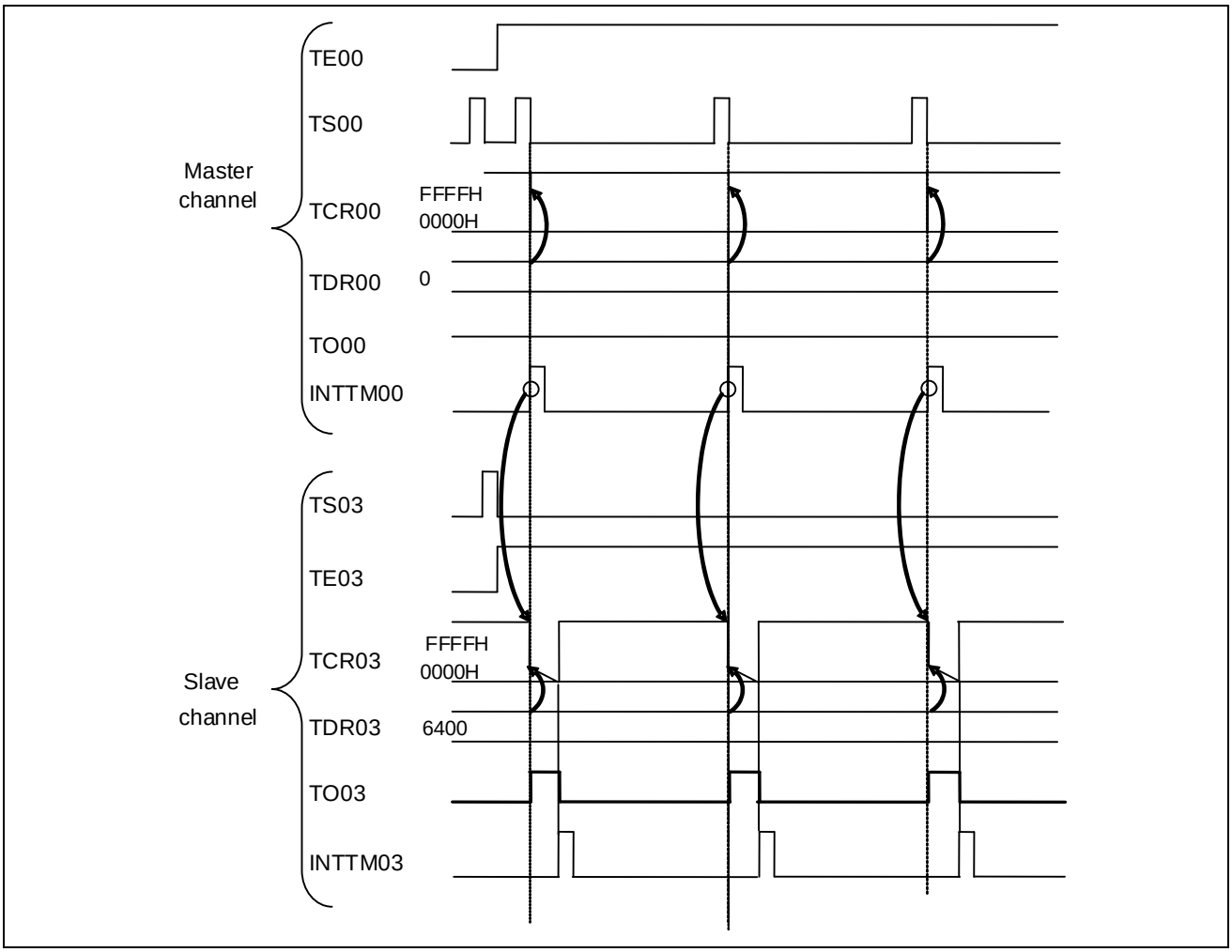

Figure 6.3 Simplified Timing Chart for One-Shot Pulse Output Operation (output timing=0)

6.4.2 List of Option Byte Setting

Table 6.5 summarizes the settings of the option bytes.

Table 6.5 Option Byte Settings

Address	Value	Description
000C0H/010C0H	01101110B	Disables the watchdog timer. (Stops counting after the release from the reset state.)
000C1H/010C1H	01111111B	LVD reset mode which uses 2.81 V (2.76 V to 2.87 V)
000C2H/010C2H	11101000B	HS mode, HOCO: 32 MHz
000C3H/010C3H	10000100B	Enables the on-chip debugger.

6.4.3 List of Constant

Table 6.6 lists the constant that is used in this sample program.

Table 6.6 Constant for the Sample Program

Constant	Setting	Description
_1900_TAU_TDR03_VALUE	0x1900U	TDR03 setting for duty of pulse width

6.4.4 List of Functions

Table 6.7 lists the functions that are used in this sample program.

Table 6.7 Functions

Function	Outline
R_TAU0_Channel0_Start	TAU0 channel 0 start processing

6.4.5 Function Specification

The followings are the functions that are used in this sample program.

[Function Name] R_TAU0_Channel0_Start

Synopsis	TAU0 channel 0 start processing
Header	r_cg_macrodriver.h r_cg_timer.h r_cg_userdefine.h
Declaration	void R_TAU0_Channel0_Start(void)
Explanation	This function unmasks TAU0 channel 0 interrupts and starts count operation.
Arguments	None
Return value	None
Remarks	None

[Function Name] r_tau0_channel0_interrupt()

Synopsis	TAU0 channel 0 timer interrupt processing
Header	r_cg_macrodriver.h r_cg_timer.h r_cg_userdefine.h
Declaration	static void __near r_tau0_channel0_interrupt(void)
Explanation	Customer can add own program in the interrupt routine.
Arguments	None
Return value	None
Remarks	None

6.4.6 Flow Chart

6.4.6.1 Overall Flow

Figure 6.4 shows the overall flow of the sample program described in this chapter.

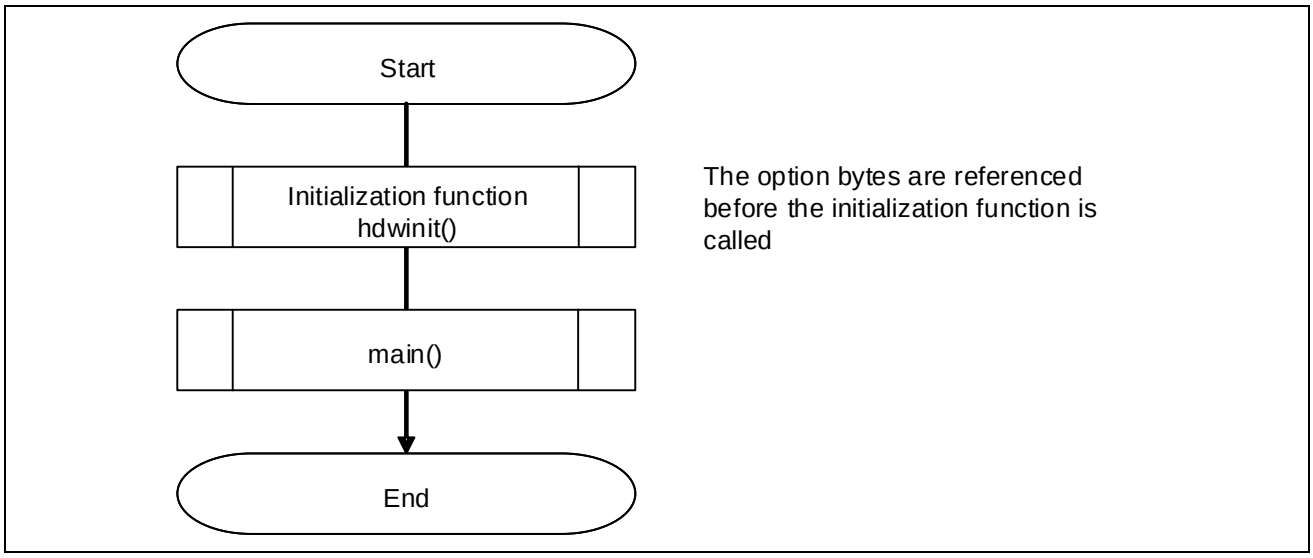

Figure 6.4 Overall Flow

6.4.6.2 Initialization Function

Figure 6.5 shows the flowchart for the initialization function.

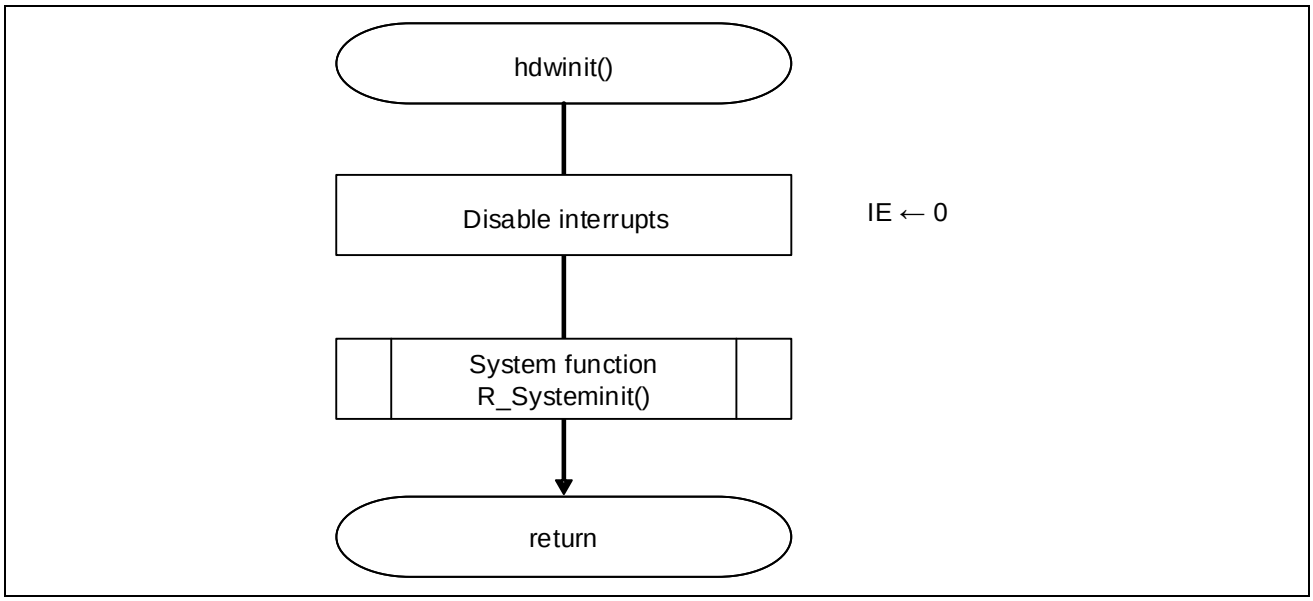

Figure 6.5 Initialization Function

6.4.6.3 System Function

Figure 6.6 shows the flowchart for the system function.

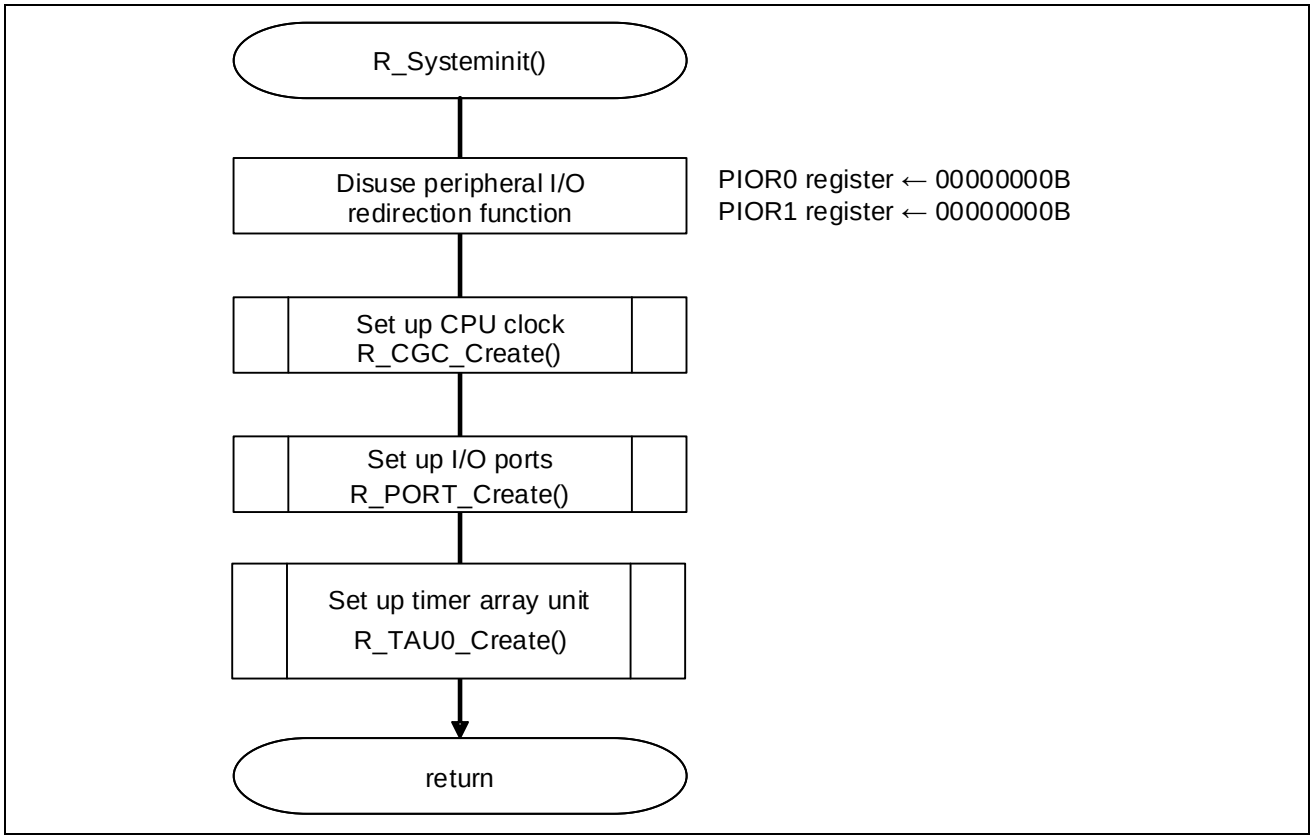

Figure 6.6 System Function

6.4.6.4 CPU Clock Setup

Figure 6.7 shows the flowchart for setting up the CPU clock.

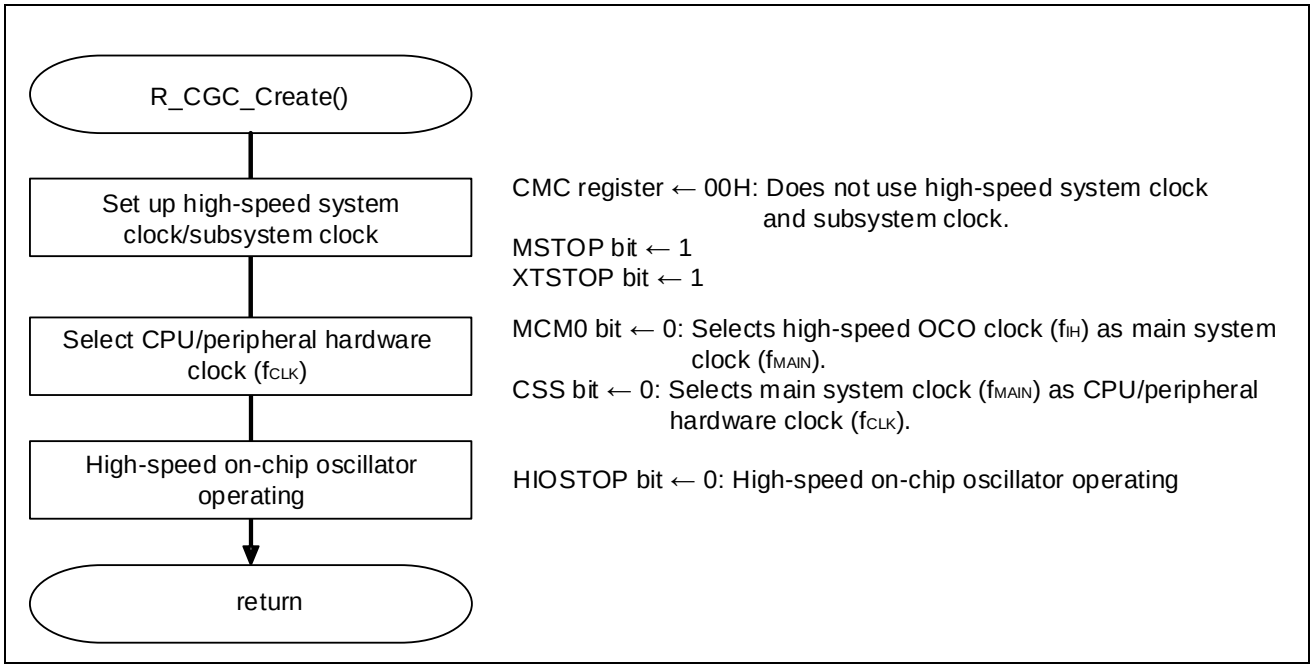

Figure 6.7 CPU Clock Setup

6.4.6.5 I/O Port Setup

Figure 6.8 shows the flowchart for setting up the I/O ports.

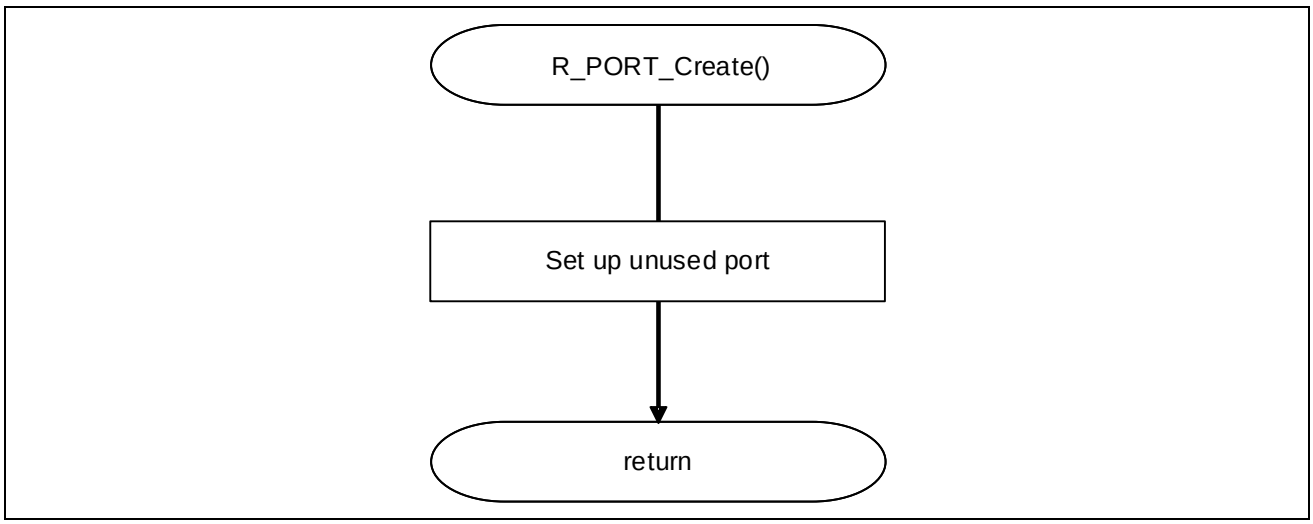

Figure 6.8 I/O Port Setup

Caution: Provide proper treatment for unused pins so that their electrical specifications are observed. Connect each of any unused input-only ports to V_{DD} or V_{SS} via a separate resistor.

6.4.6.6 Timer Array Unit Setup

Figures 6.9 and 6.10 show the flowchart for setting up the timer array unit.

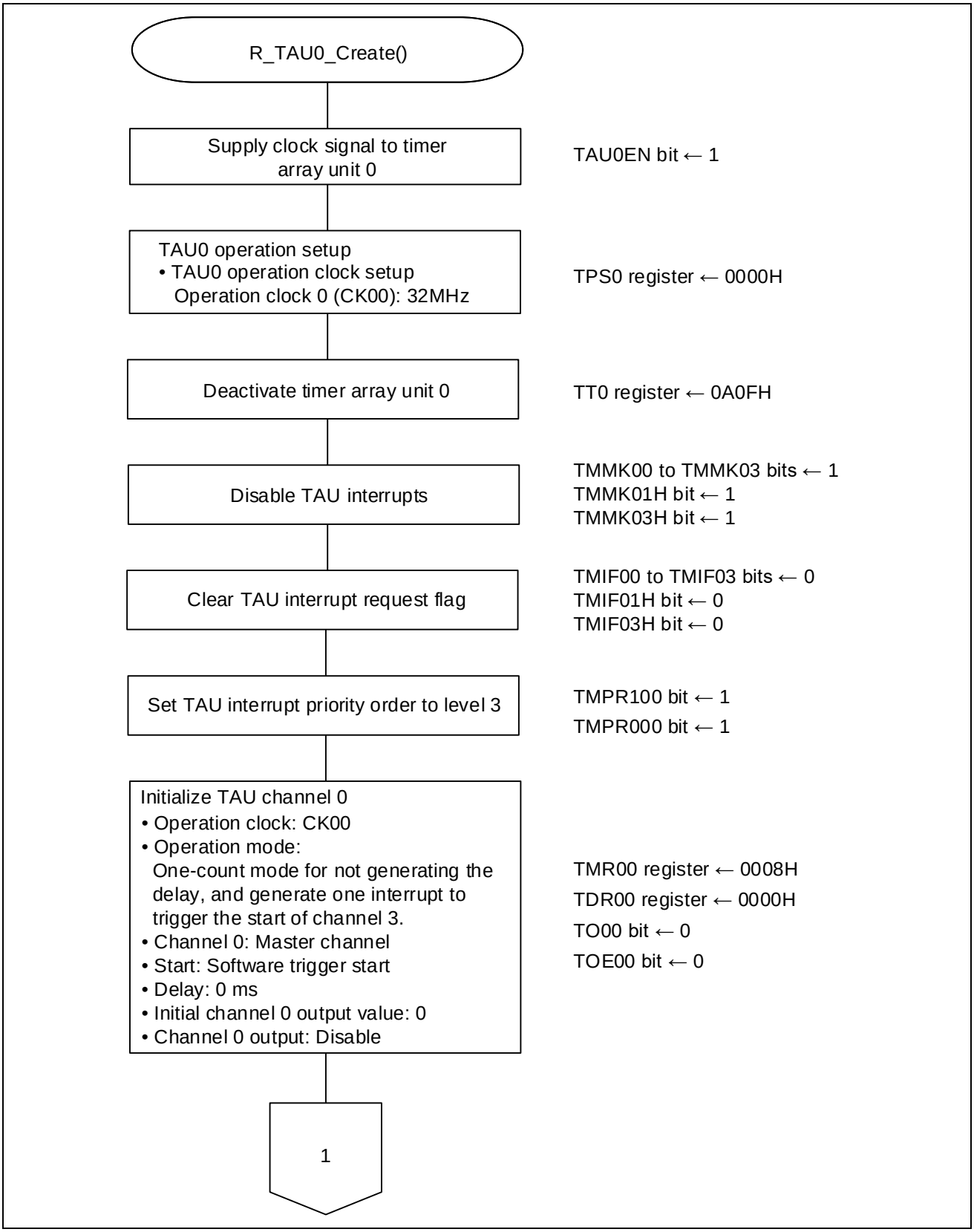

Figure 6.9 Timer Array Unit Setup (1/2)

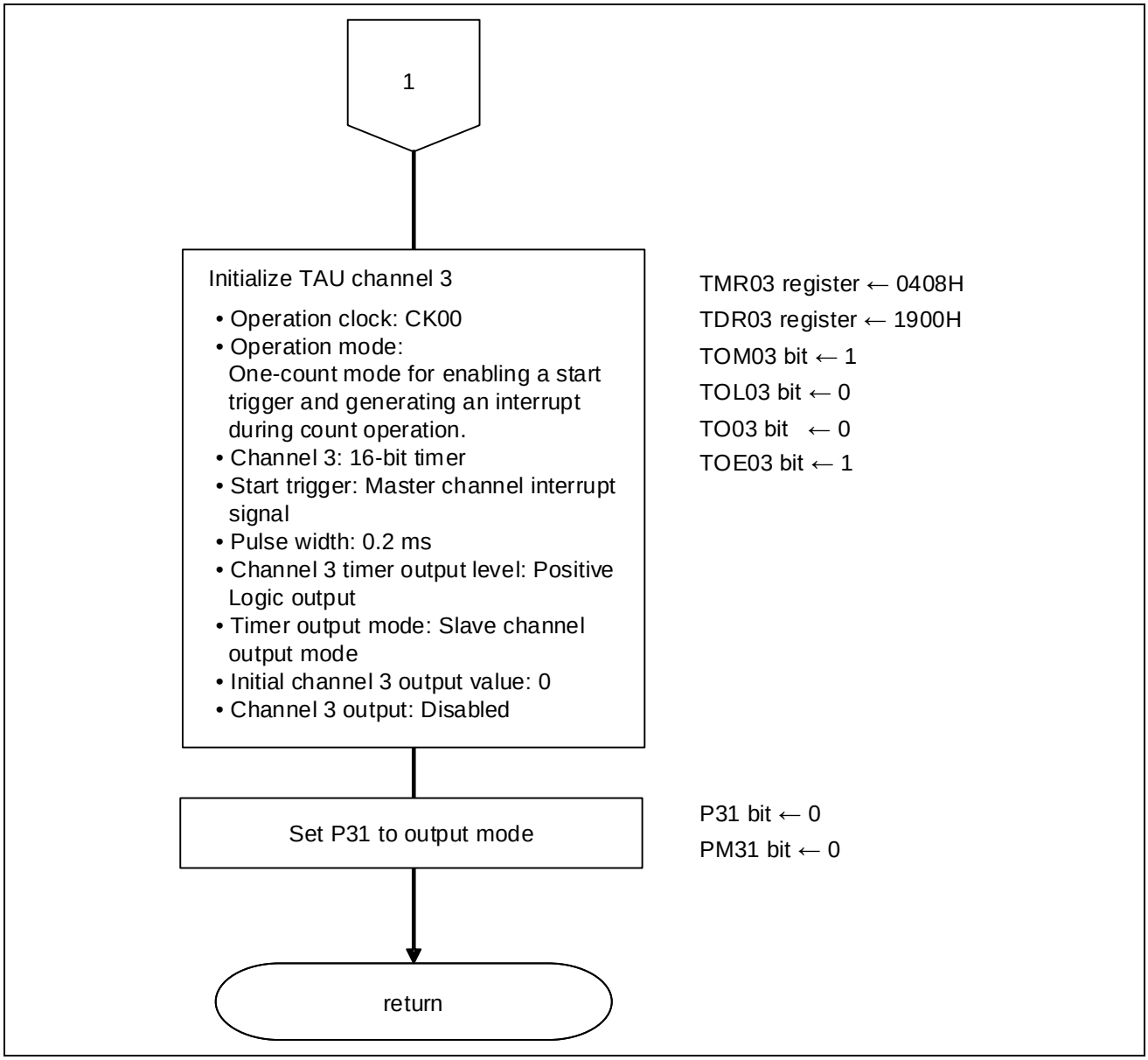

Figure 6.10 Timer Array Unit Setup (2/2)

Starting clock signal supply to the timer array unit 0

- Peripheral enable register 0 (PER0)

Start clock signal supply to the timer array unit 0.

Symbol: PER0

7	6	5	4	3	2	1	0
RTCEN	IICA1EN	ADCEN	IICA0EN	SAU1EN	SAU0EN	TAU1EN	TAU0EN
x	x	x	x	x	x	x	**1**

Bit 0

TAU0EN	Control of timer array unit 0 input clock supply
0	Stops input clock supply.
1	**Enables input clock supply.**

Caution: For details on the register setup procedures, refer to RL78/G14 User's Manual: Hardware.

x: Bits not used in this setting item

Configuring the timer clock frequency

- Timer clock select register 0 (TPS0)

  Select an operation clock for timer array unit 0.

Symbol: TPS0

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	PRS 031	PRS 030	0	0	PRS 021	PRS 020	PRS 013	PRS 012	PRS 011	PRS 010	PRS 003	PRS 002	PRS 001	PRS 000
0	0	x	x	0	0	x	x	x	x	x	x	0	0	0	0

Bits 3 to 0

PRS 003	PRS 002	PRS 001	PRS 000	Operation clock (CK00) selection					
					f_{CLK}= 2 MHz	f_{CLK}= 4 MHz	f_{CLK}= 8 MHz	f_{CLK}= 20 MHz	f_{CLK}= 32 MHz
0	0	0	0	f_{CLK}	2 MHz	4 MHz	8 MHz	20 MHz	32 MHz
0	0	0	1	$f_{CLK}/2$	1 MHz	2 MHz	4 MHz	10 MHz	16 MHz
0	0	1	0	$f_{CLK}/2^2$	500 kHz	1 MHz	2 MHz	5 MHz	8 MHz
0	0	1	1	$f_{CLK}/2^3$	250 kHz	500 kHz	1 MHz	2.5 MHz	4 MHz
0	1	0	0	$f_{CLK}/2^4$	125 kHz	250 kHz	500 kHz	1.25 MHz	2 MHz
0	1	0	1	$f_{CLK}/2^5$	62.5 kHz	125 kHz	250 kHz	625 kHz	1 MHz
0	1	1	0	$f_{CLK}/2^6$	31.3 kHz	62.5 kHz	125 kHz	313 kHz	500 kHz
0	1	1	1	$f_{CLK}/2^7$	15.6 kHz	31.3 kHz	62.5 kHz	156 kHz	250 kHz
1	0	0	0	$f_{CLK}/2^8$	7.81 kHz	15.6 kHz	31.3 kHz	78.1 kHz	125 kHz
1	0	0	1	$f_{CLK}/2^9$	3.91 kHz	7.81 kHz	15.6 kHz	39.1 kHz	62.5 kHz
1	0	1	0	$f_{CLK}/2^{10}$	1.95 kHz	3.91 kHz	7.81 kHz	19.5 kHz	31.25 kHz
1	0	1	1	$f_{CLK}/2^{11}$	977 Hz	1.95 kHz	3.91 kHz	9.77 kHz	15.6 kHz
1	1	0	0	$f_{CLK}/2^{12}$	488 Hz	977 Hz	1.95 kHz	4.88 kHz	7.81 kHz
1	1	0	1	$f_{CLK}/2^{13}$	244 Hz	488 Hz	977 Hz	2.44 kHz	3.91 kHz
1	1	1	0	$f_{CLK}/2^{14}$	122 Hz	244 Hz	488 Hz	1.22 kHz	1.95 kHz
1	1	1	1	$f_{CLK}/2^{15}$	61.0 Hz	122 Hz	244 Hz	610 Hz	977 Hz

Caution: For details on the register setup procedures, refer to RL78/G14 User's Manual: Hardware.

x: Bits not used in this setting item

Setting up the channel 0 operation mode

- Timer mode register 00 (TMR00)

Select an operation clock (f_{MCK}).
Select a count clock.
Select a start trigger and capture trigger.
Select a valid edge for timer input.
Set up the operation mode.

Symbol: TMR00

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CKS001	CKS000	0	CCS00	0	STS002	STS001	STS000	CIS001	CIS000	0	0	MD003	MD002	MD001	MD000
0	0	0	0	0	0	0	0	x	x	0	0	1	0	0	0

Bits 15 and 14

CKS001	CKS000	Selection of operation clock (f_{MCK}) of channel 0
0	0	Operation clock CK00 set by timer clock select register 0 (TPS0)
0	1	Operation clock CK02 set by timer clock select register 0 (TPS0)
1	0	Operation clock CK01 set by timer clock select register 0 (TPS0)
1	1	Operation clock CK03 set by timer clock select register 0 (TPS0)

Bit 12

CCS00	Selection of count clock (f_{TCLK}) of channel 0
0	Operation clock (f_{MCK}) specified by the CKS000 and CKS001 bits
1	Valid edge of input signal input from the TI00 pin

Bits 10 to 8

STS002	STS001	STS000	Setting of start trigger or capture trigger of channel 0
0	0	0	Only software trigger start is valid (other trigger sources are unselected).
0	0	1	Valid edge of the TI00 pin input is used as both the start trigger and capture trigger.
0	1	0	Both the edges of the TI00 pin input are used as a start trigger and a capture trigger.
1	0	0	Interrupt signal of the master channel is used (when the channel is used as a slave channel with the simultaneous channel operation function).
Other than above			Setting prohibited

Caution: For details on the register setup procedures, refer to RL78/G14 User's Manual: Hardware.
x: Bits not used in this setting item

Symbol: TMR00

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CKS 001	**CKS 000**	**0**	**CCS 00**	**0**	**STS 002**	**STS 001**	**STS 000**	**CIS 001**	**CIS 000**	**0**	**0**	**MD 003**	**MD 002**	**MD 001**	**MD 000**
0	**0**	0	**0**	0	**0**	**0**	**0**	x	x	0	0	**1**	**0**	**0**	**0**

Bits 3 to 0

MD003	MD002	MD001	MD000	Operation mode of channel 0	Corresponding function	Count operation of TCR
0	0	0	1/0	Interval timer mode	Interval timer / Square wave output / Divider function / PWM output (master)	Counting down
0	1	0	1/0	Capture mode	Input pulse interval measurement	Counting up
0	1	1	0	Event counter mode	External event counter	Counting down
1	**0**	**0**	1/**0**	**One-count mode**	Delay counter / **One-shot pulse output** / PWM output (slave)	**Counting down**
1	1	0	0	Capture & one-count mode	Measurement of high-/low-level width of input signal	Counting up
Other than above				Setting prohibited		

The operation of each mode varies depending on MD000 bit (see table below).

Operation mode (Value set by the MD003 to MD001 bits (see table above))	MD000	Setting of starting counting and interrupt
• Interval timer mode (0, 0, 0) • Capture mode (0, 1, 0)	0	Timer interrupt is not generated when counting is started (timer output does not change, either).
	1	Timer interrupt is generated when counting is started (timer output also changes).
• Event counter mode (0, 1, 1)	0	Timer interrupt is not generated when counting is started (timer output does not change, either).
• One-count mode (1, 0, 0)	**0**	**Start trigger is invalid during counting operation. At that time, interrupt is not generated.**
	1	Start trigger is valid during counting operation. At that time, interrupt is also generated.
• Capture & one-count mode (1, 1, 0)	0	Timer interrupt is not generated when counting is started (timer output does not change, either). Start trigger is invalid during counting operation. At that time interrupt is not generated.
Other than above		Setting prohibited

Caution: For details on the register setup procedures, refer to RL78/G14 User's Manual: Hardware.
x: Bits not used in this setting item

Setting up the channel 3 operation mode

- Timer mode register 03 (TMR03)

Select an operation clock (f_{MCK}).
Select a count clock.
Select the 16/8-bit timer.
Select a start trigger and capture trigger.
Select a valid edge for timer input.
Set up the operation mode.

Symbol: TMR03

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CKS031	CKS030	0	CCS03	SPLIT03	STS032	STS031	STS030	CIS031	CIS030	0	0	MD033	MD032	MD031	MD030
0	0	0	0	0	1	0	0	x	x	0	0	1	0	0	0

Bits 15 and 14

CKS031	CKS030	Selection of operation clock (f_{MCK}) of channel 3
0	0	Operation clock CK00 set by timer clock select register 0 (TPS0)
0	1	Operation clock CK02 set by timer clock select register 0 (TPS0)
1	0	Operation clock CK01 set by timer clock select register 0 (TPS0)
1	1	Operation clock CK03 set by timer clock select register 0 (TPS0)

Bit 12

CCS03	Selection of count clock (f_{TCLK}) of channel 3
0	Operation clock (f_{MCK}) specified with the CKS030 and CKS031 bits
1	Valid edge of input signal input from the TI03 pin

Bit 11

SPLIT03	Selection of 8 or 16-bit timer operation for channel 3
0	Operates as 16-bit timer (Operates in independent channel operation function or as slave channel in simultaneous channel operation function.)
1	Operates as 8-bit timer.

Bits 10 to 8

STS032	STS031	STS030	Setting of start trigger or capture trigger of channel 3
0	0	0	Only software trigger start is valid (other trigger sources are unselected).
0	0	1	Valid edge of the TI03 pin input is used as both the start trigger and capture trigger.
0	1	0	Both the edges of the TI03 pin input are used as a start trigger and a capture trigger.
1	0	0	Interrupt signal of the master channel is used (when the channel is used as a slave channel with the simultaneous channel operation function).
Others than above			Setting prohibited

Caution: For details on the register setup procedures, refer to RL78/G14 User's Manual: Hardware.
x: Bits not used in this setting item

Symbol: TMR03

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CKS 031	CKS 030	0	CCS 03	SPLIT 03	STS 032	STS 031	STS 030	CIS 031	CIS 030	0	0	MD 033	MD 032	MD 031	MD 030
0	0	0	0	0	1	0	0	x	x	0	0	1	0	0	0

Bits 3 to 0

MD033	MD032	MD031	MD030	Operation mode of channel 3	Corresponding function	Count operation of TCR
0	0	0	1/0	Interval timer mode	Interval timer / Square wave output / Divider function / PWM output (master)	Counting down
0	1	0	1/0	Capture mode	Input pulse interval measurement	Counting up
0	1	1	0	Event counter mode	External event counter	Counting down
1	**0**	**0**	1/**0**	**One-count mode**	Delay counter / **One-shot pulse output** / PWM output (slave)	**Counting down**
1	1	0	0	Capture & one-count mode	Measurement of high-/low-level width of input signal	Counting up
Other than above				Setting prohibited		

The operation of each mode varies depending on MD030 bit (see table below).

Operation mode (Value set by the MD033 to MD031 bits (see table above))	MD030	Setting of starting counting and interrupt
• Interval timer mode (0, 0, 0) • Capture mode (0, 1, 0)	0	Timer interrupt is not generated when counting is started (timer output does not change, either).
	1	Timer interrupt is generated when counting is started (timer output also changes).
• Event counter mode (0, 1, 1)	0	Timer interrupt is not generated when counting is started (timer output does not change, either).
• One-count mode (1, 0, 0)	**0**	**Start trigger is invalid during counting operation. At that time, interrupt is not generated.**
	1	Start trigger is valid during counting operation. At that time, interrupt is also generated.
• Capture & one-count mode (1, 1, 0)	0	Timer interrupt is not generated when counting is started (timer output does not change, either). Start trigger is invalid during counting operation. At that time interrupt is not generated.
Other than above		Setting prohibited

Caution: For details on the register setup procedures, refer to RL78/G14 User's Manual: Hardware.
x: Bits not used in this setting item

Configuring the delay time

- Timer data register 00 (TDR00)
  Configure no delay.

Symbol: TDR00

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Delay time = (TDR00 setting + 2) × Count clock cycle time
0 [ms] = (1/32[MHz]) × (TDR00 setting + 2)

⇒ TDR00 setting = 0

Configuring the pulse output width

- Timer data register 03 (TDR03)
  Configure the pulse output width.

Symbol: TDR03

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Pulse output width = (TDR03 setting) × Count clock cycle time
0.2 [ms] = (1/32[MHz]) × (TDR03 setting)

⇒ TDR03 setting = 6400

Setting up the timer output mode

- Timer output mode register 0 (TOM0)
  Set up the timer output mode for each channel.

Symbol: TOM0

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	TOM03	TOM02	TOM01	0
0	0	0	0	0	0	0	0	0	0	0	0	1	x	x	0

Bit 3

TOM03	Control of timer output mode of channel 3
0	Master channel output mode (to produce toggle output by timer interrupt request signal (INTTM03))
1	**Slave channel output mode (output is set by the timer interrupt request signal (INTTM03) of the master channel, and reset by the timer interrupt request signal (INTTM0p) of the slave channel)**

Caution: For details on the register setup procedures, refer to RL78/G14 User's Manual: Hardware.
x: Bits not used in this setting item

Configuring the output level for the timer output pin

- Timer output level register 0 (TOL0)

Configure the output level for the timer output pin for each channel.

Symbol: TOL0

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	TOL03	TOL02	TOL01	0
0	0	0	0	0	0	0	0	0	0	0	0	0	x	x	0

Bit 3

TOL03	Control of timer output level of channel 3
0	Positive logic output (active-high)
1	Negative logic output (active-low)

Configuring the output value for the timer output pin

- Timer output register 0 (TO0)

Configure the output value for the timer output pin for each channel.

Symbol: TO0

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	TO03	TO02	TO01	TO00
0	0	0	0	0	0	0	0	0	0	0	0	0	x	x	0

Bit 3

TO03	Timer output of channel 3
0	Timer output value is “0”
1	Timer output value is “1”

Bit 0

TO00	Timer output of channel 0
0	Timer output value is “0”
1	Timer output value is “1”

Caution: For details on the register setup procedures, refer to RL78/G14 User's Manual: Hardware.
x: Bits not used in this setting item

Enabling the timer output

- Timer output enable register 0 (TOE0)
  Enable/disable the timer output for each channel.

Symbol: TOE0

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	TOE03	TOE02	TOE01	TOE00
0	0	0	0	0	0	0	0	0	0	0	0	1	x	x	0

Bit 3

TOE03	Timer output enable/disable of channel 3
0	Timer output is disabled. Timer operation is not applied to the TO03 bit and the output is fixed. Writing to the TO03 bit is enabled and the level set in the TO03 bit is output from the TO03 pin.
1	**Timer output is enabled.** **Timer operation is applied to the TO03 bit and an output waveform is generated.** **Writing to the TO03 bit is ignored.**

Bit 0

TOE00	Timer output enable/disable of channel 0
0	**Timer output is disabled.** **Timer operation is not applied to the TO00 bit and the output is fixed.** **Writing to the TO00 bit is enabled and the level set in the TO00 bit is output from the TO00 pin.**
1	Timer output is enabled. Timer operation is applied to the TO00 bit and an output waveform is generated. Writing to the TO00 bit is ignored.

Setting up the one-shot pulse output pin

- Port mode register (PM3)
  Select the I/O mode.

Symbol: PM3

7	6	5	4	3	2	1	0
1	1	1	1	1	1	PM31	PM30
1	1	1	1	1	1	0	x

Bit 1

PM31	P31 pin I/O mode selection
0	**Output mode (the pin functions as an output port (output buffer on))**
1	Input mode (the pin functions as an input port (output buffer off))

Caution: For details on the register setup procedures, refer to RL78/G14 User's Manual: Hardware.
x: Bits not used in this setting item

6.4.6.7 Main Processing

Figure 6.11 shows the flowchart for main processing.

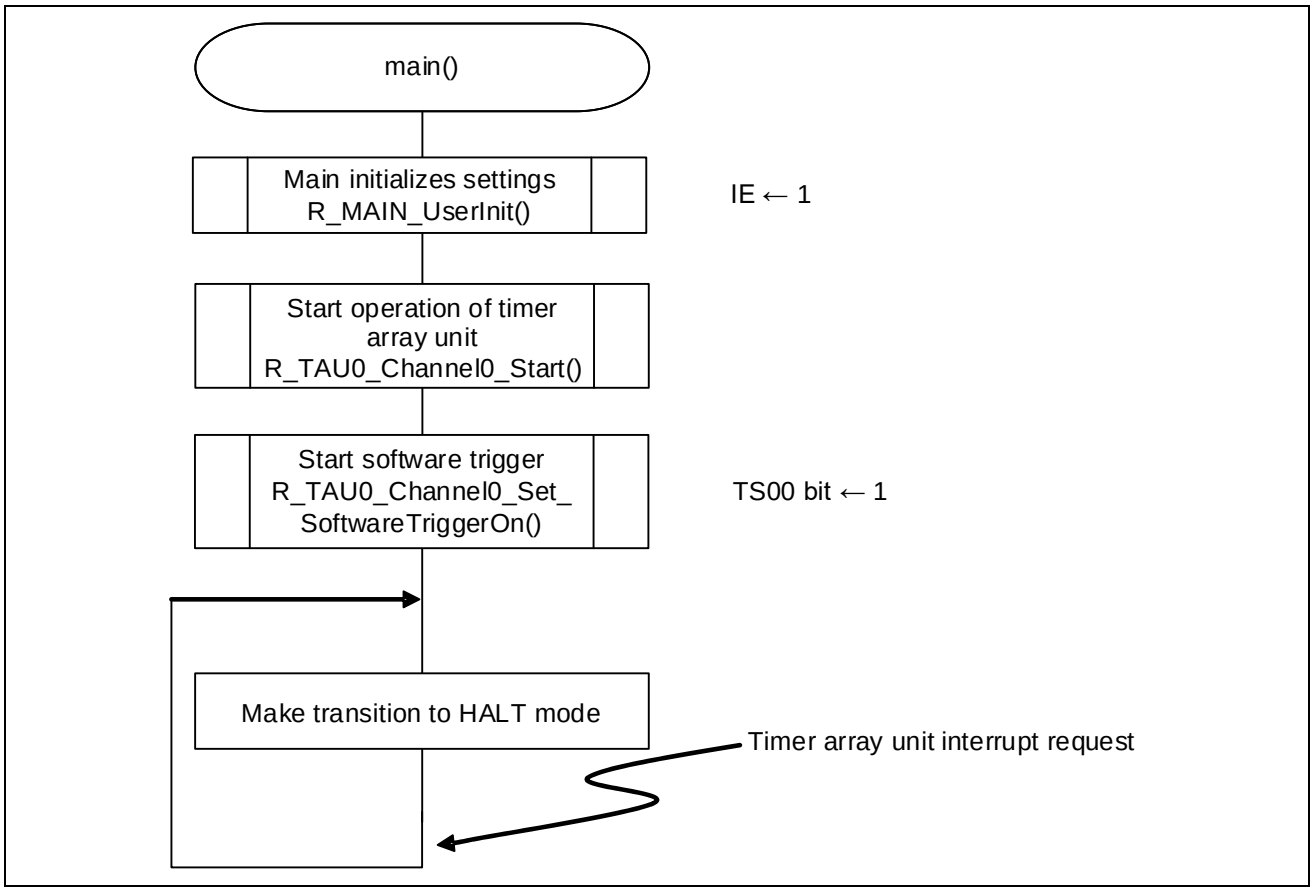

Figure 6.11 Main Processing

6.4.6.8 Timer Array Unit Startup

Figure 6.12 shows the flowchart for starting the operation of the timer array unit.

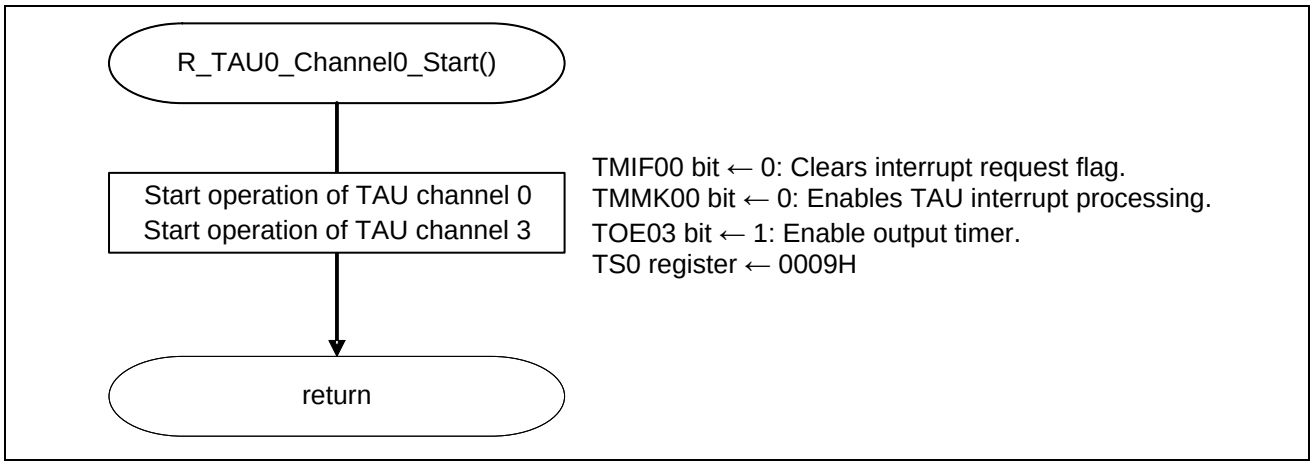

Figure 6.12 Timer Array Unit Startup

Configuring the timer interrupt

- Interrupt request flag register (IF1L)
  Clear the interrupt request flag.
- Interrupt mask flag register (MK1L)
  Enable interrupt processing.

Symbol: IF1L

7	6	5	4	3	2	1	0
TMIF03	TMIF02	TMIF01	TMIF00	IICAIF0	SREIF1 TMIF03H	SRIF1 CSIIF11 IICIF11	STIF1 CSIIF10 IICIF10
x	x	x	**0**	x	x	x	x

Bit 4

TMIF00	Interrupt request flag
0	**No interrupt request signal is generated**
1	Interrupt request is generated, interrupt request status

Symbol: MK1L

7	6	5	4	3	2	1	0
TMMK03	TMMK02	TMMK01	TMMK00	IICAMK0	SREMK1 TMMK03H	SRMK1 CSIMK11 IICMK11	STMK1 CSIMK10 IICMK10
x	x	x	**0**	x	x	x	x

Bit 4

TMMK00	Interrupt servicing control
0	**Interrupt servicing enabled**
1	Interrupt servicing disabled

Caution: For details on the register setup procedures, refer to RL78/G14 User's Manual: Hardware.
x: Bits not used in this setting item

Enable the output of timer

- Timer output enable register 0 (TOE0)

  Enable output of channel 3.

Symbol: TOE0

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	TOE03	TOE02	TOE01	TOE00
0	0	0	0	0	0	0	0	0	0	0	0	1	x	x	x

Bit 3

TOE03	Timer output enable/disable of channel 3
0	Timer output is disabled. Timer operation is not applied to the TO03 bit and the output is fixed. Writing to the TO03 bit is enabled and the level set in the TO03 bit is output from the TO03 pin.
1	**Timer output is enabled.** **Timer operation is applied to the TO03 bit and an output waveform is generated.** **Writing to the TO03 bit is ignored.**

Configuring the timer startup

- Timer channel start register 0 (TS0)

  Enable count operation of channel 0 and channel 3.

Symbol: TS0

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	TSH03	0	TSH01	0	0	0	0	0	TS03	TS02	TS01	TS00
0	0	0	0	x	0	x	0	0	0	0	0	1	x	x	1

Bit 3

TS03	Operation enable (start) trigger of channel 3
0	No trigger operation
1	**The TE03 bit is set to 1 and the count operation becomes enabled.** **The TCR03 register count operation start in the count operation enabled state varies depending on each operation mode.**

Bit 0

TS00	Operation enable (start) trigger of channel 0
0	No trigger operation
1	**The TE00 bit is set to 1 and the count operation becomes enabled.** **The TCR00 register count operation start in the count operation enabled state varies depending on each operation mode.**

Caution: For details on the register setup procedures, refer to RL78/G14 User's Manual: Hardware.

x: Bits not used in this setting item

6.4.6.9 INTTM00 Interrupt Processing

Figure 6.13 shows the flowchart for INTTM00 interrupt processing.

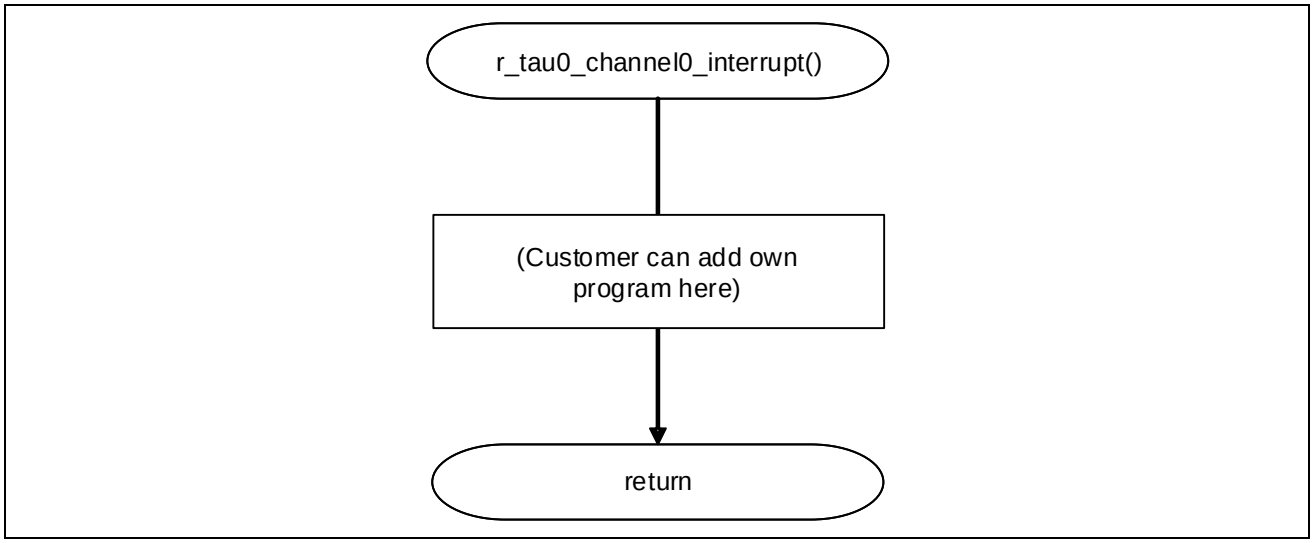

Figure 6.13 INTTM00 Interrupt Processing

7. Example of Migration from Programmable Wait One-shot Generation Mode

7.1 Specifications

When implementing programmable wait one-shot generation mode of Timer RB in R8C/36M, RL78/G14 can use one-shot pulse output of TAU.
Two channels are used as a set to generate a one-shot pulse with a specified output timing and a specified pulse width.

Table 7.1 lists the peripheral functions to be used and their uses (example of migration from programmable wait one-shot generation mode), and Figure 7.1 shows operation overview (example of migration from programmable wait one-shot generation mode).

Table 7.1 Peripheral Functions to be Used and Their Uses (Programmable Wait One-shot Generation Mode)

Peripheral Function	Use
Timer array unit (One-shot pulse output)	Generate a one-shot pulse with a specified output timing and a specified pulse width

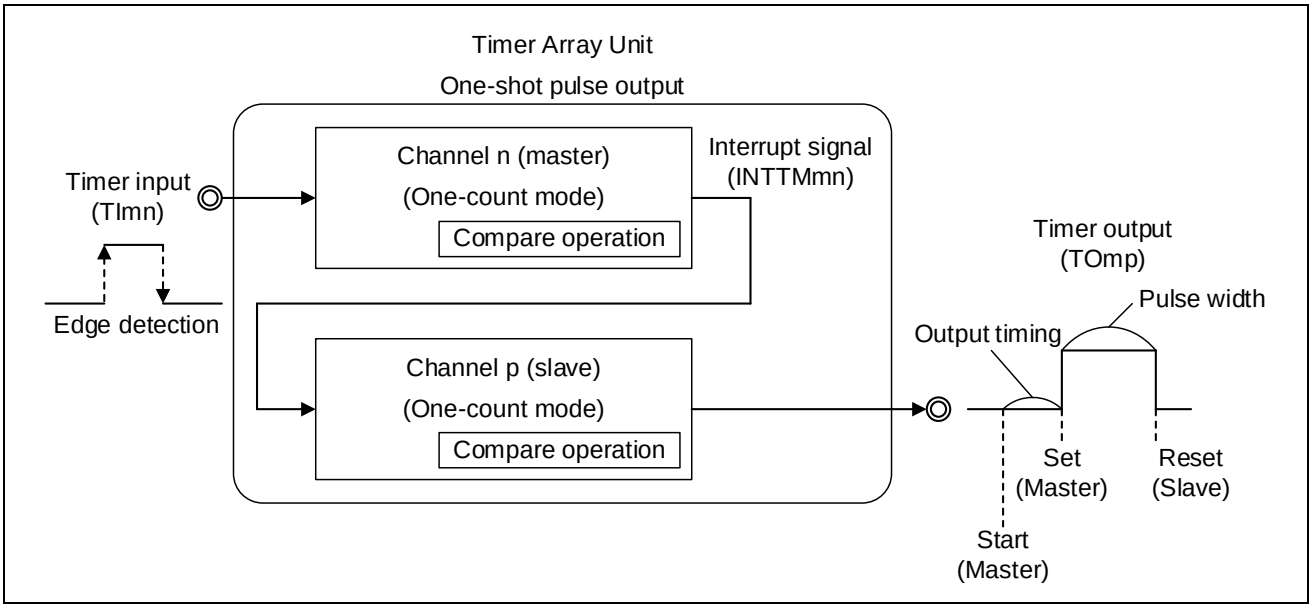

Figure 7.1 Operation Overview (Programmable Wait One-shot Generation Mode)

7.2 Operation Check Conditions

The sample code described in this application note has been checked under the conditions listed in the table below.

Table 7.2 Operation Check Conditions

Item	Description
Microcontroller used	RL78/G14 (R5F104LEAFB)
Operating frequency	High-speed on-chip oscillator (HOCO) clock: 32 MHz CPU/peripheral hardware clock: 32 MHz
Operating voltage	5.0V (can run on a voltage range of 2.9 V to 5.5 V.) LVD operation (V_{LVD}): Reset mode 2.81 V (2.76 V to 2.87 V)
Integrated development environment (CS+)	CS+ V4.01.00 from Renesas Electronics Corp.
C compiler (CS+)	CC-RL V1.03.00 from Renesas Electronics Corp.
Integrated development environment (e^2 studio)	e^2 studio V5.2.0.020 from Renesas Electronics Corp.
C compiler (e^2 studio)	CC-RL V1.03.00 from Renesas Electronics Corp.

7.3 Description of Hardware

7.3.1 Hardware Configuration Example

Figure 7.2 shows an example of the hardware configuration used for this application note.

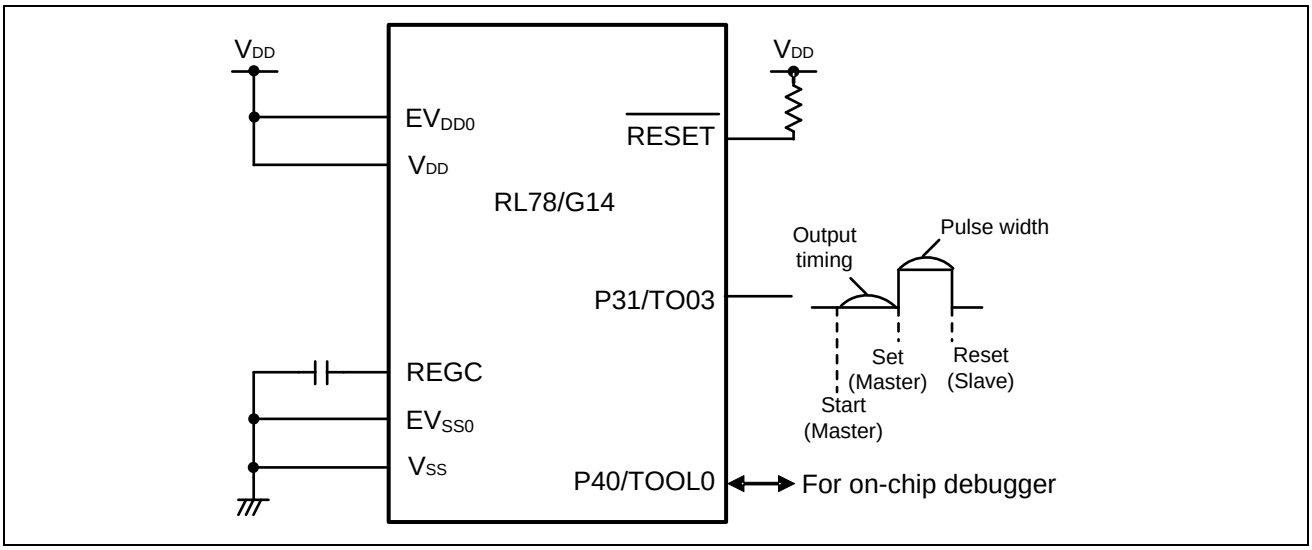

Figure 7.2 Hardware Configuration

Cautions: 1. The purpose of this circuit is only to provide the connection outline and the circuit is simplified accordingly. When designing and implementing an actual circuit, provide proper pin treatment and make sure that the hardware's electrical specifications are met (connect the input-only ports separately to V_{DD} or V_{SS} via a resistor).

2. Connect any pins whose name begins with EV_{SS} to V_{SS} and any pins whose name begins with EV_{DD} to V_{DD}, respectively.
3. V_{DD} must be held at not lower than the reset release voltage (V_{LVD}) that is specified as LVD.

7.3.2 List of Pins to be used

Table 7.3 lists the pins to be used and their functions.

Table 7.3 Pins to be Used and Their Functions

Pin Name	I/O	Description
P31/TO03	Output	One-shot pulse output port

7.4 Description of Software

7.4.1 Operation Outline

The sample program covered in this chapter implements one-shot pulse output by operating channel 0 and channel 3 together, and delivers an one-shot pulse output from P31/TO03.

Table 7.4 shows the required peripheral function and its use. Figure 7.3 is a simplified timing chart which summarizes the one-shot pulse output operation.

(1) Initialize the TAU.
<Conditions for setting>
Set the P31/TO03 pin to an one-shot pulse output.
Set TAU0 channel 0 to one-count mode and counts the 2 ms delays.
Set TAU0 channel 3 to one-count mode and counts the 0.2 ms pulse width.

(2) Operation starts when both the operation enable trigger bits for TAU0's channel 0 and channel 3 are set to 1 simultaneously. The sample program executes a HALT instruction to wait for a timer interrupt (INTTM00) from channel 0.

(3) After the start of timer operation, channel 0 generates a timer interrupt (INTTM00) at 2 ms delays.

(4) When the HALT mode is canceled by a timer interrupt (INTTM00) from channel 0, and channel 0 stops counting until the next start trigger is detected.

(5) Channel 3 starts operation using INTTM00 of channel 0 as a start trigger, and the output level of TO03 becomes active ("H" level).

(6) After the start of timer operation, channel 3 generates a timer interrupt (INTTM03) at 0.2 ms pulse width, and the output level of TO03 becomes inactive ("L" level) until the next start trigger (INTTM00 of channel 0) is detected.

Table 7.4 Required Peripheral Function and Its Use

Peripheral function	Use
Timer array unit 0	This unit is used to realize the one-shot pulse output function by operating channel 0 and channel 3 together and deliver a one-shot pulse output from the TO03 pin.

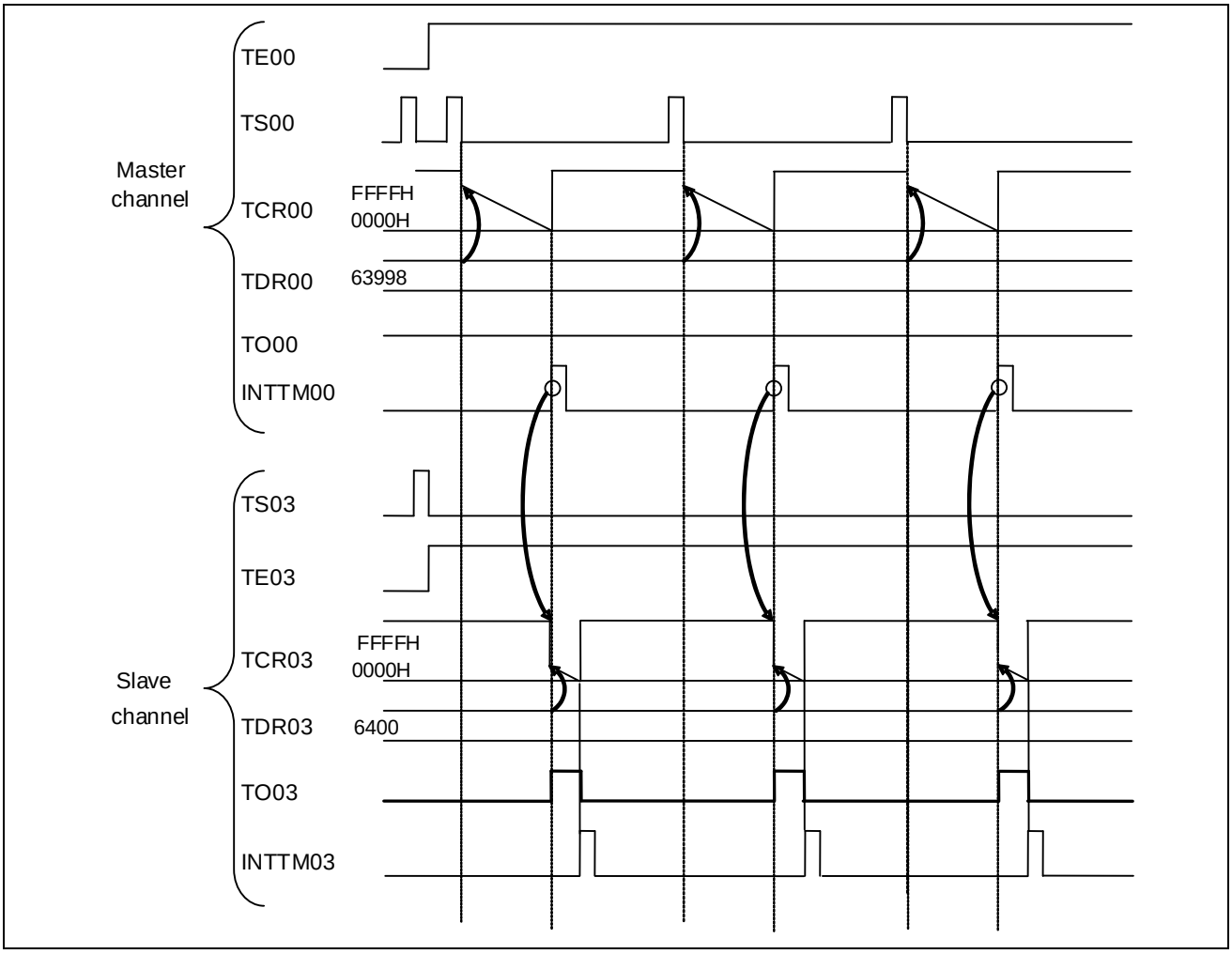

Figure 7.3 Simplified Timing Chart for One-Shot Pulse Output Operation

7.4.2 List of Option Byte Setting

Table 7.5 summarizes the settings of the option bytes.

Table 7.5 Option Byte Settings

Address	Value	Description
000C0H/010C0H	01101110B	Disables the watchdog timer. (Stops counting after the release from the reset state.)
000C1H/010C1H	01111111B	LVD reset mode which uses 2.81 V (2.76 V to 2.87 V)
000C2H/010C2H	11101000B	HS mode, HOCO: 32 MHz
000C3H/010C3H	10000100B	Enables the on-chip debugger.

7.4.3 List of Constant

Table 7.6 lists the constant that is used in this sample program.

Table 7.6 Constant for the Sample Program

Constant	Setting	Description
_1900_TAU_TDR03_VALUE	0x1900U	TDR03 setting for duty of pulse width

7.4.4 List of Functions

Table 7.7 lists the functions that are used in this sample program.

Table 7.7 Functions

Function	Outline
R_TAU0_Channel0_Start	TAU0 channel 0 start processing

7.4.5 Function Specification

The followings are the functions that are used in this sample program.

[Function Name] R_TAU0_Channel0_Start

Synopsis	TAU0 channel 0 start processing
Header	r_cg_macrodriver.h r_cg_timer.h r_cg_userdefine.h
Declaration	void R_TAU0_Channel0_Start(void)
Explanation	This function unmasks TAU0 channel 0 interrupts and starts count operation.
Arguments	None
Return value	None
Remarks	None

[Function Name] r_tau0_channel0_interrupt()

Synopsis	TAU0 channel 0 timer interrupt processing
Header	r_cg_macrodriver.h r_cg_timer.h r_cg_userdefine.h
Declaration	static void __near r_tau0_channel0_interrupt(void)
Explanation	Customer can add own program in the interrupt routine.
Arguments	None
Return value	None
Remarks	None

7.4.6 Flow Chart

7.4.6.1 Overall Flow

Figure 7.4 shows the overall flow of the sample program described in this chapter.

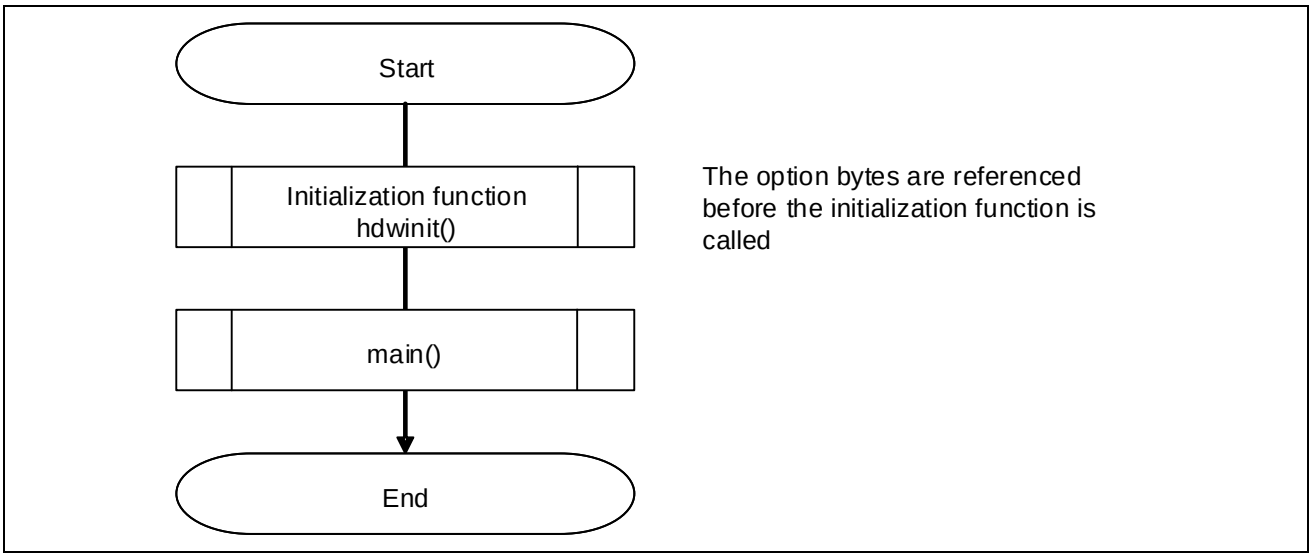

Figure 7.4 Overall Flow

7.4.6.2 Initialization Function

Figure 7.5 shows the flowchart for the initialization function.

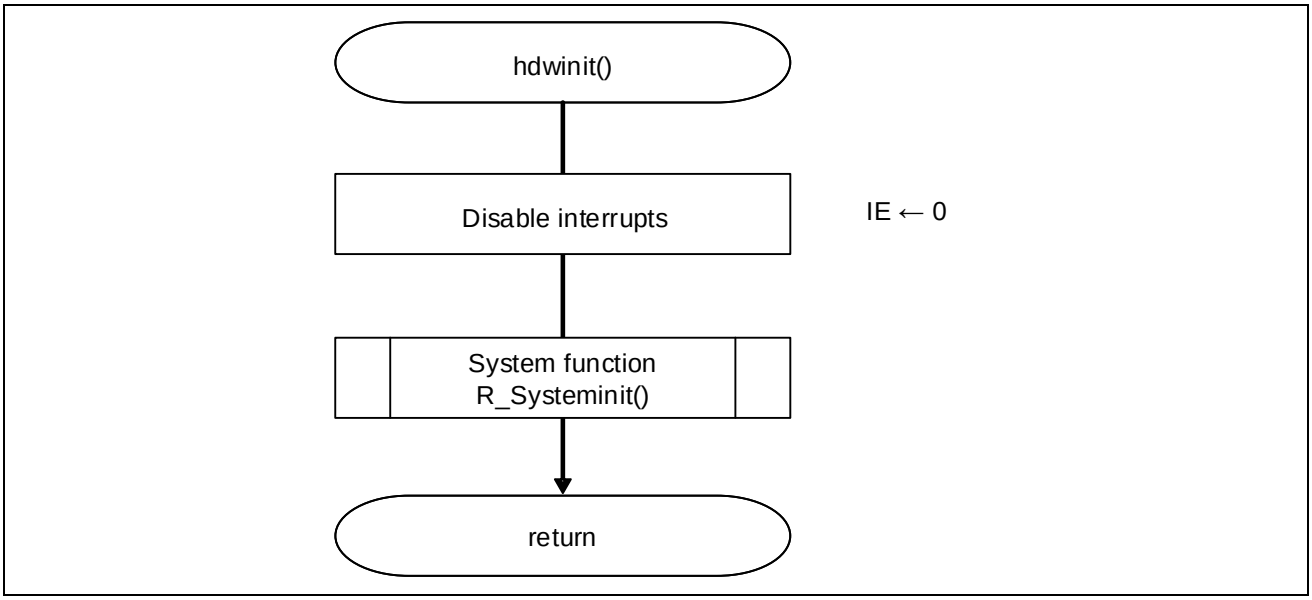

Figure 7.5 Initialization Function

7.4.6.3 System Function

Figure 7.6 shows the flowchart for the system function.

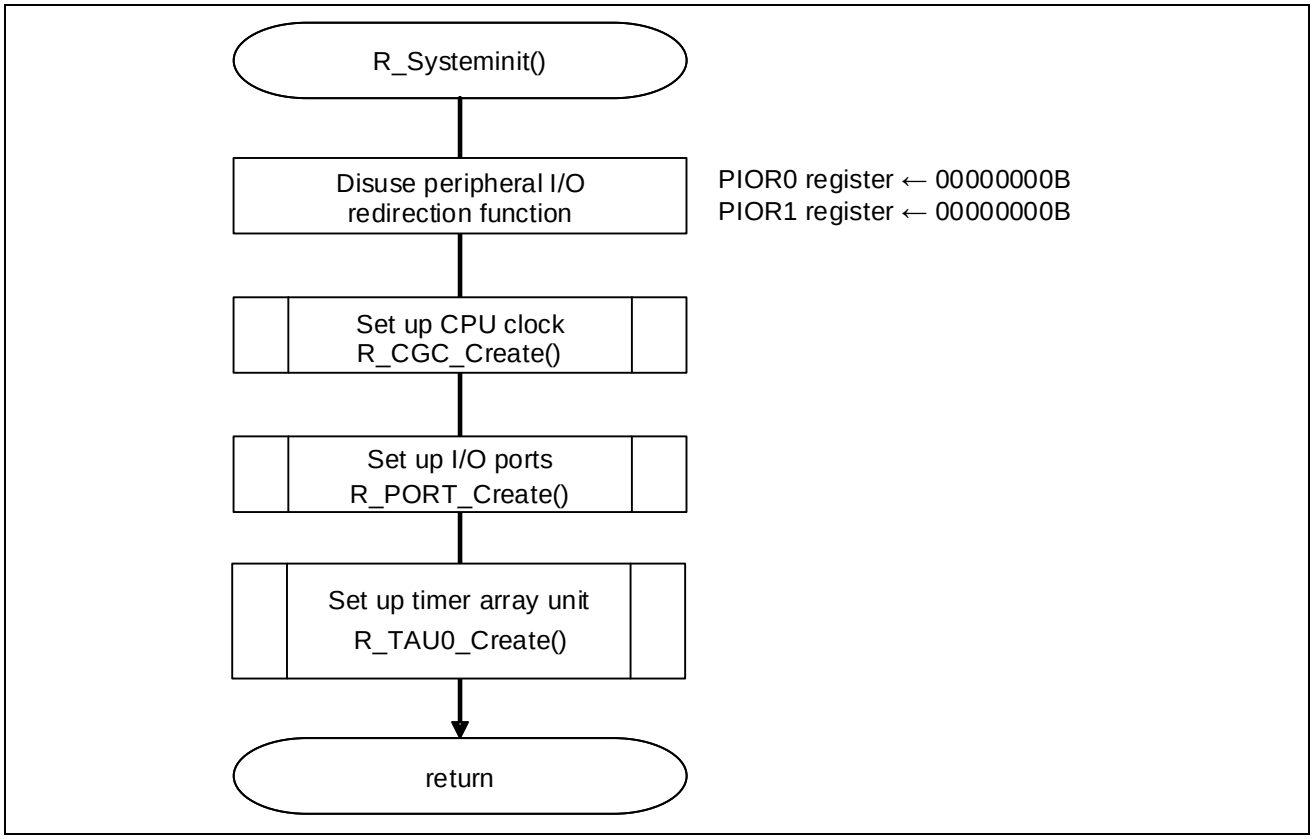

Figure 7.6 System Function

7.4.6.4 CPU Clock Setup

Figure 7.7 shows the flowchart for setting up the CPU clock.

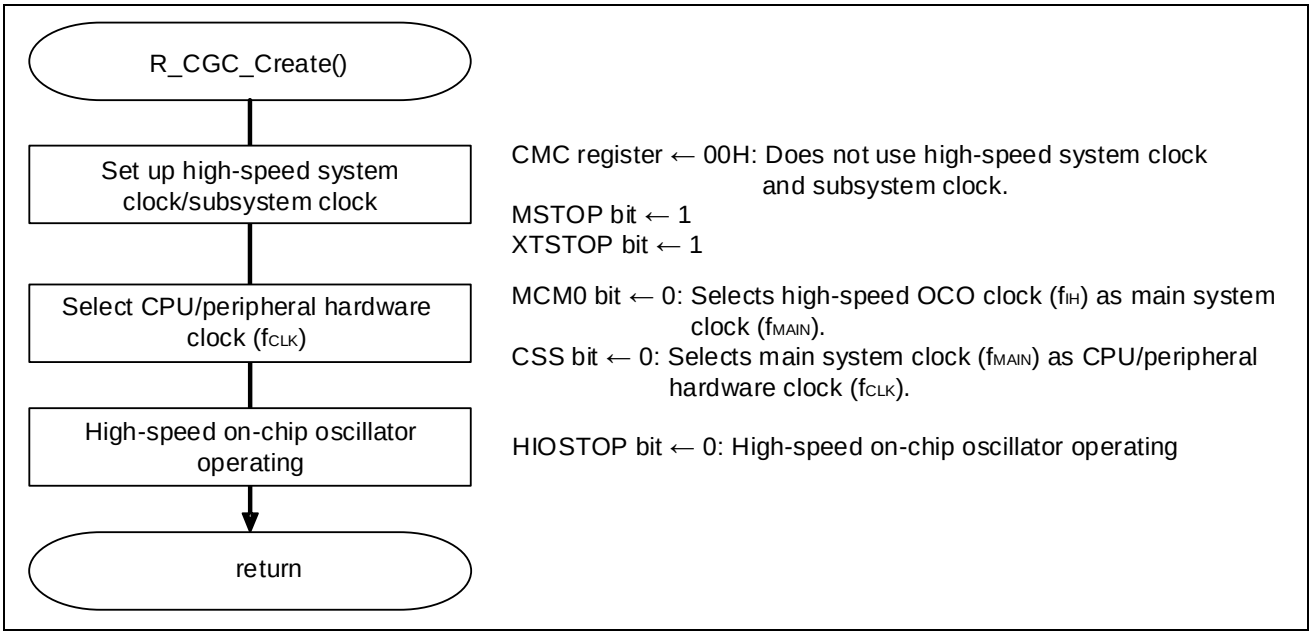

Figure 7.7 CPU Clock Setup

7.4.6.5 I/O Port Setup

Figure 7.8 shows the flowchart for setting up the I/O ports.

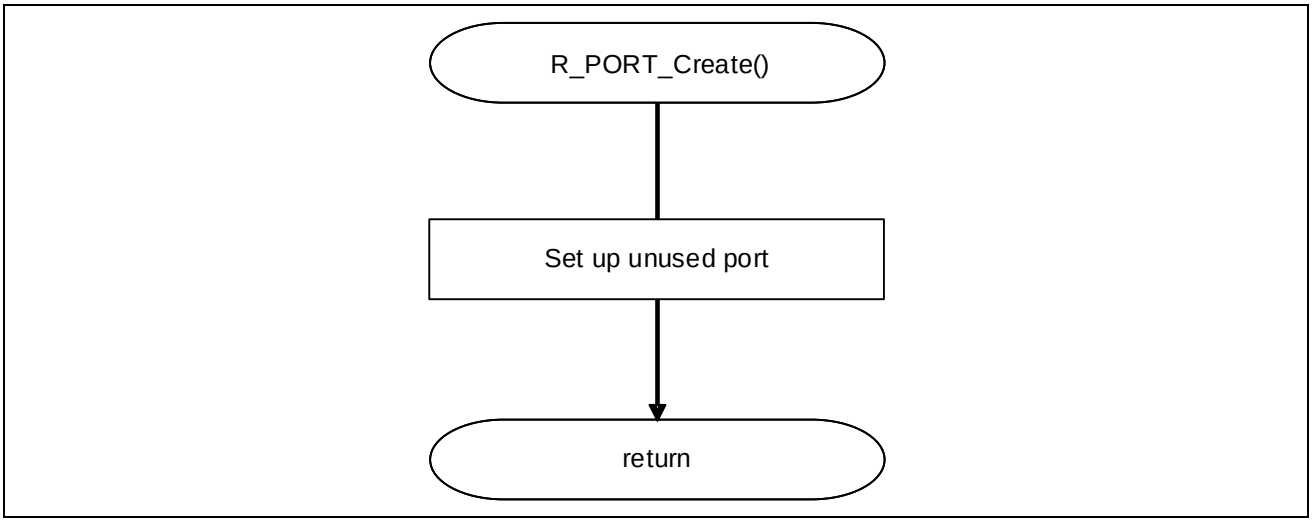

Figure 7.8 I/O Port Setup

Caution: Provide proper treatment for unused pins so that their electrical specifications are observed. Connect each of any unused input-only ports to V_{DD} or V_{SS} via a separate resistor.

7.4.6.6 Timer Array Unit Setup

Figures 7.9 and 7.10 show the flowchart for setting up the timer array unit.

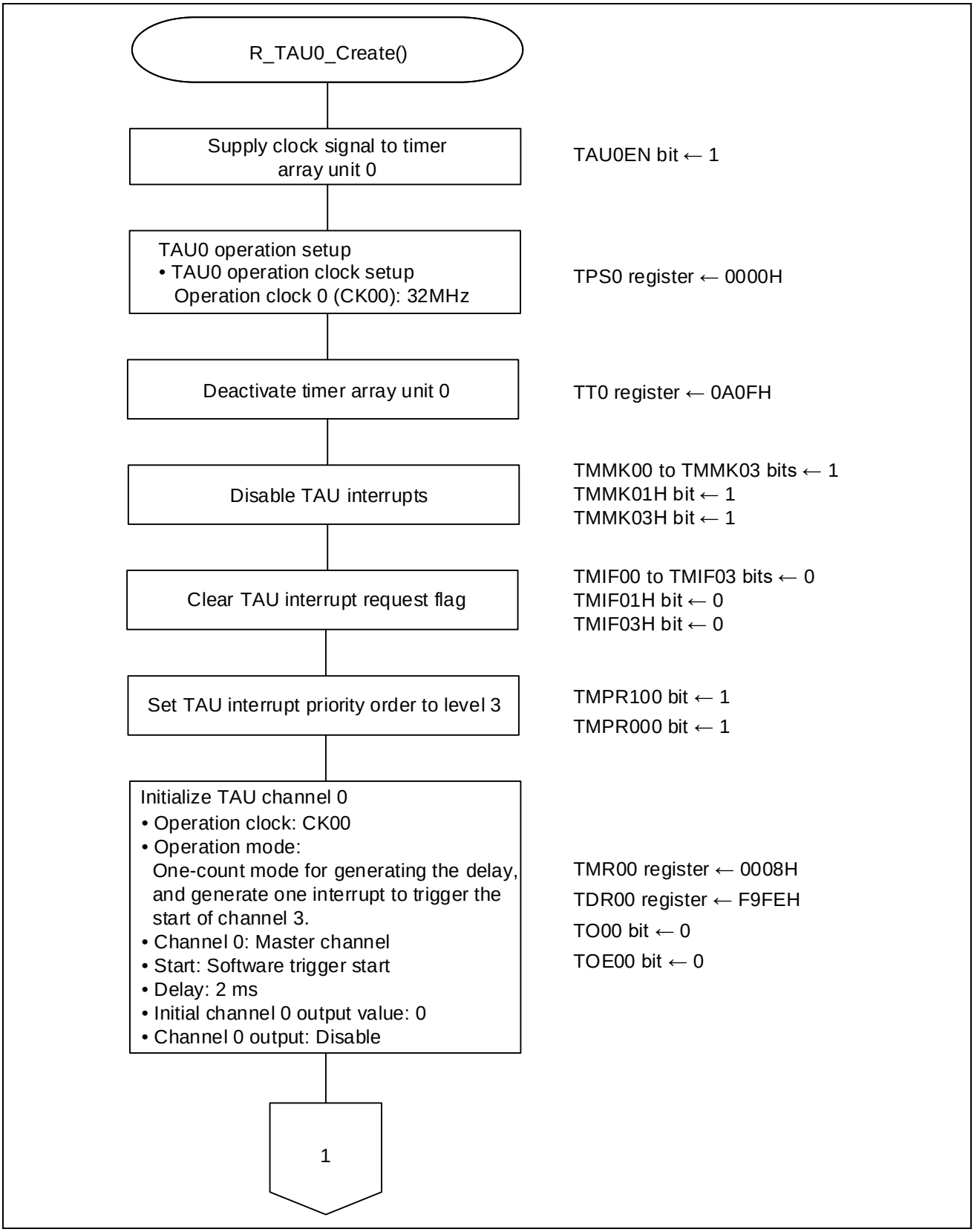

Figure 7.9 Timer Array Unit Setup (1/2)

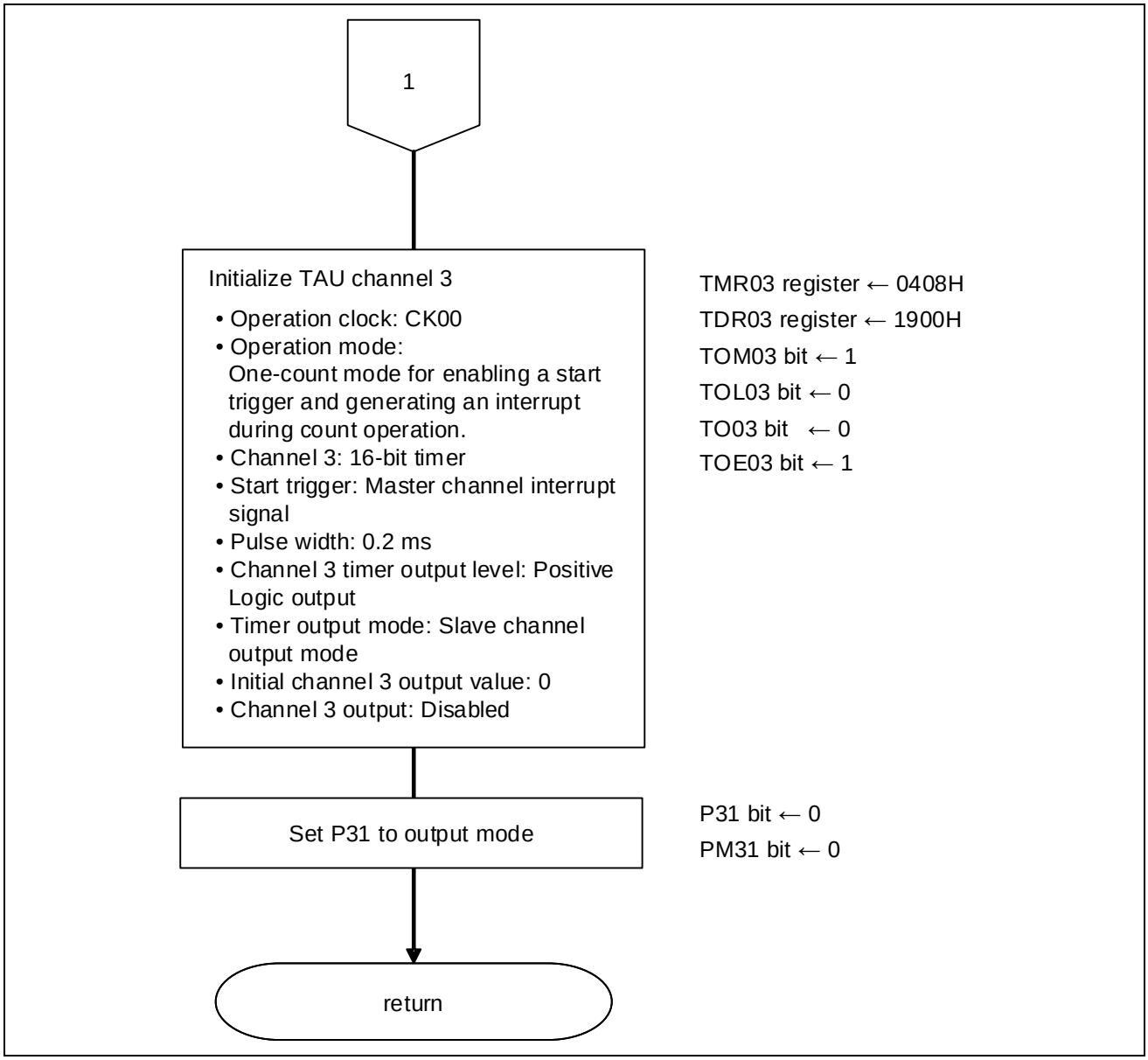

Figure 7.10 Timer Array Unit Setup (2/2)

Starting clock signal supply to the timer array unit 0

- Peripheral enable register 0 (PER0)

Start clock signal supply to the timer array unit 0.

Symbol: PER0

7	6	5	4	3	2	1	0
RTCEN	IICA1EN	ADCEN	IICA0EN	SAU1EN	SAU0EN	TAU1EN	TAU0EN
x	x	x	x	x	x	x	**1**

Bit 0

TAU0EN	Control of timer array unit 0 input clock supply
0	Stops input clock supply.
1	**Enables input clock supply.**

Caution: For details on the register setup procedures, refer to RL78/G14 User's Manual: Hardware.

x: Bits not used in this setting item

Configuring the timer clock frequency

- Timer clock select register 0 (TPS0)

  Select an operation clock for timer array unit 0.

Symbol: TPS0

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	PRS 031	PRS 030	0	0	PRS 021	PRS 020	PRS 013	PRS 012	PRS 011	PRS 010	PRS 003	PRS 002	PRS 001	PRS 000
0	0	x	x	0	0	x	x	x	x	x	x	0	0	0	0

Bits 3 to 0

PRS 003	PRS 002	PRS 001	PRS 000	Operation clock (CK00) selection					
					f_{CLK}= 2 MHz	f_{CLK}= 4 MHz	f_{CLK}= 8 MHz	f_{CLK}= 20 MHz	f_{CLK}= 32 MHz
0	0	0	0	f_{CLK}	2 MHz	4 MHz	8 MHz	20 MHz	32 MHz
0	0	0	1	$f_{CLK}/2$	1 MHz	2 MHz	4 MHz	10 MHz	16 MHz
0	0	1	0	$f_{CLK}/2^2$	500 kHz	1 MHz	2 MHz	5 MHz	8 MHz
0	0	1	1	$f_{CLK}/2^3$	250 kHz	500 kHz	1 MHz	2.5 MHz	4 MHz
0	1	0	0	$f_{CLK}/2^4$	125 kHz	250 kHz	500 kHz	1.25 MHz	2 MHz
0	1	0	1	$f_{CLK}/2^5$	62.5 kHz	125 kHz	250 kHz	625 kHz	1 MHz
0	1	1	0	$f_{CLK}/2^6$	31.3 kHz	62.5 kHz	125 kHz	313 kHz	500 kHz
0	1	1	1	$f_{CLK}/2^7$	15.6 kHz	31.3 kHz	62.5 kHz	156 kHz	250 kHz
1	0	0	0	$f_{CLK}/2^8$	7.81 kHz	15.6 kHz	31.3 kHz	78.1 kHz	125 kHz
1	0	0	1	$f_{CLK}/2^9$	3.91 kHz	7.81 kHz	15.6 kHz	39.1 kHz	62.5 kHz
1	0	1	0	$f_{CLK}/2^{10}$	1.95 kHz	3.91 kHz	7.81 kHz	19.5 kHz	31.25 kHz
1	0	1	1	$f_{CLK}/2^{11}$	977 Hz	1.95 kHz	3.91 kHz	9.77 kHz	15.6 kHz
1	1	0	0	$f_{CLK}/2^{12}$	488 Hz	977 Hz	1.95 kHz	4.88 kHz	7.81 kHz
1	1	0	1	$f_{CLK}/2^{13}$	244 Hz	488 Hz	977 Hz	2.44 kHz	3.91 kHz
1	1	1	0	$f_{CLK}/2^{14}$	122 Hz	244 Hz	488 Hz	1.22 kHz	1.95 kHz
1	1	1	1	$f_{CLK}/2^{15}$	61.0 Hz	122 Hz	244 Hz	610 Hz	977 Hz

Caution: For details on the register setup procedures, refer to RL78/G14 User's Manual: Hardware.

x: Bits not used in this setting item

Setting up the channel 0 operation mode

- Timer mode register 00 (TMR00)

Select an operation clock (f_{MCK}).
Select a count clock.
Select a start trigger and capture trigger.
Select a valid edge for timer input.
Set up the operation mode.

Symbol: TMR00

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CKS001	CKS000	0	CCS00	0	STS002	STS001	STS000	CIS001	CIS000	0	0	MD003	MD002	MD001	MD000
0	0	0	0	0	0	0	0	x	x	0	0	1	0	0	0

Bits 15 and 14

CKS001	CKS000	Selection of operation clock (f_{MCK}) of channel 0
0	0	Operation clock CK00 set by timer clock select register 0 (TPS0)
0	1	Operation clock CK02 set by timer clock select register 0 (TPS0)
1	0	Operation clock CK01 set by timer clock select register 0 (TPS0)
1	1	Operation clock CK03 set by timer clock select register 0 (TPS0)

Bit 12

CCS00	Selection of count clock (f_{TCLK}) of channel 0
0	Operation clock (f_{MCK}) specified by the CKS000 and CKS001 bits
1	Valid edge of input signal input from the TI00 pin

Bits 10 to 8

STS002	STS001	STS000	Setting of start trigger or capture trigger of channel 0
0	0	0	Only software trigger start is valid (other trigger sources are unselected).
0	0	1	Valid edge of the TI00 pin input is used as both the start trigger and capture trigger.
0	1	0	Both the edges of the TI00 pin input are used as a start trigger and a capture trigger.
1	0	0	Interrupt signal of the master channel is used (when the channel is used as a slave channel with the simultaneous channel operation function).
Other than above			Setting prohibited

Caution: For details on the register setup procedures, refer to RL78/G14 User's Manual: Hardware.
x: Bits not used in this setting item

Symbol: TMR00

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CKS 001	**CKS 000**	**0**	**CCS 00**	**0**	**STS 002**	**STS 001**	**STS 000**	**CIS 001**	**CIS 000**	**0**	**0**	**MD 003**	**MD 002**	**MD 001**	**MD 000**
0	**0**	0	**0**	0	**0**	**0**	**0**	x	x	0	0	**1**	**0**	**0**	**0**

Bits 3 to 0

MD003	MD002	MD001	MD000	Operation mode of channel 0	Corresponding function	Count operation of TCR
0	0	0	1/0	Interval timer mode	Interval timer / Square wave output / Divider function / PWM output (master)	Counting down
0	1	0	1/0	Capture mode	Input pulse interval measurement	Counting up
0	1	1	0	Event counter mode	External event counter	Counting down
1	**0**	**0**	1/**0**	**One-count mode**	Delay counter / **One-shot pulse output** / PWM output (slave)	**Counting down**
1	1	0	0	Capture & one-count mode	Measurement of high-/low-level width of input signal	Counting up
Other than above				Setting prohibited		

The operation of each mode varies depending on MD000 bit (see table below).

Operation mode (Value set by the MD003 to MD001 bits (see table above))	MD000	Setting of starting counting and interrupt
• Interval timer mode (0, 0, 0) • Capture mode (0, 1, 0)	0	Timer interrupt is not generated when counting is started (timer output does not change, either).
	1	Timer interrupt is generated when counting is started (timer output also changes).
• Event counter mode (0, 1, 1)	0	Timer interrupt is not generated when counting is started (timer output does not change, either).
• One-count mode (1, 0, 0)	**0**	**Start trigger is invalid during counting operation. At that time, interrupt is not generated.**
	1	Start trigger is valid during counting operation. At that time, interrupt is also generated.
• Capture & one-count mode (1, 1, 0)	0	Timer interrupt is not generated when counting is started (timer output does not change, either). Start trigger is invalid during counting operation. At that time interrupt is not generated.
Other than above		Setting prohibited

Caution: For details on the register setup procedures, refer to RL78/G14 User's Manual: Hardware.
x: Bits not used in this setting item

Setting up the channel 3 operation mode

- Timer mode register 03 (TMR03)

Select an operation clock (f_{MCK}).
Select a count clock.
Select the 16/8-bit timer.
Select a start trigger and capture trigger.
Select a valid edge for timer input.
Set up the operation mode.

Symbol: TMR03

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CKS 031	CKS 030	0	CCS 03	SPLIT 03	STS 032	STS 031	STS 030	CIS 031	CIS 030	0	0	MD 033	MD 032	MD 031	MD 030
0	0	0	0	0	1	0	0	x	x	0	0	1	0	0	0

Bits 15 and 14

CKS031	CKS030	Selection of operation clock (f_{MCK}) of channel 3
0	**0**	**Operation clock CK00 set by timer clock select register 0 (TPS0)**
0	1	Operation clock CK02 set by timer clock select register 0 (TPS0)
1	0	Operation clock CK01 set by timer clock select register 0 (TPS0)
1	1	Operation clock CK03 set by timer clock select register 0 (TPS0)

Bit 12

CCS03	Selection of count clock (f_{TCLK}) of channel 3
0	**Operation clock (f_{MCK}) specified with the CKS030 and CKS031 bits**
1	Valid edge of input signal input from the TI03 pin

Bit 11

SPLIT03	Selection of 8 or 16-bit timer operation for channel 3
0	**Operates as 16-bit timer (Operates in independent channel operation function or as slave channel in simultaneous channel operation function.)**
1	Operates as 8-bit timer.

Bits 10 to 8

STS032	STS031	STS030	Setting of start trigger or capture trigger of channel 3
0	0	0	Only software trigger start is valid (other trigger sources are unselected).
0	0	1	Valid edge of the TI03 pin input is used as both the start trigger and capture trigger.
0	1	0	Both the edges of the TI03 pin input are used as a start trigger and a capture trigger.
1	**0**	**0**	**Interrupt signal of the master channel is used (when the channel is used as a slave channel with the simultaneous channel operation function).**
Others than above			Setting prohibited

Caution: For details on the register setup procedures, refer to RL78/G14 User's Manual: Hardware.
x: Bits not used in this setting item

Symbol: TMR03

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CKS 031	CKS 030	0	CCS 03	SPLIT 03	STS 032	STS 031	STS 030	CIS 031	CIS 030	0	0	MD 033	MD 032	MD 031	MD 030
0	0	0	0	0	1	0	0	x	x	0	0	1	0	0	0

Bits 3 to 0

MD033	MD032	MD031	MD030	Operation mode of channel 3	Corresponding function	Count operation of TCR
0	0	0	1/0	Interval timer mode	Interval timer / Square wave output / Divider function / PWM output (master)	Counting down
0	1	0	1/0	Capture mode	Input pulse interval measurement	Counting up
0	1	1	0	Event counter mode	External event counter	Counting down
1	**0**	**0**	1/**0**	**One-count mode**	Delay counter / **One-shot pulse output** / PWM output (slave)	**Counting down**
1	1	0	0	Capture & one-count mode	Measurement of high-/low-level width of input signal	Counting up
Other than above				Setting prohibited		

The operation of each mode varies depending on MD030 bit (see table below).

Operation mode (Value set by the MD033 to MD031 bits (see table above))	MD030	Setting of starting counting and interrupt
• Interval timer mode (0, 0, 0) • Capture mode (0, 1, 0)	0	Timer interrupt is not generated when counting is started (timer output does not change, either).
	1	Timer interrupt is generated when counting is started (timer output also changes).
• Event counter mode (0, 1, 1)	0	Timer interrupt is not generated when counting is started (timer output does not change, either).
• One-count mode (1, 0, 0)	**0**	**Start trigger is invalid during counting operation. At that time, interrupt is not generated.**
	1	Start trigger is valid during counting operation. At that time, interrupt is also generated.
• Capture & one-count mode (1, 1, 0)	0	Timer interrupt is not generated when counting is started (timer output does not change, either). Start trigger is invalid during counting operation. At that time interrupt is not generated.
Other than above		Setting prohibited

Caution: For details on the register setup procedures, refer to RL78/G14 User's Manual: Hardware.
x: Bits not used in this setting item

Configuring the delay time

- Timer data register 00 (TDR00)

Configure the delay.

Symbol: TDR00

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Delay time = (TDR00 setting + 2) × Count clock cycle time

2 [ms] = (1/32[MHz]) × (TDR00 setting + 2)

⇒ TDR00 setting = 63998

Configuring the pulse output width

- Timer data register 03 (TDR03)

Configure the pulse output width.

Symbol: TDR03

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Pulse output width = (TDR03 setting) × Count clock cycle time

0.2 [ms] = (1/32[MHz]) × (TDR03 setting)

⇒ TDR03 setting = 6400

Setting up the timer output mode

- Timer output mode register 0 (TOM0)

Set up the timer output mode for each channel.

Symbol: TOM0

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	TOM03	TOM02	TOM01	0
0	0	0	0	0	0	0	0	0	0	0	0	1	x	x	0

Bit 3

TOM03	Control of timer output mode of channel 3
0	Master channel output mode (to produce toggle output by timer interrupt request signal (INTTM03))
1	**Slave channel output mode (output is set by the timer interrupt request signal (INTTM03) of the master channel, and reset by the timer interrupt request signal (INTTM0p) of the slave channel)**

Caution: For details on the register setup procedures, refer to RL78/G14 User's Manual: Hardware.

x: Bits not used in this setting item

Configuring the output level for the timer output pin

- Timer output level register 0 (TOL0)

Configure the output level for the timer output pin for each channel.

Symbol: TOL0

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	TOL03	TOL02	TOL01	0
0	0	0	0	0	0	0	0	0	0	0	0	0	x	x	0

Bit 3

TOL03	Control of timer output level of channel 3
0	Positive logic output (active-high)
1	Negative logic output (active-low)

Configuring the output value for the timer output pin

- Timer output register 0 (TO0)

Configure the output value for the timer output pin for each channel.

Symbol: TO0

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	TO03	TO02	TO01	TO00
0	0	0	0	0	0	0	0	0	0	0	0	0	x	x	0

Bit 3

TO03	Timer output of channel 3
0	Timer output value is “0”
1	Timer output value is “1”

Bit 0

TO00	Timer output of channel 0
0	Timer output value is “0”
1	Timer output value is “1”

Caution: For details on the register setup procedures, refer to RL78/G14 User's Manual: Hardware.

x: Bits not used in this setting item

Enabling the timer output

- Timer output enable register 0 (TOE0)
  Enable/disable the timer output for each channel.

Symbol: TOE0

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	TOE03	TOE02	TOE01	TOE00
0	0	0	0	0	0	0	0	0	0	0	0	1	x	x	0

Bit 3

TOE03	Timer output enable/disable of channel 3
0	Timer output is disabled. Timer operation is not applied to the TO03 bit and the output is fixed. Writing to the TO03 bit is enabled and the level set in the TO03 bit is output from the TO03 pin.
1	**Timer output is enabled.** **Timer operation is applied to the TO03 bit and an output waveform is generated.** **Writing to the TO03 bit is ignored.**

Bit 0

TOE00	Timer output enable/disable of channel 0
0	**Timer output is disabled.** **Timer operation is not applied to the TO00 bit and the output is fixed.** **Writing to the TO00 bit is enabled and the level set in the TO00 bit is output from the TO00 pin.**
1	Timer output is enabled. Timer operation is applied to the TO00 bit and an output waveform is generated. Writing to the TO00 bit is ignored.

Setting up the one-shot pulse output pin

- Port mode register (PM3)
  Select the I/O mode.

Symbol: PM3

7	6	5	4	3	2	1	0
1	1	1	1	1	1	PM31	PM30
1	1	1	1	1	1	0	x

Bit 1

PM31	P31 pin I/O mode selection
0	**Output mode (the pin functions as an output port (output buffer on))**
1	Input mode (the pin functions as an input port (output buffer off))

Caution: For details on the register setup procedures, refer to RL78/G14 User's Manual: Hardware.
x: Bits not used in this setting item

7.4.6.7 Main Processing

Figure 7.11 shows the flowchart for main processing.

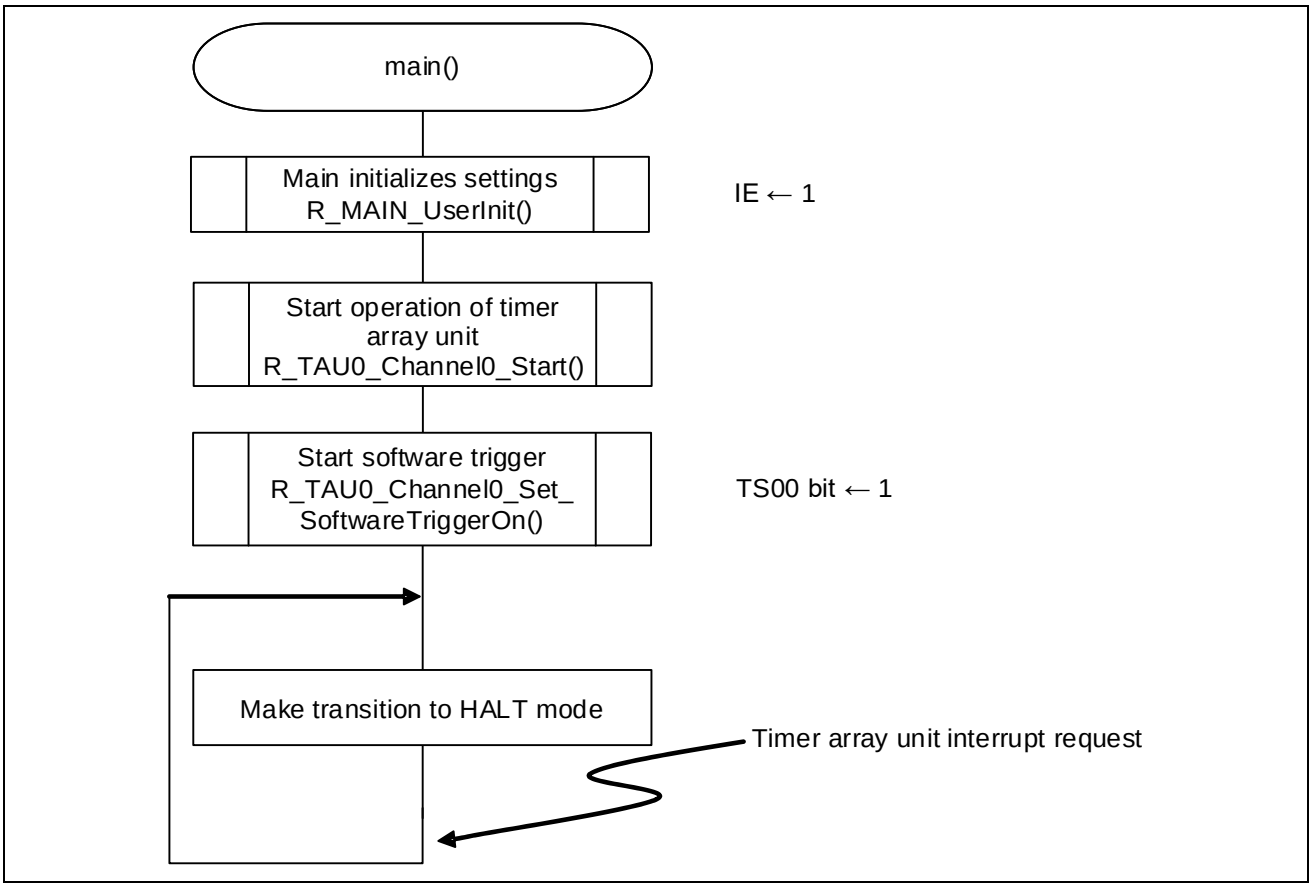

Figure 7.11 Main Processing

7.4.6.8 Timer Array Unit Startup

Figure 7.12 shows the flowchart for starting the operation of the timer array unit.

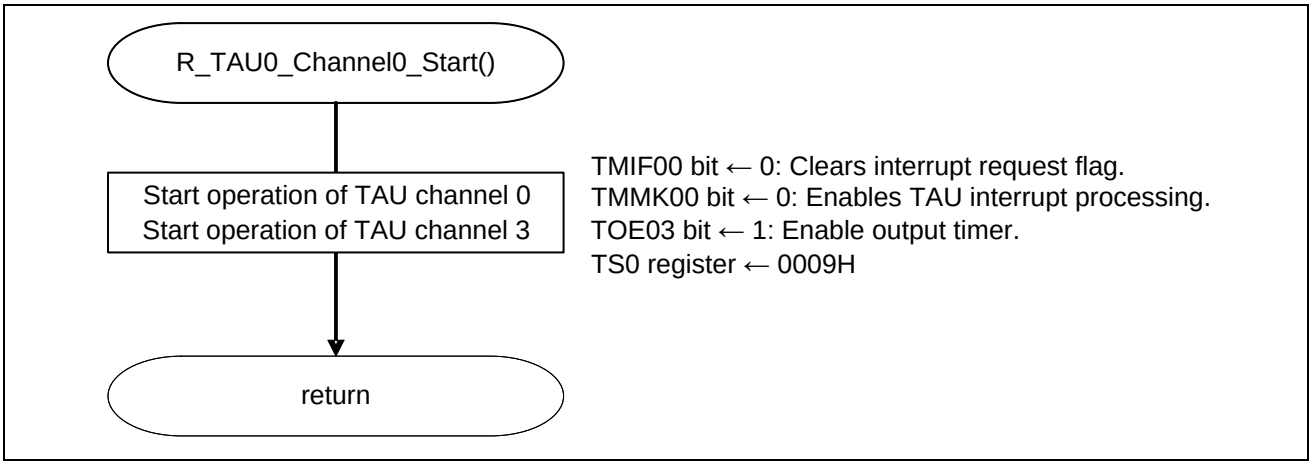

Figure 7.12 Timer Array Unit Startup

Configuring the timer interrupt

- Interrupt request flag register (IF1L)
  Clear the interrupt request flag.
- Interrupt mask flag register (MK1L)
  Enable interrupt processing.

Symbol: IF1L

7	6	5	4	3	2	1	0
TMIF03	TMIF02	TMIF01	TMIF00	IICAIF0	SREIF1 TMIF03H	SRIF1 CSIIF11 IICIF11	STIF1 CSIIF10 IICIF10
x	x	x	**0**	x	x	x	x

Bit 4

TMIF00	Interrupt request flag
0	**No interrupt request signal is generated**
1	Interrupt request is generated, interrupt request status

Symbol: MK1L

7	6	5	4	3	2	1	0
TMMK03	TMMK02	TMMK01	TMMK00	IICAMK0	SREMK1 TMMK03H	SRMK1 CSIMK11 IICMK11	STMK1 CSIMK10 IICMK10
x	x	x	**0**	x	x	x	x

Bit 4

TMMK00	Interrupt servicing control
0	**Interrupt servicing enabled**
1	Interrupt servicing disabled

Caution: For details on the register setup procedures, refer to RL78/G14 User's Manual: Hardware.
x: Bits not used in this setting item

Enable the output of timer

- Timer output enable register 0 (TOE0)

  Enable output of channel 3.

Symbol: TOE0

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	TOE03	TOE02	TOE01	TOE00
0	0	0	0	0	0	0	0	0	0	0	0	1	x	x	x

Bit 3

TOE03	Timer output enable/disable of channel 3
0	Timer output is disabled. Timer operation is not applied to the TO03 bit and the output is fixed. Writing to the TO03 bit is enabled and the level set in the TO03 bit is output from the TO03 pin.
1	**Timer output is enabled.** **Timer operation is applied to the TO03 bit and an output waveform is generated.** **Writing to the TO03 bit is ignored.**

Configuring the timer startup

- Timer channel start register 0 (TS0)

  Enable count operation of channel 0 and channel 3.

Symbol: TS0

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	TSH03	0	TSH01	0	0	0	0	0	TS03	TS02	TS01	TS00
0	0	0	0	x	0	x	0	0	0	0	0	1	x	x	1

Bit 3

TS03	Operation enable (start) trigger of channel 3
0	No trigger operation
1	**The TE03 bit is set to 1 and the count operation becomes enabled.** **The TCR03 register count operation start in the count operation enabled state varies depending on each operation mode.**

Bit 0

TS00	Operation enable (start) trigger of channel 0
0	No trigger operation
1	**The TE00 bit is set to 1 and the count operation becomes enabled.** **The TCR00 register count operation start in the count operation enabled state varies depending on each operation mode.**

Caution: For details on the register setup procedures, refer to RL78/G14 User's Manual: Hardware.

x: Bits not used in this setting item

7.4.6.9 INTTM00 Interrupt Processing

Figure 7.13 shows the flowchart for INTTM00 interrupt processing.

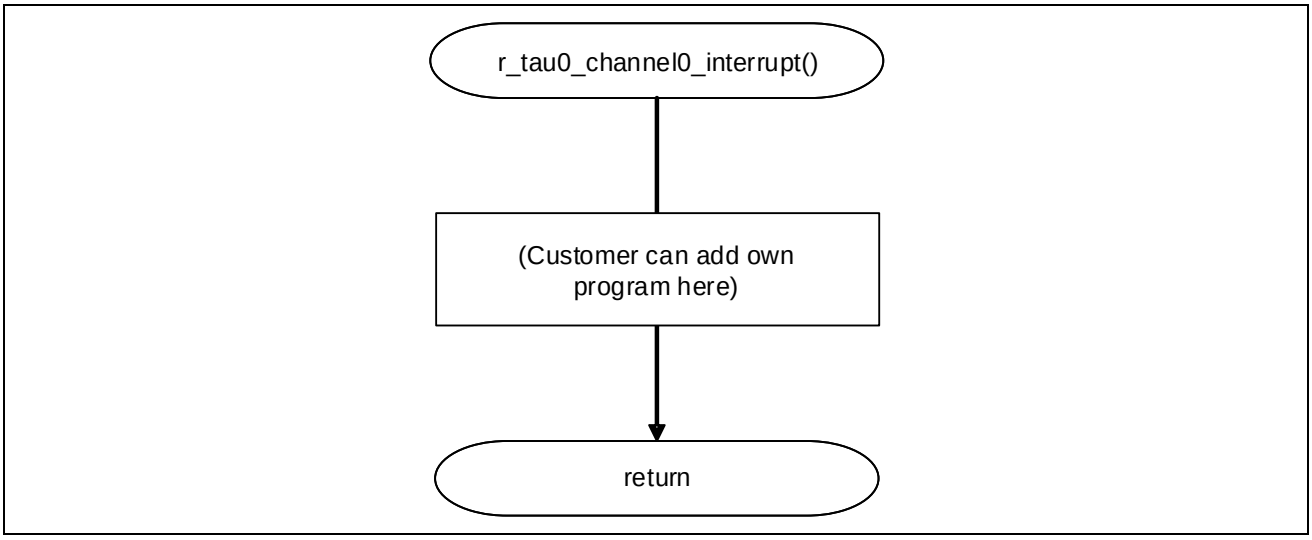

Figure 7.13 INTTM00 Interrupt Processing

8. Sample Code

Sample code can be downloaded from the Renesas Electronics website.

9. Reference Application Note

RL78/G13 Timer Array Unit (Interval Timer) CC-RL (R01AN2576)
RL78/G13 Timer Array Unit (PWM Output) CC-RL (R01AN2589)
The latest versions can be downloaded from the Renesas Electronics website.

10. Reference Documents

User's Manual: Hardware
RL78/G14 User's Manual: Hardware (R01UH0186)
R8C/36M Group User's Manual: Hardware (R01UH0259)
The latest versions can be downloaded from the Renesas Electronics website.

Technical Update/Technical News
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Revision History

		Description	
Rev.	**Date**	**Page**	**Summary**
1.00	Aug. 1, 2017	-	First edition issued

General Precautions in the Handling of Microprocessing Unit and Microcontroller Unit Products

The following usage notes are applicable to all Microprocessing unit and Microcontroller unit products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Handling of Unused Pins

   Handle unused pins in accordance with the directions given under Handling of Unused Pins in the manual.

   — The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible. Unused pins should be handled as described under Handling of Unused Pins in the manual.

2. Processing at Power-on

   The state of the product is undefined at the moment when power is supplied.

   — The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the moment when power is supplied.
   In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the moment when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the moment when power is supplied until the power reaches the level at which resetting has been specified.

3. Prohibition of Access to Reserved Addresses

   Access to reserved addresses is prohibited.

   — The reserved addresses are provided for the possible future expansion of functions. Do not access these addresses; the correct operation of LSI is not guaranteed if they are accessed.

4. Clock Signals

   After applying a reset, only release the reset line after the operating clock signal has become stable. When switching the clock signal during program execution, wait until the target clock signal has stabilized.

   — When the clock signal is generated with an external resonator (or from an external oscillator) during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Moreover, when switching to a clock signal produced with an external resonator (or by an external oscillator) while program execution is in progress, wait until the target clock signal is stable.

5. Differences between Products

   Before changing from one product to another, i.e. to a product with a different part number, confirm that the change will not lead to problems.

   — The characteristics of Microprocessing unit or Microcontroller unit products in the same group but having a different part number may differ in terms of the internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

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