RL78/G13, 78K0/Kx2

Migration Guide from 78K0 to RL78: Standby Function

Introduction

This application note describes how to migrate the Standby Function of the 78K0/Kx2 to the Standby Function of the RL78/G13.

Target Device

RL78/G13, 78K0/Kx2

When using this application note with other Renesas MCUs, careful evaluation is recommended after making modifications to comply with the alternate MCU.

Contents

1. Standby Function

Table 1.1 shows the standby function of the 78K0/Kx2 and Table 1.2 shows the standby function of the RL78/G13.

Table 1.1 Standby Function of 78K0/Kx2

Function	Explanation
HALT mode	HALT instruction execution sets the HALT mode. In the HALT mode, the CPU operation clock is stopped. If the highspeed system clock oscillator, internal high-speed oscillator, internal low-speed oscillator, or subsystem clock oscillator is operating before the HALT mode is set, oscillation of each clock continues. In this mode, the operating current is not decreased as much as in the STOP mode, but the HALT mode is effective for restarting operation immediately upon interrupt request generation and carrying out intermittent operations frequently.
STOP mode	STOP instruction execution sets the STOP mode. In the STOP mode, the high-speed system clock oscillator and internal high-speed oscillator stop, stopping the whole system, thereby considerably reducing the CPU operating current. Because this mode can be cleared by an interrupt request, it enables intermittent operations to be carried out. However, because a wait time is required to secure the oscillation stabilization time after the STOP mode is released when the X1 clock is selected, select the HALT mode if it is necessary to start processing immediately upon interrupt request generation.

Table 1.2 Standby Function of RL78/G13

Function	Explanation
HALT mode	HALT instruction execution sets the HALT mode. In the HALT mode, the CPU operation clock is stopped. If the highspeed system clock oscillator, high-speed on-chip oscillator, or subsystem clock oscillator is operating before the HALT mode is set, oscillation of each clock continues. In this mode, the operating current is not decreased as much as in the STOP mode, but the HALT mode is effective for restarting operation immediately upon interrupt request generation and carrying out intermittent operations frequently.
STOP mode	STOP instruction execution sets the STOP mode. In the STOP mode, the high-speed system clock oscillator and high-speed on-chip oscillator stop, stopping the whole system, thereby considerably reducing the CPU operating current. Because this mode can be cleared by an interrupt request, it enables intermittent operations to be carried out. However, because a wait time is required to secure the oscillation stabilization time after the STOP mode is released when the X1 clock is selected, select the HALT mode if it is necessary to start processing immediately upon interrupt request generation.
SNOOZE mode	In the case of CSIp or UARTq data reception and an A/D conversion request by the timer trigger signal (the interrupt request signal (INTRTC/INTIT)), the STOP mode is exited, the CSIp or UARTq data is received without operating the CPU, and A/D conversion is performed. This can only be specified when the high-speed on-chip oscillator is selected for the CPU/peripheral hardware clock (f_{CLK}).

Remarks 1. For RL78/G13,

20 to 64-pin products: p = 00; q = 0; m = 0

80 to 128-pin products: p = 00, 20; q = 0, 2; m = 0, 1

Remarks 2. Different products are provided with different functions. For details, refer to the appropriate user's manuals (hardware).

The 78K0/Kx2 standby function provides HALT mode and STOP mode.

Figure 1.1 shows the state transitions of the 78K0/Kx2 standby function.

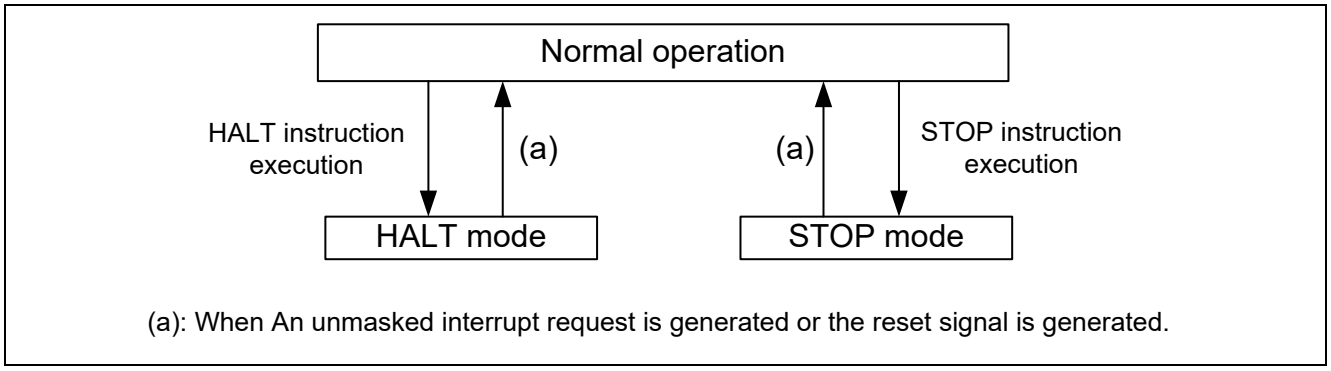

Figure 1.1 The state transitions of the 78K0/Kx2 standby function

The RL78/G13 standby function provides HALT mode, STOP mode, and SNOOZE mode.

Figure 1.2 shows the state transitions of the RL78/G13 standby function.

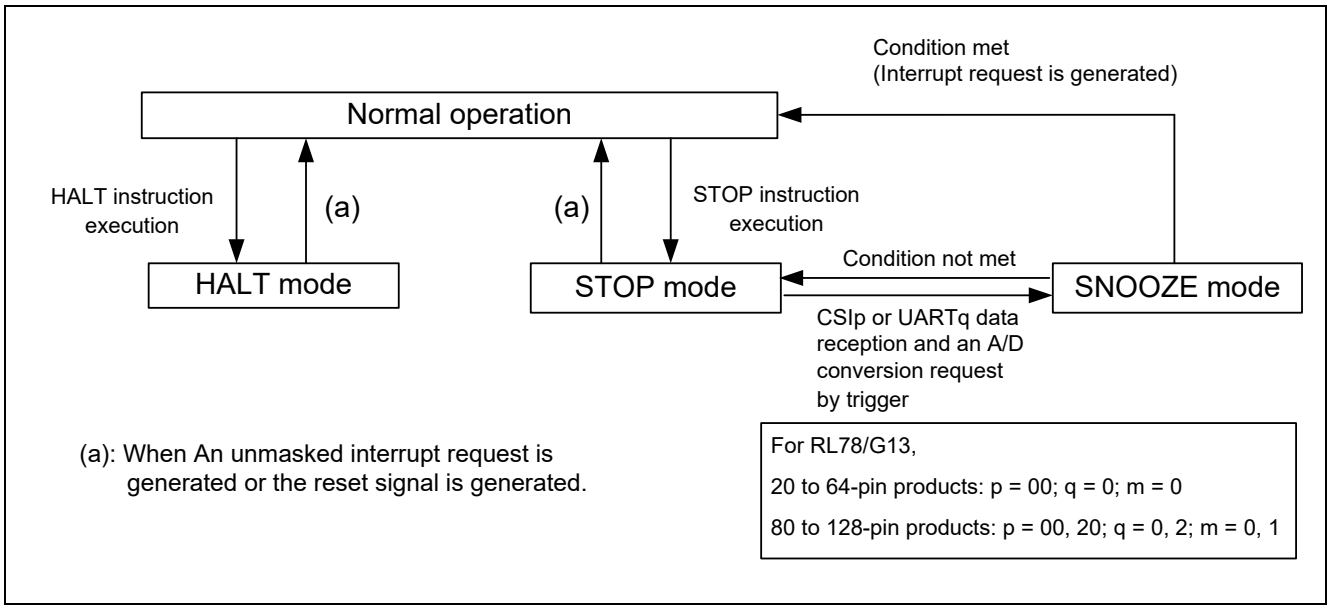

Figure 1.2 The state transitions of the RL78/G13 standby function

Table 1.3 shows the correspondence between the standby functions of the two devices.

The 78K0/Kx2 standby function provides two modes and the RL78/G13 standby function provides three modes.

Table 1.3 Correspondence between Functions

78K0/Kx2 Standby Function	RL78/G13 Standby Function
HALT mode	HALT mode
STOP mode	STOP mode
-	SNOOZE mode Note

Note. The SNOOZE mode can only be specified for CSIp, UARTq, or the A/D converter. Note that this mode can only be specified if the CPU clock is the high-speed on-chip oscillator clock.

Remarks 1. For RL78/G13,

20 to 64-pin products: p = 00; q = 0; m = 0

80 to 128-pin products: p = 00, 20; q = 0, 2; m = 0, 1

Remarks 2. Different products are provided with different functions. For details, refer to the appropriate user's manuals (hardware).

2. Differences between Standby Function

2.1 Differences between HALT mode

Table 2.1 shows the differences of the HALT modes of the two devices during HALT instruction execution while the CPU is operating on the main system clock.

Table 2.1 Differences between HALT mode (Main System Clock)

Item	78K0/Kx2	RL78/G13
CPU	Clock supply to the CPU is stopped	Clock supply to the CPU is stopped
Main system clock	The clock selected as the CPU clock continues to operate (cannot be stopped). The other clocks retain the status before HALT mode was set. The operation of the external main system clock depends on the input signals.	The clock selected as the CPU clock continues to operate (cannot be stopped). The other clocks are disabled or cannot be operated.
Subsystem clock	Status before HALT mode was set is retained. The operation of the external subsystem clock depends on the input signals.	Status before HALT mode was set is retained. The operation of the external subsystem clock depends on the input signals.
Internal low-speed oscillation clock	Status before HALT mode was set is retained.	The settings of the DSTBYON and WDTON bits of the option byte and WUTMMCK0 bit of the OSMC register enable or stop the clock oscillation.
Watchdog timer (WDT)	The LSROSC bit setting of the option byte determines the operation of the low speed on-chip oscillator used as the WDT clock.	The WDSTBYON bit setting of the option byte enables or stops the counter operation in HALT/STOP mode.

Table 2.2 shows the differences of the HALT modes of the two devices during HALT instruction execution while the CPU is operating on the subsystem clock.

Table 2.2 Differences between HALT mode (Subsystem clock)

Item	78K0/Kx2	RL78/G13
CPU	Clock supply to the CPU is stopped	Clock supply to the CPU is stopped
Main system clock	Status before HALT mode was set is retained	Operation disabled
Subsystem clock	The clock selected as the CPU clock continues to operate (cannot be stopped). The other clocks retain the status before HALT mode was set. The operation of the external subsystem clock depends on the input signals.	The clock selected as the CPU clock continues to operate (cannot be stopped). The other clocks are disabled or cannot be operated.
Internal low-speed oscillation clock	Status before HALT mode was set is retained.	The settings of the DSTBYON and WDTON bits of the option byte and WUTMMCK0 bit of the OSMC register enable or stop the clock oscillation.
Timer	Timer 00, 01, 50, 51, H0, H1 can be operated.	Timer array unit can be operated when RTCLPC = 0 (operation disabled in the other case). 12-bit interval timer can be operated.
Watchdog timer (WDT)	The LSROSC bit setting of the option byte determines the operation of the low speed on-chip oscillator used as the WDT clock.	The WDSTBYON bit setting of the option byte enables or stops the counter operation in HALT/STOP mode.
A/D converter	Operable	Operation disabled
Serial interface	UART0, UART6, CSI10, CSI11, CSIA0, IIC0 can be operated.	SAU can be operated when RTCLPC = 0 (operation disabled in the other case). IICA operation disabled.

Remark. Different products are provided with different functions. For details, refer to the appropriate user's manuals (hardware).

2.2 Differences between STOP mode

Table 2.3 show the differences between STOP mode.

Table 2.3 Differences between STOP mode

Item	78K0/Kx2 STOP mode	RL78/G13 STOP mode
CPU	Clock supply to the CPU is stopped	Clock supply to the CPU is stopped
Main system clock	Stopped	Stopped
Subsystem clock	Status before STOP mode was set is retained	Status before STOP mode was set is retained
Internal low-speed oscillation clock	Status before STOP mode was set is retained	The settings of the DSTBYON and WDTON bits of the option byte and WUTMMCK0 bit of the OSMC register enable or stop the clock oscillation.
Timer	- Timer 50 and 51 can be operated only when timer input is selected as the count clock. - Timer H0 can be operated only when TM50 output is selected as the count clock during timer 50 operation. - Timer H1 can be operated only when f_{RL}, $f_{RL}/2^7$, or $f_{RL}/2^9$ is selected as the count clock.	- Timer array unit operation disabled. - 12-bit interval timer operable.
Watchdog timer (WDT)	The LSROSC bit setting of the option byte determines the operation of the low speed on-chip oscillator used as the WDT clock.	The WDSTBYON bit setting of the option byte enables or stops the counter operation in HALT/STOP mode.
A/D converter	Operation stopped	Wakeup operation is enabled (switching to the SNOOZE mode)
Serial interface	- UART0, UART6: Operable only when TM50 output is selected as the serial clock during 8-bit timer 50 operation. - CSI10, CSI11: Operable only when external clock is selected as the serial clock. - CSIA0: Operation stopped - IIC0: Operable only when the external clock from EXSCL0/P62 pin is selected as the serial clock.	- Wakeup operation is enabled only for CSIp and UARTq (switching to the SNOOZE mode). - Operation is disabled for anything other than CSIp and UARTq. - IICA wakeup by address match operable.

Remarks1. For RL78/G13,

20 to 64-pin products: p = 00; q = 0; m = 0

80 to 128-pin products: p = 00, 20; q = 0, 2; m = 0, 1

Remarks 2. Different products are provided with different functions. For details, refer to the appropriate user's manuals (hardware).

3. Sample Code for Standby function

The sample code for Standby function is explained in the following application notes.

- RL78/G13 CPU Clock Changing and Standby Settings (C Language) CC-RL (R01AN3128)
- RL78/G13 CPU Clock Changing and Standby Settings (Assembly) CC-RL (R01AN2912)

4. Documents for Reference

User's Manual:

- RL78/G13 User's Manual: Hardware (R01UH0146)
- 78K0/Kx2 User's Manual: Hardware (R01UH0008)

  The latest versions can be downloaded from the Renesas Electronics website.

Technical Update/Technical News:

The latest information can be downloaded from the Renesas Electronics website.

Revision History

Rev.	Data	Description	
		Page	Summary
1.00	Oct.4, 2019	-	First edition issued

General Precautions in the Handling of Microprocessing Unit and Microcontroller Unit Products

The following usage notes are applicable to all Microprocessing unit and Microcontroller unit products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Precaution against Electrostatic Discharge (ESD)
   A strong electrical field, when exposed to a CMOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop the generation of static electricity as much as possible, and quickly dissipate it when it occurs. Environmental control must be adequate. When it is dry, a humidifier should be used. This is recommended to avoid using insulators that can easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors must be grounded. The operator must also be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions must be taken for printed circuit boards with mounted semiconductor devices.
2. Processing at power-on
   The state of the product is undefined at the time when power is supplied. The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the time when power is supplied. In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the time when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the time when power is supplied until the power reaches the level at which resetting is specified.
3. Input of signal during power-off state
   Do not input signals or an I/O pull-up power supply while the device is powered off. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Follow the guideline for input signal during power-off state as described in your product documentation.
4. Handling of unused pins
   Handle unused pins in accordance with the directions given under handling of unused pins in the manual. The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of the LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible.
5. Clock signals
   After applying a reset, only release the reset line after the operating clock signal becomes stable. When switching the clock signal during program execution, wait until the target clock signal is stabilized. When the clock signal is generated with an external resonator or from an external oscillator during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Additionally, when switching to a clock signal produced with an external resonator or by an external oscillator while program execution is in progress, wait until the target clock signal is stable.
6. Voltage application waveform at input pin
   Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between V_{IL} (Max.) and V_{IH} (Min.) due to noise, for example, the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between V_{IL} (Max.) and V_{IH} (Min.).
7. Prohibition of access to reserved addresses
   Access to reserved addresses is prohibited. The reserved addresses are provided for possible future expansion of functions. Do not access these addresses as the correct operation of the LSI is not guaranteed.
8. Differences between products
   Before changing from one product to another, for example to a product with a different part number, confirm that the change will not lead to problems. The characteristics of a microprocessing unit or microcontroller unit products in the same group but having a different part number might differ in terms of internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

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