RL78/G13, 78K0/Kx2

Migration Guide from 78K0 to RL78: Serial interface CSIA0 to Serial Array Unit

Introduction

This application note describes how to migrate the serial interface CSIA0 of the 78K0/Kx2 to the serial array unit (SAU) of the RL78/G13.

Target Device

RL78/G13, 78K0/Kx2

When using this application note with other Renesas MCUs, careful evaluation is recommended after making modifications to comply with the alternate MCU.

Contents

1. Functions of serial interface CSIA0 and Serial Array Unit

Table 1.1 shows the functions of the serial interface CSIA0, and Table 1.2 shows the functions of the serial array unit (SAU).

Table 1.1 Functions of serial interface CSIA0

Function	Explanation
3-wire serial I/O mode	Clock synchronous communication function by 3 lines of serial clock (SCKA0) and serial data (SIA0, SOA0).
3-wire serial I/O mode with automatic transmit/receive function	Clock synchronous communication function by 3 lines of serial clock (SCKA0) and serial data (SIA0, SOA0). The processing time of data communication can be shortened in the 3-wire serial I/O mode because transmission and reception can be simultaneously executed.

Table 1.2 Functions of Serial Array Unit

Function	Explanation
3-wire serial I/O	This is a clocked communication function that uses three lines: serial clock (SCK) and serial data (SI and SO) lines.
UART	This is a start-stop synchronization function using two lines: serial data transmission (TXD) and serial data reception (RXD) lines.
Simplified I^2C (Only master function with a single master)	This is a clocked communication function to communicate with two or more devices by using two lines: serial clock (SCL) and serial data (SDA).
LIN Communication (Note)	LIN stands for Local Interconnect Network and is a low-speed (1 to 20 kbps) serial communication protocol designed to reduce the cost of an automobile network.

Note. The LIN-bus is accepted in UART2 (channels 0 and 1 of unit 1)

Remarks1. For 78K0/Kx2, n = 0, 1 For RL78/G13, m: Unit number (m = 0, 1), n: Channel number (n = 0 to 3)

Remarks2. The functions incorporated and port functions to use are different depending on the product. For details, refer to the appropriate user's manuals (hardware).

The serial interface CSIA0 of the 78K0/Kx2 incorporates one channel of 3-line serial I/O (CSI). In the maser mode, it supports handshake pins (STB0 and BUSY0) for easy connection with peripheral ICs.

Figure 1.1 shows a block diagram of the serial interface CSIA0.

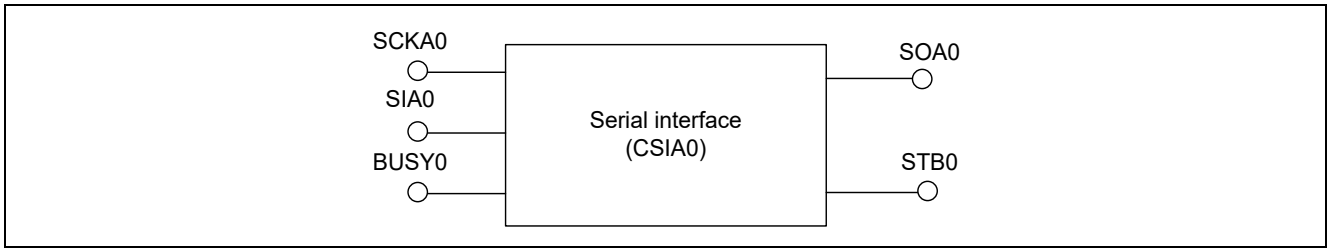

Figure 1.1 Block Diagram of Serial interface CSIA0

A single serial array unit (SAU) in the RL78/G13 has up to four serial channels. Each channel can achieve 3-wire serial (CSI), UART, and simplified I2C communication.

Figure 1.2 shows a CSI block diagram of the serial array unit 0 (SAU0) of the RL78/G13.

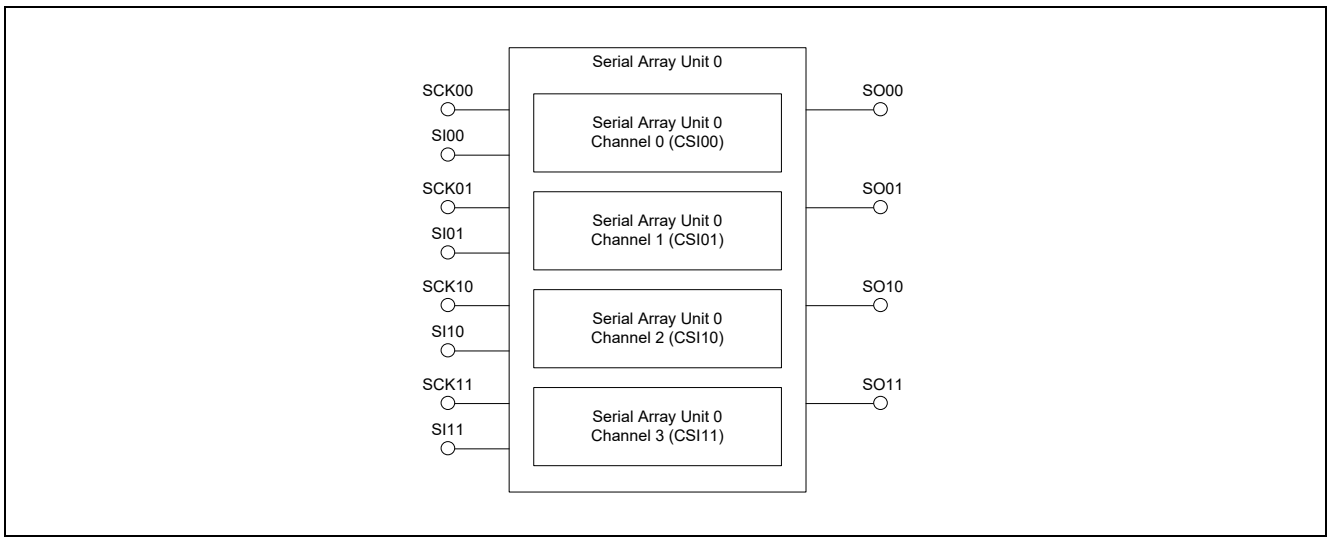

Figure 1.2 Block Diagram of Serial Array Unit 0 (SAU0) CSI

Table 1.3 shows the SAU functions corresponding to the Serial interface CSIA0.

Table 1.3 Correspondence between Functions

78K0/Kx2 Serial interface CSIA0	RL78/G13 Serial Array Unit (SAU)
3-wire serial I/O mode	3-wire serial I/O
3-wire serial I/O mode with automatic transmit/receive function	3-wire serial I/O
-	UART
-	Simplified I^2C

The 3-wire serial I/O mode and 3-wire serial I/O mode with automatic transmit/receive function of the serial interface CSIA0 correspond to the 3-wire serial I/O of the SAU.

2. Difference between Serial interface CSIA0 and Serial Array Unit

Table 2.1 and Table 2.2 shows the differences between the serial interface CSIA0.

Table 2.1 Difference between Serial interface CSIA0 (1/2)

Item	78K0/Kx2 Serial interface CSIA0	RL78/G13 Serial Array Unit (SAU) CSImn
Transfer data length	8 bits	7 bits / 8 bits
Maximum transfer rate	1.67MHz	- During master communication 16MHz (CSI00 only) (Note1) 8MHz (CSImn) (Note2) - During slave communication 4MHz
First bit specification	CSIMA0 register DIR0 = 0: MSB first DIR0 = 1: LSB first	SCRmn register DIRmn = 0: MSB first DIRmn = 1: LSB first
Selection of data and clock phase	None	SCRmn register Combination of CKPmn and DAPmn bits
Disables operation	CSIMA0 register CSIAE0 = 0	STm register STmn = 1
Enables operation	CSIMA0 register CSIAE0 = 1	SSm register SSmn = 1
Setting of operation mode	CSIMA0 register TXEA0 = 1, RXEA0 = 1: Transmission/reception TXEA0 = 1, RXEA0 = 0: Transmission only TXEA0 = 0, RXEA0 = 1: Reception only	SCRmn register TXEmn = 1, RXEmn = 1: Transmission/reception TXEmn = 1, RXEmn = 0: Transmission only TXEmn = 0, RXEmn = 1: Reception only
Automatic communication operation	CSIMA0 register ATE0 = 0:1-byte communication mode ATE0 = 1: Automatic communication mode ATM0 = 0: Single transfer mode ATM0 = 1: Repeat transfer mode	None (This can be implemented by using the CSImn and DMA controller.)
Buffer RAM	Yes (32 bytes)	None (This can be implemented by using a program and the DMA controller.)
Handshake function	Yes	None (This can be implemented by manipulating ports.)
Serial I/O shift register	SIOA0 register	Lower 8 bits of SDRmn register (SIOp)
Data transmission is started	1-byte transfer mode Write transmit data to SIOA0 register Automatic communication mode ATSTA0 bit of CSIT0 register is set to 1	Write transmit data to SIOp register (When TXEmn = 1)

Note1. Target products G (Industrial applications) is 4MHz.

Note2. Target products G (Industrial applications) is 2MHz.

Remarks1. For 78K0/Kx2, n = 0, 1
For RL78/G13, m: Unit number (m = 0, 1), n: Channel number (n = 0 to 3),
p: CSI number (p = 00, 01, 10, 11, 20, 21,30, 31)

Remarks2. The functions incorporated and port functions to use are different depending on the product. For details, refer to the appropriate user's manuals (hardware).

Table 2.2 Difference between Serial interface CSIA0 (2/2)

Item	78K0/Kx2 Serial interface CSIA0	RL78/G13 Serial Array Unit (SAU) CSImn
Data reception is started	1-byte transfer mode - Write transmit data to SIOA0 register (When TXEA0 = 1, RXEA0 = 1) - Write dummy data to SIOA0 register (When TXEA0 = 0, RXEA0 = 1) Automatic communication mode ATSTA0 bit of CSIT0 register is set to 1	- Write transmit data to SIOp register (When TXEmn = 1, RXEmn = 1) - Write FFH as dummy data to SDRmn register (When TXEmn = 0, RXEmn = 1)
Interrupt	Communication completion interrupt	SMRmn register MDmn0 = 0: Transfer end interrupt MDmn0 = 1: Buffer empty interrupt
Interrupt occurrence timing	1-byte transfer mode Transmission/reception completion Automatic communication mode - When the transfer of the range specified by the ADTP0 register is completed. - Communication suspension: When 1-byte transfer is completed after bit 1 (ATSTP0) in the CSIT0 register is set to 1. - Bit shift error: When 1-byte transfer is completed after bit 1 (ERRF0) of the CSIS0 register becomes 1 while bit 2 (ERRE0) is set to 1.	- MDmn0 = 0 After transfer of transmit/receive data is completed. - MDmn0 = 1 When data is transferred from the SDRmn register to the shift register.
Communication status flag	CSIS0 register TSF0 = 0: Communication is stopped. TSF0 = 1: Communication is in progress.	SSRmn register TSFmn = 0: Communication is stopped or suspended. TSFmn = 1: Communication is in progress.
Buffer register status indication flag	None	SSRmn register BFFmn = 0: Valid data is not stored in the SDRmn register. BFFmn = 1: Valid data is stored in the SDRmn register.
Bit error detection flag	CSIS0 register ERRF0 bit	None
Overrun error detection flag	None	SSRmn register OVFmn = 0: No error occurs. OVFmn = 1: An error occurs.
Serial data output pin	SOA0 pin	SOmn pin
Serial data input pin	SIA0 pin	SImn pin
Serial clock I/O pin	SCKA0 pin	SCKmn pin
Handshake pin	STB0 pin, BUSY0 pin	None

Remarks1. For 78K0/Kx2, n = 0, 1
For RL78/G13, m: Unit number (m = 0, 1), n: Channel number (n = 0 to 3),
p: CSI number (p = 00, 01, 10, 11, 20, 21,30, 31)
Remarks2. The functions incorporated and port functions to use are different depending on the product. For details, refer to the appropriate user's manuals (hardware).

3. Comparison between Registers

Table 3.1 to Table 3.3 compares the registers for the 78K0/Kx2 Serial interface CSIA0 and the registers for the RL78/G13 Serial Array Unit used as CSImn.

Table 3.1 Comparison between Registers (1/3)

Item	78K0/Kx2	RL78/G13
Clock supply to serial array unit	None	PER0 register SAUmEN bit
Disables operation	CSIMA0 register CSIAE0 bit	STm register STmn bit
Enables operation	CSIMA0 register CSIAE0 bit	SSm register SSmn bit
Transmit operation enable/disable	CSIMA0 register TXEA0 bit	SCRmn register TXEmn bit
Receive operation enable/disable	CSIMA0 register RXEA0 bit	SCRmn register RXEmn bit
First bit specification	CSIMA0 register DIR0 bit	SCRmn register DIRmn bit
Master/slave mode specification	CSIMA0 register MASTER0 bit	SMRmn register CCSmn bit
Base clock selection	CSIS0 register CKS00 bit	SMRmn register CKSmn bit, CCSmn bit
Selection of base clock divisor	BRGCA0 register BRGCA01 bit, BRGCA00 bit	SPSm register PRSmk3 - PRSmk0 bit Upper 7 bits of SDRmn register
Strobe output enable/disable (When Master mode)	CSIS0 register STBE0 bit	None
Busy signal detection enable/disable (When Master mode)	CSIS0 register BUSYE0 bit	None
Busy signal active level setting	CSIS0 register BUSYLV0 bit	None
Bit error detection enable/disable	CSIS0 register ERRE0 bit	None
Bit error detection flag	CSIS0 register ERRF0 bit	None
Transfer status detection flag	CSIS0 register TSF0 bit	SSRmn register TSFmn bit

Remarks1. For RL78/G13, m: Unit number (m = 0, 1), n: Channel number (n = 0 to 3),
p: CSI number (p = 00, 01, 10, 11, 20, 21,30, 31)
Remarks2. The functions incorporated and port functions to use are different depending on the product. For details, refer to the appropriate user's manuals (hardware).

Table 3.2 Comparison between Registers (2/3)

Item	78K0/Kx2	RL78/G13
Automatic communication operation enable/disable	CSIMA0 register ATE0 bit	None
Automatic communication mode specification	CSIMA0 register ATM0 bit	None
Automatic data transfer stop	CSIT0 register ATSTP0 bit	None
Automatic data transfer start	CSIT0 register ATSTA0 bit	None
Automatic data transfer address point	ADTP0 register	None
Automatic Data Transfer Interval	ADTI0 register	None
Automatic data transfer address count	ADTC0 register	None
Selection of data phase	None	SCRmn register DAPmn bit
Selection of clock phase	None	SCRmn register CKPmn bit
Start trigger selection	None	SMRmn register Set STSmn bit to 0
Controls inversion of level of receive data of channel n in UART mode	None	SMRmn register Set SISmn bit to 0
Setting of operation mode of channel n	None	SMRmn register Set MDmn2 bit to 0, MDmn1 bit to 0
Selection of interrupt source of channel n	None	SMRmn register MDmn0 bit
Mask control of error interrupt signal	None	SCRmn register EOCmn bit
Setting of parity bit in UART mode	None	SCRmn register Set PTCmn1 bit to 0, PTCmn0 bit to 0
Setting of stop bit in UART mode	None	SCRmn register Set SLCmn1 bit to 0, SLCmn0 bit to 0
Setting of data length in CSI and UART modes	None	SCRmn register DLSmn1 bit, DLSmn0 bit

Remarks1. For RL78/G13, m: Unit number (m = 0, 1), n: Channel number (n = 0 to 3),
p: CSI number (p = 00, 01, 10, 11, 20, 21,30, 31)
Remarks2. The functions incorporated and port functions to use are different depending on the product. For details, refer to the appropriate user's manuals (hardware).

Table 3.3 Comparison between Registers (3/3)

Item	78K0/Kx2	RL78/G13
Clear trigger of framing error flag	None	SIRmn register FECTmn (not used)
Clear trigger of parity error flag	None	SIRmn register PECTmn (not used)
Clear trigger of overrun error flag	None	SIRmn register OVCTmn bit
Buffer register status indication flag	None	SSRmn register BFFmn bit
Framing error detection flag	None	SSRmn register FEFmn (not used)
Parity/ACK error detection flag	None	SSRmn register PEFmn (not used)
Overrun error detection flag	None	SSRmn register OVFmn bit
Indication of operation enable/stop status	None	SEm register SEmn bit
Serial output enable/stop	None	SOEm register SOEmn bit
Clock output value setting when operation is disabled	None	SOm register CKOmn bit
Data output value setting when operation is disabled	None	SOm register SOmn bit
Selects inversion of the level of the transmit data	None	SOLm register Set SOLmn bit to 0
Selection of whether to enable or disable the generation of communication error interrupts in the SNOOZE mode	None	SSCm register SSECm bit
Setting of the SNOOZE mode	None	SSCm register SWCm bit
Switching channel 7 input of timer array unit	None	ISC register Set ISC1 bit to 0
Switching external interrupt (INTP0) input	None	ISC register Set ISC0 bit to 0
Use of noise filter	None	NFEN0 register Set SNFENn0 bit to 0

Remarks1. For RL78/G13, m: Unit number (m = 0, 1), n: Channel number (n = 0 to 3),
p: CSI number (p = 00, 01, 10, 11, 20, 21,30, 31)
Remarks2. The functions incorporated and port functions to use are different depending on the product. For details, refer to the appropriate user's manuals (hardware).

4. Sample Code for Serial Array Unit

The sample code for Serial Array Unit is explained in the following application notes.

- RL78/G13 Serial Array Unit for 3-Wire Serial I/O (Master Transmission/Reception) CC-RL (R01AN2547)
- RL78/G13 Serial Array Unit for 3-Wire Serial I/O (Slave Transmission/Reception) CC-RL (R01AN2711)
- RL78/G13 DMA Controller (3-Wire Serial I/O Sequential Reception) CC-RL (R01AN2800)
- RL78/G13 Low-power Consumption Operation (CSI in SNOOZE Mode) CC-RL (R01AN2762)

5. Documents for Reference

User's Manual:

- RL78/G13 User's Manual: Hardware (R01UH0146)
- 78K0/Kx2 User's Manual: Hardware (R01UH0008)

The latest versions can be downloaded from the Renesas Electronics website.

Technical Update/Technical News:

The latest information can be downloaded from the Renesas Electronics website.

Revision History

Rev.	Data	Description	
		Page	Summary
1.00	Jul.31, 2019	-	First edition issued

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1. Precaution against Electrostatic Discharge (ESD)
   A strong electrical field, when exposed to a CMOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop the generation of static electricity as much as possible, and quickly dissipate it when it occurs. Environmental control must be adequate. When it is dry, a humidifier should be used. This is recommended to avoid using insulators that can easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors must be grounded. The operator must also be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions must be taken for printed circuit boards with mounted semiconductor devices.
2. Processing at power-on
   The state of the product is undefined at the time when power is supplied. The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the time when power is supplied. In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the time when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the time when power is supplied until the power reaches the level at which resetting is specified.
3. Input of signal during power-off state
   Do not input signals or an I/O pull-up power supply while the device is powered off. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Follow the guideline for input signal during power-off state as described in your product documentation.
4. Handling of unused pins
   Handle unused pins in accordance with the directions given under handling of unused pins in the manual. The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of the LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible.
5. Clock signals
   After applying a reset, only release the reset line after the operating clock signal becomes stable. When switching the clock signal during program execution, wait until the target clock signal is stabilized. When the clock signal is generated with an external resonator or from an external oscillator during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Additionally, when switching to a clock signal produced with an external resonator or by an external oscillator while program execution is in progress, wait until the target clock signal is stable.
6. Voltage application waveform at input pin
   Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between V_{IL} (Max.) and V_{IH} (Min.) due to noise, for example, the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between V_{IL} (Max.) and V_{IH} (Min.).
7. Prohibition of access to reserved addresses
   Access to reserved addresses is prohibited. The reserved addresses are provided for possible future expansion of functions. Do not access these addresses as the correct operation of the LSI is not guaranteed.
8. Differences between products
   Before changing from one product to another, for example to a product with a different part number, confirm that the change will not lead to problems. The characteristics of a microprocessing unit or microcontroller unit products in the same group but having a different part number might differ in terms of internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

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