

## RL78/G13, 78K0/Kx2

### Migration Guide from 78K0 to RL78: CPU architecture

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#### Introduction

This application note describes how to migrate the CPU architecture of the 78K0/Kx2 to the CPU architecture of the RL78/G13.

#### Target Device

RL78/G13, 78K0/Kx2

When using this application note with other Renesas MCUs, careful evaluation is recommended after making modifications to comply with the alternate MCU.

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## 1. Differences in Function Overview

Table 1.1 overviews the differences between the CPU architecture of the 78K0/Kx2 and those of the RL78/G13.

Table 1.1 Differences

Item	78K0/Kx2	RL78/G13
Memory Space	64 KB (0000H - FFFFH)	1 MB (00000H - FFFFFH)
Switching of internal ROM and RAM capacities	Yes - Internal Memory Size Switching Register (IMS) - Internal Expansion RAM Size Switching Register (IXS)	None
Memory Bank Select	Yes - Memory Bank Select Register (BANK)	None
Program Counter (PC)	16-bit	20-bit
Program Status Word (PSW)	Interrupt priority: Level 0 to 1 - In-service priority flag (ISP)	Interrupt priority: Level 0 to 3 - In-service priority flags (ISP1, ISP0)
Data access to 1-Mbyte space	None	Available by using the ES register
Branch to 1-Mbyte space	None	Available by using the CS register
Special function register (SFR) addresses	FF00H - FFFFH	FFF00H - FFFFFH
Extended special function registers (2nd SFR)	None	Yes (Addresses: F0000H - F07FFH)
Mirror area	None	Yes
Boot swap	Yes - Boot cluster 0 (0000H - 0FFFH) - Boot cluster 1 (1000H - 1FFFH)	Yes - Boot cluster 0 (00000H - 00FFFH) - Boot cluster 1 (01000H - 01FFFH)

Remark: Different products are provided with different functions. For details, refer to the appropriate user's manuals (hardware).

Figure 1.1 shows the memory maps of the 78K0/KE2 and RL78/G13 products with a ROM (flash memory) capacity of 128 Kbytes.

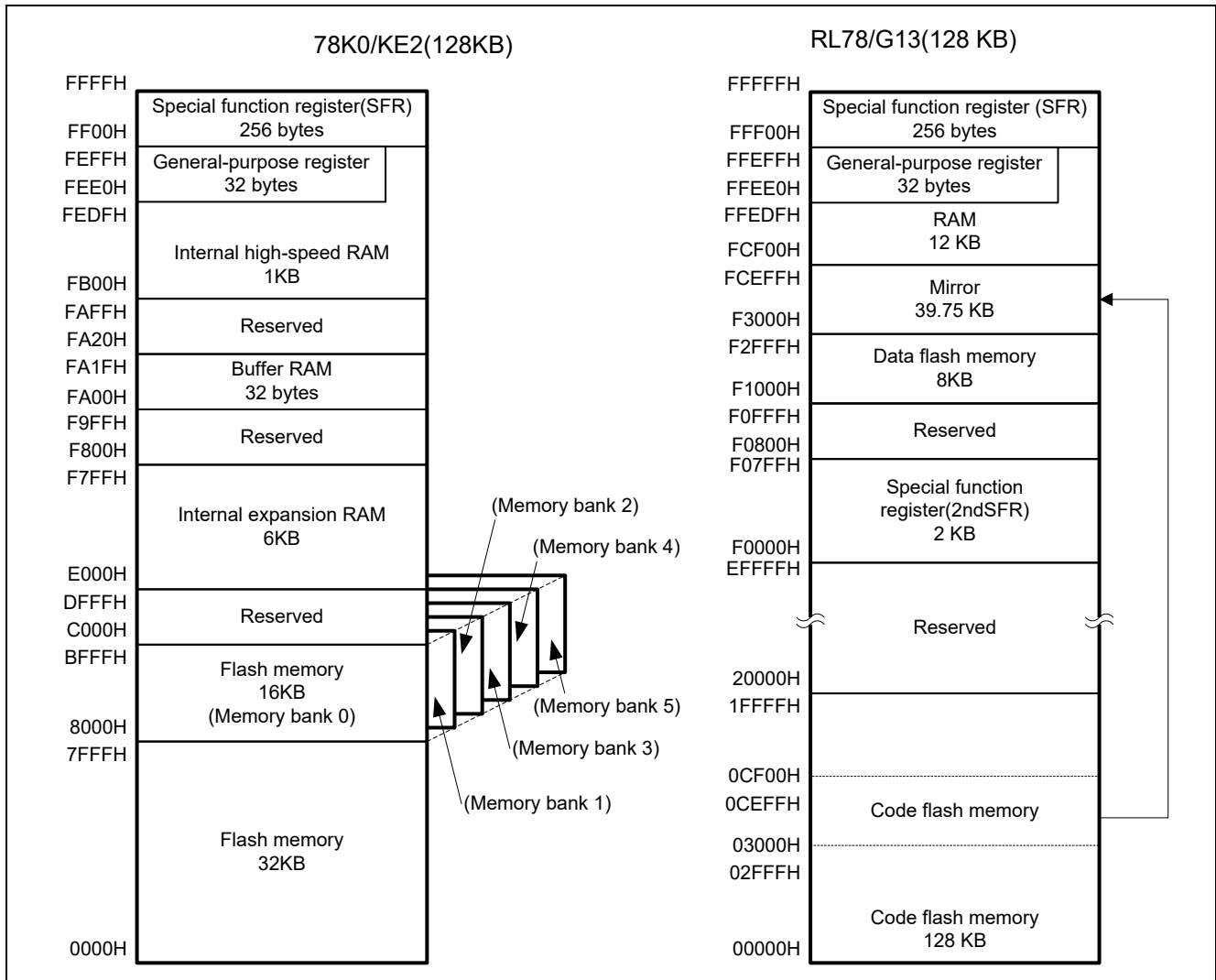


Figure 1.1 128-Kbyte Memory Maps of the 78K0/KE2 and RL78/G13

In the 78K0/Kx2, the capacities of the internal ROM (flash memory) and RAM should be set to the correct values for each product type through the internal memory size switching register (IMS) and internal expansion RAM size switching register (IXS). A 64-Kbyte memory space (0000H to FFFFH) can be accessed in the 78K0/Kx2. When the ROM area is larger than 64 Kbytes, the memory bank select register (BANK) should be used to access the ROM area beyond the 64-Kbyte space.

In the RL78/G13, in contrast, the internal ROM and RAM capacities and memory banks do not need to be changed for each product type. A 1-Mbyte memory space (00000H to FFFFFH) can be accessed by using the ES and CS registers. The RL78/G13 also provides a mirror area where the code flash contents can be read with shorter instruction code.

## 2. Reference Documents

User's Manual:

- RL78/G13 User's Manual: Hardware (R01UH0146)
- RL78 family User's Manual: Software (R01US0015)
- 78K0/Kx2 User's Manual: Hardware (R01UH0008)
- 78K/0 Series for Instructions (U12326)

The latest versions can be downloaded from the Renesas Electronics website.

Technical Update/Technical News:

The latest information can be downloaded from the Renesas Electronics website.

**Revision History**

Rev.	Date	Description	
		Page	Summary
1.00	May. 24, 2019	-	First edition issued

## General Precautions in the Handling of Microprocessing Unit and Microcontroller Unit Products

The following usage notes are applicable to all Microprocessing unit and Microcontroller unit products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

### 1. Precaution against Electrostatic Discharge (ESD)

A strong electrical field, when exposed to a CMOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop the generation of static electricity as much as possible, and quickly dissipate it when it occurs. Environmental control must be adequate. When it is dry, a humidifier should be used. This is recommended to avoid using insulators that can easily build up static electricity.

Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors must be grounded. The operator must also be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions must be taken for printed circuit boards with mounted semiconductor devices.

### 2. Processing at power-on

The state of the product is undefined at the time when power is supplied. The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the time when power is supplied. In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the time when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the time when power is supplied until the power reaches the level at which resetting is specified.

### 3. Input of signal during power-off state

Do not input signals or an I/O pull-up power supply while the device is powered off. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Follow the guideline for input signal during power-off state as described in your product documentation.

### 4. Handling of unused pins

Handle unused pins in accordance with the directions given under handling of unused pins in the manual. The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of the LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible.

### 5. Clock signals

After applying a reset, only release the reset line after the operating clock signal becomes stable. When switching the clock signal during program execution, wait until the target clock signal is stabilized. When the clock signal is generated with an external resonator or from an external oscillator during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Additionally, when switching to a clock signal produced with an external resonator or by an external oscillator while program execution is in progress, wait until the target clock signal is stable.

### 6. Voltage application waveform at input pin

Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between  $V_{IL}$  (Max.) and  $V_{IH}$  (Min.) due to noise, for example, the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between  $V_{IL}$  (Max.) and  $V_{IH}$  (Min.).

### 7. Prohibition of access to reserved addresses

Access to reserved addresses is prohibited. The reserved addresses are provided for possible future expansion of functions. Do not access these addresses as the correct operation of the LSI is not guaranteed.

### 8. Differences between products

Before changing from one product to another, for example to a product with a different part number, confirm that the change will not lead to problems. The characteristics of a microprocessing unit or microcontroller unit products in the same group but having a different part number might differ in terms of internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

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