RL78/G13, 78K0/Kx2

Migration Guide from 78K0 to RL78: 16-Bit Timer/Event Counter 00 and 01 to Timer Array Unit

Introduction

This application note describes how to migrate the 16-bit timer/event counters 00 and 01 of the 78K0/Kx2 to the timer array unit (TAU) of the RL78/G13.

Target Device

RL78/G13, 78K0/Kx2

When using this application note with other Renesas MCUs, careful evaluation is recommended after making modifications to comply with the alternate MCU.

Contents

1. Functions of 16-Bit Timer/Event Counters 00 and 01 and Timer Array Unit

Table 1.1 shows the functions of the 16-bit timer/event counters 00 and 01, and Table 1.2 shows the functions of the timer array unit (TAU).

Table 1.1 Functions of 16-Bit Timer/Event Counters 00 and 01

Function	Explanation
Interval timer	16-bit timer/event counters 00 and 01 generate an interrupt request at the preset time interval.
Square-wave output	16-bit timer/event counters 00 and 01 can output a square wave with any selected frequency.
External event counter	16-bit timer/event counters 00 and 01 can measure the number of pulses of an externally input signal.
Operation in clear & start mode entered by TI00n pin valid edge input	16-bit timer/event counters 00 and 01 clear the counters upon detection of the valid edge on the TI00n pin during count operation and start counting up again.
Free-running timer operation	16-bit timer/event counters 00 and 01 continue count up operation in synchronization with the counting clock.
PPG output operation	16-bit timer/event counters 00 and 01 can output a rectangular wave whose frequency and output pulse width can be set freely.
One-shot pulse output operation	16-bit timer event counters 00 and 01 can output a one-shot pulse whose output pulse width can be set freely.
Pulse width measurement operation	16-bit timer/event counters 00 and 01 can measure the pulse width of an externally input signal.

Table 1.2 Functions of Timer Array Unit

Function	Explanation
Interval timer	Each timer of a unit can be used as a reference timer that generates an interrupt (INTTMmn) at fixed intervals.
Square wave output	A toggle operation is performed each time INTTMmn interrupt is generated and a square wave with a duty factor of 50% is output from a timer output pin (TOmn).
External event counter	Each timer of a unit can be used as an event counter that generates an interrupt when the number of the valid edges of a signal input to the timer input pin (TImn) has reached a specific value.
Divider	A clock input from a timer input pin (TI00) is divided and output from an output pin (TO00).
Input pulse interval measurement	Counting is started by the valid edge of a pulse signal input to a timer input pin (TImn). The count value of the timer is captured at the valid edge of the next pulse. In this way, the interval of the input pulse can be measured.
Measurement of high-/low-level width of input signal	Counting is started by a single edge of the signal input to the timer input pin (TImn), and the count value is captured at the other edge. In this way, the high-level or low-level width of the input signal can be measured.
Delay counter	Counting is started at the valid edge of the signal input to the timer input pin (TImn), and an interrupt is generated after any delay period.
One-shot pulse output	Two channels are used as a set to generate a one-shot pulse with a specified output timing and a specified pulse width.
PWM output	Two channels are used as a set to generate a pulse with a specified period and a specified duty factor.
Multiple PWM output	By extending the PWM function and using one master channel and two or more slave channels, up to seven types of PWM signals that have a specific period and a specified duty factor can be generated.

Each of the 16-bit timer/event counters 00 and 01 incorporated in the 78K0/Kx2 has two timer capture/compare registers per timer counter register, two input pins, and one output pin.

Figure 1.1 shows a block diagram of the 16-bit timer/event counters 00 and 01.

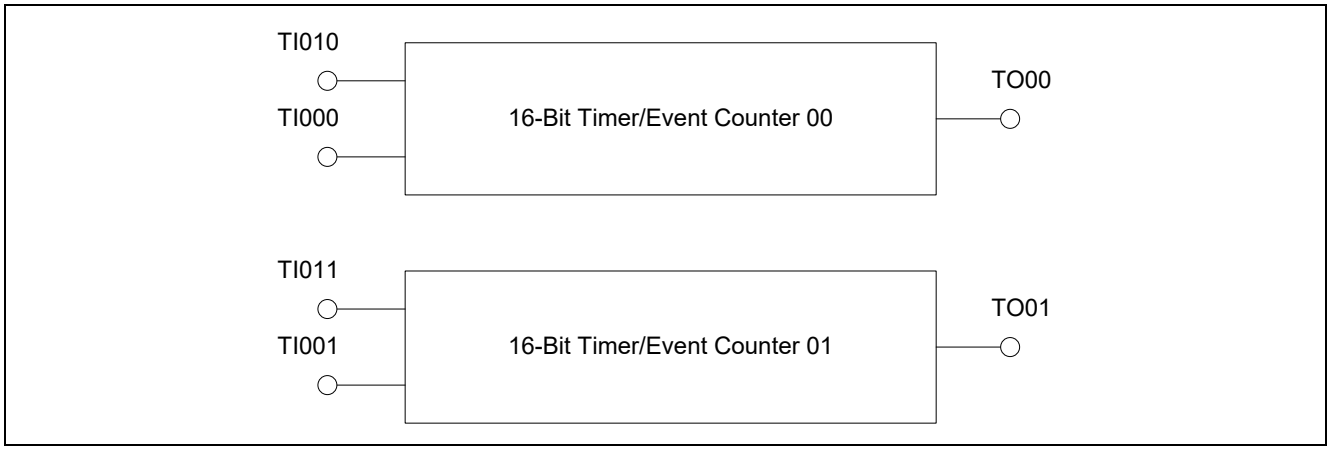

Figure 1.1 Block Diagram of 16-bit timer/event counters 00 and 01

The timer array unit (TAU) incorporated in the RL78/G13 has eight 16-bit timers. Each 16-bit timer is called a channel and can be used as an independent timer. In addition, two or more channels can be combined to serve as a higher-accuracy timer.

Each channel has one timer counter register, one timer data register, one input pin, and one output pin.

Figure 1.2 shows a block diagram of the timer array unit (TAU).

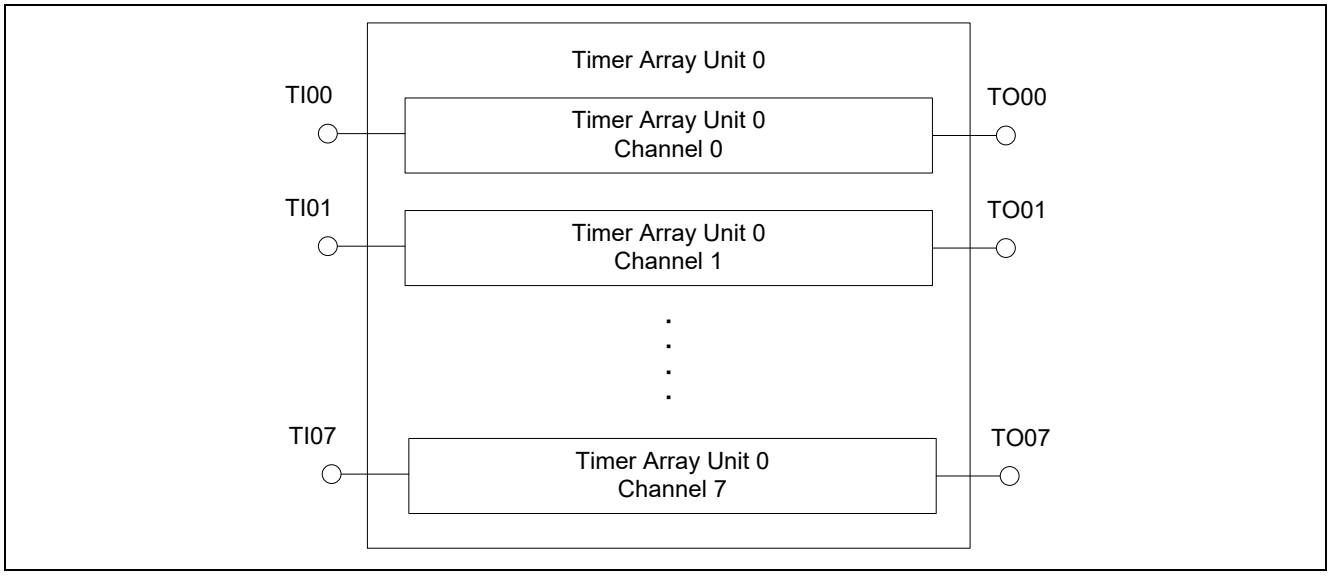

Figure 1.2 Block Diagram of Timer Array Unit

Table 1.3 shows the TAU functions corresponding to the 16-bit timer/event counters 00 and 01.

With the 16-bit timer/event counters 00 and 01, the external event counter function, the clear and start mode function entered by TI00n pin valid edge input, and the pulse width measurement function can each provide more than one operation. With the TAU, independent channels (single channel) or combined multiple channels can provide the functions equivalent to the 16-bit timer/event counters 00 and 01.

Table 1.3 Correspondence between Functions

78K0/Kx2 16-bit timer/event counters 00 and 01	RL78/G13 Timer Array Unit (TAU)	
	Operation function	Channel operation
Interval timer	Interval timer	Independent
Square-wave output	Square wave output	Independent
External event counter	External event counter	Independent
	Divider	Independent
Operation in clear & start mode entered by TI00n pin valid edge input	Input pulse interval measurement	Independent
	Measurement of high-/low-level width of input signal	Independent
Free-running timer	Input pulse interval measurement	Independent
PPG output	PWM	Simultaneous
One-shot pulse output	One-shot pulse output	Simultaneous
Pulse width measurement	Input pulse interval measurement	Independent
	Measurement of high-/low-level width of input signal	Independent

The interval timers of the 16-bit timer/event counters 00 and 01 correspond to the interval timer function of the TAU.

The square-wave output function of the 16-bit timer/event counters 00 and 01 corresponds to the square-wave output function of the TAU.

The external event counters of the 16-bit timer/event counters 00 and 01 correspond to the external event counter function or frequency divider function of the TAU.

The clear and start mode entered by TI00n pin valid edge input of the 16-bit timer/event counters 00 and 01 corresponds to the input pulse interval measurement function or input signal high-/low-level width measurement function of the TAU. With the TAU, multiple channels are used to measure the interval, high-level width, and low-level width of a single input pulse.

The free-running timers of the 16-bit timer/event counters 00 and 01 correspond to the input pulse interval measurement function of the TAU.

The PPG output function of the 16-bit timer/event counters 00 and 01 corresponds to the PWM function of the TAU.

The one-shot pulse output function of the 16-bit timer/event counters 00 and 01 corresponds to the one-shot pulse output function of the TAU.

The pulse width measurement function of the 16-bit timer/event counters 00 and 01 corresponds to the input pulse interval measurement function or input signal high-/low-level width measurement function of the TAU.

2. Differences between 16-Bit Timer/Event Counters 00 and 01 and Timer Array Unit

2.1 Summary of Differences between Functions

Table 2.1 summarizes the differences between the functions of the 16-bit timer/event counters 00 and 01 and TAU.

Table 2.1 Summary of Differences between Functions

Item	78K0/Kx2 16-bit timer/event counters 00 and 01	RL78/G13 Timer Array Unit (TAU)
Configuration	16-bit timer	16-bit timer (Note1)
Count clock	f_{PRS}, $f_{PRS}/2^2$, $f_{PRS}/2^8$, $f_{PRS}/2^4$, $f_{PRS}/2^6$	f_{TCLK} (f_{CLK} ～ $f_{CLK}/2^{15}$), f_{SUB}, f_{IL},
Counter	TM0n register	TCRmn register
Count setting value	CR00n register	TDRmn register
Count Mode	Count up	Count up, Count down (Note3)
Operation Mode	• Interval timer • Square-wave output • External event counter • Clear & start mode entered by TI00n pin valid edge input • Free-running timer • PPG output • One-shot pulse output • Pulse width measurement	• Iinterval timer • Square wave output • External event counter • Frequency divider (channel 0 of unit 0 only) • Input pulse interval measurement • Input signal high-/low-level width measurement • Delay counter • One-shot pulse output function (Note2) • PWM output (Note2) • Multiple PWM output (Note2)
Simultaneous channel operation function	Not applicable	Applicable (Note2)
Timer input	TI00n, TI01n	TI00-TI07, TI10-TI17
Timer output	TO0n, Output controller	TO00-TO07, TO10-TO17, Output controller

Note 1. Channels 1 and 3 can be each used in 2-channel 8-bit timer configuration.

Note 2. Realized by combining master and slave channels.

Note 3. Depends on the mode.

Remarks 1. For 78K0/Kx2, n = 0, 1

For RL78/G13, m: Unit number (m = 0, 1), n: Channel number (n = 0 to 7)

Remarks 2. Different products are provided with different functions. For details, refer to the appropriate user's manuals (hardware).

2.2 Differences between Interval Timers

The interval timers of the 16-bit timer/event counters 00 and 01 of the 78K0/Kx2 correspond to the interval timer of the TAU of the RL78/G13.

Table 2.2 shows the differences between the interval timers.

Table 2.2 Differences between Interval Timers

Item	78K0/Kx2 16-bit timer/event counters 00 and 01	RL78/G13 Timer Array Unit (TAU)
Count clock	f_{PRS}, $f_{PRS}/2^2$, $f_{PRS}/2^8$	f_{TCLK} (f_{CLK} ～ $f_{CLK}/2^{15}$), f_{SUB}(Note), f_{IL}(Note)
Enable supplying the clock to the timer array unit	None	Setting the TAUmEN bit in the PER0 register to 1
Count mode	Count up	Count down
Generation period of interrupt	(Set value of CR00n + 1) × Period of count clock	(Set value of TDRmn＋1) × Period of count clock
Interrupt occur timing	When the TM0n register value matches the CR00n register value and then the next count clock pulse (selected by PRM00 register) is generated	- When TCRmn reaches 0000H and then the next count clock pulse (fMCK) is generated - When count operation starts (only if MDmn0 bit in the TMRmn register is set to 1)
Starts count operation	Setting the TMC0n3 and TMC0n2 bits in the TMC0n register to 11	Setting the TSmn bit in the TSm register to 1
Stops count operation	Setting the TMC0n3 and TMC0n2 bits in the TMC0n register to 00	Setting the TTmn bit in the TTm register to 1
Counter value initialization timing	- When an interrupt occurs - When count operation stops	- When count operation starts - When an interrupt occurs
Acquires timer counter value	Reading the TM0n register when the TMC0n3 and TMC0n2 bits in the TMC0n register are not 00	Reading the TCRmn register

Note. Channel 5 only

Remarks 1. For 78K0/Kx2, n = 0, 1

For RL78/G13, m: Unit number (m = 0, 1), n: Channel number (n = 0 to 7)

Remarks 2. Different products are provided with different functions. For details, refer to the appropriate user's manuals (hardware).

2.3 Differences between Square-Wave Output Functions

The square-wave output function of the 16-bit timer/event counters 00 and 01 of the 78K0/Kx2 corresponds to the square-wave output function of the TAU of the RL78/G13.

Table 2.3 shows the differences between the square-wave output functions.

Table 2.3 Differences between Square-Wave Output Functions

Item	78K0/Kx2 16-bit timer/event counters 00 and 01	RL78/G13 Timer Array Unit (TAU)
Count clock	f_{PRS}, $f_{PRS}/2^2$, $f_{PRS}/2^8$	f_{TCLK} (f_{CLK} ～ $f_{CLK}/2^{15}$), f_{SUB}(Note1), f_{IL}(Note1)
Enable supplying the clock to the timer array unit	None	Setting the TAUmEN bit in the PER0 register to 1
Count mode	Count up	Count down
Square wave frequency	Frequency of count clock / { (Set value of CR00n＋1) x 2}	Frequency of count clock / { (Set value of TDRmn＋1) x 2 }
Interrupt occur timing	When the TM0n register value matches the CR00n register value and then the next count clock pulse (selected by PRM0n register) is generated	- When TCRmn reaches 0000H and then the next count clock pulse (fMCK) is generated - When count operation starts (only if MDmn0 bit in TMRmn register is set to 1)
Starts count operation	Setting the TMC0n3 and TMC0n2 bits in the TMC0n register to 11	Setting the TSmn bit in the TSm register to 1
Stops count operation	Setting the TMC0n3 and TMC0n2 bits in the TMC0n register to 00	Setting the TTmn bit in the TTm register to 1
Counter value initialization timing	- When an interrupt occurs - When count operation stops	- When count operation starts - When an interrupt occurs
Acquires timer counter value	Reading the TM0n register when the TMC0n3 and TMC0n2 bits in the TMC0n register are not 00	Reading the TCRmn register
Output level when timer output is disabled	Fixed to low (TOE0n = 0). Can also be fixed to high by setting 1 to the port latch of the multiplexed pin. Set 0 to the above latch at the start of timer output.	TOmn bit setting in the TOm register Valid only when TOEmn = 0.
Output level when timer operation starts	LVS0n and LVR0n bit setting in the TOC0n register Output level is inverted upon match between the TM0n register value and CR00n register value. Valid only when PM01 = P01 = 0, and PM06 = P06 = 0.	TOmn bit setting in the TOm register after port output is enabled. When MDmn0 = 1, output level is inverted after timer operation starts. When MDmn0 = 0, output level is not inverted after timer operation starts. Valid only when PMxx = Pxx =0, and PMCxx = 0. (Note2)
Output pin	TO0n pin	TOmn pin

Note 1. Channel 5 only

Note 2. Refer to tables, Setting Examples of Registers and Output Latches When Using Alternate Function, in the RL78/G13 User's Manual: Hardware.

Remarks 1. For 78K0/Kx2, n = 0, 1

For RL78/G13, m: Unit number (m = 0, 1), n: Channel number (n = 0 to 7)

Remarks 2. Different products are provided with different functions. For details, refer to the appropriate user's manuals (hardware).

2.4 Differences between External Event Counters

The external event counters of the 16-bit timer/event counters 00 and 01 of the 78K0/Kx2 correspond to the external event counter of the TAU of the RL78/G13.

Table 2.4 shows the differences between the external event counters.

Table 2.4 Differences between External Event Counters

Item	78K0/Kx2 16-bit timer/event counters 00 and 01	RL78/G13 Timer Array Unit (TAU)
Enable supplying the clock to the timer array unit	None	Setting the TAUmEN bit in the PER0 register to 1
Count mode	Count up	Count down
Setting for number of times of detection of external event input	CR00n register	TDRmn register
Interrupt occur timing	Second time or later: When the valid edge on the TI00n pin is detected for the times indicated by (set value of CR00n register + 1) First time only: When the valid edge on the TI00n pin is detected for the times indicated by (set value of CR00n register + 2)	When the valid edge on the TImn pin is detected for the times indicated by (set value of TDRmn register + 1)
Detects valid edge	Sampling clock: f_{PRS} Level detection: Match 2 times in a row	When TNFENmn = 1, Sampling clock: f_{MCK} Level detection: Match 2 times in a row When TNFENmn = 0, Sampling clock: f_{MCK} Level detection: Match 1 time (synchronized with f_{MCK})
Starts count operation	Setting the TMC0n3 and TMC0n2 bits in the TMC0n register to 11	Setting the TSmn bit in the TSm register to 1
Stops count operation	Setting the TMC0n3 and TMC0n2 bits in the TMC0n register to 00	Setting the TTmn bit in the TTm register to 1
Counter value initialization timing	- When an interrupt occurs - When count operation stops	- When count operation starts - When an interrupt occurs
Acquires timer counter value	Reading the TM0n register when the TMC0n3 and TMC0n2 bits in the TMC0n register are not 00	Reading the TCRmn register
Input pin	TI00n pin	TImn pin
Output pin	TO0n pin	Substituted by port manipulation using an interrupt or frequency divider (channel 0 of unit 0 only).

Remarks 1. For 78K0/Kx2, n = 0, 1

For RL78/G13, m: Unit number (m = 0, 1), n: Channel number (n = 0 to 7)

Remarks 2. Different products are provided with different functions. For details, refer to the appropriate user's manuals (hardware).

2.5 Differences from Clear and Start Mode Entered by TI00n Pin Valid Edge Input

The clear and start mode entered by TI00n pin valid edge input of the 16-bit timer/event counters 00 and 01 of the 78K0/Kx2 corresponds to the input pulse interval measurement function or input signal high-/low-level width measurement function of the TAU of the RL78/G13.

Table 2.5 shows the operation in clear and start mode entered by TI00n pin valid edge input.

Table 2.5 Operation in Clear and Start Mode Entered by TI00n Pin Valid Edge Input

CR00n, CR01n operating mode	Operation
Compare register	The INTTM00n or INTTM01n signal is generated upon a match between TM0n and CR00n or a match between TM0n and CR01n.
Capture register	The count value of TM0n is captured to CR00n and the INTTM00n signal is generated when the valid edge is input to the TI01n pin (or when the phase reverse to that of the valid edge is input to the TI00n pin). The count value of TM0n is captured to CR01n and the INTTM01n signal is generated when the valid edge is input to the TI00n pin. The counter is cleared to 0000H simultaneously with the capture operation upon valid edge input to the TI00n pin.

To provide the TAU of the RL78/G13 with the clear and start mode function entered by TI00n pin valid edge input of the 16-bit timer/event counters 00 and 01 of the 78K0/Kx2, select the appropriate functions of the TAU according to the CR00n and CR01n settings of the 78K0/Kx2.

Table 2.6 shows the correspondence between start and clear mode entered by TI00n pin valid edge input and the TAU functions.

Table 2.6 Correspondence between Start and Clear Mode Entered by TI00n Pin Valid Edge Input and TAU Functions

78K0/Kx2		RL78/G13
Clear & start mode entered by TI00n pin valid edge input		TAU Function
CR00n operating mode	CR01n operating mode	
Compare register	Compare register	Substituted by port manipulation using an interrupt
Compare register	Capture register	Input pulse interval measurement
Capture register	Compare register	Input signal high-/low-level width measurement
Capture register	Capture register	Input signal high-/low-level width measurement or Input pulse interval measurement

2.5.1 When CR00n: Compare Register and CR01n: Capture Register

The clear and start mode (CR00n: compare register and CR01n: capture register) entered by TI00n pin valid edge input of the 16-bit timer/event counters 00 and 01 of the 78K0/Kx2 corresponds to the input pulse interval measurement function of the TAU of the RL78/G13.

Table 2.7 shows the differences between the 16-bit timer/event counters 00 and 01 of the 78K0/Kx2 (TOC0n = 13H, PRM0n = 10H, CRC0n = 04H, TMC0n = 08H, and CR00n = 0001H) and the input pulse interval measurement function of the TAU of the RL78/G13.

Table 2.7 Differences between Clear and Start Mode Entered by TI00n Pin Valid Edge Input (CR00n: Compare Register and CR01n: Capture Register) and Input Pulse Interval Measurement Function

Item	78K0/Kx2 16-bit timer/event counters 00 and 01	RL78/G13 Timer Array Unit (TAU)
Count clock	f_{PRS}, $f_{PRS}/2^2$, $f_{PRS}/2^8$	f_{TCLK} (f_{CLK} to $f_{CLK}/2^{15}$), f_{SUB}(Note1), f_{IL}(Note1)
Enable supplying the clock to the timer array unit	None	Setting the TAUmEN bit in the PER0 register to 1
Count mode	Count up	Count up
Input pulse interval (Note2)	Period of count clock × { (Captured value of CR01n +1) + (10000H × OVF0n)}	Period of count clock × { (Captured value of TDRmn +1) + (10000H × OVF)}
Interrupt occur timing	- When the valid edge on the TI00 pin is detected - When the TM0n register value matches the CR00n register value and then the next count clock pulse (selected by PRM0n register) is generated	- When the valid edge on the TImn pin is detected - When count operation starts (only if MDmn0 bit in TMRmn register is set to 1)
Capture timing to capture register	When the valid edge (rising edge) on the TI00 pin is detected	When the valid edge (falling or rising edge) on the TImn pin is detected
Operation upon match between timer counter value and compare register value	Inverts TO0n output.	Not supported (Substituted by port manipulation using an interrupt)
Starts count operation	Setting the TMC0n3 and TMC0n2 bits in the TMC0n register to 10	Setting the TSmn bit in the TSm register to 1
Stops count operation	Setting the TMC0n3 and TMC0n2 bits in the TMC0n register to 00	Setting the TTmn bit in the TTm register to 1
Counter value initialization timing	- When the valid edge (rising edge) on the TI00n pin is detected - When count operation stops	When the valid edge (falling or rising edge) on the TImn pin is detected
Acquires timer counter value	Reading the TM0n register when the TMC0n3 and TMC0n2 bits in the TMC0n register are not 00	Reading the TCRmn register
Output level when timer output is disabled	Fixed to low (TOE0n = 0). Can also be fixed to high by setting 1 to the port latch of the multiplexed pin. Set 0 to the above latch at the start of timer output.	Not supported (Substituted by port manipulation using an interrupt)
Output level when timer operation starts	LVS0n and LVR0n bit setting in the TOC0n register. Valid only when PM01 = P01 = 0, and PM06 = P06 = 0.	Not supported (Substituted by port manipulation using an interrupt)
Input pin	TI00n pin	TImn pin
Output pin	TO0n pin	Not supported (Substituted by port manipulation using an interrupt)

(Notes and Remarks are listed on the next page.)

Note 1. Channel 5 only

Note 2. If an overflow occurs two or more times, the correct interval cannot be measured.

Remarks 1. For 78K0/Kx2, n = 0, 1

For RL78/G13, m: Unit number (m = 0, 1), n: Channel number (n = 0 to 7)

Remarks 2. Different products are provided with different functions. For details, refer to the appropriate user's manuals (hardware).

2.5.2 When CR00n: Capture Register and CR01n: Compare Register

The clear and start mode (CR00n: capture register and CR01: compare register) entered by TI00n pin valid edge input of the 16-bit timer/event counters 00 and 01 of the 78K0/Kx2 corresponds to the input signal high-/low-level width measurement function of the TAU of the RL78/G13.

Table 2.8 and Table 2.9 shows the differences between the 16-bit timer/event counters 00 and 01 of the 78K0/Kx2 (TOC0n = 13H, PRM0n = 10H, CRC0n = 03H, TMC0n = 08H, and CR01n = 0001H) and the input signal high-/low-level width measurement function of the TAU of the RL78/G13.

Table 2.8 Differences between Clear and Start Mode Entered by TI00n Pin Valid Edge Input (CR00n: Capture Register and CR01n: Compare Register) and Input Signal High-/Low-Level Width Measurement Function (1/2)

Item	78K0/Kx2 16-bit timer/event counters 00 and 01	RL78/G13 Timer Array Unit (TAU)
Count clock	f_{PRS}, $f_{PRS}/2^2$, $f_{PRS}/2^8$	f_{TCLK} (f_{CLK} to $f_{CLK}/2^{15}$), f_{SUB}(Note1), f_{IL}(Note1)
Enable supplying the clock to the timer array unit	None	Setting the TAUmEN bit in the PER0 register to 1
Count mode	Count up	Count up
Input pulse high-level width(Note2)	Period of count clock × { (Captured value of CR00n +1) + (10000H × OVF0n)}	Period of count clock × { (Captured value of TDRmn +1) + (10000H × OVF)}
Interrupt occur timing	When the TM0n register value matches the CR00n register value and then the next count clock pulse (selected by PRM0n register) is generated	When the falling edge on the TImn pin is detected (If high-level width is measured)
Capture timing to capture register	When the phase reverse (rising edge) to that of the TI00n pin valid edge is detected	When the falling edge on the TImn pin is detected (If high-level width is measured)
Operation upon match between timer counter value and compare register value	Inverts TO0n output.	Not supported (Substituted by port manipulation using an interrupt)
Starts count operation	Setting the TMC0n3 and TMC0n2 bits in the TMC0n register to 10	Detection of the TImn pin input rising edge (if high-level width is to be measured) after setting the TSmn bit in the TSm register to 1 to set the start edge detection wait status
Stops count operation	Setting the TMC0n3 and TMC0n2 bits in the TMC0n register to 00	Setting the TTmn bit in the TTm register to 1
Counter value initialization timing	- When the valid edge (rising edge) on the TI00n pin is detected - When count operation stops	When the falling edge on the TImn pin is detected (If high-level width is measured)
Acquires timer counter value	Reading the TM0n register when the TMC0n3 and TMC0n2 bits in the TMC0n register are not 00	Reading the TCRmn register

Note 1. Channel 5 only

Note 2. If an overflow occurs two or more times, the correct interval cannot be measured.

Remarks 1. For 78K0/Kx2, n = 0, 1

For RL78/G13, m: Unit number (m = 0, 1), n: Channel number (n = 0 to 7)

Remarks 2. Different products are provided with different functions. For details, refer to the appropriate user's manuals (hardware).

Table 2.9 Differences between Clear and Start Mode Entered by TI00n Pin Valid Edge Input (CR00n: Capture Register and CR01n: Compare Register) and Input Signal High-/Low-Level Width Measurement Function (2/2)

Item	78K0/Kx2 16-bit timer/event counters 00 and 01	RL78/G13 Timer Array Unit (TAU)
Output level when timer output is disabled	Fixed to low (TOE0n = 0). Can also be fixed to high by setting 1 to the port latch of the multiplexed pin. Set 0 to the above latch at the start of timer output.	Not supported (Substituted by port manipulation using an interrupt)
Output level when timer operation starts	LVS0n and LVR0n bit setting in the TOC0n register. Valid only when PM01 = P01 = 0, and PM06 = P06 = 0.	Not supported (Substituted by port manipulation using an interrupt)
Input pin	TI00n pin	TImn pin
Output pin	TO0n pin	Not supported (Substituted by port manipulation using an interrupt)

Remarks 1. For 78K0/Kx2, n = 0, 1

For RL78/G13, m: Unit number (m = 0, 1), n: Channel number (n = 0 to 7)

Remarks 2. Different products are provided with different functions. For details, refer to the appropriate user's manuals (hardware).

2.5.3 When CR00n: Capture Register and CR01n: Capture Register

The clear and start mode (CR00n: capture register and CR01: capture register) entered by TI00n pin valid edge input of the 16-bit timer/event counters 00 and 01 of the 78K0/Kx2 corresponds to the input signal high-/low-level width measurement function of the TAU of the RL78/G13. Two or three TAU channels are combined to measure the high-level width, low-level width, and pulse interval of each input pulse.

Table 2.10 and Table 2.11 shows the differences between the 16-bit timer/event counters 00 and 01 of the 78K0/Kx2 (TOC0n = 13H, PRM0n = 00H, CRC0n = 07H, and TMC0n = 0AH) and the input signal high-/low-level width measurement function of the TAU of the RL78/G13.

Table 2.10 Differences between Clear and Start Mode Entered by TI00n Pin Valid Edge Input (CR00n: Capture Register and CR01n: Capture Register) and Input Signal High-/Low-Level Width Measurement Function(1/2)

Item	78K0/Kx2 16-bit timer/event counters 00 and 01	RL78/G13 Timer Array Unit (TAU)
Count clock	f_{PRS}, $f_{PRS}/2^2$, $f_{PRS}/2^8$	f_{TCLK} (f_{CLK} to $f_{CLK}/2^{15}$), f_{SUB}(Note1), f_{IL}(Note1)
Enable supplying the clock to the timer array unit	None	Setting the TAUmEN bit in the PER0 register to 1
Count mode	Count up	Count up
Input pulse high-level width(Note2)	Period of count clock × {(Captured value of CR01n) - (Captured value of CR00n)}	Period of count clock × { (Captured value of TDRmn +1) + (10000H × OVF)}
Input pulse low-level width (Note2)	Period of count clock × {(Captured value of CR00n + 1)}	Period of count clock × { (Captured value of TDRmn +1) + (10000H × OVF)}
Input pulse width(Note2)	Period of count clock × {(Captured value of CR01n + 1) + (10000H × OVF0n)}	Calculated {(high-level width) + (low-level width)} or the input pulse interval measurement function used.
Interrupt occur timing	When the valid edge (falling edge) on the TI00n pin is detected	- When the falling edge of the TImn pin is detected (High-level width measurement channel) - When the rising edge of the TImn pin is detected (Low-level width measurement channel)
Capture timing to capture register	- When the TI00n pin valid edge is detected - When the phase reverse to that of the TI00n pin valid edge is detected	- When the falling edge on the TImn pin is detected (High-level width measurement channel) - When the rising edge on the TImn pin is detected (Low-level width measurement channel)

Note 1. Channel 5 only
Note 2. If an overflow occurs two or more times, the correct interval cannot be measured. In addition, high-/low-level width cannot be measured with the 78K0/Kx2 if an overflow occurs.
Remarks 1. For 78K0/Kx2, n = 0, 1

For RL78/G13, m: Unit number (m = 0, 1), n: Channel number (n = 0 to 7)

Remarks 2. Different products are provided with different functions. For details, refer to the appropriate user's manuals (hardware).

Remarks 3. It is also possible to use only the independent channels of the TAU to measure the pulse interval, high-level width, and low-level width of each input pulse. For details, refer to the application note below.

RL78/G13 Timer Array Unit (Pulse Interval Measurement (Both edges)) CC-RL (R01AN4259E)

Table 2.11 Differences between Clear and Start Mode Entered by TI00n Pin Valid Edge Input (CR00n: Capture Register and CR01n: Capture Register) and Input Signal High-/Low-Level Width Measurement Function (2/2)

Item	78K0/Kx2 16-bit timer/event counters 00 and 01	RL78/G13 Timer Array Unit (TAU)
Starts count operation	Setting the TMC0n3 and TMC0n2 bits in the TMC0n register to 10	- When the rising edge on the TImn pin is detected (High-level width measurement channel) - When the falling edge on the TImn pin is detected (Low-level width measurement channel)
Stops count operation	Setting the TMC0n3 and TMC0n2 bits in the TMC0n register to 00	Setting the TTmn bit in the TTm register to 1
Counter value initialization timing	- When the valid edge (falling edge) on the TI00n pin is detected - When count operation stops	- When the rising edge on the TImn pin is detected (High-level width measurement channel) - When the falling edge on the TImn pin is detected (Low-level width measurement channel)
Acquires timer counter value	Reading the TM0n register when the TMC0n3 and TMC0n2 bits in the TMC0n register are not 00	Reading the TCRmn register
Input pin	TI00n pin	TImn pin

Remarks 1. For 78K0/Kx2, n = 0, 1

For RL78/G13, m: Unit number (m = 0, 1), n: Channel number (n = 0 to 7)

Remarks 2. Different products are provided with different functions. For details, refer to the appropriate user's manuals (hardware).

Remarks 3. It is also possible to use only the independent channels of the TAU to measure the pulse interval, high-level width, and low-level width of each input pulse. For details, refer to the application note below.

RL78/G13 Timer Array Unit (Pulse Interval Measurement (Both edges)) CC-RL (R01AN4259E)

2.6 Differences from Free-Running Timers

The free-running timers of the 16-bit timer/event counters 00 and 01 of the 78K0/Kx2 correspond to the input pulse interval measurement function of the TAU of the RL78/G13.

Table 2.12 shows the differences between the 16-bit timer/event counters 00 and 01 of the 78K0/Kx2 (TOC0n = 13H, PRM0n = 50H, CRC0n = 05H, and TMC0n = 04H) and the input pulse interval measurement function of the TAU of the RL78/G13. Two TAU channels are used in the RL78/G13 to measure two input waveforms.

Table 2.12 Differences between Free-Running Timer (CR00n: Capture Register and CR01n: Capture Register) and Input Pulse Interval Measurement

Item	78K0/Kx2 16-bit timer/event counters 00 and 01	RL78/G13 Timer Array Unit (TAU)
Count clock	f_{PRS}, $f_{PRS}/2^2$, $f_{PRS}/2^8$	f_{TCLK} (f_{CLK} to $f_{CLK}/2^{15}$), f_{SUB} (Note1), f_{IL} (Note1)
Enable supplying the clock to the timer array unit	None	Setting the TAUmEN bit in the PER0 register to 1
Count mode	Count up	Count up
Input pulse width (Note2)	- TI00n pin: (Captured value of CR01n) - (Previously captured value of CR01n) + (10000H × OVF0n) - TI01n pin: (Captured value of CR00n) - (Previously captured value of CR00n) + (10000H × OVF0n)	Period of count clock × { (Captured value of TDRmn +1) + (10000H × OVF)}
Interrupt occur timing	- INTTM00n Interrupt : When the valid edge on the TI01n pin is detected - INTTM01n Interrupt : When the valid edge on the TI01n pin is detected	- When the valid edge on the TImn pin is detected - When count operation starts (only if MDmn0 bit in TMRmn register is set to 1)
Capture timing to capture register	When the TI00n or TI01n pin valid edge (rising edge) is detected	When the valid edge (falling or rising edge) on the TImn pin is detected
Starts count operation	Setting the TMC0n3 and TMC0n2 bits in the TMC0n register to 10	Setting the TSmn bit in the TSm register to 1
Stops count operation	Setting the TMC0n3 and TMC0n2 bits in the TMC0n register to 00	Setting the TTmn bit in the TTm register to 1
Acquires timer counter value	Reading the TM0n register when the TMC0n3 and TMC0n2 bits in the TMC0n register are not 00	Reading the TCRmn register
Input pin	TI00n pin, TI01n pin	TImn pin

Note 1. Channel 5 only

Note 2. If an overflow occurs two or more times, the correct interval cannot be measured.

Remarks 1. For 78K0/Kx2, n = 0, 1

For RL78/G13, m: Unit number (m = 0, 1), n: Channel number (n = 0 to 7)

Remarks 2. Different products are provided with different functions. For details, refer to the appropriate user's manuals (hardware).

2.7 Differences from PPG Output Function

The PPG output function of the 16-bit timer/event counters 00 and 01 of the 78K0/Kx2 corresponds to the PWM function of the TAU of the RL78/G13.

Table 2.11 and Table 2.12 show the differences between the PPG output function of the 16-bit timer/event counters 00 and 01 of the 78K0/Kx2 and the PWM function of the TAU of the RL78/G13.

Table 2.13 Differences from PPG Output Function (1/2)

Item	78K0/Kx2 16-bit timer/event counters 00 and 01	RL78/G13 Timer Array Unit (TAU)
Count clock	f_{PRS}, $f_{PRS}/2^2$, $f_{PRS}/2^8$	f_{TCLK} (f_{CLK} to $f_{CLK}/2^{15}$), f_{SUB}(Note1), f_{IL}(Note1)
Enable supplying the clock to the timer array unit	None	Setting the TAUmEN bit in the PER0 register to 1
Count mode	Count up	Count down
Period of output waveform	Period of count clock × (Set value of CR00n ＋1)	Period of count clock × { Set value of TDRmn (Master) + 1}
High-level width of output waveform (Note2)	- When LVS0n = 1, LVR0n =0 Period of count clock × (Set value of CR01n ＋1) - When LVS0n = 0, LVR0n =1 Period of count clock × {(Set value of CR00n) - (Set value of CR01n)}	- When TOLm = 0 (active high) Period of count clock × {Set value of TDRmp (Slave)} - When TOLm = 1 (active low) Period of count clock × [{Set value of TDRmn (Master) + 1} - {Set value of TDRmp (Slave) }]
Interrupt occur timing	When the TM0n register value matches the CR00n or CR01n register value and then the next count clock pulse (selected by PRM0n register) is generated	- When count operation starts (master) - When TCRmn reaches 0000H and then the next count clock pulse (fMCK) is generated (master) - When TCRmp reaches 0000H and then the next count clock pulse (fMCK) is generated (slave)
Compare register update timing (software)	CR01n setting is updated when INTTM01n is generated.	When INTTMmn is generated by master channel
Compare register setting	CR01n setting is changed only when high-level (low-level) width is to be changed.	- TDRmn (master) setting is changed only when the period is to be changed. - TDRmp (slave) setting is changed only when the high-level width (TOLm = 0) or low-level width (TOLm = 1) is to be changed.
Starts count operation	Setting the TMC0n3 and TMC0n2 bits in the TMC0n register to 10	Setting the TSmn bit in the TSm register to 1
Stops count operation	Setting the TMC0n3 and TMC0n2 bits in the TMC0n register to 00	Setting the TTmn bit in the TTm register to 1
Acquires timer counter value	Reading the TM0n register when the TMC0n3 and TMC0n2 bits in the TMC0n register are not 00	Reading the TCRmn register Reading the TCRmp register

Note 1. Channel 5 only
Note 2. 0000H < CR01n < CR00n ≤ FFFFH must be satisfied.
Remarks 1. For 78K0/Kx2, n = 0, 1

For RL78/G13, m: Unit number (m = 0, 1), n: Channel number (n = 0, 2, 4, 6)
p: Slave channel number (n < p ≤ 7)

Remarks 2. Different products are provided with different functions. For details, refer to the appropriate user's manuals (hardware).

Table 2.14 Differences from PPG Output Function (2/2)

Item	78K0/Kx2 16-bit timer/event counters 00 and 01	RL78/G13 Timer Array Unit (TAU)
Output level when timer output is disabled	Fixed to low (TOE0n = 0). Can also be fixed to high by setting 1 to the port latch of the multiplexed pin. Set 0 to the above latch at the start of timer output.	TOmn bit setting in the TOm register Valid only when TOEmn = 0.
Output level when timer operation starts	LVS0n and LVR0n bit setting in the TOC0n register. LVS0n = 1, LVR0n = 0 : High level LVS0n = 0, LVR0n = 1 : Low level Valid only when PM01 = P01 = 0, and PM06 = P06 = 0.	TOmp bit setting in the TOm register after port output is enabled. Output level after timer operation starts is: when TOLmp = 0, high level when TOLmp = 1, low level. However, valid only when PMxx = Pxx =0 and PMCxx = 0. (Note)
Output pin	TO0n pin	TOmp pin

Note. Refer to tables, Setting Examples of Registers and Output Latches When Using Alternate Function, in the RL78/G13 User's Manual: Hardware.

Remarks 1. For 78K0/Kx2, n = 0, 1

For RL78/G13, m: Unit number (m = 0, 1), n: Channel number (n = 0, 2, 4, 6)
p: Slave channel number (n < p ≤ 7)

Remarks 2. Different products are provided with different functions. For details, refer to the appropriate user's manuals (hardware).

2.8 Differences between One-Shot Pulse Output Functions

The one-shot pulse output function of the 16-bit timer/event counters 00 and 01 of the 78K0/Kx2 corresponds to the one-shot pulse output function of the TAU of the RL78/G13.

Table 2.13 shows the differences between the one-shot pulse output function of the 16-bit timer/event counters 00 and 01 of the 78K0/Kx2 and the one-shot pulse output function of the TAU of the RL78/G13.

Table 2.15 Differences between One-Shot Pulse Output Functions

Item	78K0/Kx2 16-bit timer/event counters 00 and 01	RL78/G13 Timer Array Unit (TAU)
Count clock	f_{PRS}, $f_{PRS}/2^2$, $f_{PRS}/2^8$	f_{TCLK} (f_{CLK} ～ $f_{CLK}/2^{15}$), f_{SUB} (Note1), f_{IL} (Note1)
Enable supplying the clock to the timer array unit	None	Setting the TAUmEN bit in the PER0 register to 1
Count mode	Count up	Count down
Time from trigger detection to pulse output	Period of count clock × (Set value of CR01n +1)	{Set value of TDRmn (Master) + 2} × Period of count clock
Active level width of output pulse (Note2)	Period of count clock × {(Set value of CR00n) - (Set value of CR01n)}	{Set value of TDRmp (Slave)} × Period of count clock
Interrupt occur timing	When the TM0n register value matches the CR00n or CR01n register value and then the next count clock pulse (selected by PRM0n register) is generated	- When TCRmn reaches 0000H and then the next count clock pulse (fMCK) is generated (master) - When TCRmp reaches 0000H and then the next count clock pulse (fMCK) is generated (slave)
Starts count operation	Setting the TMC0n3 and TMC0n2 bits in the TMC0n register to 01 or 10	- When the valid edge on the TImn pin is detected - Software trigger (TSmn = 1)
Stops count operation	Setting the TMC0n3 and TMC0n2 bits in the TMC0n register to 00	Setting the TTmn bit in the TTm register to 1
Acquires timer counter value	Reading the TM0n register when the TMC0n3 and TMC0n2 bits in the TMC0n register are not 00	Reading the TCRmn register Reading the TCRmp register
Counter value initialization timing	- When 1 is written to the one-shot pulse trigger bit (OSPT0n). - When the valid edge on the TI00n pin is detected - When count operation stops	TCRmn register (Master) - When the valid edge on the TImn pin is detected - Software trigger (TSmn = 1) TCRmp register (Slave) - When TCRmn reaches 0000H and then the next count clock pulse (fMCK) is generated
Output level when timer output is disabled	Fixed to low (TOE0n = 0). Can also be fixed to high by setting 1 to the port latch of the multiplexed pin. Set 0 to the above latch at the start of timer output.	TOmn bit setting in the TOm register Valid only when TOEmn = 0.
Output level when timer operation starts	LVS0n and LVR0n bit setting in the TOC0n register. Valid only when PM01 = P01 = 0, and PM06 = P06 = 0.	TOmp bit setting in the TOm register after port output is enabled. Output level after timer operation starts is: when TOLmp = 0, high level when TOLmp = 1, low level. However, valid only when PMxx = Pxx =0 and PMCxx = 0. (Note3)
Output pin	TO0n pin	TOmp pin

(Notes and Remarks are listed on the next page.)

Note 1. Channel 5 only

Note 2. 0000H < CR01n < CR00n ≤ FFFFH must be satisfied.

Note 3. Refer to tables, Setting Examples of Registers and Output Latches When Using Alternate Function, in the RL78/G13 User's Manual: Hardware.

Remarks 1. For 78K0/Kx2, n = 0, 1

For RL78/G13, m: Unit number (m = 0, 1), n: Channel number (n = 0, 2, 4, 6)
p: Slave channel number (n < p ≤ 7)

Remarks 2. Different products are provided with different functions. For details, refer to the appropriate user's manuals (hardware).

2.9 Differences from Pulse Width Measurement Function

The pulse width measurement function of the 16-bit timer/event counters 00 and 01 of the 78K0/Kx2 corresponds to the input pulse interval measurement function or input signal high-/low-level width measurement function of the TAU of the RL78/G13.

Table 2.14 shows the correspondence between the pulse width measurement function and the TAU functions. The differences between each function are described in the previous sections in this document, and the sections are indicated in the table.

Table 2.16 Correspondence between Pulse Width Measurement and TAU Functions

78K0/Kx2		RL78/G13	Reference Section and Page in This Document
Clear & start mode entered by TI00n pin valid edge input	CR00n：Compare register, CR01n：Capture register	Input pulse interval measurement	Section 2.5.1 (page 11)
	CR00n：Capture register, CR01n：Compare register	Measurement of high-/low-level width of input signal	Section 2.5.2 (page 13)
	CR00n：Capture register, CR01n：Capture register	Measurement of high-/low-level width of input signal or Input pulse interval measurement	Section 2.5.3 (page 15)
Free-running timer operation		Input pulse interval measurement	Section 2.6 (page 17)

3. Sample Code for Timer Array Unit

The sample code for the timer array unit is explained in the following application notes.

- RL78/G13 Timer Array Unit (Interval Timer) CC-RL (R01AN2576)
- RL78/G13 Timer Array Unit (Pulse Interval Measurement) CC-RL (R01AN2702)
- RL78/G13 Timer Array Unit (Pulse Interval Measurement (Both edges)) CC-RL (R01AN4259)
- RL78/G13 Timer Array Unit (PWM Output) CC-RL (R01AN2589)

4. Documents for Reference

User's Manual:

RL78/G13 User's Manual: Hardware (R01UH0146)

78K0/Kx2 User's Manual: Hardware (R01UH0008)

The latest versions can be downloaded from the Renesas Electronics website.

Technical Update/Technical News:

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Revision History

Rev.	Date	Description	
		Page	Summary
1.00	Mar. 29, 2019.	-	First edition issued

General Precautions in the Handling of Microprocessing Unit and Microcontroller Unit Products

The following usage notes are applicable to all Microprocessing unit and Microcontroller unit products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Precaution against Electrostatic Discharge (ESD)
   A strong electrical field, when exposed to a CMOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop the generation of static electricity as much as possible, and quickly dissipate it when it occurs. Environmental control must be adequate. When it is dry, a humidifier should be used. This is recommended to avoid using insulators that can easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors must be grounded. The operator must also be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions must be taken for printed circuit boards with mounted semiconductor devices.
2. Processing at power-on
   The state of the product is undefined at the time when power is supplied. The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the time when power is supplied. In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the time when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the time when power is supplied until the power reaches the level at which resetting is specified.
3. Input of signal during power-off state
   Do not input signals or an I/O pull-up power supply while the device is powered off. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Follow the guideline for input signal during power-off state as described in your product documentation.
4. Handling of unused pins
   Handle unused pins in accordance with the directions given under handling of unused pins in the manual. The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of the LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible.
5. Clock signals
   After applying a reset, only release the reset line after the operating clock signal becomes stable. When switching the clock signal during program execution, wait until the target clock signal is stabilized. When the clock signal is generated with an external resonator or from an external oscillator during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Additionally, when switching to a clock signal produced with an external resonator or by an external oscillator while program execution is in progress, wait until the target clock signal is stable.
6. Voltage application waveform at input pin
   Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between V_{IL} (Max.) and V_{IH} (Min.) due to noise, for example, the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between V_{IL} (Max.) and V_{IH} (Min.).
7. Prohibition of access to reserved addresses
   Access to reserved addresses is prohibited. The reserved addresses are provided for possible future expansion of functions. Do not access these addresses as the correct operation of the LSI is not guaranteed.
8. Differences between products
   Before changing from one product to another, for example to a product with a different part number, confirm that the change will not lead to problems. The characteristics of a microprocessing unit or microcontroller unit products in the same group but having a different part number might differ in terms of internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

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Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu,
Koto-ku, Tokyo 135-0061, Japan
www.renesas.com

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