RL78/G12

Timer Array Unit (Interval Timer) CC-RL

Introduction

This application note describes the interval timer function of the timer array unit (TAU). This unit inverts the LED indication each time a timer interrupt occurs. Also, it changes the timer interrupt cycle time based on the number of times the switch is pressed.

Target Device

RL78/G12

When applying the sample program covered in this application note to another microcomputer, modify the program according to the specifications for the target microcomputer and conduct an extensive evaluation of the modified program.

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1. Specifications

This application note shows example settings for using timer interrupts (INTTM00) from the interval timer and interrupts (INTP0) generated on pin input edge detection. The TAU inverts the LED indication each time a timer interrupt (INTTM00) occurs. Also, this unit changes the timer interrupt (INTTM00) cycle time based on the number of times the switch (SW) is pressed.

Table 1.1 lists the peripheral functions to be used and their uses. Figure 1.1 shows the timer and its interrupt operation.

Table 1.1 Peripheral Functions to be Used and Their Uses

Peripheral Function	Use
Timer array unit (channel 0)	Time interval control for inversion of the P13 pin output (LED indication)
P13	Output port for LED indications
P137/INTP0	Switch input for changing the timer interrupt (INTTM00) cycle time

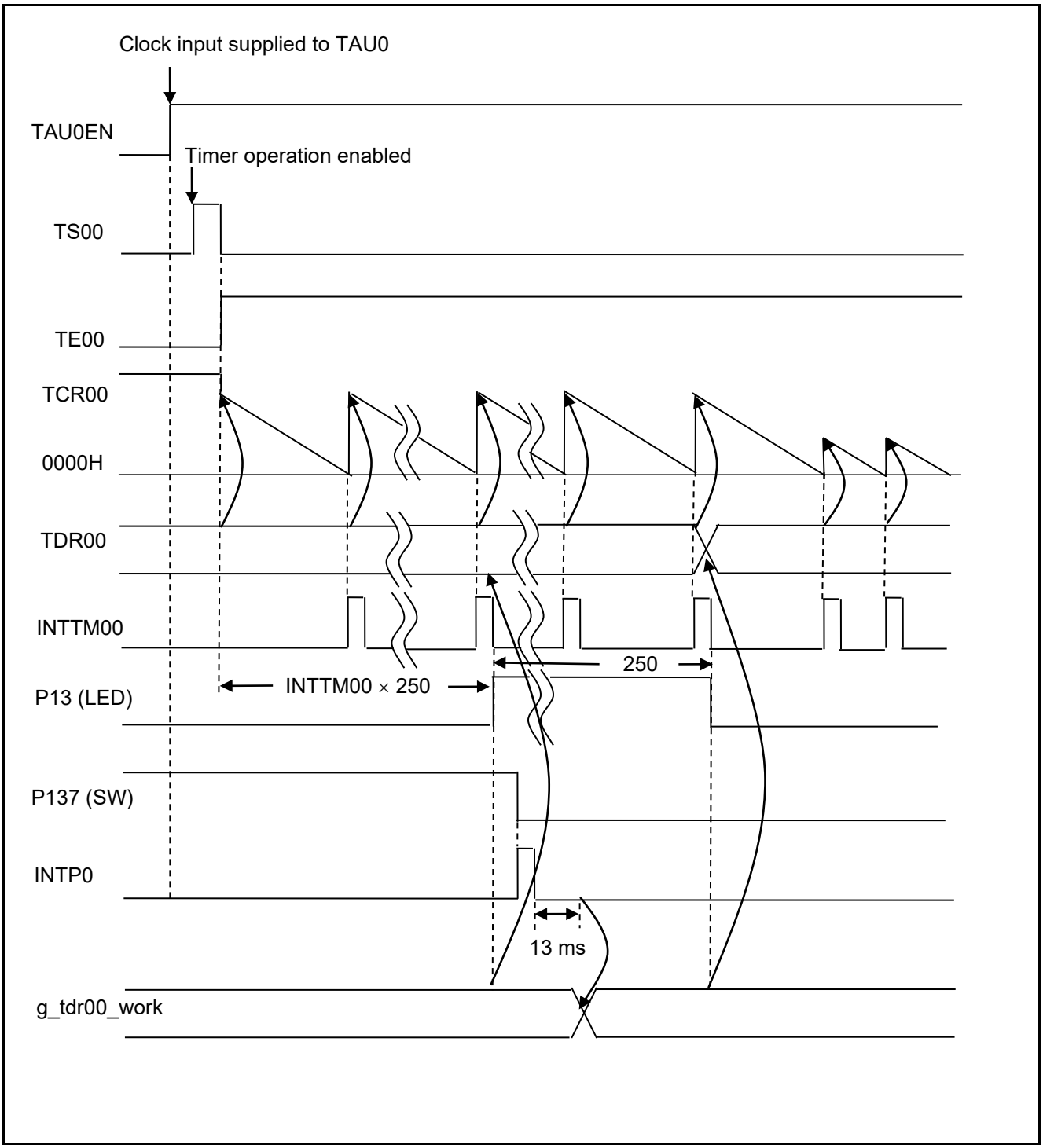


Figure 1.1 Overview of Timer Operation and Interrupts

2. Operation Check Conditions

The sample code contained in this application note has been checked under the conditions listed in the table below.

Table 2.1 Operation Check Conditions

Item	Description
Microcontroller used	RL78/G12 (R5F1026A)
Operating frequency	• High-speed on-chip oscillator (HOCO) clock: 24 MHz • CPU/peripheral hardware clock: 24 MHz
Operating voltage	5.0V (can run on a voltage range of 2.9 V to 5.5 V.) LVD operation (V_{LVD}): Reset mode 2.81 V (2.76 V to 2.87 V)
Integrated development environment (CS+)	CS+ for CC V8.07.00 from Renesas Electronics Corp.
C compiler (CS+)	CC-RL V1.11.00 from Renesas Electronics Corp.
Integrated development environment (e^2 studio)	e^2 studio V2022-01 (22.1.0) from Renesas Electronics Corp.
C compiler (e^2 studio)	CC-RL V1.11.00 from Renesas Electronics Corp.
Integrated development environment (IAR)	IAR Embedded Workbench for Renesas RL78 V4.21.3 from IAR Systems
C compiler (IAR)	IAR C/C++ Compiler for Renesas RL78 V4.21.3.2447 from IAR Systems

3. Related Application Note

The application note that is related to this application note is listed below for reference.

- RL78/G13 Timer Array Unit (Interval Timer) CC-RL (R01AN2576E) Application Note

4. Description of the Hardware

4.1 Hardware Configuration Example

Figure 4.1 shows an example of hardware configuration that is used for this application note.

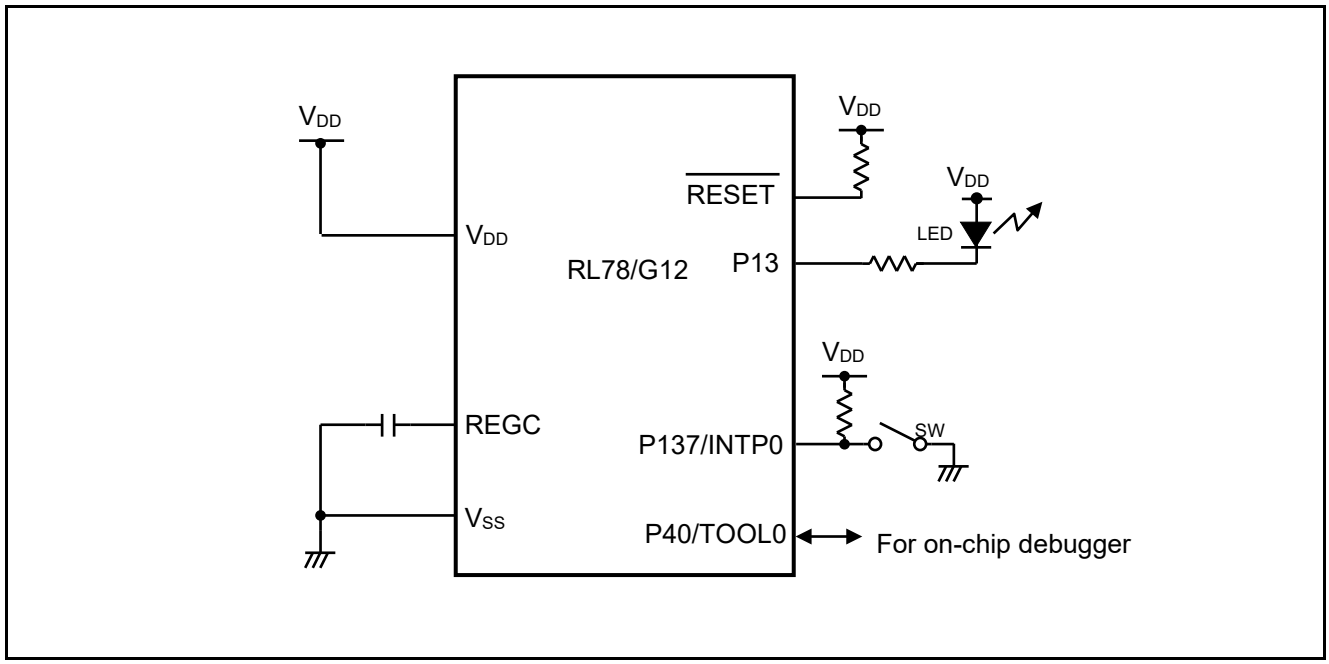


Figure 4.1 Hardware Configuration

Cautions: 1. The purpose of this circuit is only to provide the connection outline and the circuit is simplified accordingly. When designing and implementing an actual circuit, provide proper pin treatment and make sure that the hardware's electrical specifications are met (connect the input-only ports separately to V_{DD} or V_{SS} via a resistor).

2. V_{DD} must be held at not lower than the reset release voltage (V_{LVD}) that is specified as LVD.

4.2 List of Pins to be Used

Table 4.1 lists the pins to be used and their functions.

Table 4.1 Pins to be Used and Their Functions

Pin Name	I/O	Description
P13	Output	Output port for LED indications
P137/INTP0	Input	Switch (SW) input pin (external interrupt request input pin)

5. Description of the Software

5.1 Operation Outline

This application note describes how to set up the interval timer function of TAU0.

This setup is followed by operation for counting the number of timer interrupts (INTTM00) generated by the interval timer. Each time the count reaches 250, the LED indication is inverted. The timer interrupt (INTTM00) cycle time is changed according to the number of times the switch is pressed. The LED on/off cycle time is changed as follows.

666 ms → 333 ms → 166 ms → 83.3 ms → 666 ms → …

(1) Initialize the TAU.
- Use the interval timer mode as the timer operation mode.
- Initialize timer data register 00 (TDR00) to 2 ms.
- Set the timer output enable register to disable operation.
- Use timer interrupts (INTTM00) from timer channel 0.

(2) Initialize the external edge detection interrupt.
- Select a falling edge as the valid edge for INTP0.
- Use INTP0 interrupts.

(3) Execute a HALT instruction to wait for timer interrupts (INTTM00).

(4) After the HALT mode is cancelled by a timer interrupt (INTTM00), the number of INTTM00 interrupts generated is counted.

(5) When the timer interrupt count reaches 250, the LED indication is inverted. The value (g_tdr00_work) in RAM for the timer data register is set in the timer data register (TDR00).

(6) INTP0 interrupt processing changes the switch input count (INTP0 interrupt count) and g_tdr00_work value.

5.2 List of Option Byte Settings

Table 5.1 summarizes the settings of the option bytes.

Table 5.1 Option Byte Settings

Address	Value	Description
000C0H/010C0H	01101110B	Disables the watchdog timer. (Stops counting after the release from the reset state.)
000C1H/010C1H	01111111B	LVD reset mode, 2.81 V (2.76 V to 2.87 V)
000C2H/010C2H	11101000B	HS mode, HOCO: 32 MHz
000C3H/010C3H	10000100B	Enables the on-chip debugger.

5.3 List of Constants

Table 5.2 lists the constants that are used in this sample program.

Table 5.2 Constants for the Sample Program

Constant	Setting	Description
_01_INTP0_EDGE_FALLING_SEL	01h	Selects a falling edge as the valid edge of INTP0.
g_tdr00_data[]	(64000-1) (32000-1) (16000-1) (8000-1)}	TDR00 settings by number of times the switch is pressed
g_13ms_count[]	(5+1) (10+1) (20+1) (40+1)	13 ms timer count values by number of times the switch is pressed

5.4 List of Variables

Table 5.3 lists the global variable that is used by this sample program.

Table 5.3 Global Variables for the Sample Program

Type	Variable Name	Contents	Function Used
__saddr uint8_t	g_sw_counter	Switch press count	r_intc0_interrupt() main() r_invert_led()
__saddr uint16_t	g_tdr00_work	Value which is set in TDR00 each time the timer interrupt count reaches 250.	r_intc0_interrupt() main() r_invert_led()
__saddr uint8_t	g_inttm00counter	The number of timer interrupt generation	main() r_invert_led()

5.5 List of Functions

Table 5.4 lists the functions that are used by this sample program.

Table 5.4 Functions

Function Name	Outline
R_TAU0_Channel0_Start	Starts operation of TAU0 channel 0.
r_tau0_channel0_interrupt	Processes timer interrupts on TAU0 channel 0.
r_invert_led	Counts the number of INTTM00 interrupts generated. Inverts the LED indication each time the interrupt count reaches 250.
R_INTC0_Start	Enables INTP0 interrupts.
r_intc0_interrupt	Processes INTP0 interrupts.

5.6 Function Specifications

This section describes the specifications for the functions that are used in the sample code.

[Function Name] R_TAU0_Channel0_Start	
Synopsis	TAU0 channel 0 operation start
Header	r_cg_macrodriver.h r_cg_timer.h r_cg_userdefine.h
Declaration	void R_TAU0_Channel0_Start(void)
Explanation	This function unmasks TAU0 channel 0 interrupts and starts count operation.
Arguments	None
Return value	None
Remarks	None

[Function Name] r_tau0_channel0_interrupt	
Synopsis	TAU0 channel 0 timer interrupt processing
Header	r_cg_macrodriver.h r_cg_timer.h r_cg_userdefine.h
Declaration	static void __near r_tau0_channel0_interrupt(void)
Explanation	This function calls the function which will invert the LED indication.
Arguments	None
Return value	None
Remarks	None

[Function Name] r_invert_led	
Synopsis	LED indication inversion processing
Header	r_cg_macrodriver.h r_cg_cgc.h r_cg_port.h r_cg_intc.h r_cg_timer.h r_cg_userdefine.h
Declaration	void r_invert_led(void)
Explanation	This function counts 250 timer interrupts (INTTM00) and then inverts the LED indication (for port latch inversion). It also changes the TDR00 setting to the value specified with g_tdr00_work.
Arguments	None
Return value	None
Remarks	None

[Function Name] R_INTC0_Start	
Synopsis	INTP0 interrupt enable
Header	r_cg_intc.h
Declaration	void R_INTC0_Start(void)
Explanation	This function clears the interrupt request flag. It enables INTP0 interrupts and starts taking in the switch input.
Arguments	None
Return value	None
Remarks	None

[Function Name] r_intc0_interrupt	
Synopsis	INTP0 interrupt processing
Header	r_cg_macrodriver.h r_cg_intc.h r_cg_userdefine.h
Declaration	static void __near r_intc0_interrupt(void)
Explanation	This function processes INTP0 interrupts as they occur. It waits 13 ms and then scans P13.7 (SW input pin). When the switch is pressed, this function changes the g_tdr00_work value.
Arguments	None
Return value	None
Remarks	None

5.7 Flowcharts

Figure 5.1 shows the overall flow of the sample program described in this application note.

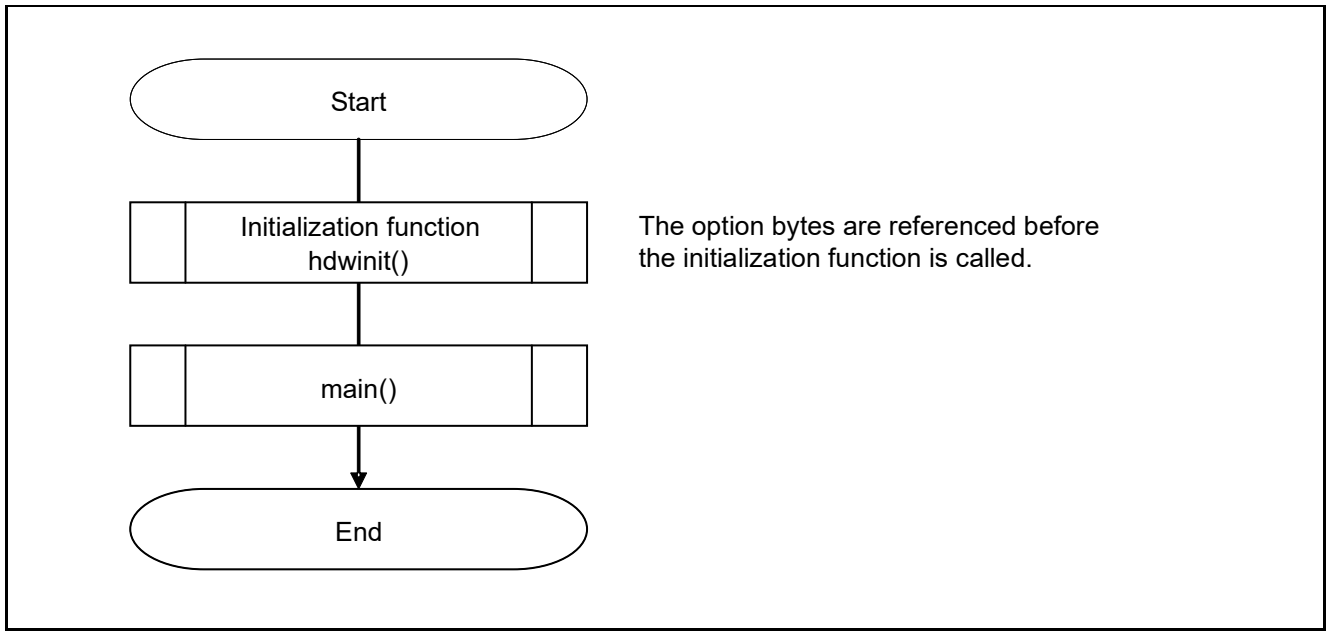


Figure 5.1 Overall Flow

Note: Startup routine is executed before and after the initialization function.

5.7.1 Initialization Function

Figure 5.2 shows the flowchart for the initialization function.

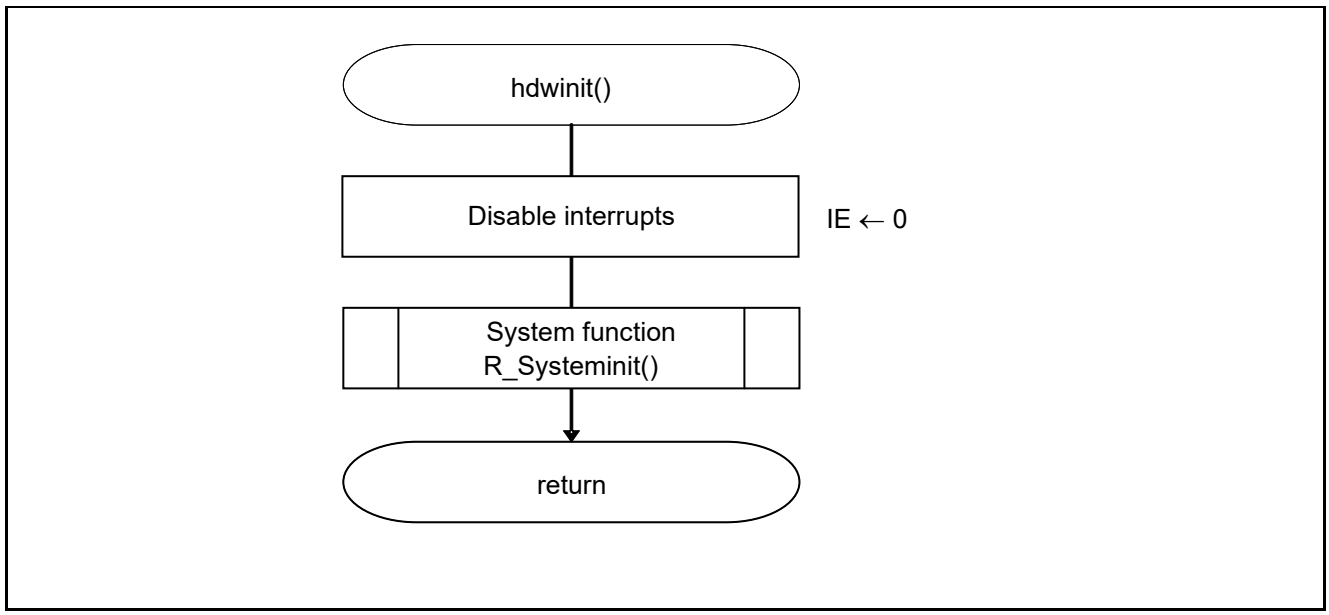


Figure 5.2 Initialization Function

5.7.2 System Function

Table 5.3 shows the flowchart for the system function.

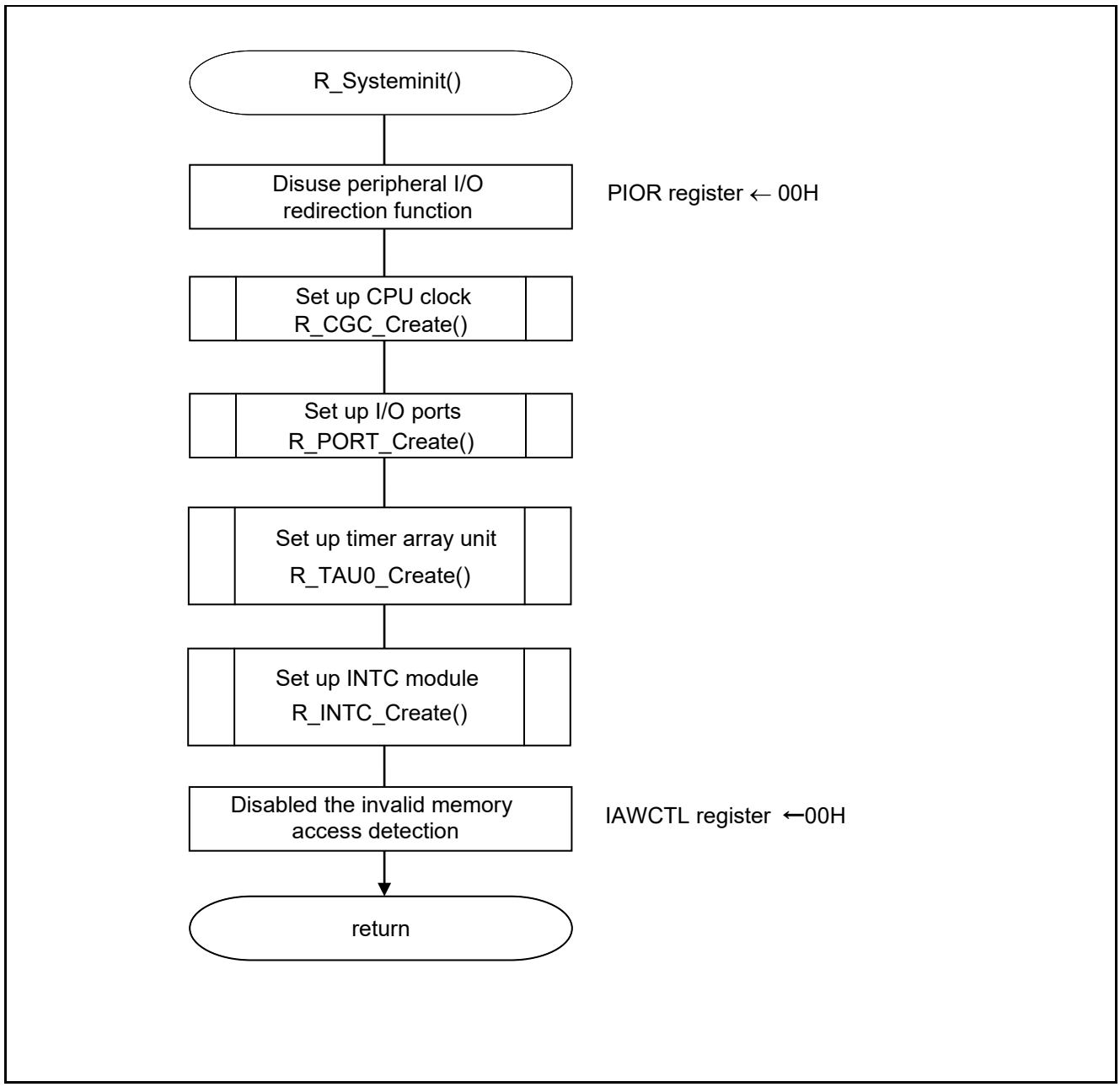


Figure 5.3 System Function

5.7.3 I/O Port Setup

Table 5.4 shows the flowchart for I/O port setup.

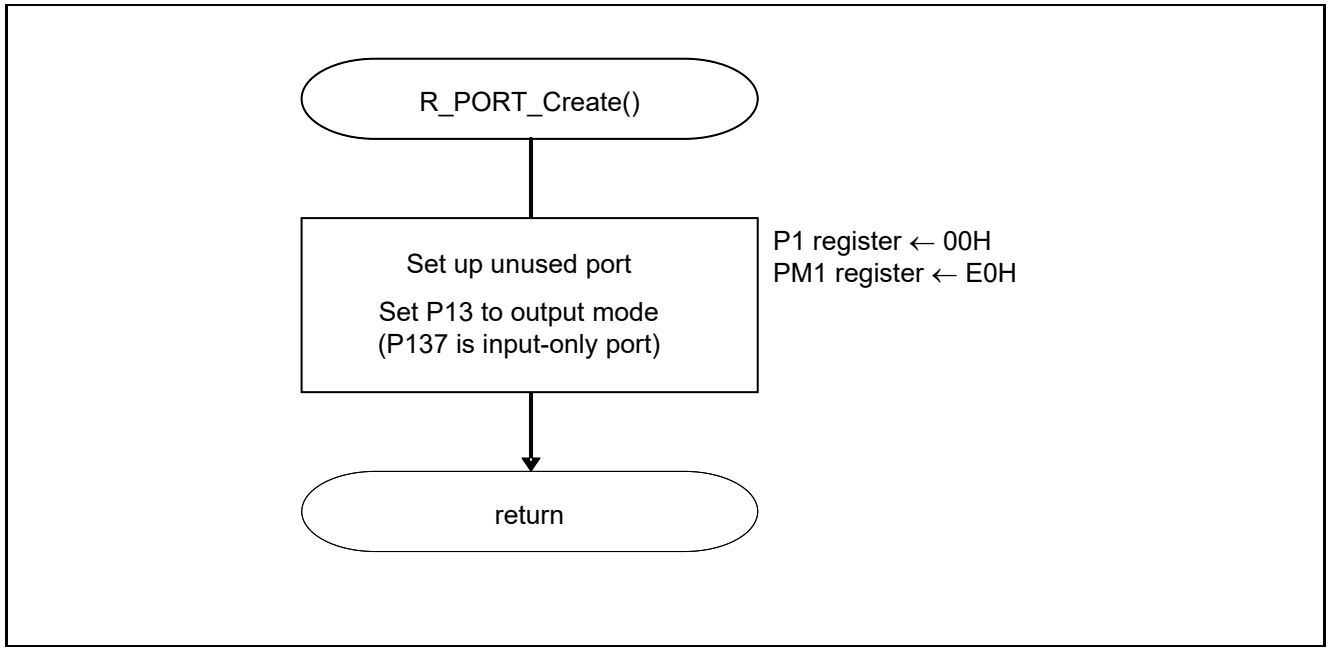


Figure 5.4 I/O Port Setup

Note: Refer to RL78/G12 User's Manual: Hardware for the configuration of the unused ports.

Caution: Provide proper treatment for unused pins so that their electrical specifications are observed. Connect each of any unused input-only ports to V_{DD} or V_{SS} via a separate resistor.

Setting up the LED port

- Port mode register 1 (PM1)
  Select I/O mode for the port.

Symbol: PM1

7	6	5	4	3	2	1	0
1	1	1	PM14	PM13	PM12	PM11	PM10
1	1	1	0	**0**	0	0	0

Bit 3

PM13	P13 pin I/O mode selection
0	**Output mode (output buffer on)**
1	Input mode (output buffer off)

Caution: For details on the register setup procedures, refer to RL78/G12 User's Manual: Hardware.

5.7.4 CPU Clock Setup

Figure 5.5 shows the flowchart for setting up the CPU clock.

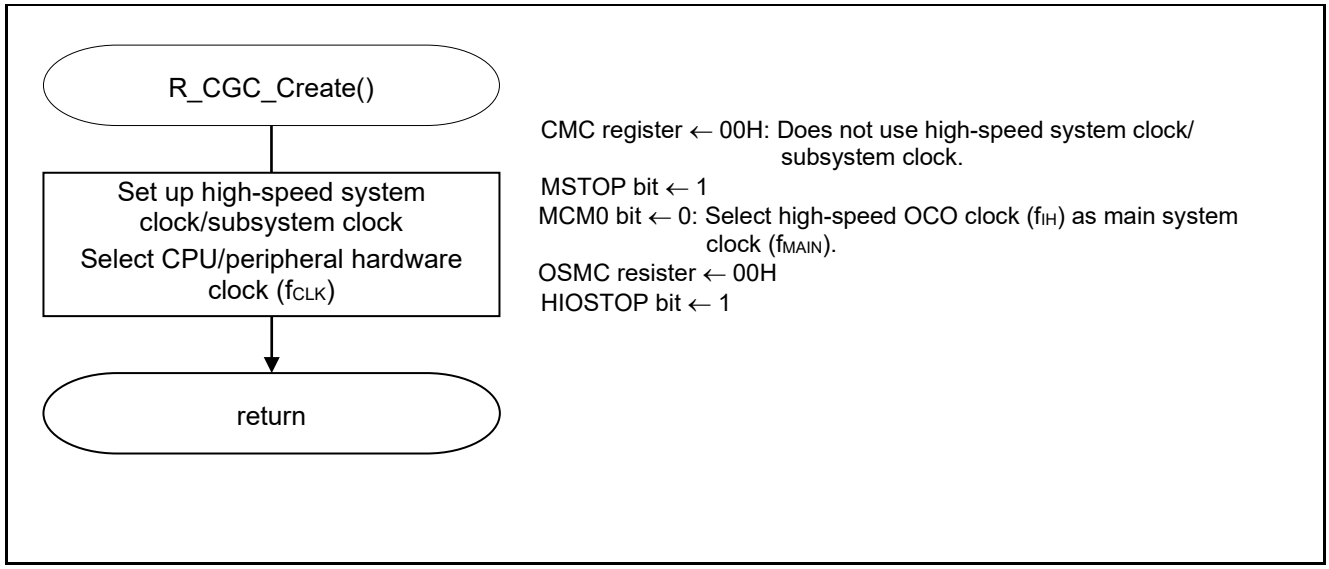


Figure 5.5 CPU Clock Setup

Caution: For details on the procedure for setting up the CPU clock (R_CGC_Create ()), refer to RL78/G12 User's Manual: Hardware.

5.7.5 Timer Array Unit Setup

Figure 5.6 shows the flowchart for setting up the timer array unit.

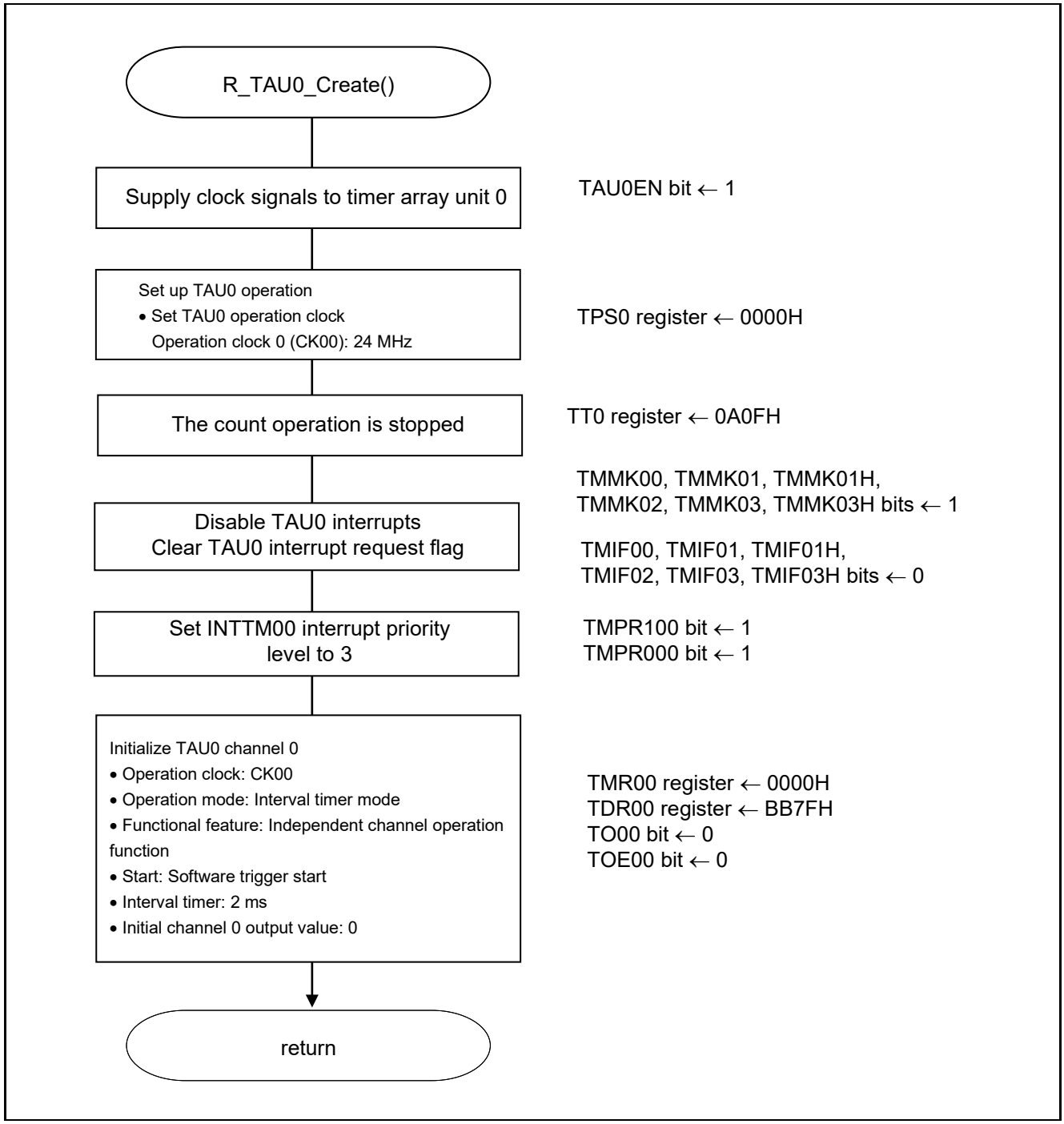


Figure 5.6 Timer Array Unit Setup

Starting clock signal supply to the timer array unit 0

- Peripheral enable register 0 (PER0)
  Start supplying clock signals to the timer array unit 0.

Symbol: PER0

7	6	5	4	3	2	1	0
TMKAEN	0	ADCEN	IICA0EN	SAU1EN	SAU0EN	0	TAU0EN
x	0	x	x	x	x	x	**1**

Bit 0

TAU0EN	Control of timer array unit 0 input clock supply
0	Stops input clock supply.
1	**Enables input clock supply.**

Caution: For details on the register setup procedures, refer to RL78/G12 User's Manual: Hardware.

Configuring the timer clock frequency

- Timer clock select register 0 (TPS0)
  Select an operation clock for timer array unit 0.

Symbol: TPS0

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	PRS 031	PRS 030	0	0	PRS 021	PRS 020	PRS 013	PRS 012	PRS 011	PRS 010	PRS 003	PRS 002	PRS 001	PRS 000
x	x	x	x	x	x	x	x	x	x	x	x	**0**	**0**	**0**	**0**

Bits 3 to 0

PRS 003	PRS 002	PRS 001	PRS 000	Operation clock (CK00) selection					
					f_{CLK}= 2 MHz	f_{CLK}= 4 MHz	f_{CLK}= 8 MHz	f_{CLK}= 20 MHz	f_{CLK}= 24 MHz
0	**0**	**0**	**0**	**f_{CLK}**	2 MHz	4 MHz	8 MHz	20 MHz	**24 MHz**
0	0	0	1	$f_{CLK}/2$	1 MHz	2 MHz	4 MHz	10 MHz	12 MHz
0	0	1	0	$f_{CLK}/2^2$	500 kHz	1 MHz	2 MHz	5 MHz	6 MHz
0	0	1	1	$f_{CLK}/2^3$	250 kHz	500 kHz	1 MHz	2.5 MHz	3 MHz
0	1	0	0	$f_{CLK}/2^4$	125 kHz	250 kHz	500 kHz	1.25 MHz	1.5 MHz
0	1	0	1	$f_{CLK}/2^5$	62.5 kHz	125 kHz	250 kHz	625 kHz	750 kHz
0	1	1	0	$f_{CLK}/2^6$	31.3 kHz	62.5 kHz	125 kHz	312.5 kHz	375 kHz
0	1	1	1	$f_{CLK}/2^7$	15.6 kHz	31.3 kHz	62.5 kHz	156.2 kHz	188 kHz
1	0	0	0	$f_{CLK}/2^8$	7.81 kHz	15.6 kHz	31.3 kHz	78.1 kHz	93.8 kHz
1	0	0	1	$f_{CLK}/2^9$	3.91 kHz	7.81 kHz	15.6 kHz	39.1 kHz	46.9 kHz
1	0	1	0	$f_{CLK}/2^{10}$	1.95 kHz	3.91 kHz	7.81 kHz	19.5 kHz	23.4 kHz
1	0	1	1	$f_{CLK}/2^{11}$	977 Hz	1.95 kHz	3.91 kHz	9.76 kHz	11.7 kHz
1	1	0	0	$f_{CLK}/2^{12}$	488 Hz	977 Hz	1.95 kHz	4.88 kHz	5.86 kHz
1	1	0	1	$f_{CLK}/2^{13}$	244 Hz	488 Hz	977 Hz	2.44 kHz	2.93 kHz
1	1	1	0	$f_{CLK}/2^{14}$	122 Hz	244 Hz	488 Hz	1.22 kHz	1.46 kHz
1	1	1	1	$f_{CLK}/2^{15}$	61.0 Hz	122 Hz	244 Hz	610 Hz	732 Hz

Caution: For details on the register setup procedures, refer to RL78/G12 User's Manual: Hardware.

Setting up channel 0 operation mode

- Timer mode register 00 (TMR00)
  Select an operation clock (f_{MCK}).
  Select a count clock.
  Select the software trigger start.
  Set up the operation mode.

Symbol: TMR00

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CKS001	CKS000	0	CCS00	0	STS002	STS001	STS000	CIS001	CIS000	0	0	MD003	MD002	MD001	MD000
0	**0**	0	**0**	0	**0**	**0**	**0**	**0**	**0**	0	0	**0**	**0**	**0**	**0**

Bits 15 and 14

CKS001	CKS000	Channel 0 operation clock (f_{MCK}) selection
0	**0**	**Operation clock CK00 set by timer clock select register 0 (TPS0)**
0	1	**Operation clock CK02 set by timer clock select register 0 (TPS0)**
1	0	**Operation clock CK01 set by timer clock select register 0 (TPS0)**
1	1	**Operation clock CK03 set by timer clock select register 0 (TPS0)**

Bit 12

CCS00	Channel 0 count clock (f_{TCLK}) selection
0	**Operation clock (f_{MCK}) specified by the CKS000 and CKS001 bits**
1	Valid edge of input signal input from the TI00 pin

Bit 11

MASTER00	Selection between using channel 0 independently or simultaneously with another channel (as a slave or master)
0	**Operates in independent channel operation function or as slave channel in simultaneous channel operation function.**
1	**Operates as master channel in simultaneous channel operation function.**

Caution: For details on the register setup procedures, refer to RL78/G12 User's Manual: Hardware.

Symbol: TMR00

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CKS 001	CKS 000	0	CCS 00	0	STS 002	STS 001	STS 000	CIS0 01	CIS0 00	0	0	MD0 03	MD0 02	MD0 01	MD0 00
0	**0**	0	**0**	0	**0**	**0**	**0**	**0**	**0**	0	0	**0**	**0**	**0**	**0**

Bits 10 to 8

STS002	STS001	STS000	Setting of start trigger or capture trigger of channel 0
0	**0**	**0**	**Only software trigger start is valid (other trigger sources are unselected).**
0	0	1	**Valid edge of the TI00 pin input is used as both the start trigger and capture trigger.**
0	1	0	Both the edges of the TI00 pin input are used as a start trigger and a capture trigger.
1	0	0	Interrupt signal of the master channel is used (when the channel is used as a slave channel with the simultaneous channel operation function).
Other than above			Setting prohibited

Bits 7 to 6

CIS001	CIS000	Selection of TI00 pin input valid edge
0	**0**	**Falling edge**
0	1	Rising edge
1	0	Both edges (when low-level width is measured) Start trigger: Falling edge, Capture trigger: Rising edge
1	1	Both edges (when high-level width is measured) Start trigger: Rising edge, Capture trigger: Falling edge

Caution: For details on the register setup procedures, refer to RL78/G12 User's Manual: Hardware.

Symbol: TMR00

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CKS 001	CKS 000	0	CCS 00	0	STS 002	STS 001	STS 000	CIS0 01	CIS0 00	0	0	MD0 03	MD0 02	MD0 01	MD0 00
0	**0**	0	**0**	0	**0**	**0**	**0**	**0**	**0**	0	0	**0**	**0**	**0**	**0**

Bits 3 to 0

MD0 03	MD0 02	MD0 01	MD0 00	Operation mode of channel 0	Related function	TCR counting operation
0	**0**	**0**	1/**0**	**Interval timer mode**	**Interval timer / Square wave output / Divider function / PWM output (master)**	**Counting down**
0	1	0	1/0	Capture mode	Input pulse interval measurement	Counting up
0	1	1	0	Event counter mode	External event counter	Counting down
1	0	0	1/0	One-count mode	Delay counter / One-shot pulse output / PWM output (slave)	Counting down
1	1	0	0	Capture & one-count mode	Measurement of high-/low-level width of input signal	Counting up
Other than above				Setting prohibited		

The MD000 bit operation varies depending on the operation mode (see the table below)

Operation mode (selected with MD003 to MD001) (See the table above)	MD000	TCR counting operation
• **Interval timer mode (0, 0, 0)** • **Capture mode (0, 1, 0)**	**0**	**Timer interrupt is not generated when counting is started (timer output does not change, either).**
	1	Timer interrupt is generated when counting is started (timer output also changes).
• Event counter mode (0, 1, 1)	0	Timer interrupt is not generated when counting is started (timer output does not change, either).
• One-count mode (1, 0, 0)	0	Start trigger is invalid during counting operation. At that time, interrupt is not generated, either.
	1	Start trigger is valid during counting operation. At that time, interrupt is also generated.
• Capture/one-count mode (1, 1, 0)	0	Timer interrupt is not generated when counting is started (timer output does not change, either). Start trigger is invalid during counting operation. At that time, interrupt is not generated, either.
Other than above		Setting prohibited

Caution: For details on the register setup procedures, refer to RL78/G12 User's Manual: Hardware.

Configuring the interval timer cycle time

- Timer data register 00 (TDR00)
  Configure the interval timer compare value.

Symbol: TDR00

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Timer interrupt (INTTM00) occurrence = (TDR00 setting + 1) × Count clock cycle time

Enabling the timer output

- Timer output enable register 0 (TOE0)
  Enable/disable the timer output for each channel.

Symbol: TOE0

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	TOE03	TOE02	TOE01	TOE00
0	0	0	0	0	0	0	0	0	0	0	0	x	x	x	**0**

Bit 0

TOE00	Timer output enable/disable of channel 0
0	**The TO00 operation stopped by count operation (timer channel output bit).** **Writing to the TO00 bit is enabled.** **The TO00 pin function as data output, and it outputs the level set to the TO00 bit.** **The output level of the TO00 pin can be manipulated be software.**
1	The TO00 operation enabled by count operation (timer channel output bit). **Writing to the TO00 bit is disabled (writing is ignored).** **The TO00 pin functions as timer output, and the TOE00 bit is set or reset depending on the timer operation.** **The TO00 pin outputs the square-wave or PWM depending on the timer operation.**

Caution: For details on the register setup procedures, refer to RL78/G12 User's Manual: Hardware.

5.7.6 INTP0 Initialization

Figure 5.7 shows the flowchart for INTP0 initialization.

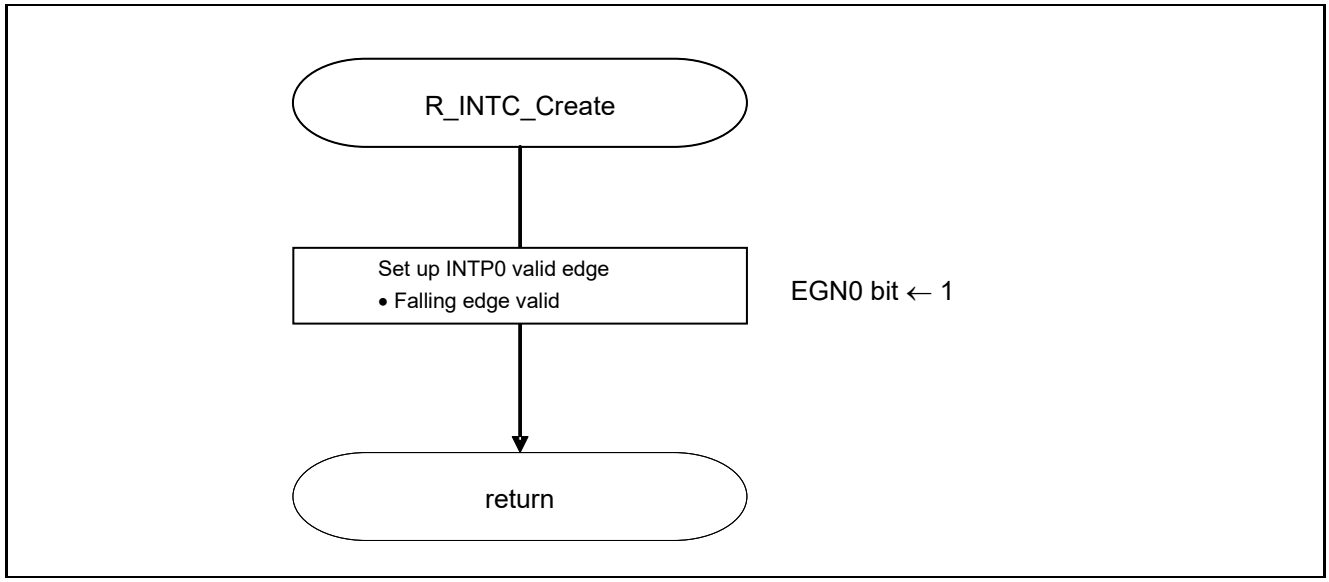


Figure 5.7 INTC Module Setup

Setup for INTP0 pin edge detection

- External interrupt rising edge enable register (EGP0)
- External interrupt falling edge enable register (EGN0)
  Select a valid edge for INTP0

Symbol: EGP0

7	6	5	4	3	2	1	0
0	0	0	0	EGP3	EGP2	EGP1	EGP0
0	0	0	0	x	x	x	**0**

Symbol: EGN0

7	6	5	4	3	2	1	0
0	0	EGN5	EGN4	EGN3	EGN2	EGN1	EGN0
0	0	x	x	x	x	x	**1**

EGP0	EGN0	INTP0 pin valid edge selection
0	0	Edge detection disabled.
0	**1**	**Falling edge**
1	0	Rising edge
1	1	Both rising and falling edges

Caution: For details on the register setup procedures, refer to RL78/G12 User's Manual: Hardware.

5.7.7 Main Processing

Figure 5.8 shows the flowchart for main processing.

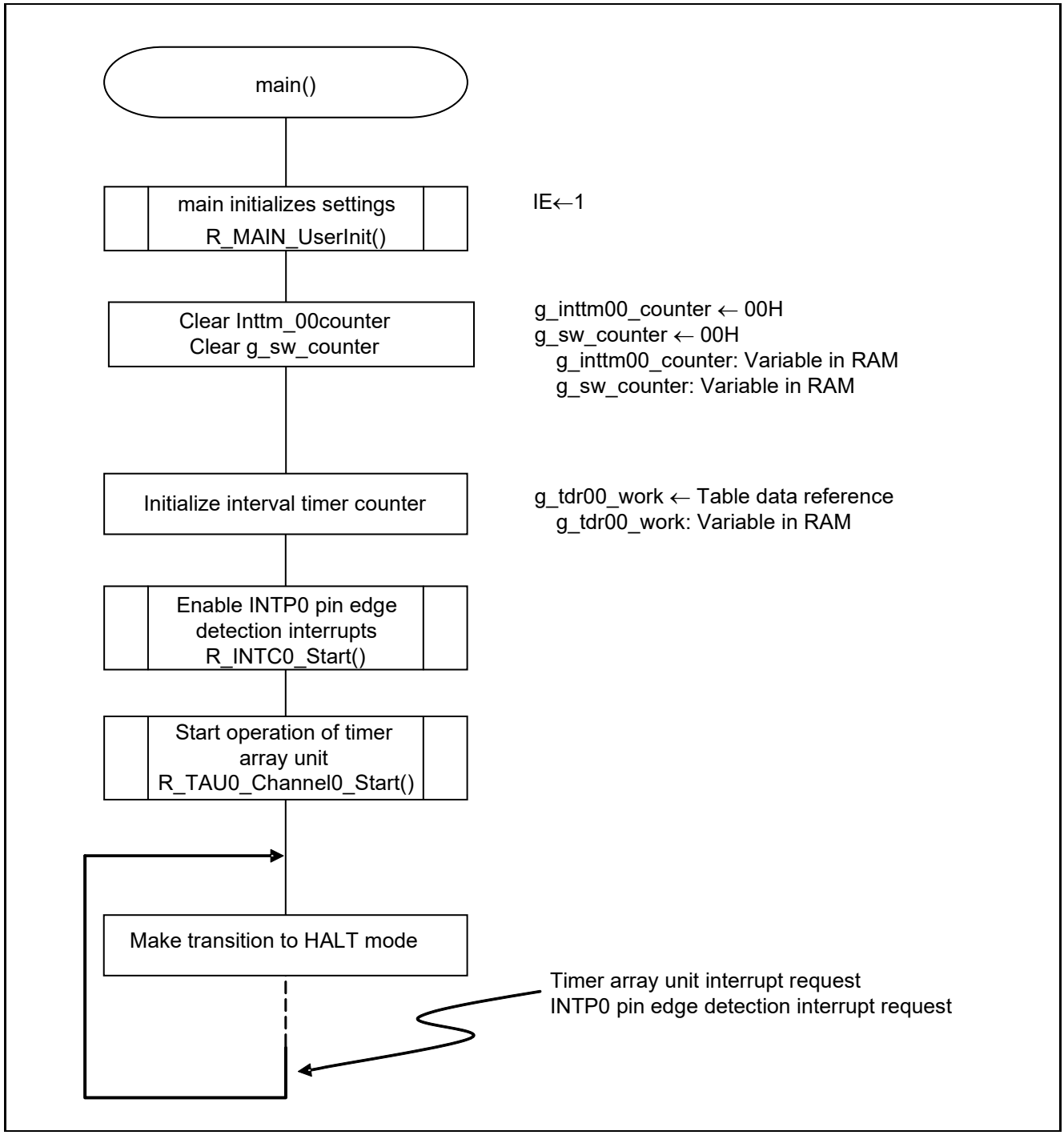


Figure 5.8 Main Processing

5.7.8 Main initializes settings

Figure 5.9 shows the flowchart for the main initializes settings.

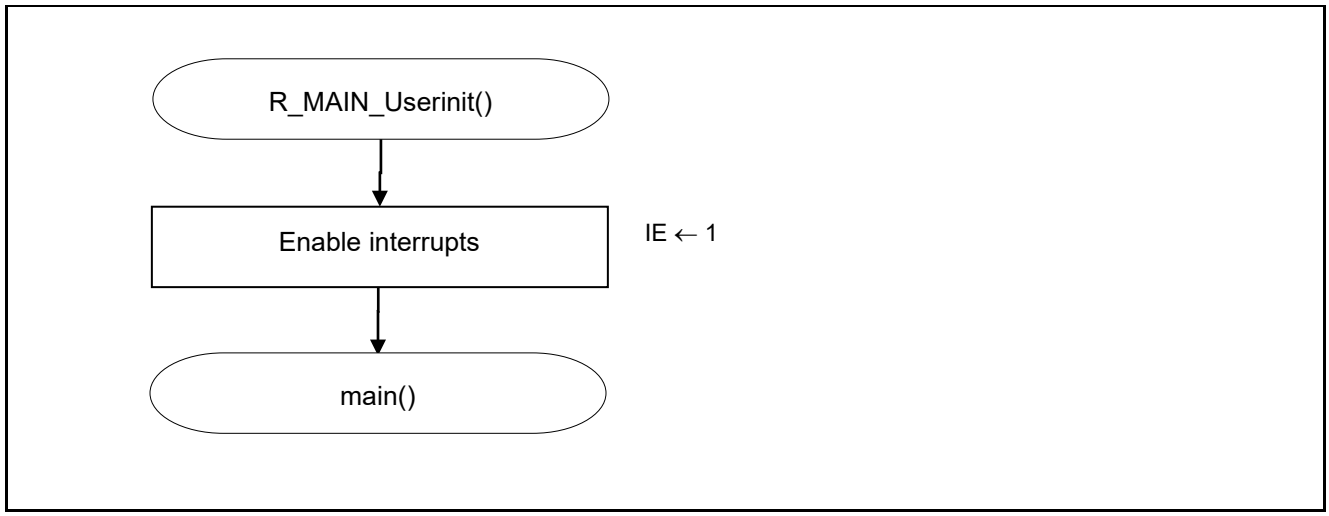


Figure 5.9 Main initializes settings

5.7.9 INTP0 Operation Start

Figure 5.10 shows the flowchart for starting INTP0 operation.

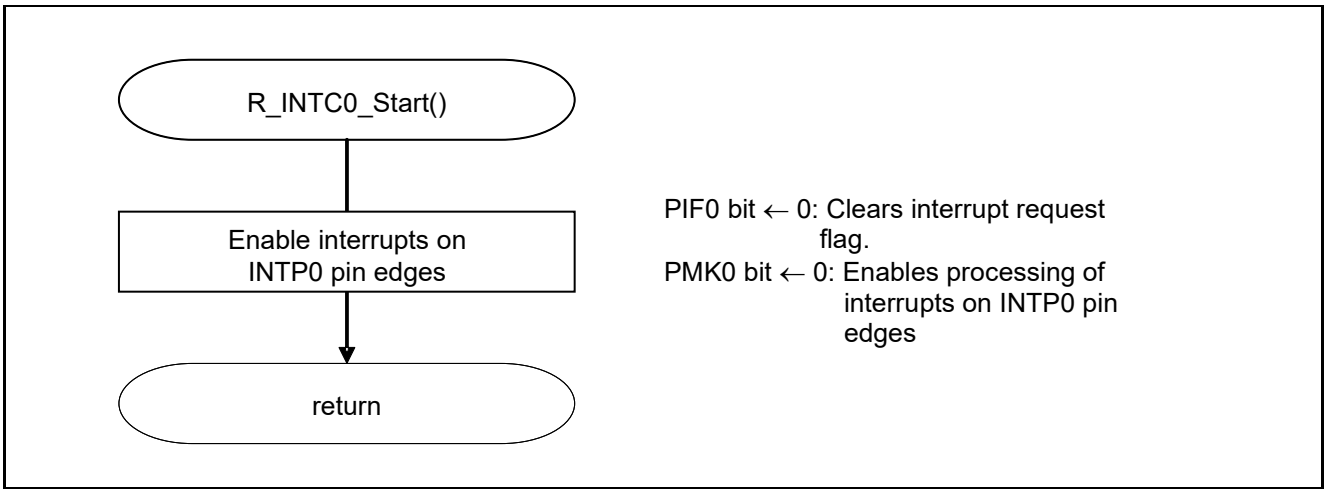


Figure 5.10 INTP0 Operation Start

Setup for INTP0 Interrupts

- Interrupt request flag register (IF0L)
  Clear interrupt request flag.
- Interrupt mask flag register (MK0L)
  Clear interrupt mask.

Symbol: IF0L

7	6	5	4	3	2	1	0
DMAIF1	DMAIF0	PIF3	PIF2	PIF1	PIF0	LVIIF	WDTIIF
x	x	x	x	x	**0**	x	x

Bit 2

PIF0	Interrupt request flag
0	**No interrupt request signal is generated**
1	Interrupt request is generated, interrupt request status

Symbol: MK0L

7	6	5	4	3	2	1	0
DMAMK1	DMAMK0	PMK3	PMK2	PMK1	PMK0	LVIMK	WDTIMK
x	x	x	x	x	**0**	x	x

Bit 2

PMK0	Interrupt processing control
0	**Enables interrupt processing.**
1	Disables interrupt processing.

Caution: For detailed information about setting the registers, see RL78/G12 User's Manual: Hardware.

5.7.10 Timer Array Unit 0 Operation Start

Figure 5.11 shows the flowchart for starting timer array unit operation.

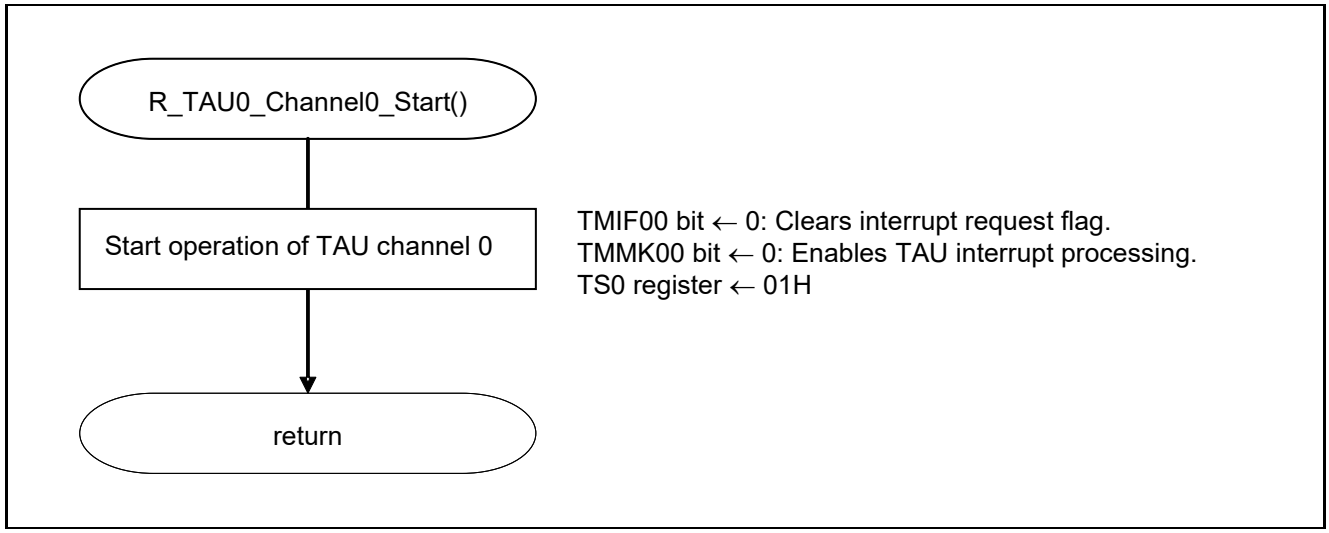


Figure 5.11 Timer Array Unit 0 Operation Start

Configuring the timer interrupt

- Interrupt request flag register (IF0H)
  Clear the interrupt request flag.
- Interrupt mask flag register (MK0H)
  Enable interrupt processing.

Symbol: IF0H

7	6	5	4	3	2	1	0
TMIF01	TMIF00	IICAIF0	TMIF03H	TMIF01H	SREIF0	SRIF0 CSIIF01 IICIF01	STIF0 CSIIF00 IICIF00
x	x	x	**0**	x	x	x	x

Bit 4

TMIF00	Interrupt request flag
0	**No interrupt request signal is generated.**
1	Interrupt request is generated, interrupt request status

Symbol: MK0H

7	6	5	4	3	2	1	0
TMMK01	TMMK00	IICAMK0	TMMK03H	TMMK01H	SREMK0	SRMK0 CSIMK01 IICMK01	STMK0 CSIMK00 IICMK00
x	x	x	**0**	x	x	x	x

Bit 4

TMMK00	Interrupt processing control
0	**Enables interrupt processing.**
1	Disables interrupt processing.

Caution: For details on the register setup procedures, refer to RL78/G12 User's Manual: Hardware.

5.7.11 INTTM00 Interrupt Processing

Figure 5.12 shows the flowchart for INTTM00 interrupt processing.

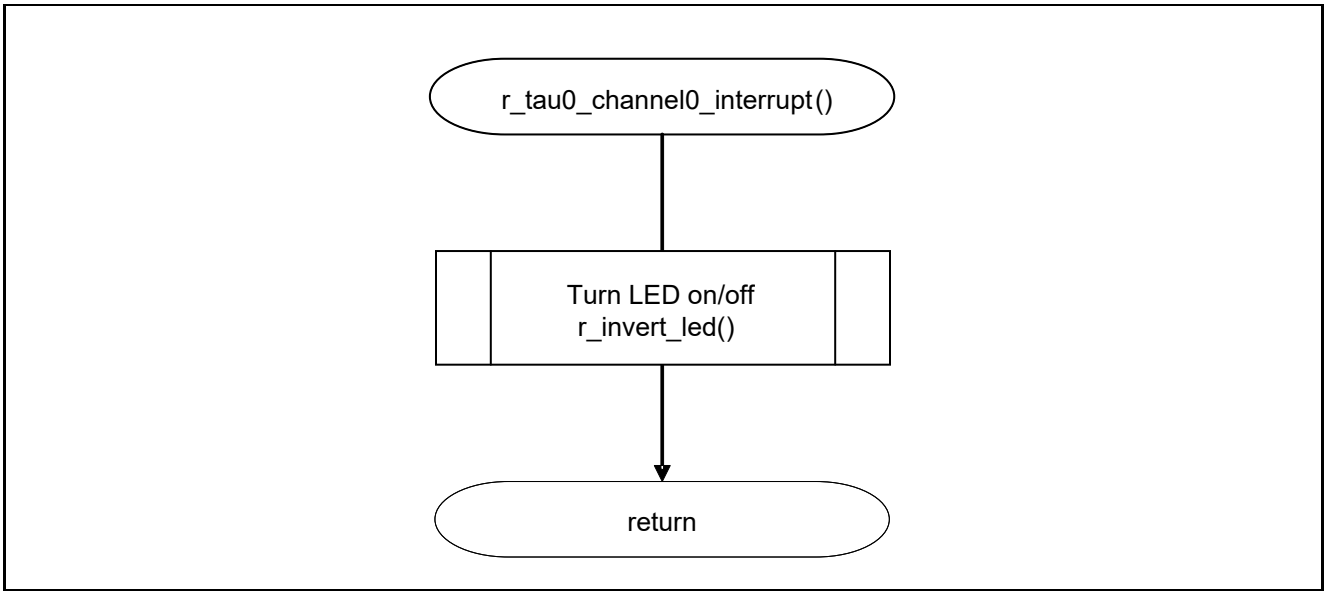


Figure 5.12 INTTM00 Interrupt Processing

5.7.12 LED Turn-On/Off Processing

Figure 5.13 shows the flowchart for LED turn-on/off processing.

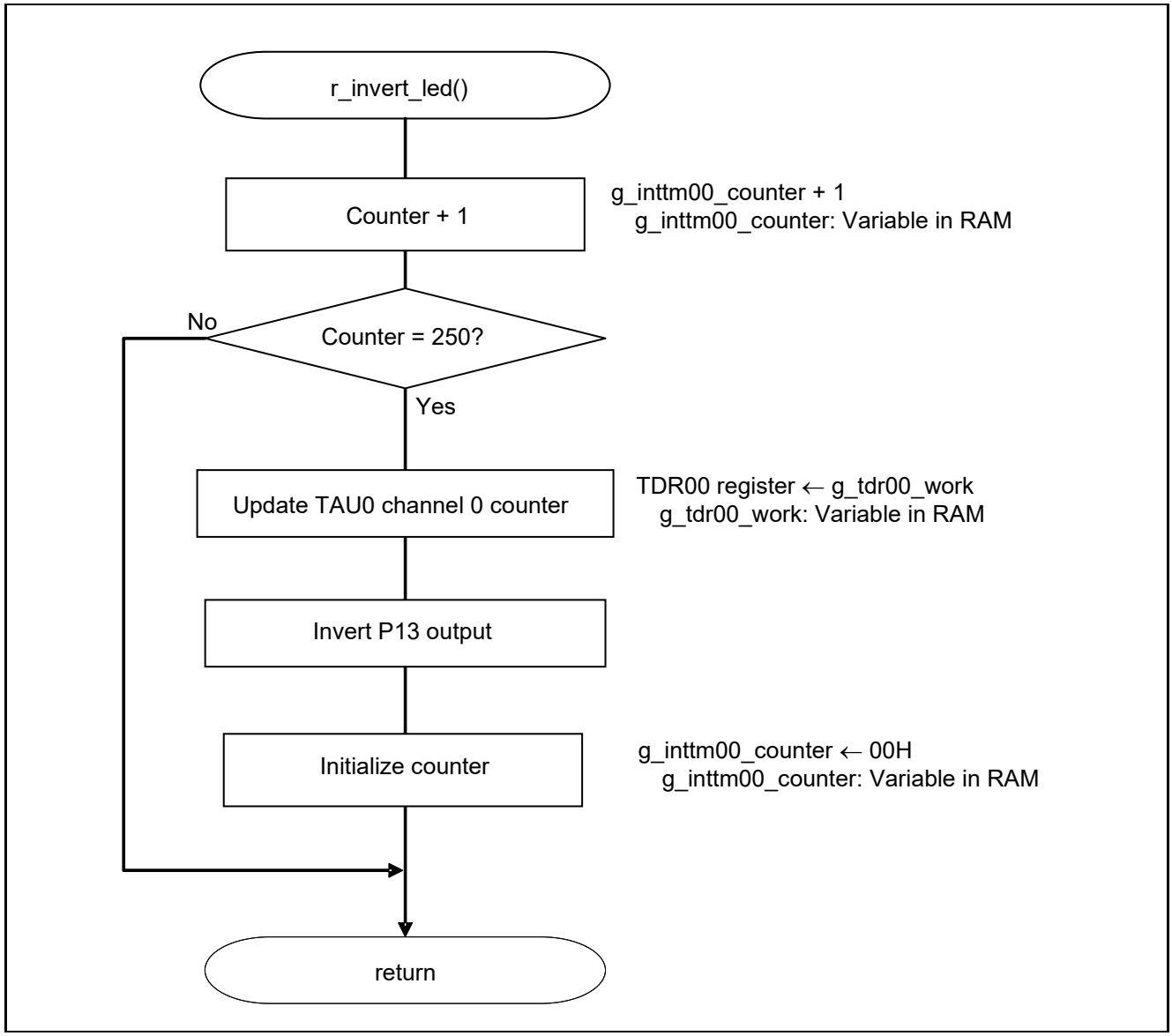


Figure 5.13 Checking Whether 666 ms Have Elapsed

5.7.13 INTP0 Interrupt Processing

Figures 5.14 and 5.15 show the flowchart for INTP0 interrupt processing.

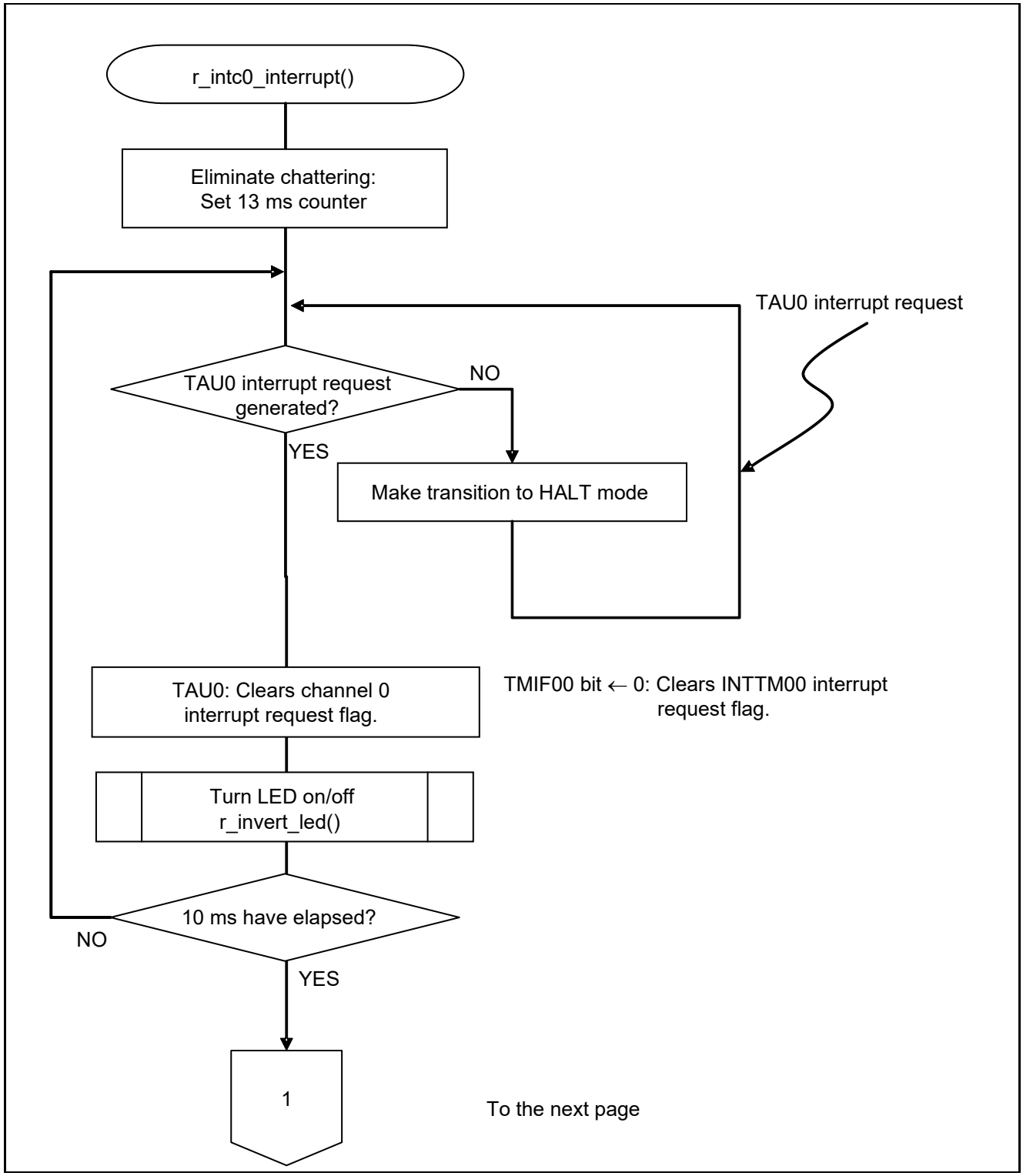


Figure 5.14 INTP0 Interrupt Processing (1/2)

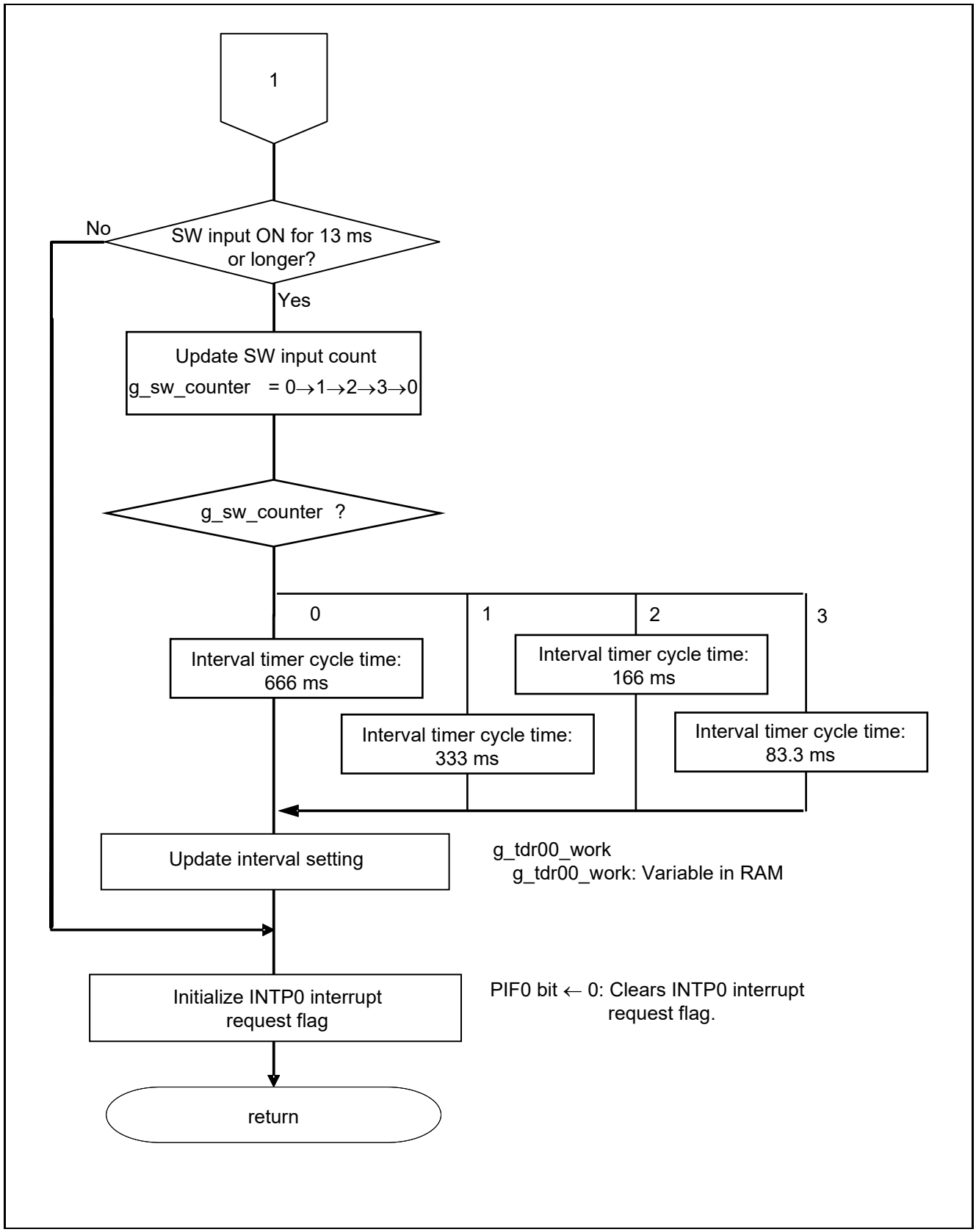


Figure 5.15 INTP0 Interrupt Processing (2/2)

6. Sample Code

The sample code is available on the Renesas Electronics Website.

7. Documents for Reference

User's Manual:

RL78/G12 User's Manual: Hardware (R01UH0200E)
RL78 Family User's Manual: Software (R01US0015E)
The latest version can be downloaded from the Renesas Electronics website.

Technical Updates/Technical News

The latest information can be downloaded from the Renesas Electronics website.

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Revision History

Rev.	Date	Description	
		Page	Summary
1.00	May 31, 2017	—	First edition issued
1.10	May 11 2022	4	Updated Figure 1.1
		5	Updated 4. Operation Check Conditions
		7	Updated 5.1 Operation Outline
		8	Updated 5.3List of Constants
		10	Updated description of r_intc0_interrupt
		29	Update Figure 5.13
		30	Update Figure 5.14
		31	Update Figure 5.15

General Precautions in the Handling of Microprocessing Unit and Microcontroller Unit Products

The following usage notes are applicable to all Microprocessing unit and Microcontroller unit products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Precaution against Electrostatic Discharge (ESD)

   A strong electrical field, when exposed to a CMOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop the generation of static electricity as much as possible, and quickly dissipate it when it occurs. Environmental control must be adequate. When it is dry, a humidifier should be used. This is recommended to avoid using insulators that can easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors must be grounded. The operator must also be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions must be taken for printed circuit boards with mounted semiconductor devices.

2. Processing at power-on

   The state of the product is undefined at the time when power is supplied. The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the time when power is supplied. In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the time when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the time when power is supplied until the power reaches the level at which resetting is specified.

3. Input of signal during power-off state

   Do not input signals or an I/O pull-up power supply while the device is powered off. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Follow the guideline for input signal during power-off state as described in your product documentation.

4. Handling of unused pins

   Handle unused pins in accordance with the directions given under handling of unused pins in the manual. The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of the LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible.

5. Clock signals

   After applying a reset, only release the reset line after the operating clock signal becomes stable. When switching the clock signal during program execution, wait until the target clock signal is stabilized. When the clock signal is generated with an external resonator or from an external oscillator during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Additionally, when switching to a clock signal produced with an external resonator or by an external oscillator while program execution is in progress, wait until the target clock signal is stable.

6. Voltage application waveform at input pin

   Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between V_{IL} (Max.) and V_{IH} (Min.) due to noise, for example, the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between V_{IL} (Max.) and V_{IH} (Min.).

7. Prohibition of access to reserved addresses

   Access to reserved addresses is prohibited. The reserved addresses are provided for possible future expansion of functions. Do not access these addresses as the correct operation of the LSI is not guaranteed.

8. Differences between products

   Before changing from one product to another, for example to a product with a different part number, confirm that the change will not lead to problems. The characteristics of a microprocessing unit or microcontroller unit products in the same group but having a different part number might differ in terms of internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

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