RL78/G12

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Serial Interface IICA (for Slave Transmission/Reception) CC-RL

Introduction

This application note describes slave transmission and reception implemented via the serial interface IICA. Using IICA, the single master system described here performs slave operation (address reception and data transmission/reception).

Target Device

RL78/G12

When applying the sample program covered in this application note to another microcomputer, modify the program according to the specifications for the target microcomputer and conduct an extensive evaluation of the modified program.

Contents

1. Specifications

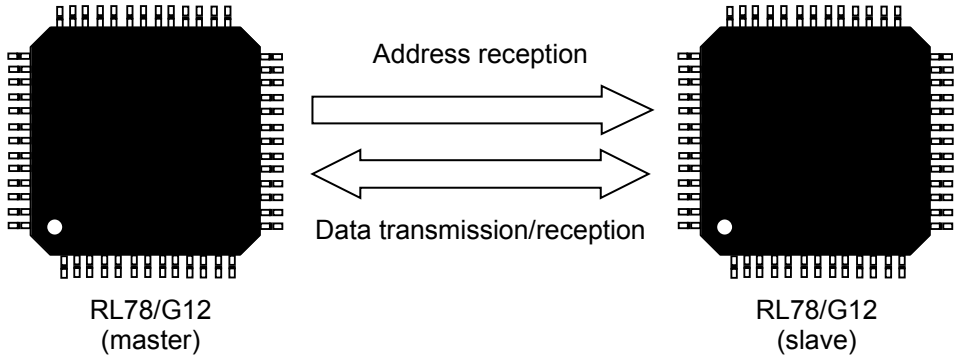
This application note describes how the single master system performs slave transmission and reception (address reception and data transmission/reception) through the serial interface IICA.

Table 1.1 lists the peripheral function to be used and its use. Figure 1.1 presents an overview of IIC communication.

Figures 1.2 to 1.8 show timing charts for explaining the IIC communication.

Table 1.1 Peripheral Function to be Used and Its Use

Peripheral Function	Use
Serial interface IICA	IIC slave transmission/reception in a single master system (using the SCLA0 and SDAA0 pins)



Address reception: Each device connected to the IIC bus has a unique address. Each device receives the address of a transfer destination (slave) from the master. That is, it receives one byte of data consisting of 7 bits (indicating the address) and 1 bit (indicating the transfer direction). The slave generates an acknowledgement after receiving one byte of data.
Data transmission/reception: The slave sends/receives data to/from the master after receiving the address.

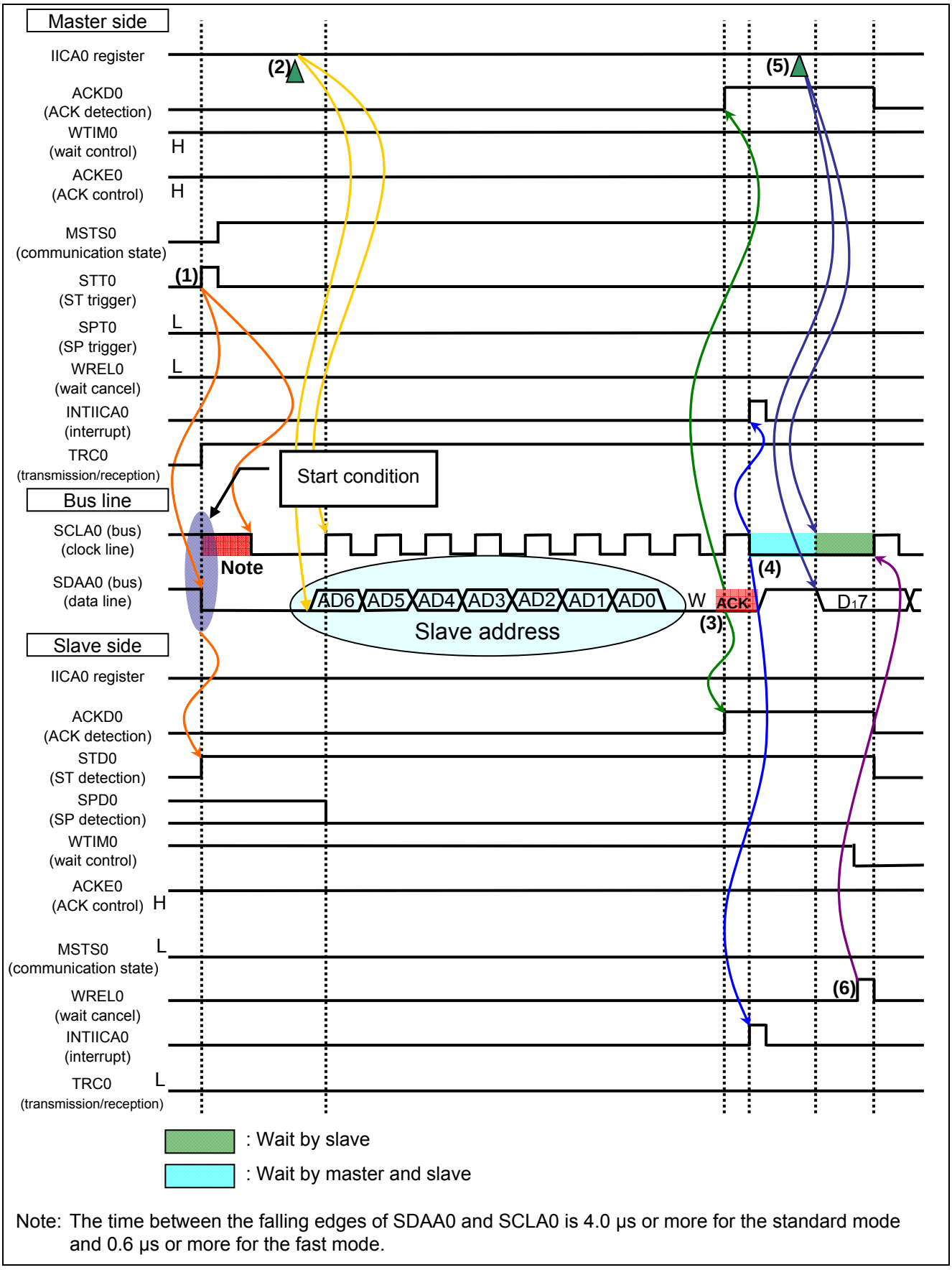
Figure 1.1 Overview of IIC Communication

1.1 Specifications of Communication as Slave

This slave program includes a 16-byte data buffer. When communication starts, this program stores/reads data in/from the start of the data buffer. After 16 bytes or more of data is transmitted from the master, the 17th data byte is stored in/read from the start of the data buffer. This program performs ACK response to data transmission from the master. After data reception, set bit 4 of all the data in the data buffer in preparation for next communication.

Remark: For reference, the subsequent pages show the examples of IIC bus operation.

(1) Master-to-slave communication 1 (start condition – address – data)



Note: The time between the falling edges of SDAA0 and SCLA0 is 4.0 µs or more for the standard mode and 0.6 µs or more for the fast mode.

Figure 1.2 IIC Communication Timing Chart (Master-to-Slave Communication Example) (1/4)

(1) The start condition trigger is set (STT0 = 1) on the master side. Then, the SDAA0 line falls, thereby generating a start condition. Later, when the start condition is detected (STD0 = 1), the master enters a master device communication state (MSTS0 = 1). The SCLA0 line falls at the end of the hold period. This completes preparations for communication.

(2) The values of the address and data direction bit W (transmission) are written to the IICA0 register on the master side. Then, the slave address is transmitted.

(3) If the received address and slave address match [Note], the slave hardware sends ACK0 to the master. When the ninth clock signal rises, the master detects ACK (ACKD0 = 1).

(4) When the ninth clock signal falls, an address transmission end interrupt (INTIICA0) occurs on the master side. If the addresses match, an address match interrupt (INTIICA0) occurs on the slave side. Both the master and the slave which has the matching address enter a wait state (SCLA0 line: Low) [Note].

(5) The master writes transmit data to the IICA0 register and cancels the wait.

(6) The slave selects an 8-clock wait (WTIM0 = 0) because it receives data. When the slave cancels the wait (WREL0 = 1), the master starts transferring data to the slave.

Note: If the received address and local address do not match, the slave does not return ACK to the master (NACK). The INTIICA0 interrupt (address match interrupt) does not occur on the slave side and thus the slave does not enter a wait state. However, the INTIICA0 interrupt (address transmission end interrupt) occurs on the master side regardless of whether the master receives ACK or NACK.

(2) Master-to-slave communication 2 (address – data – data)

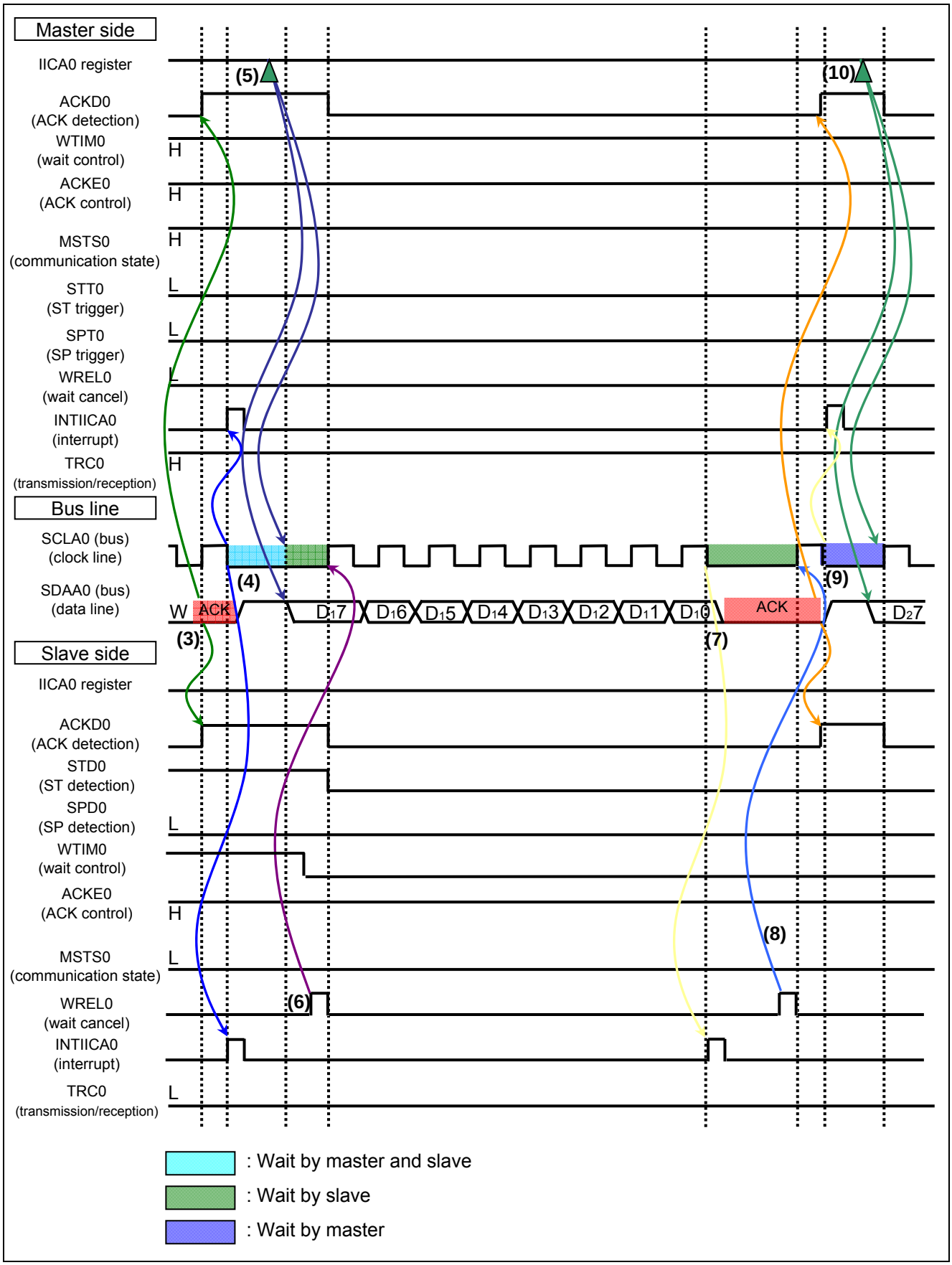


Figure 1.1 IIC Communication Timing Chart (Master-to-Slave Communication Example) (2/4)

(3) If the received address and slave address match [Note], the slave hardware sends ACK to the master. When the ninth clock signal rises, the master detects ACK (ACKD0 = 1).

(4) When the ninth clock signal falls, an address transmission end interrupt (INTIICA0) occurs on the master side. If the addresses match, an address match interrupt (INTIICA0) occurs on the slave side. Both the master and the slave which has the matching address enter a wait state (SCLA0 line: Low).

(5) The master writes transmit data to the IICA0 register and cancels the wait.

(6) The slave selects an 8-clock wait (WTIM0 = 0) because it receives data. When the slave cancels the wait (WREL0 = 1), the master starts transferring data to the slave.

(7) When the eighth clock signal falls after the data transfer, the slave hardware generates a wait (SCLA0 line: Low) and a transfer end interrupt (INTIICA0) occurs on the slave side.

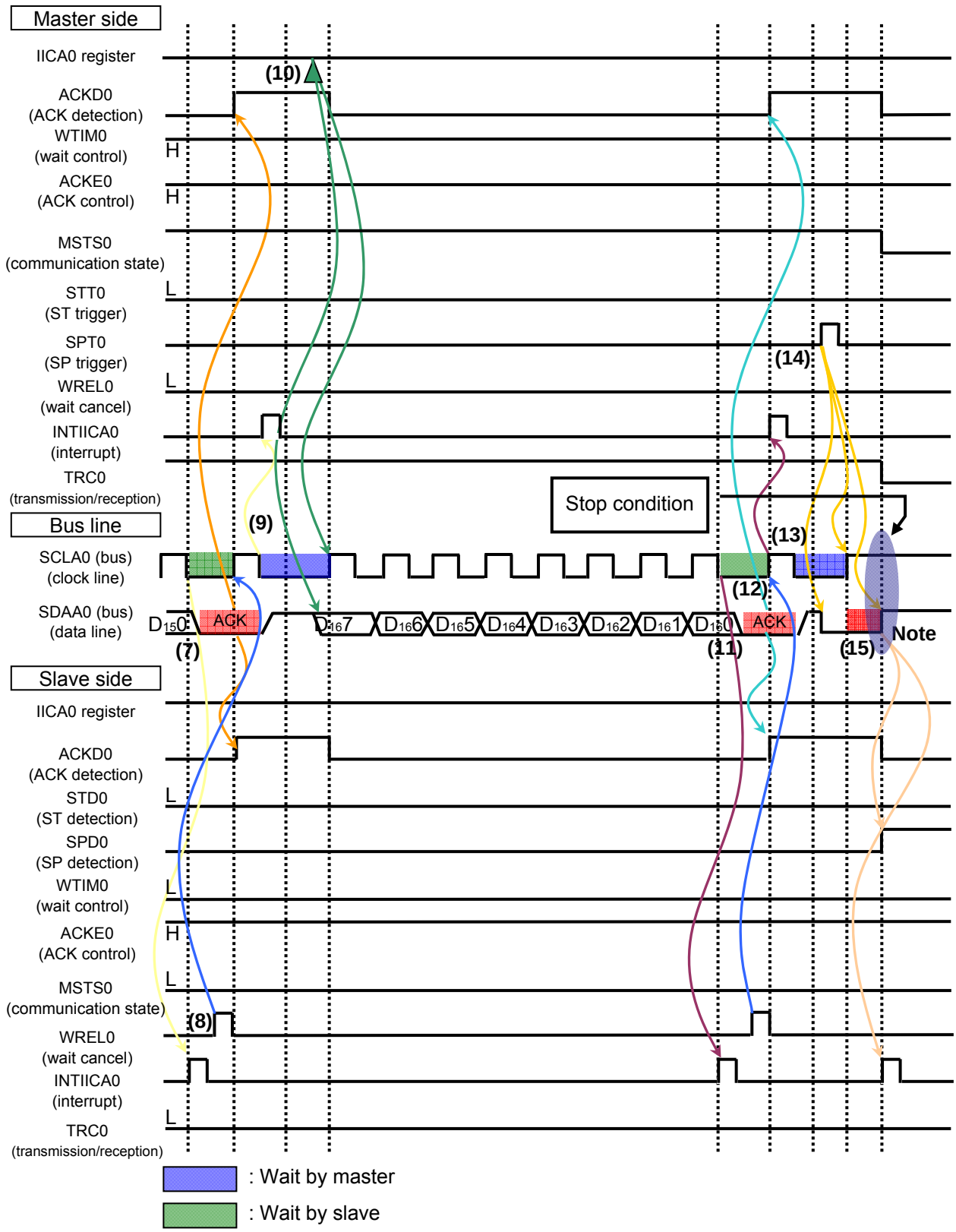
(8) When the slave reads the receive data and cancels the wait (WREL0 = 1), the slave sends ACK to the master. When the ninth clock signal rises, the master detects ACK (ACKD0 = 1).

(9) When the ninth clock signal falls, the master generates a wait (SCLA0 line: Low) and a transfer end interrupt (INTIICA0) occurs on the master side.

(10) The master writes transmit data to the IICA0 register and cancels the wait. Then, the master starts transferring data to the slave.

Note: If the received address and local address do not match, the slave does not return ACK to the master (NACK). The INTIICA0 interrupt (address match interrupt) does not occur on the slave side and thus the slave does not enter a wait state. However, the INTIICA0 interrupt (address transmission end interrupt) occurs on the master side regardless of whether the master receives ACK or NACK.

(3) Master-to-slave communication 3 (data – data – stop condition)

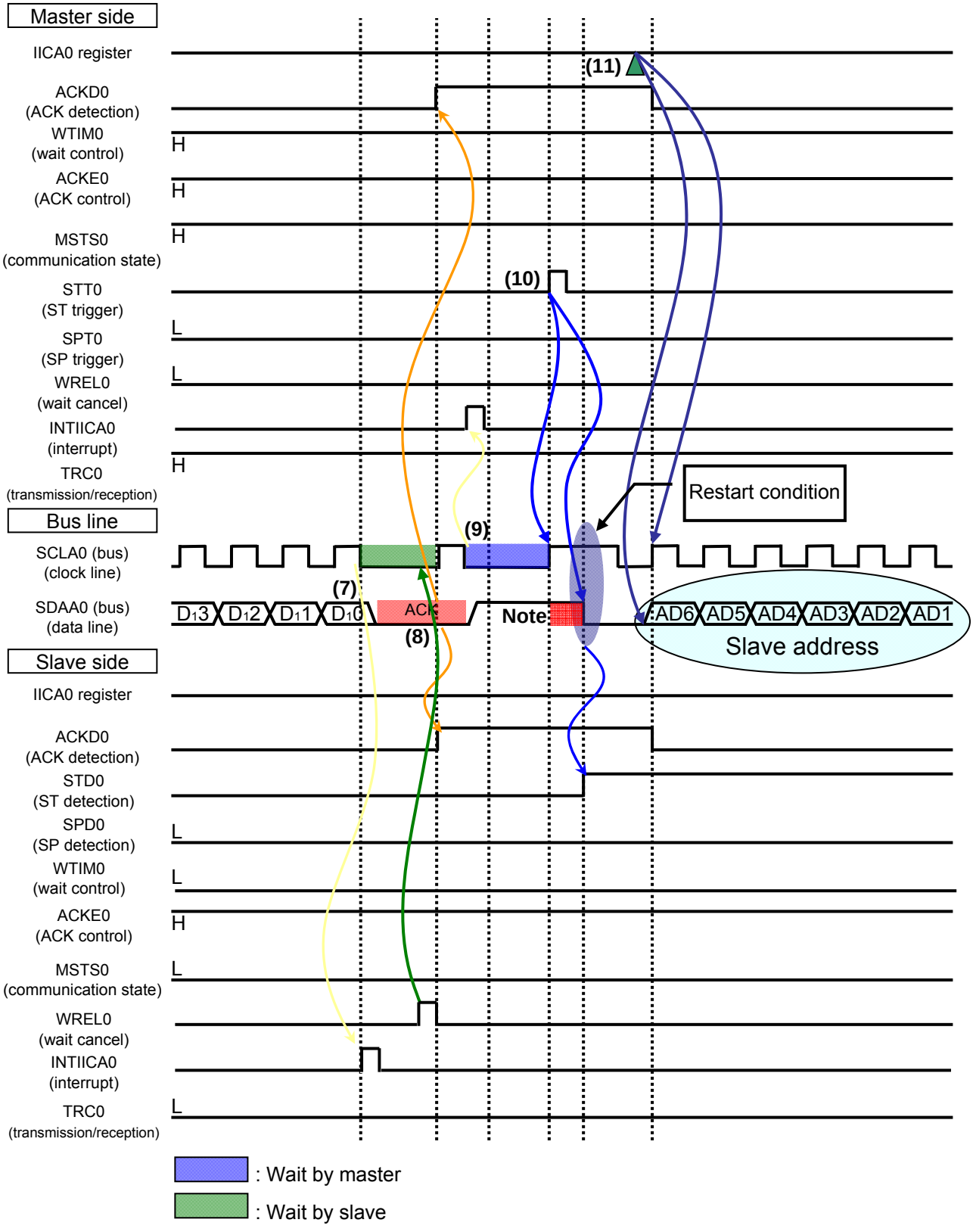


Note: The time from when SCLA0 rises after a stop condition is issued till when a stop condition is generated is 4.0 µs or more for the standard mode and 0.6 µs or more for the fast mode.

Figure 1.2 IIC Communication Timing Chart (Master-to-Slave Communication Example) (3/4)

(7) When the eighth clock signal falls after the data transfer, the slave hardware generates a wait (SCLA0 line: Low) and a transfer end interrupt (INTIICA0) occurs on the slave side.
(8) When the slave reads the receive data and cancels the wait (WREL0 = 1), the slave sends ACK to the master. When the ninth clock signal rises, the master detects ACK (ACKD0 = 1).
(9) When the ninth clock signal falls, the master generates a wait (SCLA0 line: Low) and an address transmission end interrupt (INTIICA0) occurs on the master side.
(10) The master writes transmit data to the IICA0 register and cancels the wait. Then, the master starts transferring the data to the slave.
(11) When the eighth clock signal falls after the data transfer, the slave hardware generates a wait (SCLA0 line: Low) and a transfer end interrupt (INTIICA0) occurs on the slave side.
(12) When the slave reads the receive data and cancels the wait (WREL0 = 1), the slave sends ACK to the master. When the ninth clock signal rises, the master detects ACK (ACKD0 = 1).
(13) When the ninth clock signal falls, the master generates a wait (SCLA0 line: Low) and a transfer end interrupt (INTIICA0) occurs on the master side.
(14) When the stop condition trigger is set (SPT0 = 1), the SDAA0 line falls and the SCLA0 line rises. Upon the elapse of the stop condition setup time, the SDAA0 line rises, thereby generating a stop condition.
(15) When the stop condition is generated, the slave detects it (SPD0 = 1) and an IICA0 interrupt (stop condition interrupt) occurs on the slave side.

(4) Master-to-slave communication 4 (data – restart condition – address)



Note: The time from when SCLA0 rises after a restart condition is issued till when a start condition is generated is 4.7 µs or more for the standard mode and 0.6 µs or more for the fast mode.

Figure 1.3 IIC Communication Timing Chart (Master-to-Slave Communication Example) (4/4)

(7) When the eighth clock signal falls after the data transfer, the slave hardware generates a wait (SCLA0 line: Low) and a transfer end interrupt (INTIICA0) occurs on the slave side.

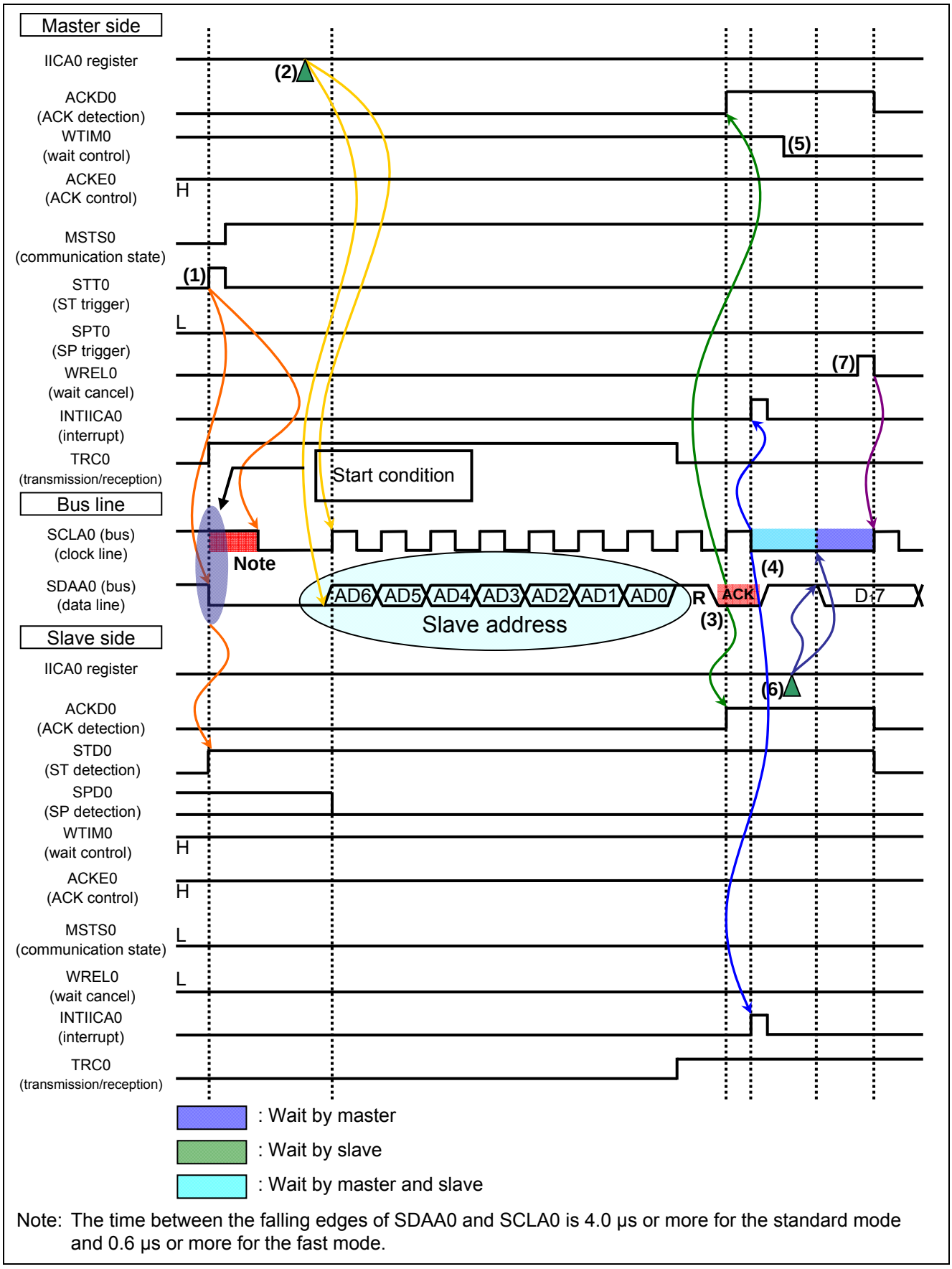
(8) The slave reads the receive data and cancels the wait (WREL0 = 1). Then, the slave sends ACK to the master. When the ninth clock signal rises, the master detects ACK (ACKD0 = 1).

(9) When the ninth clock signal falls, the master generates a wait (SCLA0 line: Low) and a transfer end interrupt (INTIICA0) occurs on the master side.

(10) The start condition trigger is set (STT0 = 1) on the master side again. Then, the SCLA0 line rises. Upon the elapse of the restart condition setup time, the SDAA0 line falls, thereby generating a start condition. Later, at the end of the hold period after the start condition is detected (STD0 = 1), the bus clock line falls, thereby completing preparations for communication.

(11) The master writes the slave address to the IICA0 register and starts transferring the address to the slave.

(5) Slave-to-master communication 1 (start condition – address – data)



Note: The time between the falling edges of SDAA0 and SCLA0 is 4.0 µs or more for the standard mode and 0.6 µs or more for the fast mode.

Figure 1.4 IIC Communication Timing Chart (Slave-to-Master Communication Example) (1/3)

(1) The start condition trigger is set (STT0 = 1) on the master side. Then, the SDAA0 line falls, thereby generating a start condition. Later, when the start condition is detected (STD0 = 1), the master enters a master device communication state (MSTS0 = 1). The SCLA0 line falls at the end of the hold period. This completes preparations for communication.
(2) The values of the address and data direction bit R (reception) are written to the IICA0 register on the master side. Then, the slave address is transmitted.
(3) If the received address and slave address match [Note], the slave hardware sends ACK to the master. When the ninth clock signal rises, the master detects ACK (ACKD0 = 1).
(4) When the ninth clock signal falls, an address transmission end interrupt (INTIICA0) occurs on the master side. If the addresses match, an address match interrupt (INTIICA0) occurs on the slave side. Both the master and the slave which has the matching address enter a wait state (SCLA0 line: Low).
(5) The master selects an 8-clock wait (WTIM0 = 0) because it receives data.
(6) The slave writes transmit data to the IICA0 register and cancels the wait.
(7) When the master cancels the wait (WREL0 = 1), the slave starts transferring data to the master.

Note: If the received address and local address do not match, the slave does not return ACK to the master (NACK). The INTIICA0 interrupt (address match interrupt) does not occur on the slave side and thus the slave does not enter a wait state. However, the INTIICA0 interrupt (address transmission end interrupt) occurs on the master side regardless of whether the master receives ACK or NACK.

(6) Slave-to-master communication 2 (address – data – data)

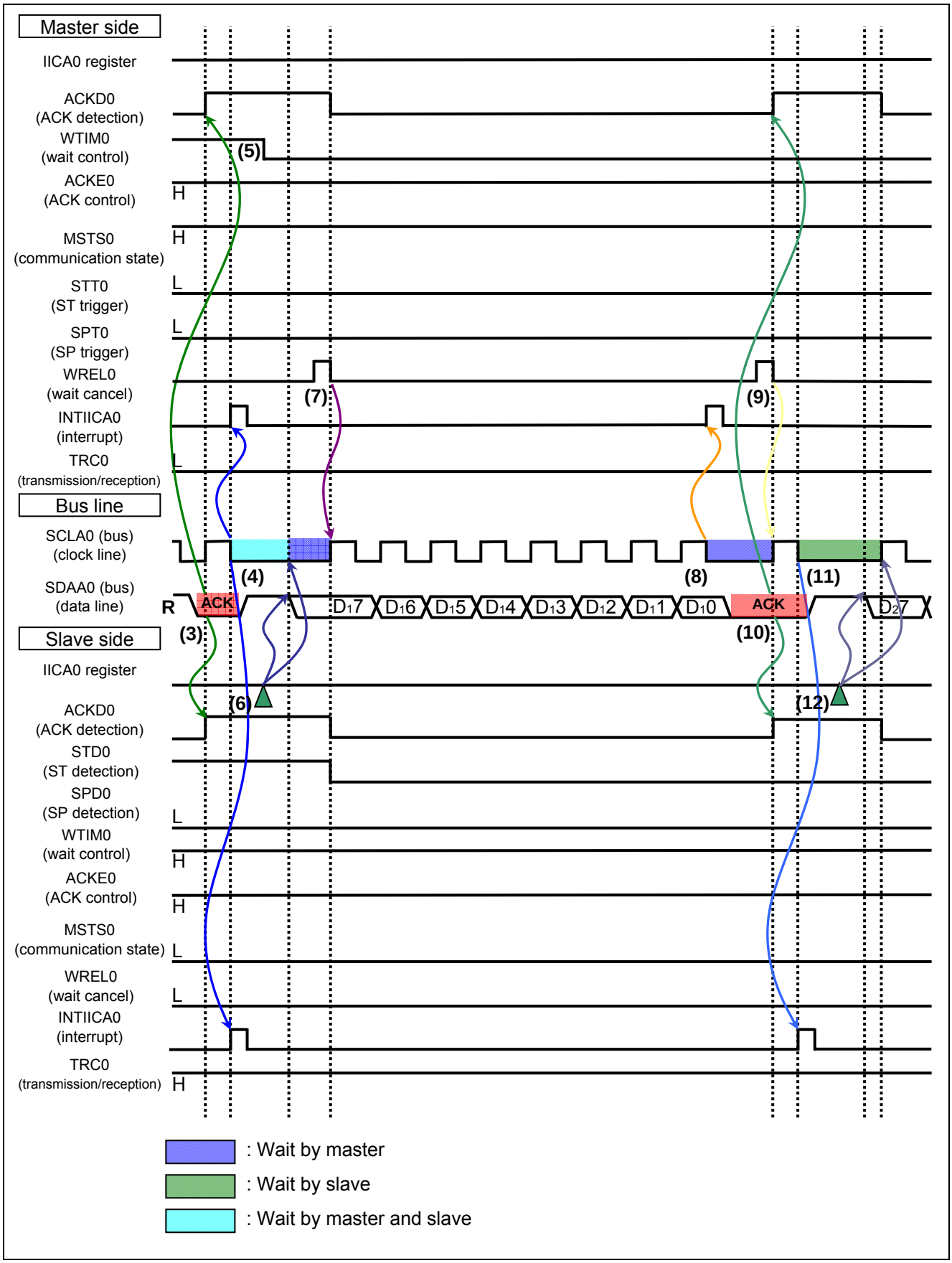
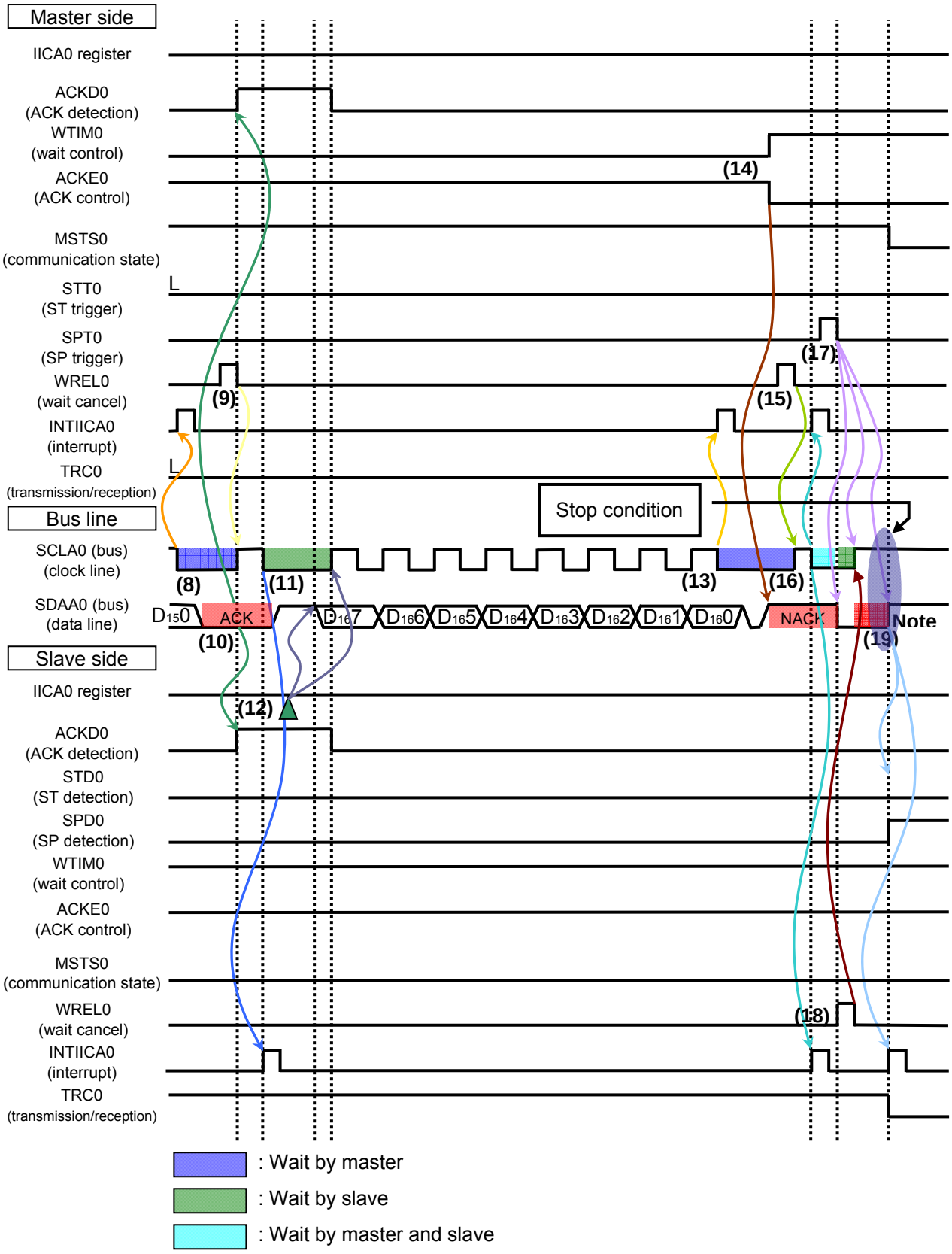


Figure 1.5 IIC Communication Timing Chart (Slave-to-Master Communication Example) (2/3)

(3) If the received address and slave address match [Note], the slave hardware sends ACK to the master. When the ninth clock signal rises, the master detects ACK (ACKD0 = 1).
(4) When the ninth clock signal falls, an address transmission end interrupt (INTIICA0) occurs on the master side. If the addresses match, an address match interrupt (INTIICA0) occurs on the slave side. Both the master and the slave which has the matching address enter a wait state (SCLA0 line: Low).
(5) The master selects an 8-clock wait (WTIM0 = 0) because it receives data.
(6) The slave writes transmit data to the IICA0 register and cancels the wait.
(7) When the master cancels the wait (WREL0 = 1), the slave starts transferring data to the master.
(8) When the eighth clock signal falls, the master generates a wait (SCLA0 line: Low) and a transfer end interrupt (INTIICA0) occurs on the master side. The master hardware sends ACK to the slave.
(9) The master reads the receive data and cancels the wait (WREL0 = 1).
(10) When the ninth clock signal rises, the slave detects ACK (ACKD0 = 1).
(11) When the ninth clock signal falls, the slave generates a wait (SCLA0 line: Low) and a transfer end interrupt (INTIICA0) occurs on the slave side.
(12) The slave writes transmit data to the IICA0 register and cancels the wait. Then, the slave starts transferring data to the master.

Note: If the received address and local address do not match, the slave does not return ACK to the master (NACK). The INTIICA0 interrupt (address match interrupt) does not occur on the slave side and thus the slave does not enter a wait state. However, the INTIICA0 interrupt (address transmission end interrupt) occurs on the master side regardless of whether the master receives ACK or NACK.

(7) Slave-to-master communication 3 (data – data – stop condition)



Note: The time from when SCLA0 rises after a stop condition is issued till when a stop condition is generated is 4.0 µs or more for the standard mode and 0.6 µs or more for the fast mode.

Figure 1.6 IIC Communication Timing Chart (Slave-to-Master Communication Example) (3/3)

(8) When the eighth clock signal falls, the master generates a wait (SCLA0 line: Low) and a transfer end interrupt (INTIICA0) occurs on the master side. The master hardware sends ACK to the slave.
(9) The master reads the receive data and cancels the wait (WREL0 = 1).
(10) When the ninth clock signal rises, the slave detects ACK (ACKD0 = 1).
(11) When the ninth clock signal falls, the slave generates a wait (SCLA0 line: Low) and a transfer end interrupt (INTIICA0) occurs on the slave side.
(12) The slave writes transmit data to the IICA0 register and cancels the wait. Then, the slave starts transferring data to the master.
(13) When the eighth clock signal falls, a transfer end interrupt (INTIICA0) occurs on the master side and the master generates a wait (SCLA0 line: Low). The master hardware sends ACK to the slave.
(14) The master sets a NACK response (ACKE0 = 0) to inform the slave that the master has sent the last data (at the end of communication). Then, the master changes the wait time to 9 clock periods (WTIM0 = 1).
(15) After the master cancels the wait (WREL0 = 1), the slave detects NACK (ACKD0 = 0) at the rising edge of the ninth clock signal.
(16) When the ninth clock signal falls, the master and slave generate a wait (SCLA0 line: Low) and a transfer end interrupt (INTIICA0) occurs on the master and slave sides.
(17) When the master issues a stop condition (SPT0 = 1), the SDAA0 line falls, thereby canceling the wait on the master side. Later, the master waits until the SCLA0 line rises.
(18) The slave cancels the wait (WREL0 = 1) to terminate communication. Then, the SCLA0 line rises.
(19) The master confirms that the SCLA0 line has risen. Upon the elapse of the stop condition setup time after this confirmation, the master makes the SDAA0 line rise and issues a stop condition. When the stop condition is generated, the slave detects the stop condition (SPD0 = 1) and a stop condition interrupt (INTIICA0) occurs on the master and slave sides.

2. Operation Check Conditions

The sample code contained in this application note has been checked under the conditions listed in the table below.

Table 2.1 Operation Check Conditions

Item	Description
Microcontroller used	RL78/G12 (R5F1026A)
Operating frequency	• High-speed on-chip oscillator (HOCO) clock: 24 MHz • CPU/peripheral hardware clock: 24 MHz
Operating voltage	5.0 V (Operation is possible over a voltage range of 2.9 V to 5.5 V.) LVD operation (V_{LVD}): Reset mode which uses 2.81 V (2.76 V to 2.87 V)
Integrated development environment (CS+)	CS+ for CC V3.01.00 from Renesas Electronics Corp.
Assembler (CS+)	CC-RL V1.01.00 from Renesas Electronics Corp.
Integrated development environment (e^2 studio)	e^2 studio V4.0.2.008 from Renesas Electronics Corp.
Assembler (e^2 studio)	CC-RL V1.01.00 from Renesas Electronics Corp.
Board to be used	RL78/G12 target board (QB-R5F1026A-TB)

3. Related Application Notes

The application notes that are related to this application note are listed below for reference.

RL78/G12 Initialization (R01AN2582E) Application Note
RL78/G12 Serial Interface IICA (for Master Transmission/Reception) (R01AN2987E) Application Note

4. Description of the Hardware

4.1 Hardware Configuration Example

Figure 4.1 shows an example of hardware configuration that is used for this application note.

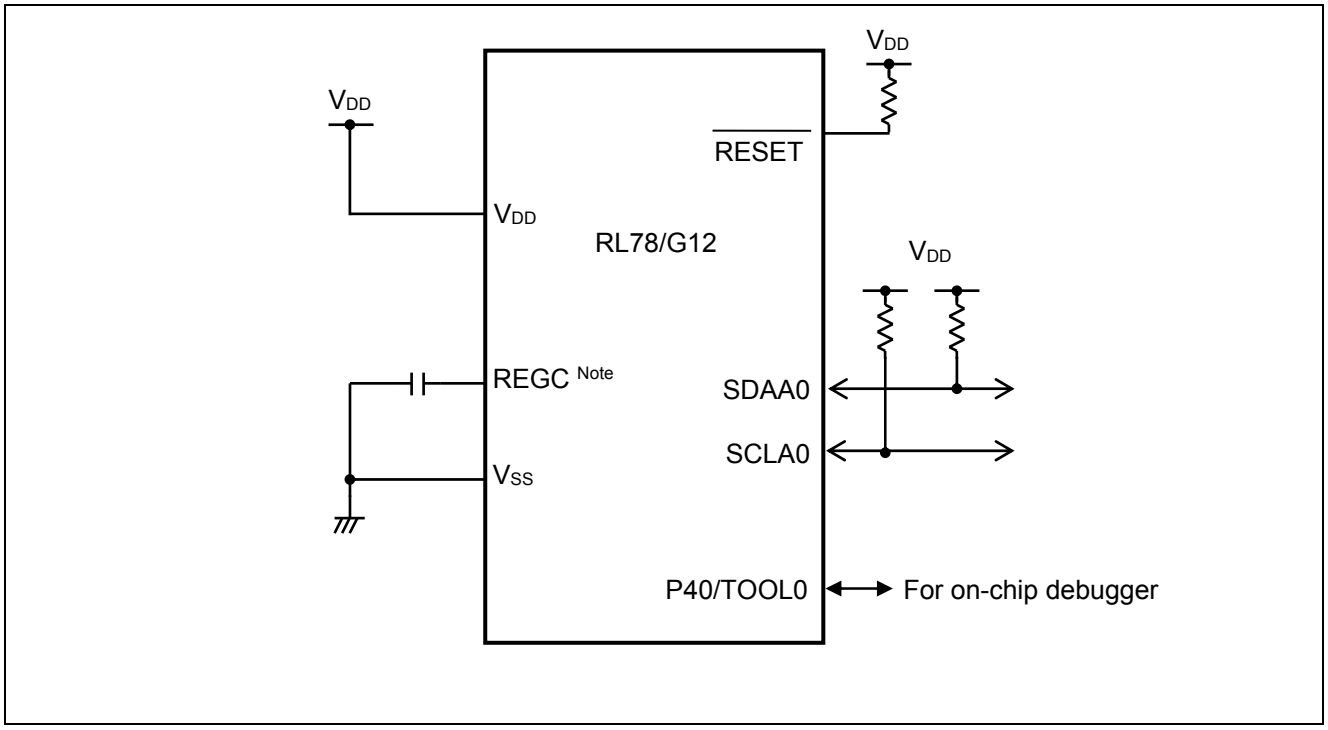


Figure 4.1 Hardware Configuration

Note: Only for 30-pin products.

Cautions: 1. The purpose of this circuit is only to provide the connection outline and the circuit is simplified accordingly. When designing and implementing an actual circuit, provide proper pin treatment and make sure that the hardware's electrical specifications are met (connect the input-only ports separately to V_{DD} or V_{SS} via a resistor).

2. V_{DD} must be held at not lower than the reset release voltage (V_{LVD}) that is specified as LVD.

4.2 List of Pins to be Used

Table 4.1 lists the pins to be used and their functions.

Table 4.1 Pins to be Used and their Functions

Pin Name	I/O	Description
P60/KR4/SCLA0	I/O	IICA0 serial clock I/O pin
P61/KR5/SDAA0	I/O	IICA0 serial data transmission/reception pin

5. Description of the Software

5.1 Operation Outline

The sample program covered in this application note provides IICA slave transmission and reception (address reception, and data transmission/reception) through the serial interface IICA.

(1) Initialize serial interface IICA.
<Conditions for setting>

- Select the fast mode as the operation mode.
- Set the transfer clock frequency to 400 kHz.
- Set the local address to A0H.
- Turn the digital filter on
- Generate an interrupt in response to the ninth clock signal
- Enable stop condition interrupts.
- Use the P60/KR4/SCLA0 pin for transfer clock I/O and the P61/KR5/SDAA0 pin for data transmission/reception.

(2) Get the communication buffer (16 bytes) ready for use.

(3) After setting is completed, use the wakeup function of IICA to reduce the power consumption. Execute a STOP instruction and wait for a local address/extension code reception interrupt (INTIICA0).

(4) When the local address or extension code is received, perform wakeup operation and start data communication.

(5) When data is received from the master, the data is stored in the communication buffer.

(6) When data is transmitted to the master, transmit data to the master.

(7) Repeat steps (2) to (6).

Caution: This sample code is related to RL78/G12 Serial Interface IICA (for Master Transmission/Reception) (R01AN2987E) Application Note.
The conditions for completing communication are as follows: detection of a stop condition during data transmission/reception, and NACK detection during transmission. After data reception, set bit 4 of all the data in the data buffer in preparation for transmission.

5.2 List of Option Byte Settings

Table 5.1 summarizes the settings of the option bytes.

Table 5.1 Option Byte Settings

Address	Value	Description
000C0H	01101110B	Disables the watchdog timer. (Stops counting after the release from the reset state.)
000C1H	01111111B	LVD reset mode, 2.81 V (2.76 to 2.87 V)
000C2H	11100000B	HS mode, HOCO: 24 MHz
000C3H	10000101B	Enables the on-chip debugger.

5.3 List of Constants

Table 5.2 lists the constants that are used in this sample program.

Table 5.2 Constants for the Sample Program

Constant	Setting	Description
BAUDRATE	400	Transfer speed in units of kbps (400 kbps (fast mode))
FHOCO	24	HOCO oscillation frequency in units of MHz (24 MHz)
OPCLK	FHOCO/2	IICA0 operation clock frequency in units of MHz (12 MHz)
DIICWL	(13 * OPCLK + 9) / 10	Value set in IICWH0 register (16)
RISETIME	100	Signal rise time (100 ns)
FALLTIME	100	Signal fall time (100 ns)
WIDTHHIGH	1200 – (RISETIME + FALLTIME)	SCLA0 high-level width (1000 ns)
DIICWH	(WIDTHHIGH * OPCLK + 999) / 1000	Value set in IICWH0 register (12)
CSLFADDR	0A0H	Slave address
CDATAANO	16	Data buffer size

5.4 List of Variables

Table 5.3 lists the global variables that are used in this sample program.

Table 5.3 Global Variables for the Sample Program

Type	Variable Name	Contents	Function Used
8 bits × 16 arrays	RRCVBUF	Data buffer	main, SINTIICA0
8 bits	RBUFFPOS	Buffer pointer	main, SINTIICA0
8 bits	RIICINF0	IICA0 operation mode flag bit 7 : Flag which indicates whether communication is in progress 0: Communication is not in progress. 1: Communication is in progress. bit 6 : Communication direction flag 0: Reception 1: Transmission bit 5 : (not used) 0: Not ready 1: Ready (Communication is possible) bit 4 : Last communication mode 0: Transmission mode 1: Reception mode	main, SINTIICA0

5.5 List of Functions (Subroutines)

Table 5.4 summarizes the functions (subroutines) that are used in this sample program.

Table 5.4 Functions (Subroutines)

Function Name	Outline
STARTIICA0	Make initial setting of IICA0 and put it in communication standby state
IINTIICA0	INTIICA0 interrupt processing routine
SINTIICA0	Perform processing by INTIICA0 interrupt

5.6 Function Specifications

This section describes the specifications for the functions that are used in this sample program.

[Function Name] STARTIICA0

Synopsis	Initial setup of IICA0 hardware
Explanation	This function initializes the local address of IICA0 to A0H for fast mode.
Arguments	None
Return value	None
Remarks	None

[Function Name] IINTIICA0

Synopsis	INTIICA0 interrupt processing
Explanation	This function performs a routine which accepts and processes INTIICA0. Subroutine SINTIICA0 processes communication.
Arguments	None
Return value	None
Remarks	None

[Function Name] SINTIICA0

Synopsis	IICA0 interrupt handler processing
Explanation	This function performs main communication processing which uses INTIICA0.
Arguments	None
Return value	None
Remarks	This function sets status in each bit of RIICINF0.

5.7 Flowcharts

Figure 5.1 shows the overall flow of the sample program described in this application note.

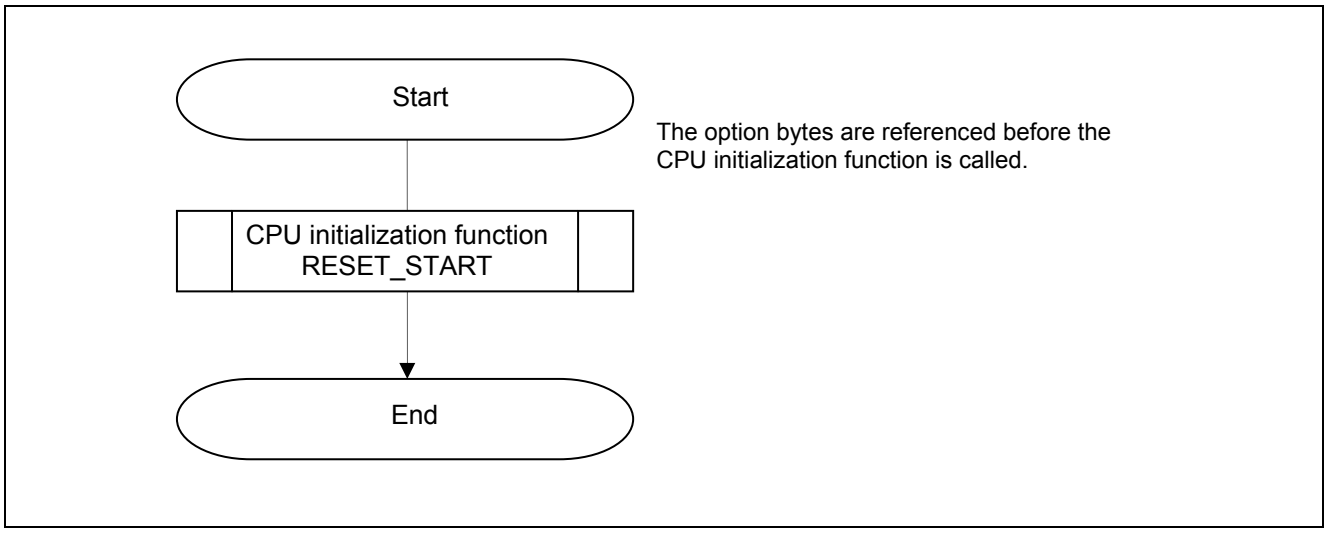


Figure 5.1 Overall Flow

5.7.1 CPU Initialization Function

Figure 5.2 shows the flowchart for the CPU initialization function.

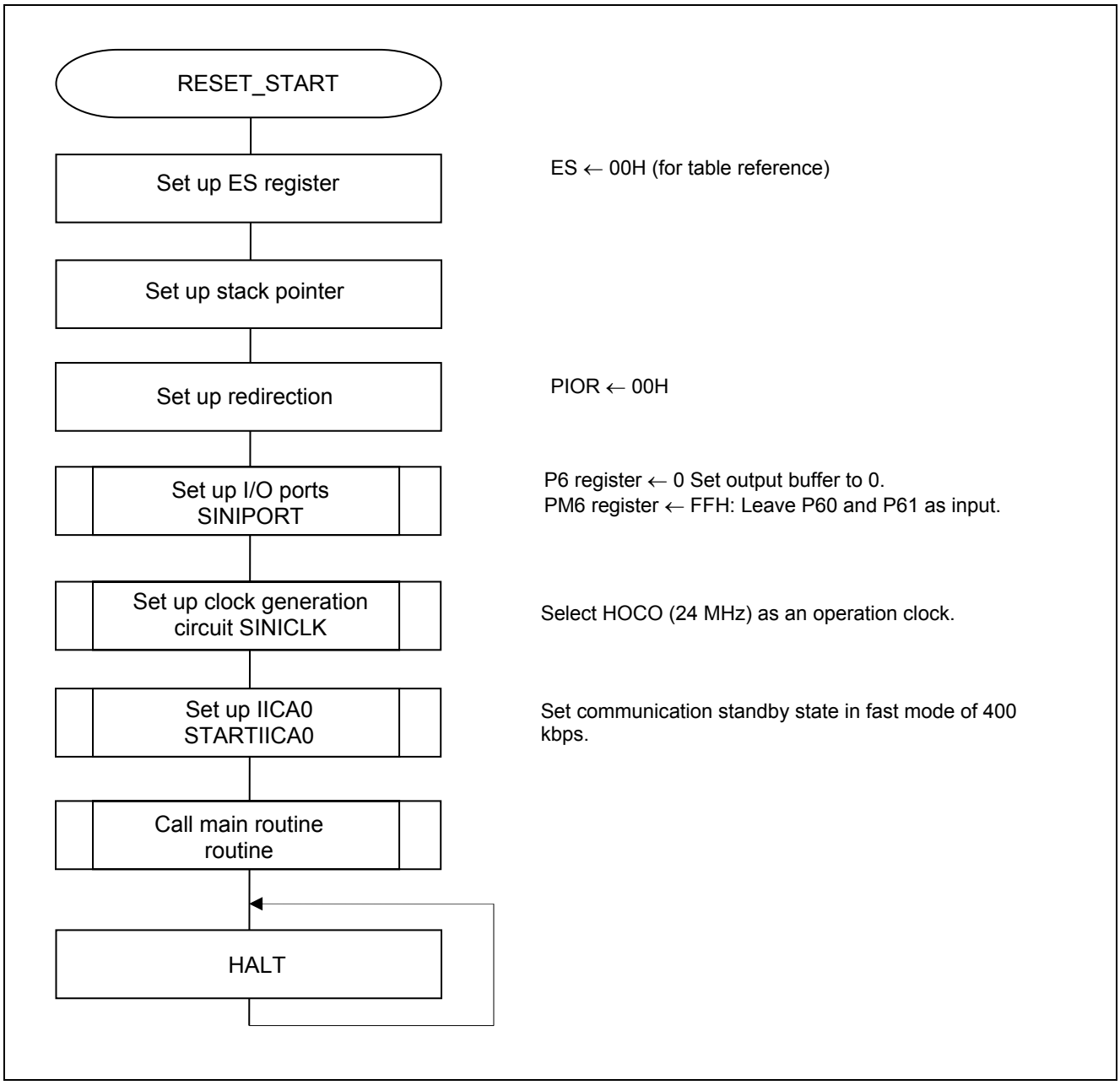


Figure 5.2 CPU Initialization Function

5.7.2 I/O Port Setup

Figure 5.3 shows the flowchart for I/O port setup.

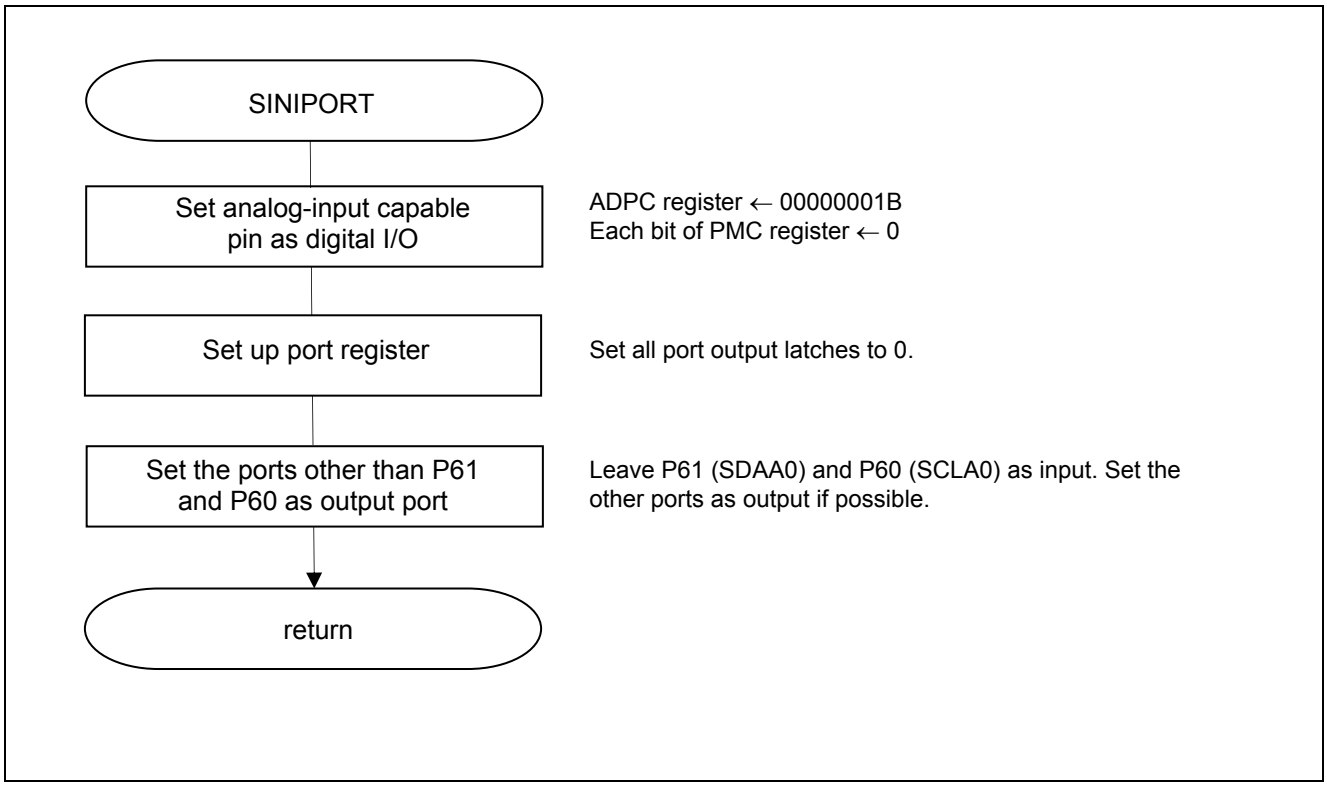


Figure 5.3 I/O Port Setup

Note: Refer to the section entitled "Flowcharts" in RL78/G12 Initialization Application Note (R01AN2582E) for the configuration of the unused ports.

Caution: Provide proper treatment for unused pins so that their electrical specifications are observed. Connect each of any unused input-only ports to V_{DD} or V_{SS} via separate resistors.

5.7.3 Clock Generation Circuit Setup

Figure 5.4 shows the flowchart for setting up the CPU clock.

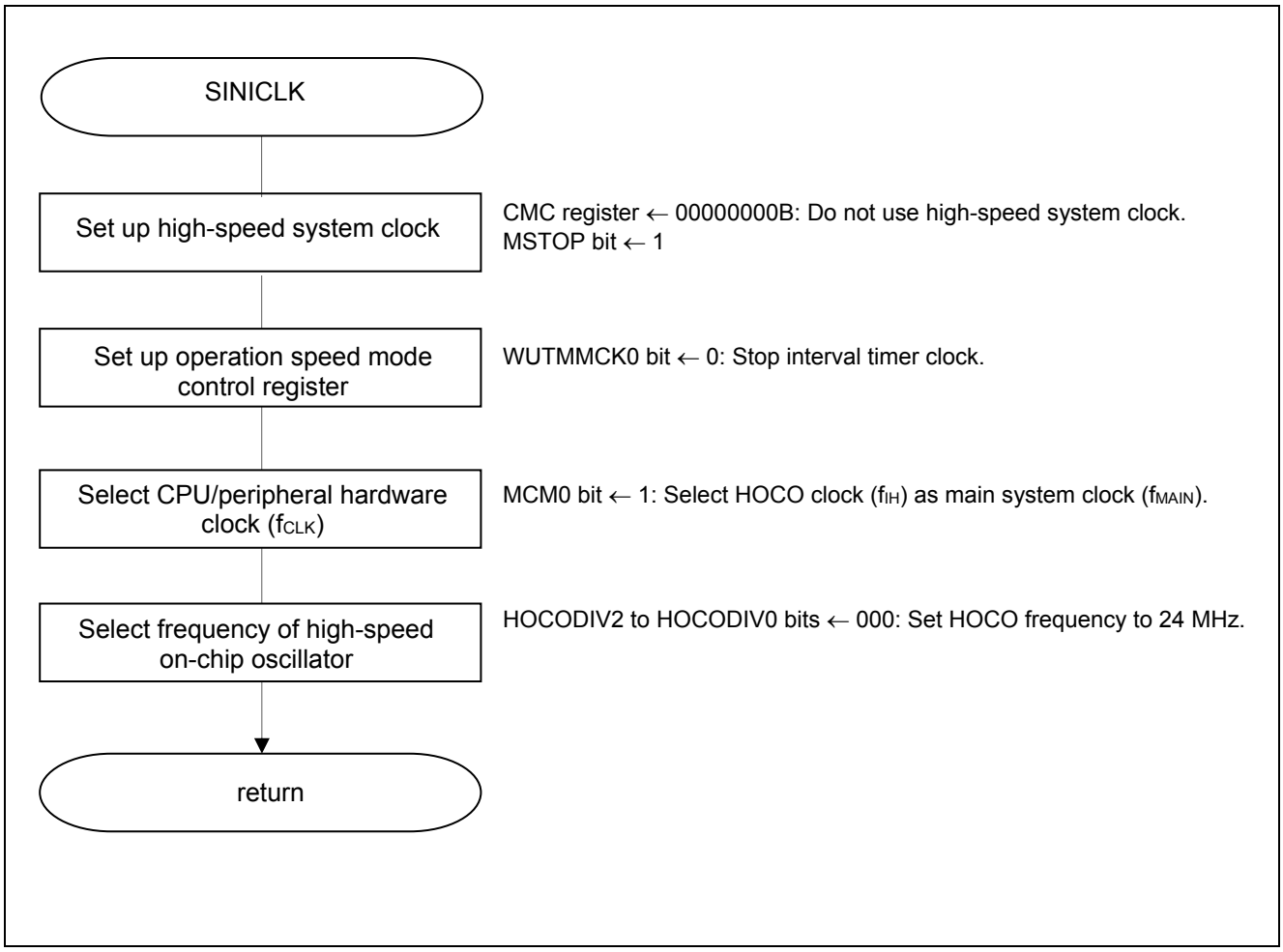


Figure 5.4 Clock Generation Circuit Setup

5.7.4 Serial Interface IICA Setup

Figure 5.5 shows the flowchart for serial interface IICA setup.

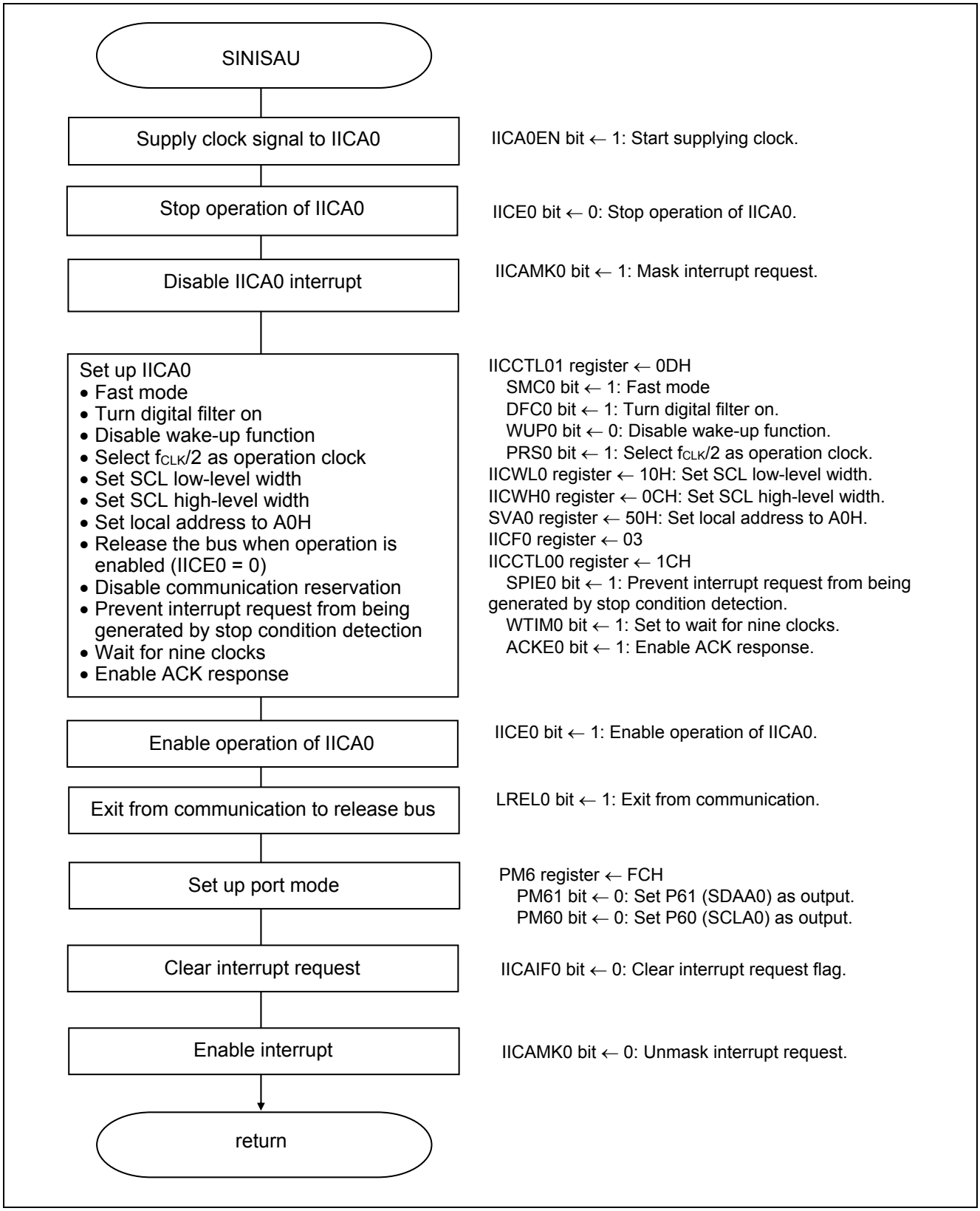


Figure 5.5 Serial Interface IICA Setup

Starting clock signal supply to serial interface IICA0

- Peripheral enable register 0 (PER0)
  Start supplying clock signals to IICA0 by using IICA0EN.

Symbol: PER0

7	6	5	4	3	2	1	0
TMKAEN	0	ADCEN	IICA0EN	SAU1EN	SAU0EN	0	TAU0EN
x	0	x	**1**	0	x	0	x

Bit 4

IICA0EN	Control of serial interface IICA0 input clock supply
0	Stops supply of input clock.
1	**Enables supply of input clock.**

Caution: For details on the register setup procedures, refer to RL78/G12 User's Manual: Hardware.

Setting up the IICA0 operation mode

- IICA control register 01 (IICCTL01)
  Select an operation clock frequency.
  Turn the digital filter on.
  Select the fast mode.
  Disable the wakeup function.

Symbol: IICCTL01

7	6	5	4	3	2	1	0
WUP0	0	CLD0	DAD0	SMC0	DFC0	0	PRS0
0	0	x	x	**1**	**1**	0	**1**

Bit 7

WUP0	Address match wakeup control
0	**Disable the address match wakeup function in STOP mode.**
1	Enable the address match wakeup function in STOP mode.

Bit 3

SMC0	Operation mode selection
0	Standard mode
1	**Fast mode**

Bit 2

DFC0	Digital filter operation control
0	Turns the digital filter off.
1	**Turns the digital filter on.**

Bit 0

PRS0	Operation clock frequency selection
0	Selects f_{CLK} as the operation clock frequency.
1	**Selects f_{CLK}/2 as the operation clock frequency.**

Caution: For details on the register setup procedures, refer to RL78/G12 User's Manual: Hardware.

Configuring the transfer clock

- IICA low-level width setting register 0 (IICWL0)
- IICA high-level width setting register 0 (IICWH0)
  Set the low-level width and high-level width of the SCLA0 pin signal.

Symbol: IICWL0

7	6	5	4	3	2	1	0
0	**0**	**0**	**1**	**0**	**0**	**0**	**0**

Symbol: IICWH0

7	6	5	4	3	2	1	0
0	**0**	**0**	**0**	**1**	**1**	**0**	**0**

Setting the local address

- Slave address register 0 (SVA0)
  Set the local address.

Symbol: SVA0

7	6	5	4	3	2	1	0
1	**0**	**1**	**0**	**0**	**0**	**0**	**0**

Caution: For details on the register setup procedures, refer to RL78/G12 User's Manual: Hardware.

Setting up the IICA operation

- IICA control register 00 (IICCTL00)
  Enable I^2C operation.
  Disable stop condition interrupts.
  Set the wait and interrupt request generation timing.
  Enable acknowledgement output.

Symbol: IICCTL00

7	6	5	4	3	2	1	0
IICE0	LREL0	WREL0	SPIE0	WTIM0	ACKE0	STT0	SPT0
0/1	**0/1**	x	**1**	**1**	**1**	x	x

Bit 7

IICE0	Enabling/disabling of I^2C operation
0	**Stops operation.**
1	**Enables operation.**

Bit 6

LREL0	Transition from the communication state
0	**Normal operation**
1	**Makes a transition from the current communication state to the standby state. Automatically cleared to 0 after the transition.**

Bit 4

SPIE0	Enabling/disabling generation of interrupt requests due to stop condition detection
0	Disabled
1	**Enabled**

Bit 3

WTIM0	Wait/interrupt request control
0	Interrupt request is generated at the falling edge of the eighth clock signal.
1	**Interrupt request is generated at the falling edge of the ninth clock signal.**

Bit 2

ACKE0	Acknowledgement control
0	Disables acknowledgements.
1	**Enables acknowledgements. During the ninth clock period, the SDAA0 line is set to low level.**

Caution: For details on the register setup procedures, refer to RL78/G12 User's Manual: Hardware.

Setting up the IICA pins

- Port mode register 6 (PM6)
  Use P60 for SCLA0 and P61 for SDAA0 in output mode.

Symbol: PM6

7	6	5	4	3	2	1	0
0	0	0	0	PM63	PM62	PM61	PM60
0	0	0	0	x	x	**0**	**0**

Bit 1

PM61	P61 I/O mode selection
0	**Output mode (output buffer on)**
1	Input mode (output buffer off)

Bit 0

PM60	P60 I/O mode selection
0	**Output mode (output buffer on)**
1	Input mode (output buffer off)

Caution: For details on the register setup procedures, refer to RL78/G12 User's Manual: Hardware.

5.7.5 Main Processing

Figures 5.6 and 5.7 show the flowcharts for the main processing.

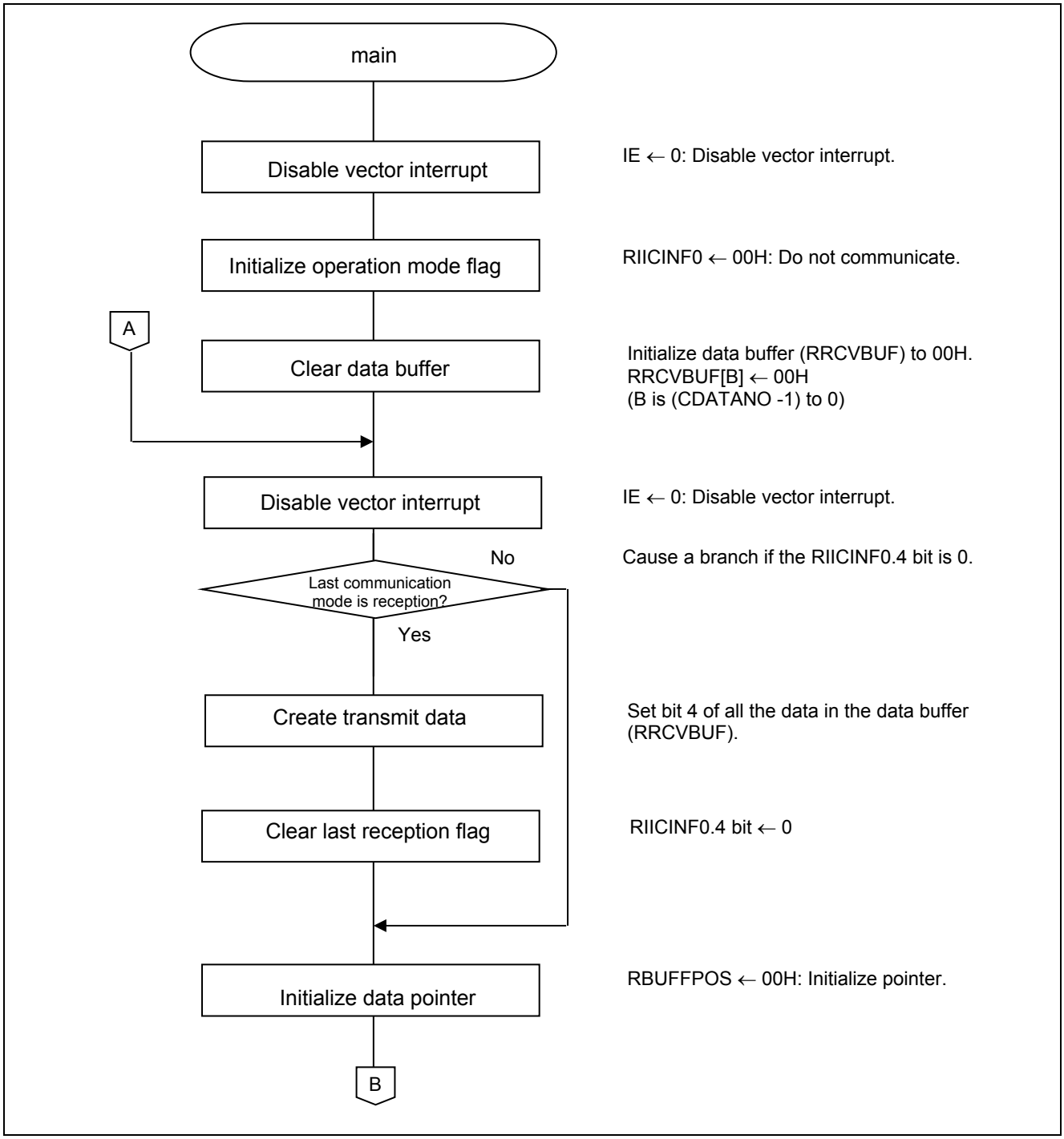


Figure 5.6 Main Processing (1/2)

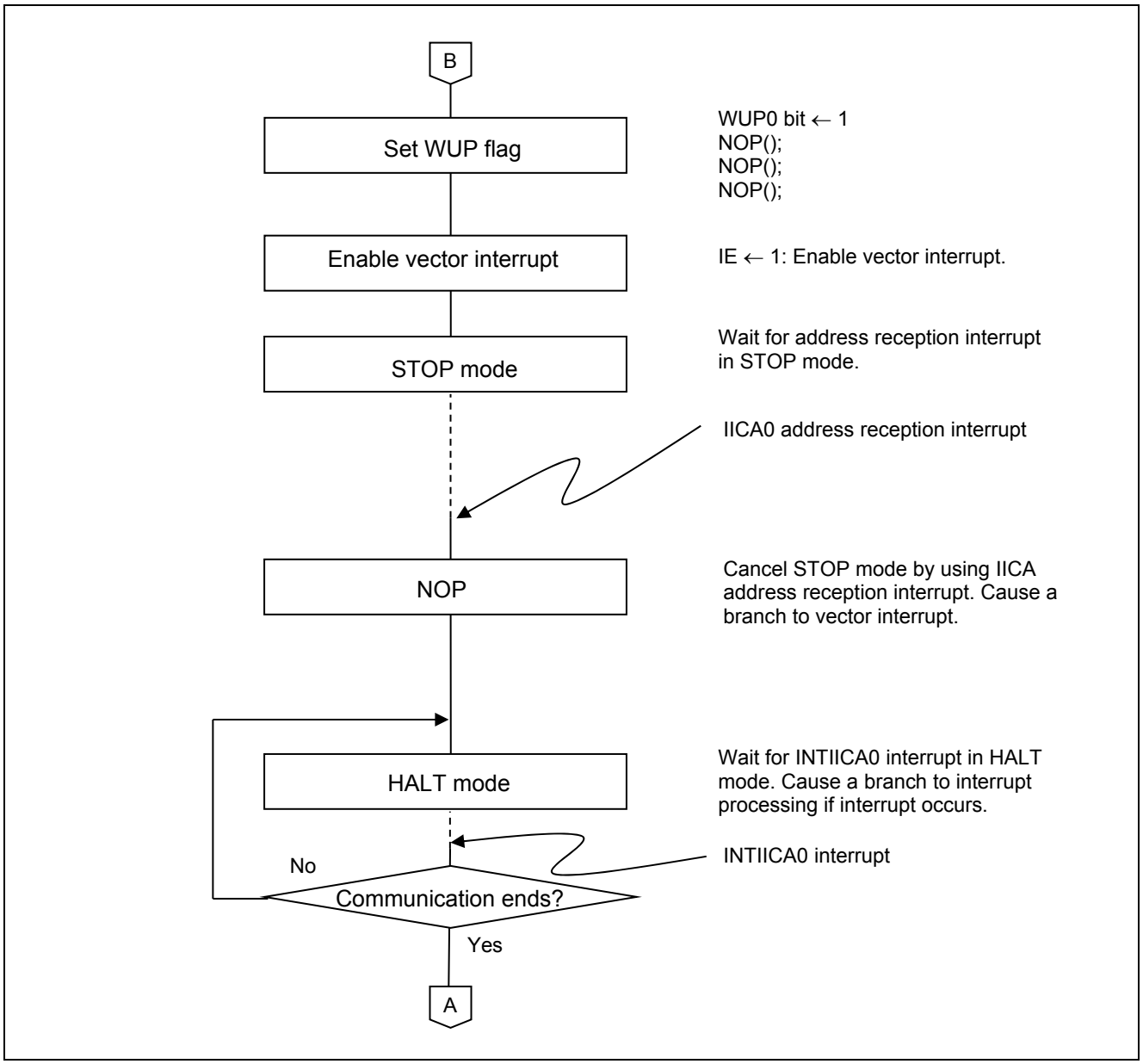


Figure 5.7 Main Processing (2/2)

Setting up the wakeup function

- IICA control register 01 (IICTL01)
  Enable the wakeup function.

Symbol: IICCTL01

7	6	5	4	3	2	1	0
WUP0	0	CLD0	DAD0	SMC0	DFC0	0	PRS0
1	0	x	x	1	1	0	1

Bit 7

WUP0	Address match wakeup control
0	Disables the address match wakeup function in STOP mode
1	**Enables the address match wakeup function in STOP mode**

Communication exit setting

- IICA control register 00 (IICCTL00)
  Terminate the current communication, and make the system enter a communication standby state

Symbol: IICCTL00

7	6	5	4	3	2	1	0
IICE0	LREL0	WREL0	SPIE0	WTIM0	ACKE0	STT0	SPT0
1	**1**	x	0/1	0/1	0/1	0	0

Bit 6

LREL0	Exit from communications
0	Normal operation
1	**Exits from the current communications and sets standby mode.**

Caution: For details on the register setup procedures, refer to RL78/G12 User's Manual: Hardware.

5.7.6 IICA0 Interrupt Processing

Figure 5.8 shows the flowchart for IICA0 interrupt processing.

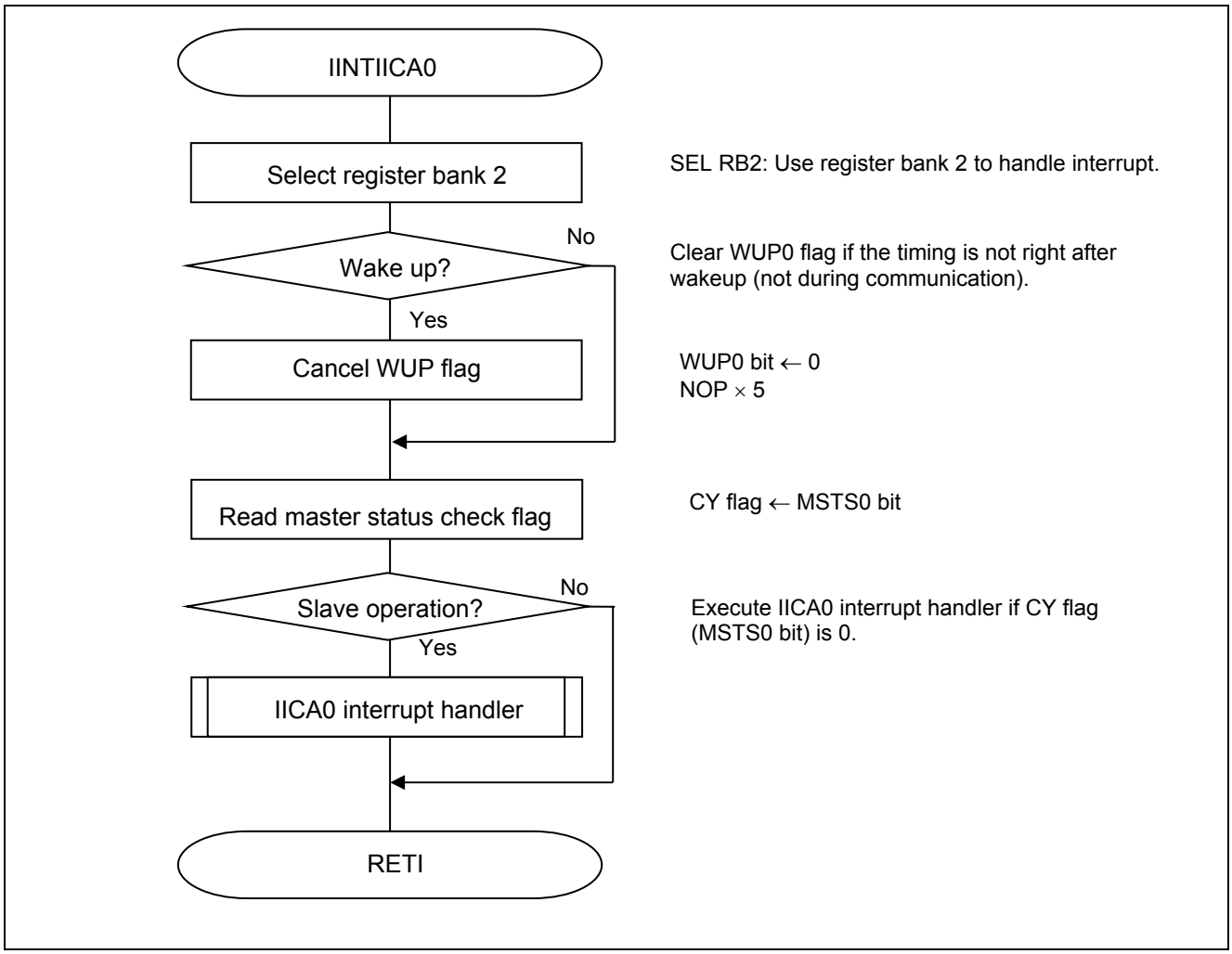


Figure 5.8 IICA0 Interrupt Processing

Disabling the setup of the wakeup function

- IICA control register 01 (IICTL01)
  Disable the wakeup function.

Symbol: IICCTL01

7	6	5	4	3	2	1	0
WUP0	0	CLD0	DAD0	SMC0	DFC0	0	PRS0
0	0	x	x	1	1	0	1

Bit 7

WUP0	Address match wakeup control
0	**Disables the address match wakeup function in STOP mode**
1	Enables the address match wakeup function in STOP mode

Caution: For details on the register setup procedures, refer to RL78/G12 User's Manual: Hardware.

5.7.7 IICA0 Interrupt Handler

Figures 5.9 and 5.10 show the flowcharts for the IICA0 interrupt handler.

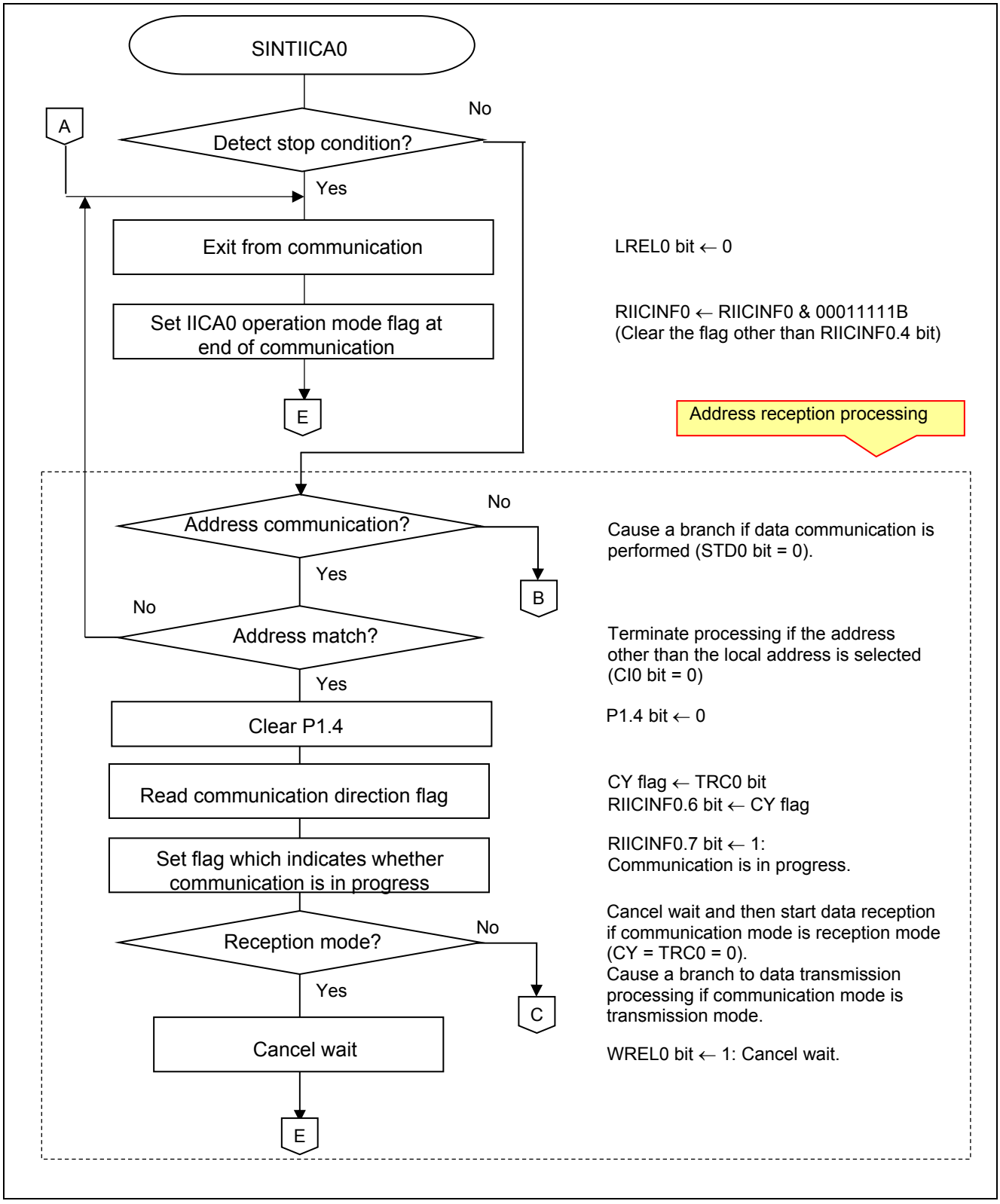


Figure 5.9 IICA0 Interrupt Handler (1/2)

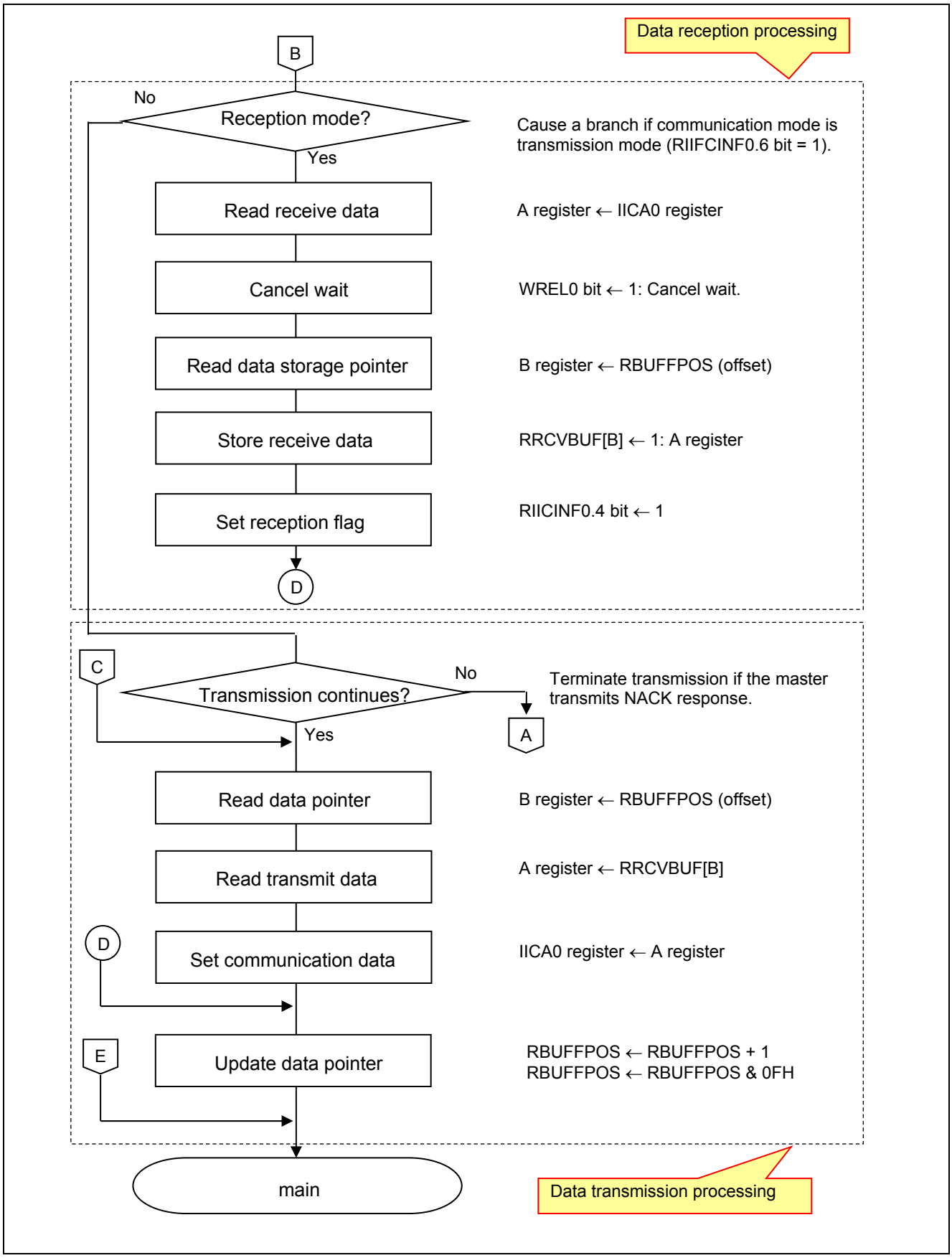


Figure 5.10 IICA0 Interrupt Handler (2/2)

Communication exit setting and wait cancellation setting

- IICA control register 00 (IICCTL00)
  Terminate the current communication, and make the system enter a communication standby state
  Cancel wait and prepare for next data reception

Symbol: IICCTL00

7	6	5	4	3	2	1	0
IICE0	LREL0	WREL0	SPIE0	WTIM0	ACKE0	STT0	SPT0
1	**0/1**	**0/1**	0/1	0/1	0/1	0	0

Bit 6

LREL0	Exit from communications
0	Normal operation
1	**Exits from the current communications and sets standby mode.**

Bit 5

WREL0	Wait cancellation
0	Do not cancel wait
1	**Cancel wait.**

Caution: For details on the register setup procedures, refer to RL78/G12 User's Manual: Hardware.

6. Sample Code

The sample code is available on the Renesas Electronics Website.

7. Documents for Reference

RL78/G12 User's Manual: Hardware (R01UH0200E)

RL78 Family User's Manual: Software (R01US0015E)

(The latest versions of the documents are available on the Renesas Electronics Website.)

Technical Updates/Technical Brochures

(The latest versions of the documents are available on the Renesas Electronics Website.)

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Revision Record	RL78/G12 Serial Interface IICA (for Slave Transmission/Reception) CC-RL

Rev.	Date	Description	
		Page	Summary
1.00	Oct. 20, 2015	—	First edition issued

General Precautions in the Handling of Microprocessing Unit and Microcontroller Unit Products

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1. Handling of Unused Pins

   Handle unused pins in accordance with the directions given under Handling of Unused Pins in the manual.

   ¾ The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible. Unused pins should be handled as described under Handling of Unused Pins in the manual.

2. Processing at Power-on

   The state of the product is undefined at the moment when power is supplied.

   ¾ The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the moment when power is supplied.
   In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the moment when power is supplied until the reset process is completed.
   In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the moment when power is supplied until the power reaches the level at which resetting has been specified.

3. Prohibition of Access to Reserved Addresses

   Access to reserved addresses is prohibited.

   ¾ The reserved addresses are provided for the possible future expansion of functions. Do not access these addresses; the correct operation of LSI is not guaranteed if they are accessed.

4. Clock Signals

   After applying a reset, only release the reset line after the operating clock signal has become stable. When switching the clock signal during program execution, wait until the target clock signal has stabilized.

   ¾ When the clock signal is generated with an external resonator (or from an external oscillator) during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Moreover, when switching to a clock signal produced with an external resonator (or by an external oscillator) while program execution is in progress, wait until the target clock signal is stable.

5. Differences between Products

   Before changing from one product to another, i.e. to a product with a different part number, confirm that the change will not lead to problems.

   ¾ The characteristics of Microprocessing unit or Microcontroller unit products in the same group but having a different part number may differ in terms of the internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

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