RL78/G12

Initialization CC-RL

Introduction

This application note describes the basic setting items that are necessary for initializing the RL78/G12.

The sample program discussed in this application note initializes the RL78/G12 and provides On/Off control of three LEDs according to the combination of two switch input states.

Target Device

RL78/G12

Contents

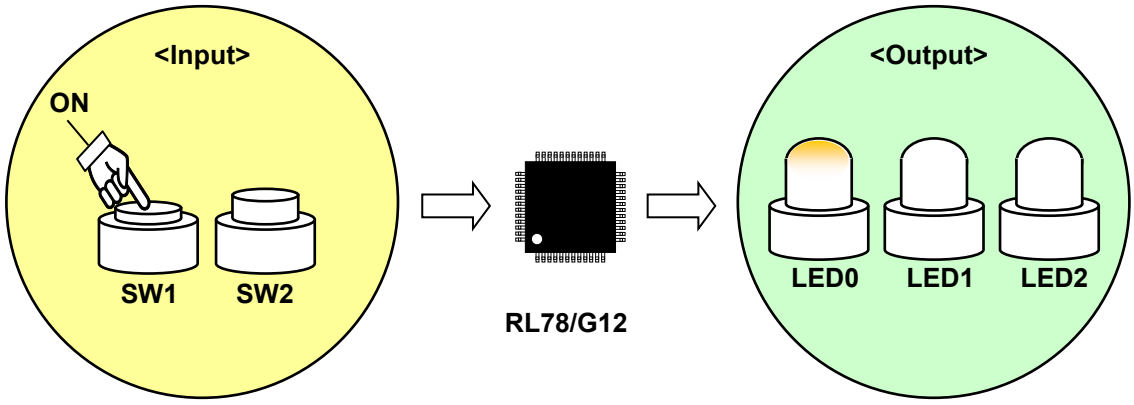
1. Specification

The sample program described in this application note performs basic initialization steps such as the setup of the clock frequency and input/output ports. After the initialization, the program controls, in its main processing routine, the On/Off of three LEDs according to the combination of two switch input states.

Table 1.1 lists the peripheral functions to be used and their usage and figure 1.1 shows the outline of the processing.

Table 1.1 Peripheral Functions to be Used and their Usage

Peripheral Function	Usage
Port input/output	Switch input (SW1 and SW2) LED On/Off control (LED0 to LED2)



Switch Input States		LED Output		
SW1 (P10)	SW2 (P11)	LED0 (P12)	LED1 (P13)	LED2 (P14)
Off	Off	Off	Off	Off
On	Off	On	Off	Off
Off	On	Off	On	Off
On	On	Off	Off	On

Figure 1.1 Operation Processing Outline

2. Operation Evaluate Conditions

The sample code contained in this application note has been evaluated under the conditions listed in the table below.

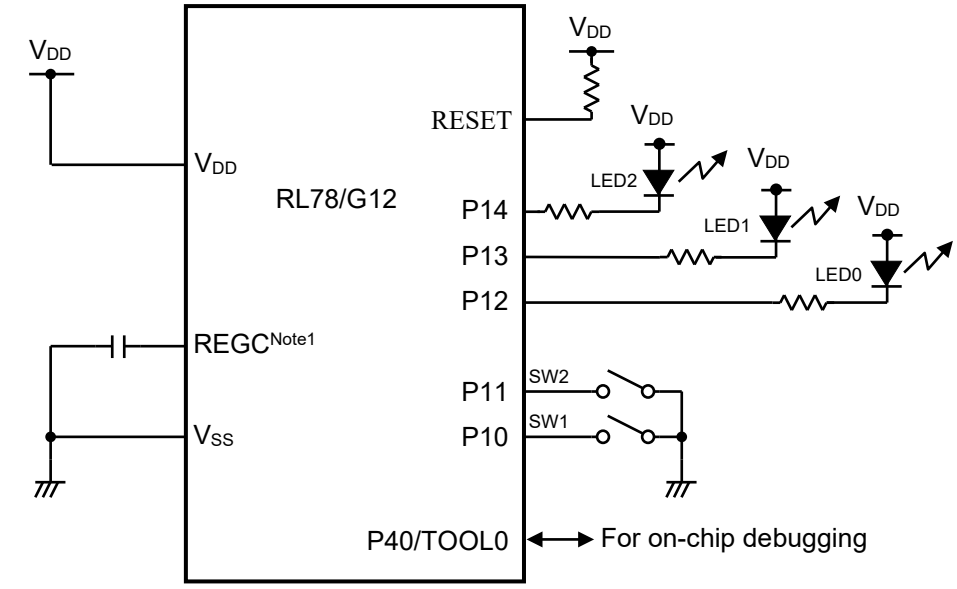
Table 2.1 Operation Check Conditions

Item	Description
Microcontroller used	RL78/G12 (R5F1026A)
Operating frequency	High-speed on-chip oscillator (HOCO) clock: 24 MHz CPU/peripheral hardware clock: 24 MHz
Operating voltage	5.0 V (can run on a voltage range of 2.9 V to 5.5 V.) LVD operation (V_{LVD}): Reset mode 2.81 V (2.76 V to 2.87 V)
Integrated development environment (CS+)	CS+ for CC V3.01.00 from Renesas Electronics Corp.
Assembler (CS+)	CC-RL V1.01.00 from Renesas Electronics Corp.
Integrated development environment (e^2 studio)	e^2 studio V4.0.2.008 from Renesas Electronics Corp.
Assembler (e^2 studio)	CC-RL V1.01.00 from Renesas Electronics Corp.
Integrated development environment (IAR)	IAR Embedded Workbench for Renesas RL78 V4.21.3 from IAR Systems.
Assembler (IAR)	IAR Assembler for Renesas RL78 V4.21.2.2420 from IAR Systems.
Board used	RL78/G12 target board (QB-R5F1026A-TB) + SW and LED

3. Description of the Hardware

3.1 Hardware Configuration Example

The example of configuration of the hardware that is used for this application note is shown below.



Note 1. 30-pin products only.

Figure 3.1 Hardware Configuration

Notes 1. The purpose of this circuit is only to provide the connection outline and the circuit is simplified accordingly. When designing and implementing an actual circuit, provide proper pin treatment and make sure that the hardware's electrical characteristics conditions are met (connect the input-dedicated ports separately to V_{DD} or V_{SS} via a resistor).

2. V_{DD} must be held at not lower than the LVD detection voltage (V_{LVD}) that is specified as LVD.

3.2 List of Pins to be used

Table 3.1 lists the pins to be used and their functions.

Table 3.1 Pins to be Used and Their Functions

Pin Name	I/O	Description
P10	Input	Switch input (SW1) port
P11	Input	Switch input (SW2) port
P12	Output	LED (LED0) control port
P13	Output	LED (LED1) control port
P14	Output	LED (LED2) control port

4. Description of the Software

4.1 Operation Outline

The sample program described in this application note initializes the CPU (e.g., selecting the CPU clock frequency) and sets up its I/O ports.

After completing the hardware setup, the sample program controls the On/Off of three LEDs (LED0 to LED2) according to the combination of states of two switch inputs (SW1 and SW2).

1. CPU initialization[Note1]
   — Sets up the peripheral I/O redirection function.
   — Sets up the I/O ports.
   — Sets up the CPU clock.

Note 1. The option bytes are referenced before the CPU is initialized.

<Setup conditions>

- Sets the reset value because the CPU does not use the peripheral I/O redirection function (PIOR register).
- Makes the following configurations for the I/O ports:
  1. Configures the ports that are configured for analog input after the release of the reset state for digital I/O (ADPC register and port mode control registers).
  2. Configures P10 and P11 which are used as switch inputs (SW1 and SW2) for input and the other ports for output (port mode register).
  3. Connects on-chip pull-up resistors to P10 and P11 which are to be used as switch inputs (SW1 and SW2) (pull-up resistor option register).
  4. Sets P12 to P14 which are used for On/Off control of LEDs (LED0 to LED2) to 1 and the other unused pins to 0 (port register).
- Sets up the CPU clock.
  1. Sets the reset value because the high-speed system clock is not to be in use (clock operation mode control (CMC) register and clock operation status control (CSC) register).
  2. Selects the HOCO (f_{IH}) as the CPU/peripheral hardware clock (f_{CLK}) (system clock control (CKC) register).

2. Executes the main processing.
   — Performs the LED output control as summarized in table 4.1 according to the state of the switch inputs (SW1 and SW2).

Table 4.1 Main Processing

Switch Input States		LED Output		
SW1 (P10)	**SW2 (P11)**	**LED0 (P12)**	**LED1 (P13)**	**LED2 (P14)**
Off	Off	Off	Off	Off
On	Off	On	Off	Off
Off	On	Off	On	Off
On	On	Off	Off	On

Note: Refer to RL78/G12 User's Manual Manual for notes on device use.

4.2 List of Option Byte Settings

Table 4.2 summarizes the settings of the option bytes.

Table 4.2 Option Byte Settings

Address	Value	Description
000C0H	01101110B	Stops the watchdog timer operation. (Stops counting after the release of the reset state.)
000C1H	01111111B	LVD reset mode 2.81 V (2.76 V to 2.87 V)
000C2H	11100000B	HS mode, HOCO: 24 MHz
000C3H	10000101B	Enables the on-chip debugging function.

4.3 List of Functions (Subroutine)

Table 4.3 lists the functions that are used by this sample program.

Table 4.3 Functions (Subroutine)

Function (Subroutine) Name	Outline
RESET_START	Initializes the hardware settings and calls main function.
SINIPORT	Initializes the I/O ports.
SINICLK	Initializes the clock generator.
main	Main function

4.4 Function (Subroutine) Specifications

This section describes the specifications for the functions that are used in the sample code.

[Function Name] RESET_START

Synopsis	Initialize CPU at reset start.
Declaration	—
Explanation	Sets the stack pointer and, after making initial hardware settings, calls the main processing routine.
Arguments	None
Return value	None
Remarks	None

[Function Name] SINIPORT

Synopsis	Set I/O ports.
Declaration	—
Explanation	Sets P10 and P11 as input points (internal pull-up resistor enabled) and P12, P13, and P14 as output ports (high-level output). Sets all other I/O ports, except P40, as output ports (low-level output).
Arguments	None
Return value	None
Remarks	None

[Function Name] SINICLK

Synopsis	Set clock generator circuit.
Declaration	—
Explanation	Initializes the registers related to the clock generator.
Arguments	None
Return value	None
Remarks	None

[Function Name] main

Synopsis	Main function
Declaration	—
Explanation	The main processing function of the sample code. Outputs the following values to P1 according to the values of SW1 (P10) and SW2 (P11): SW2 : SW1 : PORT1 0 : 0 : 00001100B 0 : 1 : 00010100B 1 : 0 : 00011000B 1 : 1 : 00011100B
Arguments	None
Return value	None
Remarks	

4.5 Flowcharts

Figure 4.1 shows the overall flow of the sample program described in this application note.

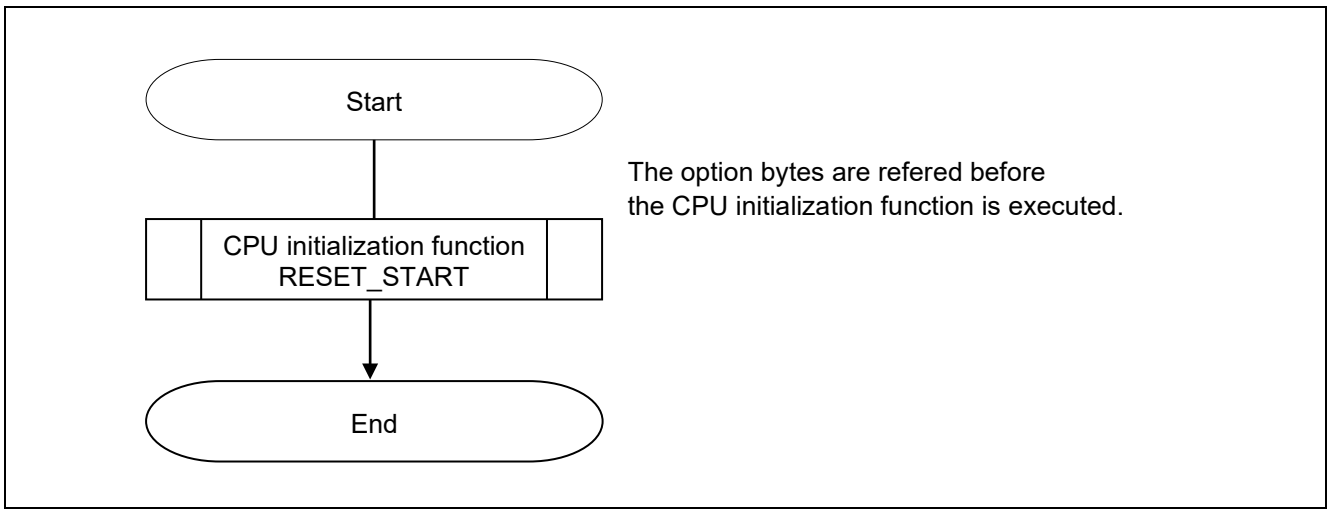


Figure 4.1 Overall Flow

Option Byte Configuration Outline

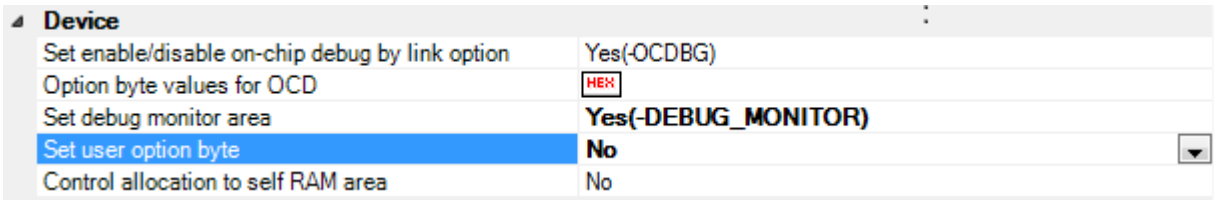
The option bytes of the RL78/G12 are made up of user option bytes (000C0H-000C2H) and on-chip debugging option bytes (000C3H).

The option bytes are automatically refered and the prespecified functions are set up when power is first supplied or after the release of the reset state. The option bytes cannot be set up by any user program.

The option bytes can exercise the controls listed below. The settings of the option bytes are contained in the file opt.asm.

- User option bytes
  - Makes settings related to the watchdog timer (000C0H).
  - Makes LVD-related and RESET pin function settings (000C1H).
  - Sets up the HOCO and flash memory operation mode (000C2H).
- On-chip debugging option bytes (000C3H)

The option byte settings can be specified through “User Option Byte Values” in the “Device” panel of the “Link Option” tag in CS+. Settings made via the “Link Option” tag take precedence over settings specified in software programs. Therefore, “Set user option bytes” should be set to “No,” as shown below.



Note: For details on the procedure for setting up the CS+ link options, refer to the CS+ tutorial.

(1) 000C0H (Watchdog Timer Related Settings)

7	6	5	4	3	2	1	0
WDTINT	WINDOW1	WINDOW0	WDTON	WDCS2	WDCS1	WDCS0	WDSTBYON
0	1	1	0	1	1	1	0

Bit 0

WDSTBYON	Control of Watchdog Timer Counter (HALT/STOP mode)
0	**Disables counter operation in HALT/STOP mode.**
1	Enables counter operation in HALT/STOP mode.

Bits 3 to 1

WDCS2 to WDCS0	Watchdog Timer Overflow Time
000	$2^6/f_{IL}$
001	$2^7/f_{IL}$
020	$2^8/f_{IL}$
011	$2^9/f_{IL}$
100	$2^{11}/f_{IL}$
101	$2^{13}/f_{IL}$
110	$2^{14}/f_{IL}$
111	**$2^{16}/f_{IL}$**

Bit 4

WDTON	Control of Watchdog Timer Counter
0	**Disables counter operation. (Stops counter after the release of reset sequence.)**
1	Enables counter operation. (Starts counter after the release of reset sequence.)

Bits 6 and 5

WINDOW1 and WINDOW0	Watchdog Timer Window Open Period
00	Setting prohibited
01	50%
10	75%
11	**100%**

Bit 7

WDTINT	Use of Interval Interrupts of watchdog timer
0	**Interval interrupt is not used.**
1	An interval interrupt is generated when 75%+1/2f_{IL} is reached.

(2) 000C1H (LVD-Related Settings)

7	6	5	4	3	2	1	0
VPOC2	VPOC1	VPOC0	PORTSELB	LVIS1	LVIS0	LVIMDS1	LVIMDS0
0	1	1	1	1	1	1	1

When Used as Interrupt and Reset Mode

Detection Voltage			Option Byte Setting Value						
V_{LVDH}		V_{LVDL}							
Rising edge	Falling edge	Falling edge	LVIMDS1	LVIMDS0	VPOC2	VPOC1	VPOC0	LVIS1	LVIS0
1.98 V	1.94 V	1.84 V	1	0	0	0	1	1	0
2.09 V	2.04 V							0	1
3.13 V	3.06 V							0	0
2.61 V	2.55 V	2.45 V			0	1	0	1	0
2.71 V	2.65 V							0	1
3.75 V	3.67 V							0	0
2.92 V	2.86 V	2.75 V			0	1	1	1	0
3.02 V	2.96 V							0	1
4.06 V	3.98 V							0	0
Other than above			Setting prohibited						

When Used as Reset Mode

Detection Voltage		Option Byte Setting Value						
V_{LVD}								
Rising edge	Falling edge	LVIMDS1	LVIMDS0	VPOC2	VPOC1	VPOC0	LVIS1	LVIS0
1.88 V	1.84 V	**1**	**1**	0	0	1	1	1
1.98 V	1.94 V			0	0	1	1	0
2.09 V	2.04 V			0	0	1	0	1
2.50 V	2.45 V			0	1	0	1	1
2.61 V	2.55 V			0	1	0	1	0
2.71 V	2.65 V			0	1	0	0	1
2.81 V	**2.75 V**			**0**	**1**	**1**	**1**	**1**
2.92 V	2.86 V			0	1	1	1	0
3.02 V	2.96 V			0	1	1	0	1
3.13 V	3.06 V			0	0	1	0	0
3.75 V	3.67 V			0	1	0	0	0
4.06 V	3.98 V			0	1	1	0	0
Other than above		Setting prohibited						

When Used as Interrupt Mode

Detection Voltage		Option Byte Setting Value						
V_{LVD}								
Rising edge	Falling edge	LVIMDS1	LVIMDS0	VPOC2	VPOC1	VPOC0	LVIS1	LVIS0
1.88 V	1.84 V	0	1	0	0	1	1	1
1.98 V	1.94 V			0	0	1	1	0
2.09 V	2.04 V			0	0	1	0	1
2.50 V	2.45 V			0	1	0	1	1
2.61V	2.55 V			0	1	0	1	0
2.71 V	2.65 V			0	1	0	0	1
2.81 V	2.75 V			0	1	1	1	1
2.92 V	2.86 V			0	1	1	1	0
3.02 V	2.96 V			0	1	1	0	1
3.13 V	3.06 V			0	0	1	0	0
3.75 V	3.67 V			0	1	0	0	0
4.06 V	3.98 V			0	1	1	0	0
Other than above		Setting prohibited						

When LVD Is Off

Detection Voltage		Option Byte Setting Value						
V_{LVD}								
Rising edge	Falling edge	LVIMDS1	LVIMDS0	VPOC2	VPOC1	VPOC0	LVIS1	LVIS0
—	—	×	1	1	×	×	×	×
Other than above		Setting prohibited						

Remarks: × = don't care

PORTSELB	P125/$\overline{\text{RESET}}$ pin control
0	Port function (P125/KR1/SI01)
1	**$\overline{\text{RESET}}$ input (PU125 = 1, internal pull-up resistor enabled)**

(3) 000C2H (HOCO and Flash Memory Operation Settings)

7	6	5	4	3	2	1	0
CMODE1	**CMODE0**	1	0	**FRQSEL3**	**FRQSEL2**	**FRQSEL1**	**FRQSEL0**
1	**1**	1	0	**0**	**0**	**0**	**0**

Bits 7 and 6

CMODE1	CMODE0	Setting of Flash Memory Operating Mode		
			Operating Frequency Range	Operating Voltage Range
1	0	LV (low voltage main) mode	1 MHz to 8 MHz	1.8 V to 5.5 V
1	**1**	**HS (high speed main) mode**	1 MHz to 16 MHz	2.4 V to 5.5 V
			1 MHz to 24 MHz	**2.7 V to 5.5 V**
Other than above		Setting prohibited		

Bits 3 to 0

FRQSEL3	FRQSEL2	FRQSEL1	FRQSEL0	HOCO Frequency
0	**0**	**0**	**0**	**24 MHz**
1	0	0	1	16 MHz
0	0	0	1	12 MHz
1	0	1	0	8 MHz
1	0	1	1	4 MHz
1	1	0	1	1 MHz
Other than above				Setting prohibited

(4) 000C3H (On-Chip Debugging Option Bytes)

7	6	5	4	3	2	1	0
OCDENSET	0	0	0	0	1	0	**OCDERSD**
1	0	0	0	0	1	0	**1**

Bits 7 and 0

OCDENSET	OCDERSD	Control of On-chip Debugging Operation
0	0	Disables on-chip debugging.
0	1	Setting prohibited
1	0	Enables operation and erases flash memory data when authentication of security ID fails.
1	**1**	**Enables operation but does not erase flash memory data when authentication of security ID fails.**

4.5.1 CPU Initialization Function

Figure 4.2 shows a flowchart of the CPU initialization function.

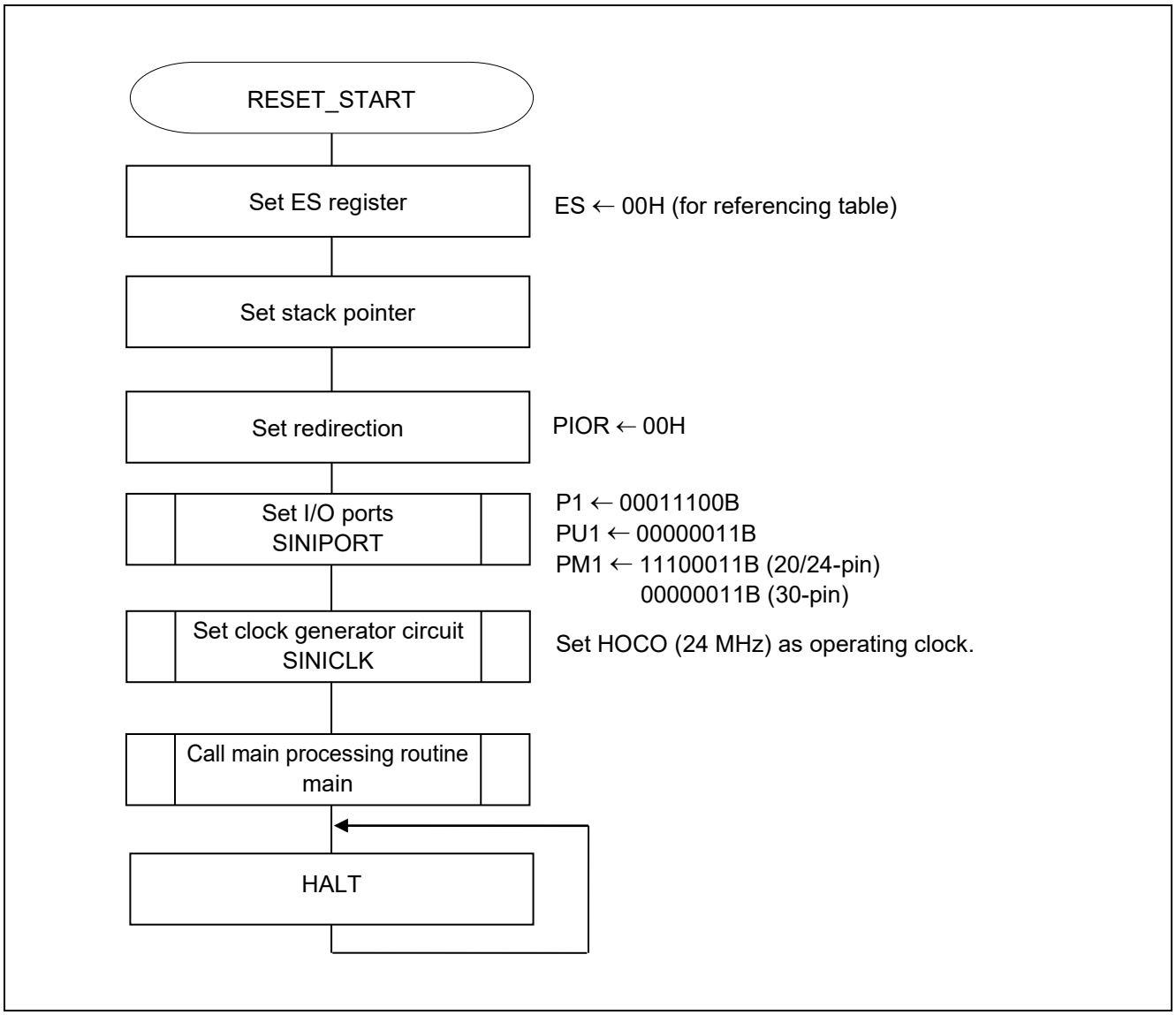


Figure 4.2 CPU Initialization Function

4.5.2 Setting up the I/O Ports

Figure 4.3 shows the flowchart for setting up the I/O ports.

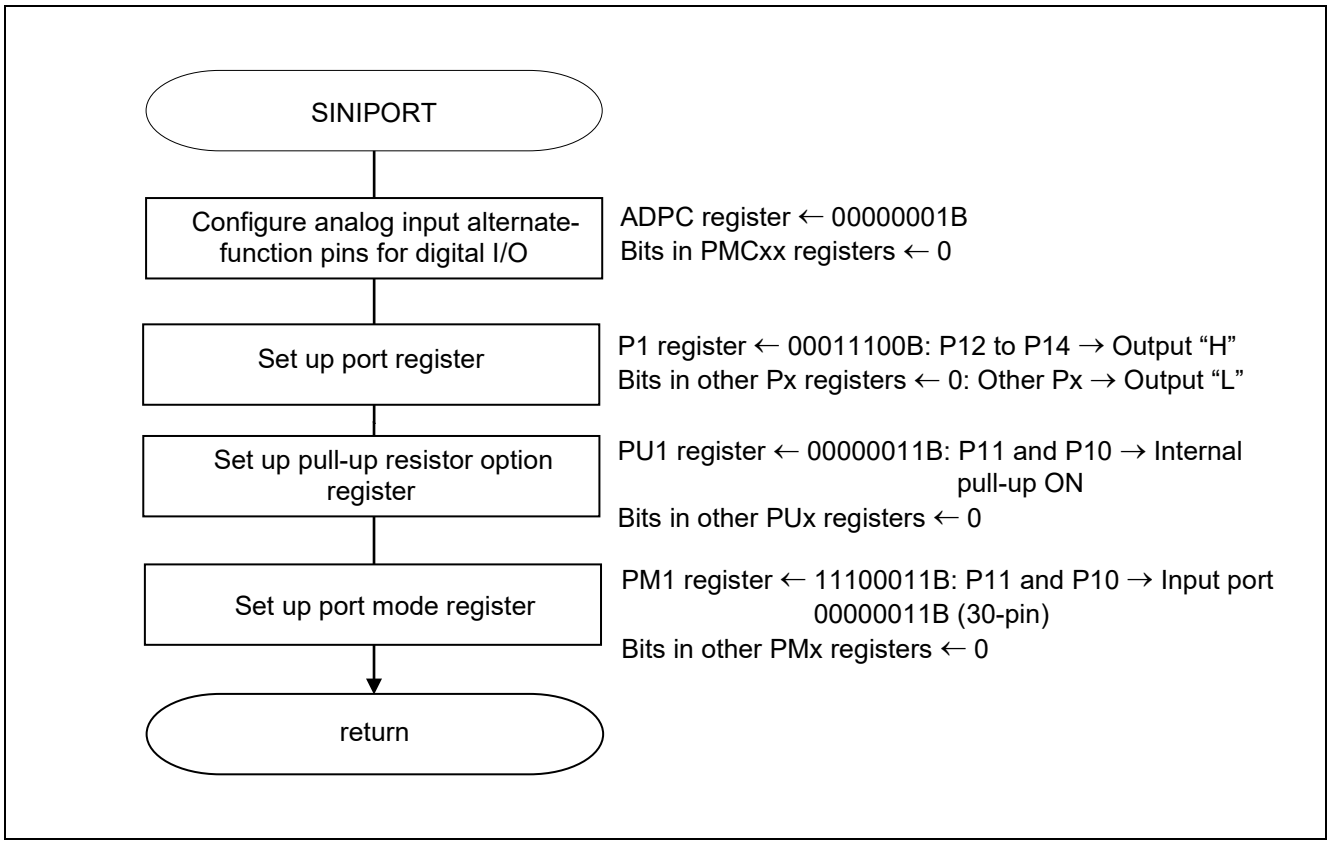


Figure 4.3 I/O Port Setup

Outline of I/O Port Setup

The RL78/G12 is equipped with digital I/O ports so that it can provide a variety of controls.

The I/O ports serve multiple pin functions in addition to serving as digital I/O ports.

The I/O ports are controlled by the registers listed below. They must be set up during the system initialization routine that is executed when power is first supplied or after the release of the reset state.

Registers that are used to manipulate ports:

- Port mode register (PMxx)
- Port register (Pxx)
- Pull-up resistor option register (PUxx)
- Port input mode register (PIMx)
- Port output mode register (POMx)
- Port mode control register (PMCxx)Note1
- A/D port configuration register (ADPC)Note1

Note 1. A register used to place port pins in digital I/O or analog input mode. Since the port pins are configured for analog input when a reset signal occurs, the pins that are to be used for digital I/O must always be set up with this register after the release of the reset state. For the sample program described in this application note, all port pins are configured for digital I/O.

Notes 1. Refer to RL78/G12 User's Manual Manual: Hardware for the procedure to set up registers to configure ports as alternate-function pins for peripheral functions.
2. Provide proper treatment for unused pins so that their electrical specifications are observed. Connect each of any unused input-only ports to V_{DD} or V_{SS} via a resistor, independently.

Given below is an example of manipulating ports that are used in this sample code.

Setting Up Ports for LEDs

- Port mode register 1 (PM1)
  P12: LED0
  P13: LED1
  P14: LED2

Setting Up Ports for Switches

- Port mode register 1 (PM1)
- Pull-up resistor option register 1 (PU1)
  P10: SW1
  P11: SW2

Symbol: PM1

7	6	5	4	3	2	1	0
PM17	**PM16**	**PM15**	**PM14**	**PM13**	**PM12**	**PM11**	**PM10**
0/1 Note1	**0/1**Note1	**0/1**Note1	**0**	**0**	**0**	**1**	**1**

PM1n	PM1n Pin I/O Mode Selection (n = 0 to 4)
0	**Output mode (output buffer on)**
1	**Input mode (output buffer off)**

Note 1. The setting differs depending on the product. These pins are not present on 20/24-pin products, so the setting is 1. On 30-pin products the setting is 0.

Notes 1. This sample code configures any unused ports for output to minimize the adverse influence of through current.
2. For details on the procedure for setting up the registers, refer to RL78/G12 User's Manual: Hardware.

Symbol: PU1

7	6	5	4	3	2	1	0
PU17	PU16	PU15	PU14	PU13	PU12	**PU11**	**PU10**
0	0	0	0	0	0	**1**	**1**

PU1n	Selection of On-Chip Pull-Up Resistor for P1n Pin
0	On-chip pull-up resistor not connected.
1	**On-chip pull-up resistor connected.**

4.5.3 Clock Generator Circuit Settings

Figure 4.4 shows a flowchart of the clock generator circuit settings.

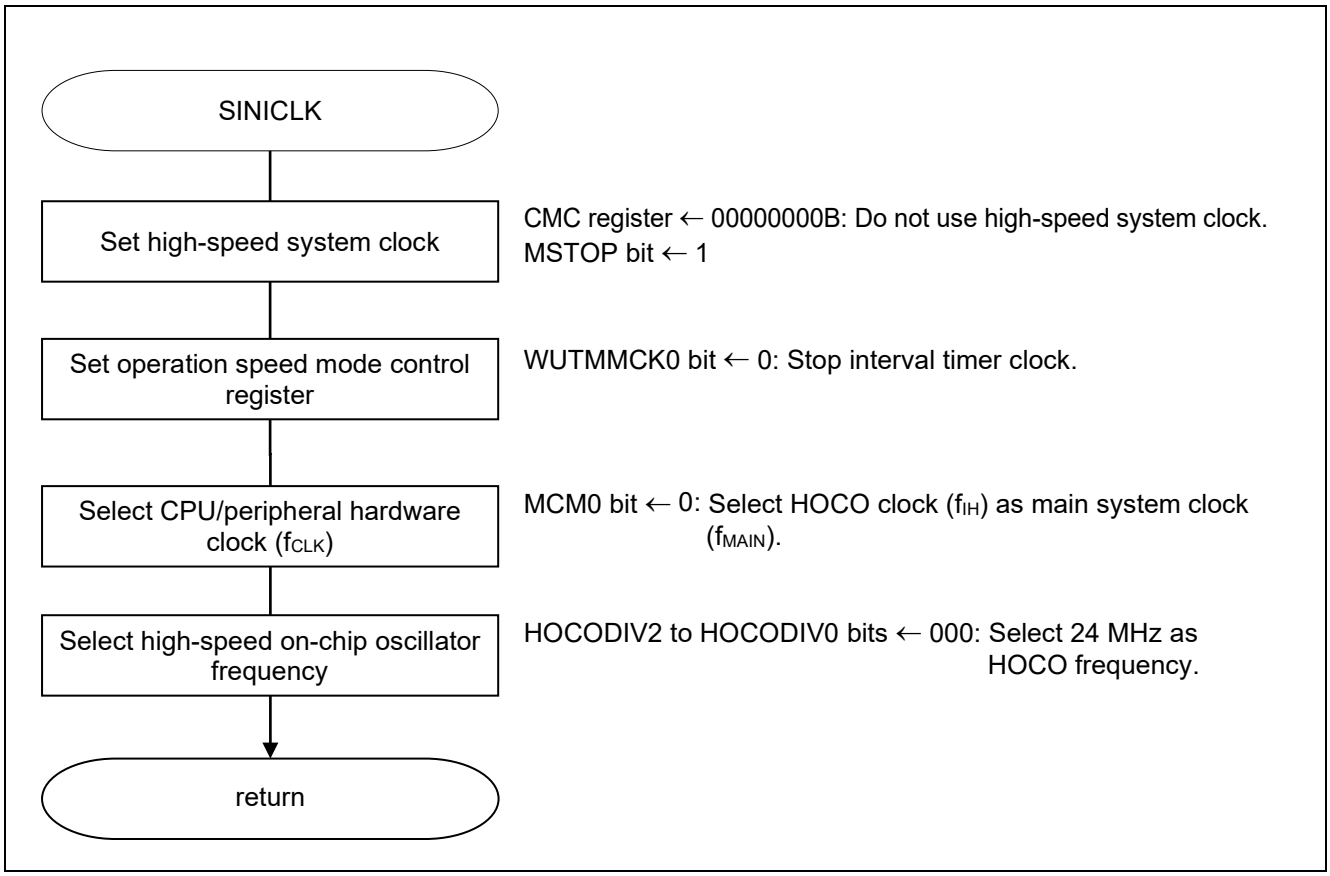


Figure 4.4 Clock Generator Circuit Settings

Outline of CPU Clock Setup

The RL78/G12 allows the user to select the system clock source from the high-speed on-chip oscillator (HOCO) and main system clock oscillator/external clock input.

The system clock is controlled by the registers listed below.

The CPU clock must be initialized during the system initialization routine that is executed when power is first supplied or after the release of the reset state.

Registers that are used to initialize the clock generator:

- Clock operation mode control register (CMC)
- Clock operation status control register (CSC)
- Operation speed mode control register (OSMC)
- System clock control register (CKC)
- High-speed on-chip oscillator frequency selection register (HOCODIV)
- Peripheral enable register 0 (PER0)

Given below is an example of setting up the clock generator for this sample code.

Setting Up the Clock Operating Mode

- Clock operation mode control register (CMC)
  High-speed system clock pin's operating mode: Input port mode
  X1 clock oscillation frequency control: 1 MHz ≤ fx ≤ 10 MHz

Symbol: CMC

7	6	5	4	3	2	1	0
EXCLK	**OSCSEL**	0	0	0	0	0	**AMPH**
0	**0**	0	0	0	0	0	**0**

Bit 0

AMPH	Control of X1 Clock Oscillation Frequency
0	**1 MHz ≤ fx ≤ 10 MHz**
1	10 MHz < fx ≤ 20 MHz

Bit 7 and 6

EXCLK	OSCSEL	High-speed System Clock Pin Operating Mode	X1/P121 Pin	X2/EXCLK/P122 Pin
0	**0**	**Input port mode**	**Input port**	
0	1	X1 oscillation mode	Connected to crystal/ceramic oscillator	
1	0	Input port mode	Input port	
1	1	External clock input mode	Input port	External clock input

Note: For details on the procedure for setting up the registers, refer to RL78/G12 User's Manual: Hardware.

Controlling Clock Operations

- Clock operation status control register (CSC)
  High-speed system clock operation control: Stop X1 oscillator.
  HOCO clock operation control: HOCO operation

Symbol: CSC

7	6	5	4	3	2	1	0
MSTOP	1	0	0	0	0	0	**HIOSTOP**
1	1	0	0	0	0	0	**0**

Bit 0

HIOSTOP	Control of HOCO Clock Operation
0	**Runs HOCO.**
1	Stops HOCO.

Bit 7

MSTOP	Control of High-speed System Clock Operation		
	X1 Oscillation Mode	External Clock Input Mode	Input Port Mode
0	Runs X1 oscillator.	Enables external clock from the EXCLKS pin.	**Input port**
1	**Stops X1 oscillator.**	**Disables external clock from the EXCLK pin.**	

Note: For details on the procedure for setting up the registers, refer to RL78/G12 User's Manual: Hardware.

Setting Up the CPU/Peripheral Hardware Clock (f_{CLK})

- System clock control register (CKC)
  f_{CLK} status: Main system clock
  f_{CLK} selection: HOCO clock (f_{IH})

Symbol: CKC

7	6	**5**	**4**	3	2	1	0
0	0	**MCS**	**MCM0**	0	0	0	0
0	0	**0**	**0**	0	0	0	0

Bit 4

MCM0	Control of Main System Clock (f_{MAIN}) Operation
0	**Selects HOCO clock (f_{IH}) as the main system cock (f_{MAIN}).**
1	Selects high-speed system clock (f_{MX}) as the main system clock (f_{MAIN}).

Bit 5

MCS	Main system clock (f_{MAIN}) state
0	**HOCO clock (f_{IH})**
1	High-speed system clock (f_{MX})

Note: For details on the procedure for setting up the registers, refer to RL78/G12 User's Manual: Hardware.

Setting Use/Disuse of Peripheral Hardware Macros

- Peripheral enable register 0 (PER0)
  Hardware input clock control: Stop input clocks.

Symbol: PER0

7	6	**5**	**4**	**3**	**2**	1	**0**
TMKAEN	0	**ADCEN**	**IICA0EN**	**SAU1EN**Note1	**SAU0EN**	0	**TAU0EN**
0	0	**0**	**0**	**0**	**0**	0	**0**

Bit 0

TAU0EN	Control of Timer Array Unit 0 Input Clock Supply
0	**Stops input clock supply.** • **SFR used by timer array unit 0 cannot be written.** • **Timer array unit 0 is in the reset status.**
1	Enables input clock supply. • SFR used by timer array unit 0 can be read and written.

Bit 3 and 2

SAUmEN	Control of Serial Array Unit m Input Clock Supply
0	**Stops input clock supply.** • **SFR used by serial array unit m cannot be written.** • **Serial array unit m is in the reset status.**
1	Enables input clock supply. • SFR used by serial array unit m can be read and written.

Bit 4

IICA0EN	Control of Serial Interface IICA0 Input Clock Supply
0	**Stops input clock supply.** • **SFR used by the serial interface IICA0 cannot be written.** • **Serial interface IICA0 is in the reset state.**
1	Enables input clock supply. • SFR used by the serial interface IICA0 can be read and written.

Bit 5

ADCEN	Control of A/D Converter Input Clock Supply
0	**Stops input clock supply.** • **SFR used by the A/D converter cannot be written.** • **A/D converter is in the reset status.**
1	Enables input clock supply. • SFR used by the A/D converter can be read and written.

Bit 7

TMKAEN	Control of 12-Bit Interval Timer Input Clock Supply
0	**Stops input clock supply.** • **SFR used by the 12-bit interval timer cannot be written.** • **The 12-bit interval timer is in the reset status.**
1	Enables input clock supply. • SFR used by the 12-bit interval timer can be read and written.

Note 1. For 30-pin products only.

Note: Power saving and noise reduction are achieved by stopping the supply of clocks to any unused hardware macros.

Controlling the Operation Speed Mode

- Operation speed mode control register (OSMC)
  Selection of interval timer operation clock: Clock supply stopped

Symbol: OSMC

7	6	5	**4**	3	2	1	0
0	0	0	**WUTMMCK0**	0	0	0	0
0	0	0	**0**	0	0	0	0

Bit 4

WUTMMCK0	Selection of Operation Clock for Realtime Clock and Interval Timer
0	**Clock supply stopped.**
1	Enables LOCO Clock (f_{IL}) supply.

Note: The OSMC register is designed to reduce the operating current in STOP mode and thereby lower power consumption. For details on the procedure for setting up the registers, refer to RL78/G12 User's Manual: Hardware.

4.5.4 Main Processing

Figure 4.5 shows the flowchart for the main processing routine.

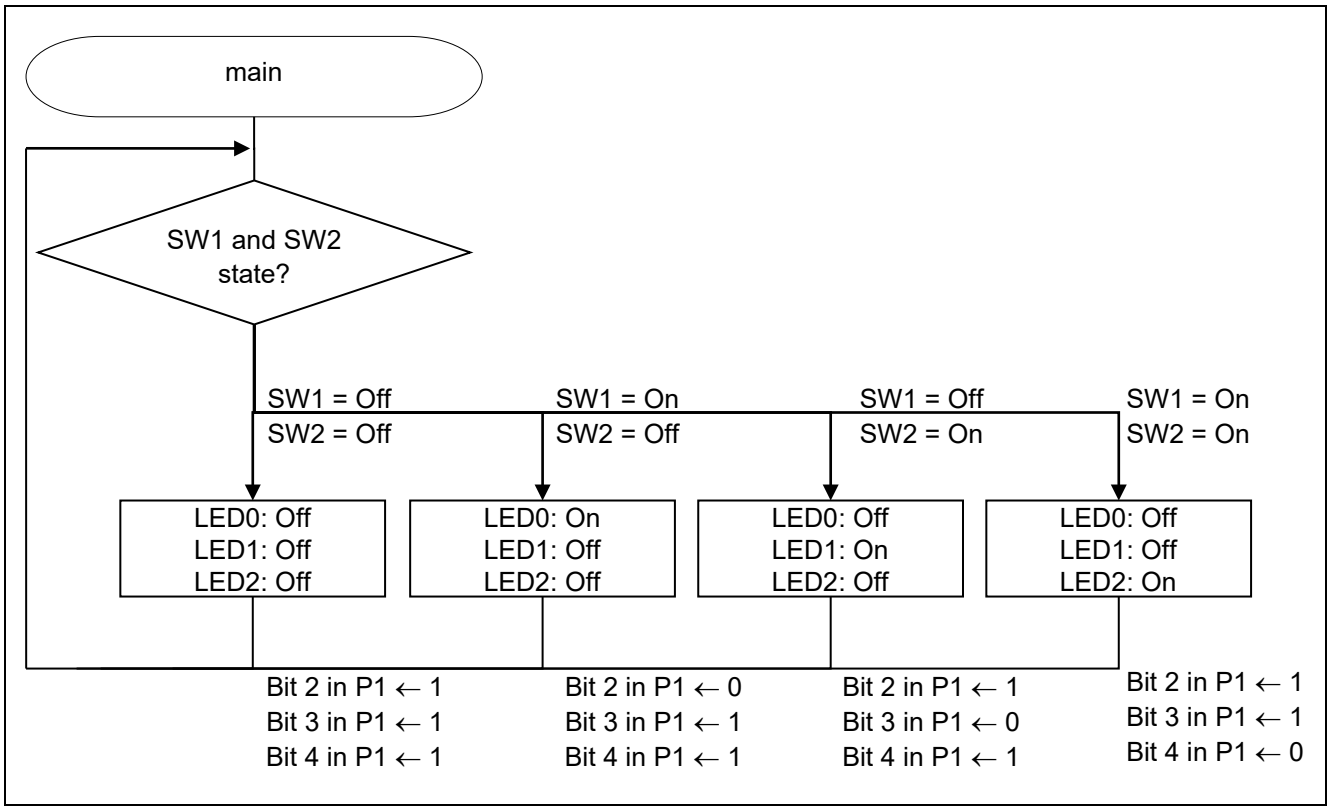


Figure 4.5 Main Processing

5. Selecting/Changing the Target Device

5.1 Selecting the Target Device

Depending on the pin count, the number of available pins differs. To accommodate this difference, the CPU initialization function of the sample program includes a file (r_init.asm) that uses the assembler control instructions $IF … $ENDIF to allow selection of the instructions appropriate to each product. The name of the product to be used is defined as shown below. For example, when using the 20-pin product without data flash memory, only R5F1026 should be preceded by **(.set 1)** and the other product names preceded by **(.set 0)**

```
R5F1026 .set 1      ; 20 pins with data flash memory ⇐ This is the product to be used.
R5F1036 .set 0      ; 20 pins without data flash memory
R5F1027 .set 0      ; 24 pins with data flash memory
R5F1037 .set 0      ; 24 pins without data flash memory
R5F102A .set 0      ; 30 pins with data flash memory
R5F103A .set 0      ; 30 pins without data flash memory
```

Figure 5.1 Specifying the Product to Be Used

When the product version is defined in this way, among the P1-related settings (which differ depending on the product) only those for which the $IF control instruction contains R5F1026 are true, and the subsequent lines up to $ENDIF or $ELSEIF are processed by the assembler.

```
$IF( R5F1026 + R5F1036 + R5F1027 + R5F1037)

;---------------------------------------------------------------------
;       for 20 and 24 pins
;---------------------------------------------------------------------
        MOV    PM1,    #11100011B    ; P12-P14 to output port
                                     ; P10 and P11 to input port

$ELSEIF( R5F102A + R5F103A)

;---------------------------------------------------------------------
;       for 30 pins
;---------------------------------------------------------------------
        MOV    PM1,    #00000011B    ; P12-P17 to output port
                                     ; P10 and P11 to input port

$ENDIF
```

R5F1026 is included, so this portion only is processed by the assembler.

This portion is ignored by the assembler.

Figure 5.2 Program Example

Note: **LIST/NOLIST** control instructions have been added so that device settings for other than the specified product version are not output to the assemble list file. This means that unnecessary information, including the $IF control instructions, etc., are not visible. However, $LIST/$NOLIST is output.

5.2 Changing the Target Device

To change the target device used with the sample program it is necessary to create a new project. The sample project should be used as the basis when doing this.

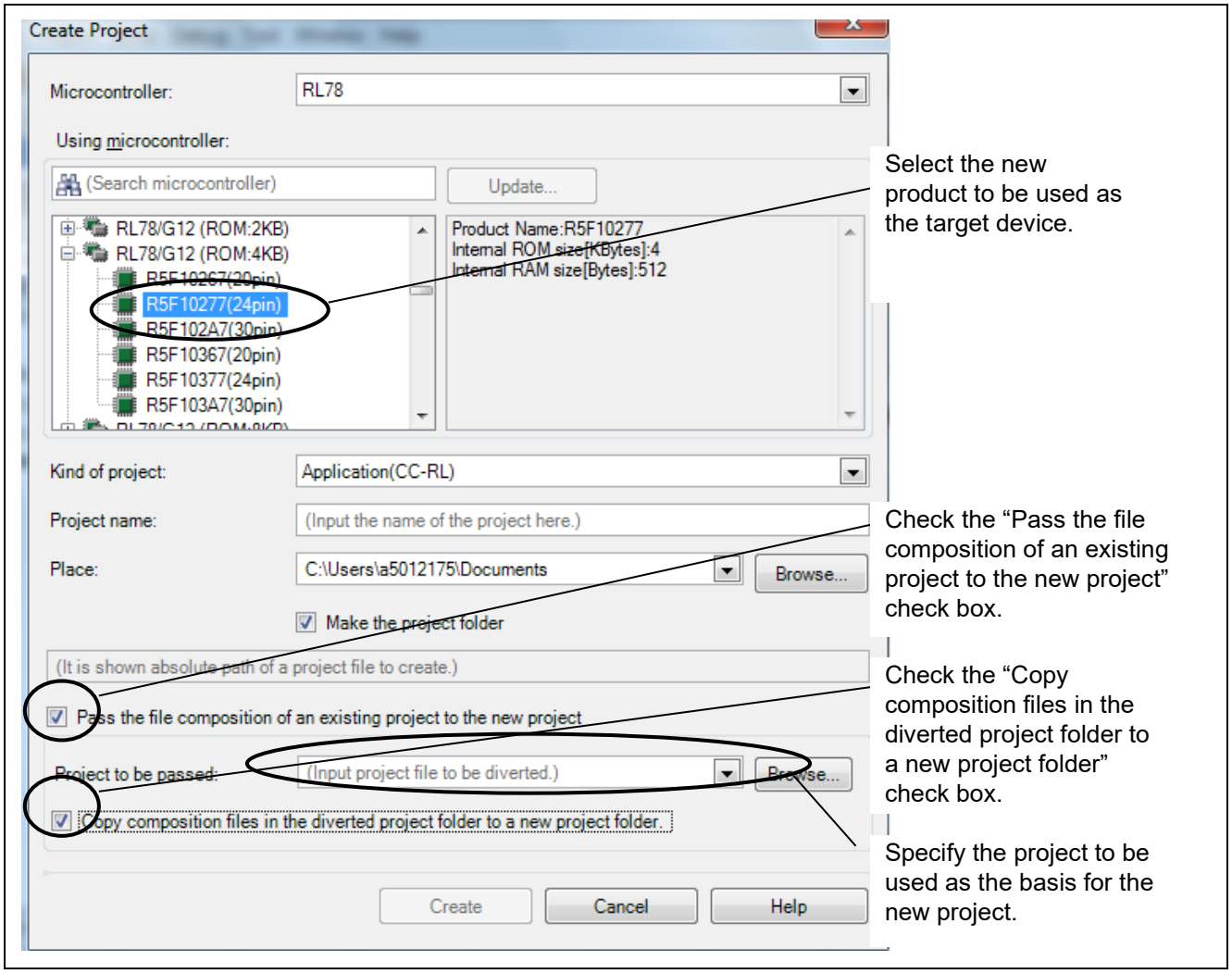


Figure 5.3 Example of Creating a New Project in Order to Change the Target Device

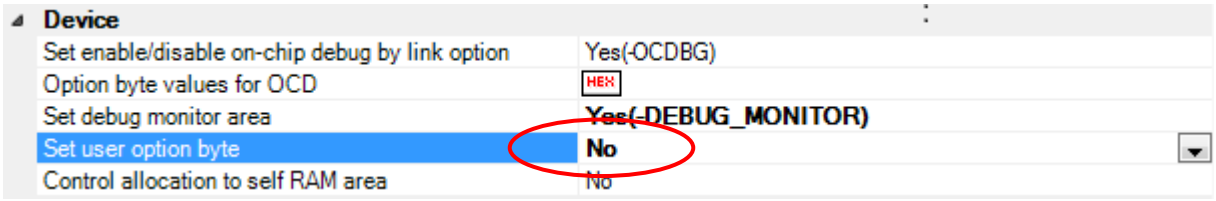
6. Notes on Using the Sample Code

The sample code is written entirely in assembly language. This means that the code generation function of CS+ cannot be used. As a consequence, care must be exercised with regard to certain settings.

6.1 CS+ Settings

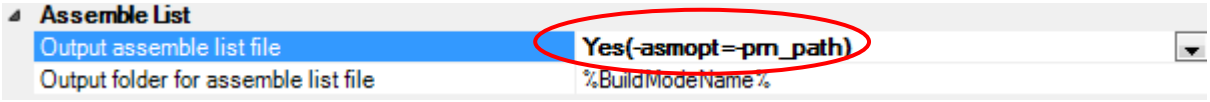
Since the sample code is written entirely in assembly language, some functions of CS+ must be disabled.

- Set the link options in the CC-RL properties as shown below. If this setting is not made, the watchdog timer may reset the device at regular intervals.



This will cause the following warning (W0403029 and W0403023) to appear in the output messages during code generation, but the warning can be ignored.

- Assemble Option Settings
  The setting shown below is recommended but not required. It enables output lists that addresses are determined after linking.
  Open the “Assemble List” settings and change the setting of the second item, “Output assemble list file,” to “Yes.”

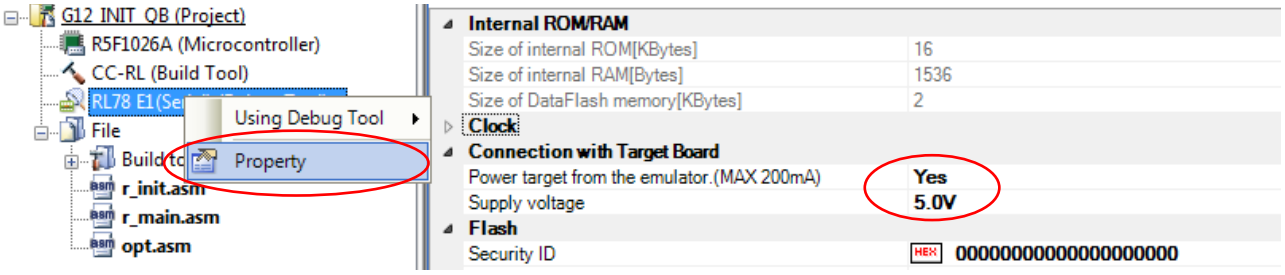


6.2 Debug Tool Settings

The sample code can be used to check the operation of the device simply by adding two switches and one LED to the RL78/G12 target board (QB-R5F1026A-TB). Power can be supplied to the target board from the emulator. This makes it possible to use a simple circuit to perform debugging.

The necessary settings are as follows:

(1) Open the RL78 E1 (Serial) (Debug Tool) properties.
(2) Under “Connection to target board,” set “Supply power from emulator” to “Yes” and set the voltage to “5.0 V.”



7. Sample Code

The sample code is available on the Renesas Electronics Website.

8. Documents for Reference

RL78/G12 User's Manual Manual: Hardware (R01UH0200E)

RL78 Family User's Manual: Software (R01US0015E)

(The latest versions of the documents are available on the Renesas Electronics Website.)

Technical Updates/Technical Brochures

(The latest versions of the documents are available on the Renesas Electronics Website.)

Revision History

Rev.	Date	Description	
		Page	Summary
1.00	Mar. 20, 2015	—	First edition issued
2.00	Nov. 11, 2015	3	Table 2.1: Added e^{2}studio
		3	Table 2.1:Change the version information of CS+
2.10	June. 24. 2022	3	Operation check condition is updated.

General Precautions in the Handling of Microprocessing Unit and Microcontroller Unit Products

The following usage notes are applicable to all Microprocessing unit and Microcontroller unit products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Precaution against Electrostatic Discharge (ESD)
   A strong electrical field, when exposed to a CMOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop the generation of static electricity as much as possible, and quickly dissipate it when it occurs. Environmental control must be adequate. When it is dry, a humidifier should be used. This is recommended to avoid using insulators that can easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors must be grounded. The operator must also be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions must be taken for printed circuit boards with mounted semiconductor devices.
2. Processing at power-on
   The state of the product is undefined at the time when power is supplied. The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the time when power is supplied. In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the time when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the time when power is supplied until the power reaches the level at which resetting is specified.
3. Input of signal during power-off state
   Do not input signals or an I/O pull-up power supply while the device is powered off. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Follow the guideline for input signal during power-off state as described in your product documentation.
4. Handling of unused pins
   Handle unused pins in accordance with the directions given under handling of unused pins in the manual. The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of the LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible.
5. Clock signals
   After applying a reset, only release the reset line after the operating clock signal becomes stable. When switching the clock signal during program execution, wait until the target clock signal is stabilized. When the clock signal is generated with an external resonator or from an external oscillator during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Additionally, when switching to a clock signal produced with an external resonator or by an external oscillator while program execution is in progress, wait until the target clock signal is stable.
6. Voltage application waveform at input pin
   Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between V_{IL} (Max.) and V_{IH} (Min.) due to noise, for example, the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between V_{IL} (Max.) and V_{IH} (Min.).
7. Prohibition of access to reserved addresses
   Access to reserved addresses is prohibited. The reserved addresses are provided for possible future expansion of functions. Do not access these addresses as the correct operation of the LSI is not guaranteed.
8. Differences between products
   Before changing from one product to another, for example to a product with a different part number, confirm that the change will not lead to problems. The characteristics of a microprocessing unit or microcontroller unit products in the same group but having a different part number might differ in terms of internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

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Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu,
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