R2A20113A

Application Note

R03AN0006EJ0100
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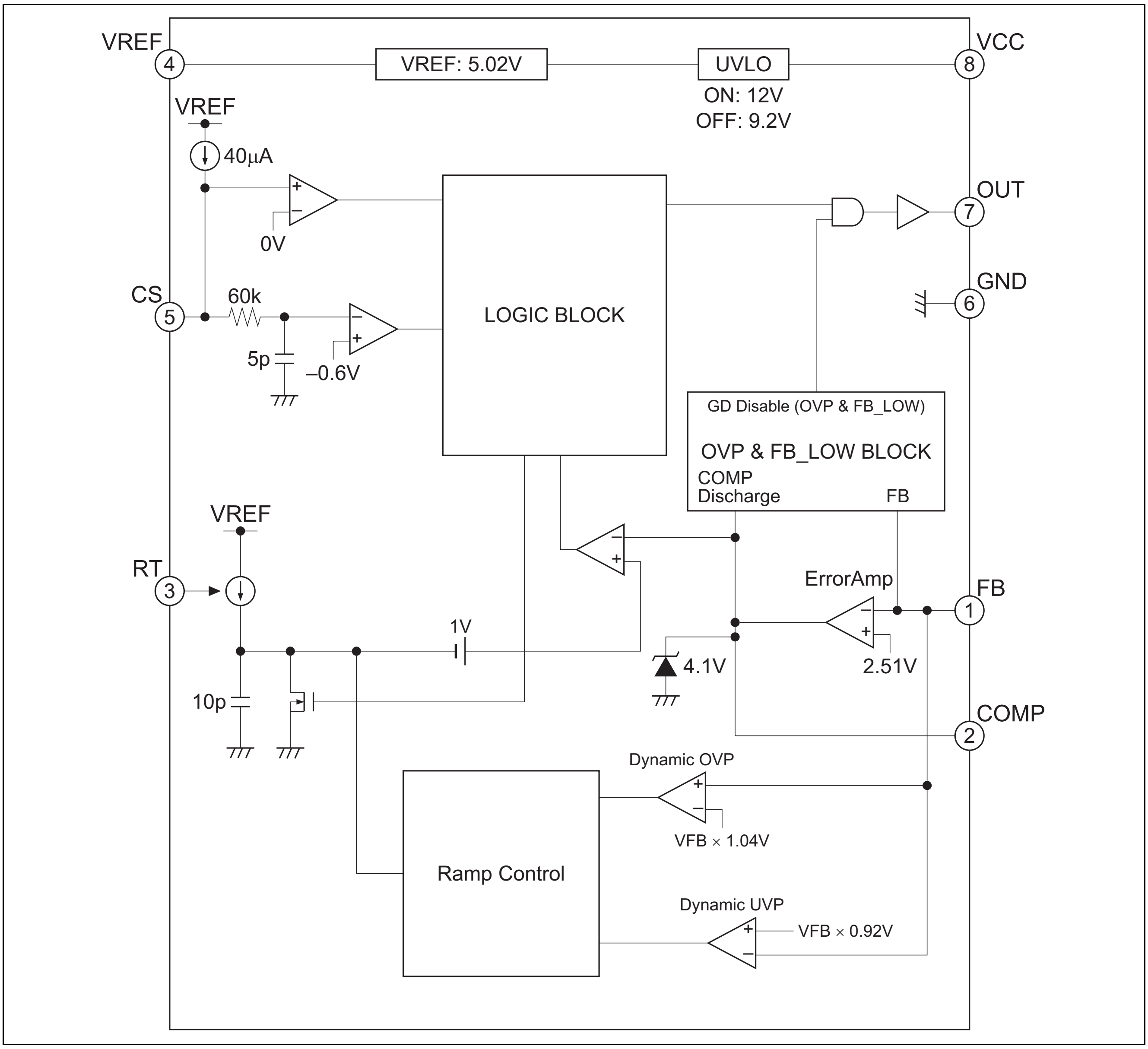
1. Outline

The R2A20113A is the active power factor correction controller that operates in the critical conduction mode (CRM).

The R2A20113A is the voltage mode CRM, such that the Power MOSFET controlled by this IC is turned on when the current of the boost inductor reaches zero and also controlled to keep ON time of the Power MOSFET constant. So, the peak current of the boost inductor follows the input voltage waveform.

The voltage mode CRM PFC controller does not need the input voltage sense line. So, the power loss of the system can be reduced.

2. Block Diagram



3. Descriptions of the R2A20113A Functional Blocks

3.1 Reference Voltage Output (VREF)

R2A20113A has 5 V reference voltage output terminal (VREF). (accuracy: 5.02 V ± 1.5%)

VREF pin outputs 5 V when the UVLO protection is released.

If VREF output is used for an external circuit, the load should be under the current source capacity of 5 mA (Max).

3.2 Zero-Current Detection

The Zero-Current Detection (ZCD) detects the zero-current of the inductor, and the Power MOSFET is turned on at that time. After being converted from the GND-current to the voltage by the sensing resistor Rcs, the ZCD signal is supplied to the CS-pin.

The threshold voltage for ZCD is 0 V (typ.). The delay time is set to 0.44 μs, in which the drain voltage of the MOSFET decreases after the threshold voltage is detected.

Due to the offset of the zero-current, it is advised to tune the threshold voltage for ZCD to the negative side by inputting the resistor for the filtering between Rcs and the CS-pin.

Furthermore, as the threshold voltage of the ZCD is small, such as several mV, R2A20113A has the 0.2 μs mask function to prevent erroneous operations due to noises. By the 0.2 μs mask function, the output signal of the ZCD would be sent to the latter part, only when the zero current continues over the 0.2 μs mask period.

The delay time is fixed and includes 0.2 μs of the mask function.

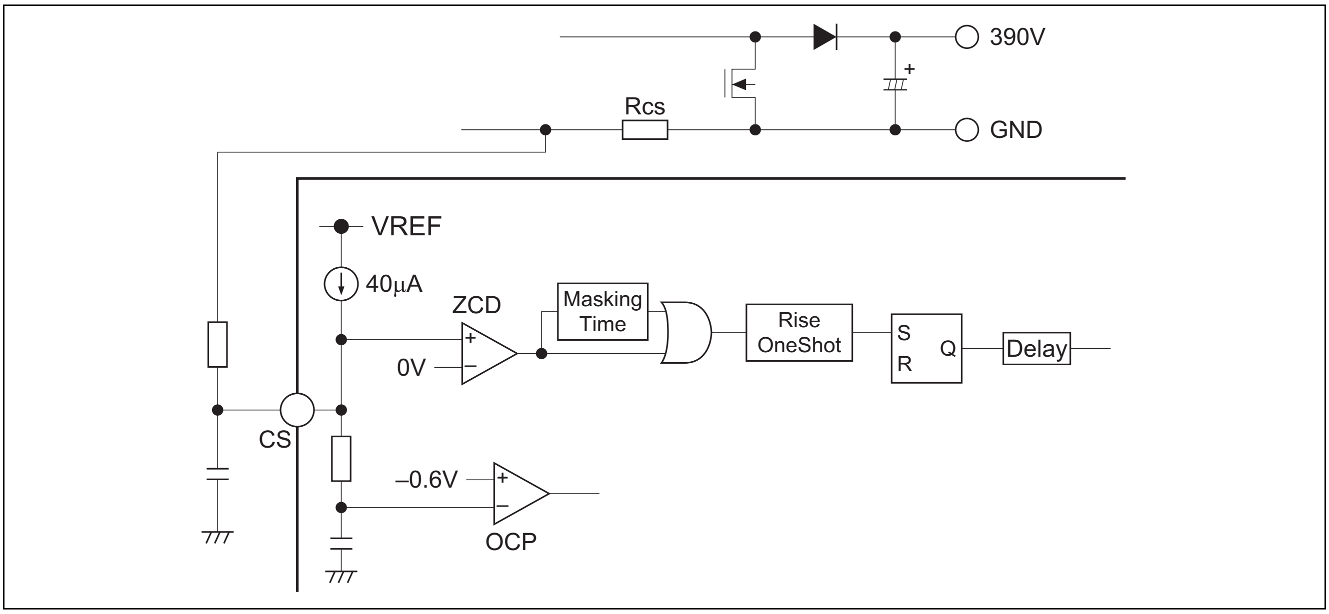


Figure 1

3.3 Error Amplifier

The error amplifier of PFC control is a trance conductance amplifier.

The output current changes according to a voltage difference between FB pin voltage and the internal reference voltage.

COMP pin which is output of error amplifier is clamped by 4.1 V (typ).

3.4 RAMP Slope (IC-Internal)

The slope at point RAMP within the chip depends on the current determined by the external resistor R_{RT} on the RT pin and on-chip 10-pF capacitor.

The resistor R_{RT} is connected between the RT pin and the GND level.

The maximum ON time, tonmax, is determined when the output voltage of the error amplifier is 4.1 V (typ.). The RAMP circuit starts charging the RAMP capacitor when the ZCD circuit detects inductor zerocurrent and at the same time, the voltage at the point, "RAMP portion" is smaller than 0.2 V.

The RAMP circuit starts discharging the "RAMP portion" when the RAMP slope reaches COMP voltage.

And when the output voltage of the error amplifier is smaller than 1 V, the Power MOSFET ON time is zero, due to the built-in level shift voltage of 1 V.

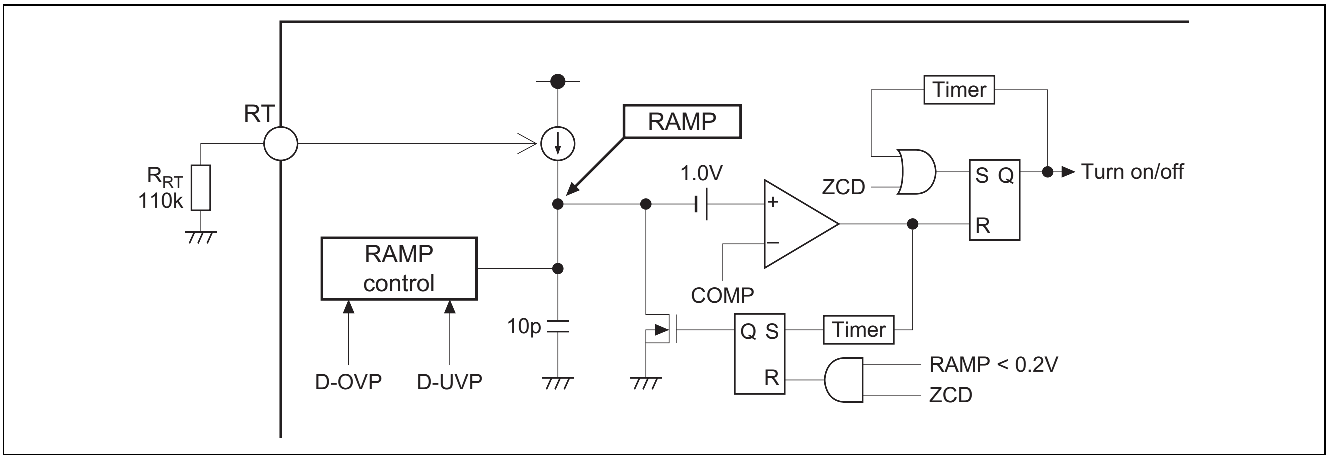


Figure 2

3.5 Output Stage

R2A20113A contains the single totem-pole output stage.

The drivability is +900 mA/–500 mA (peak). "+" means that the current flows into the IC.

Basically, direct driving of the power MOSFET is possible. However, please adjust drivability of the driver circuit on the board by selecting the appropriate parameters of the circuit according to the characteristics of the Power MOSFET to be used.

Due to zero-current switching, the speed of turning-off affects power loss more strongly than the speed of turning-on. The following figures show examples of driver circuits.

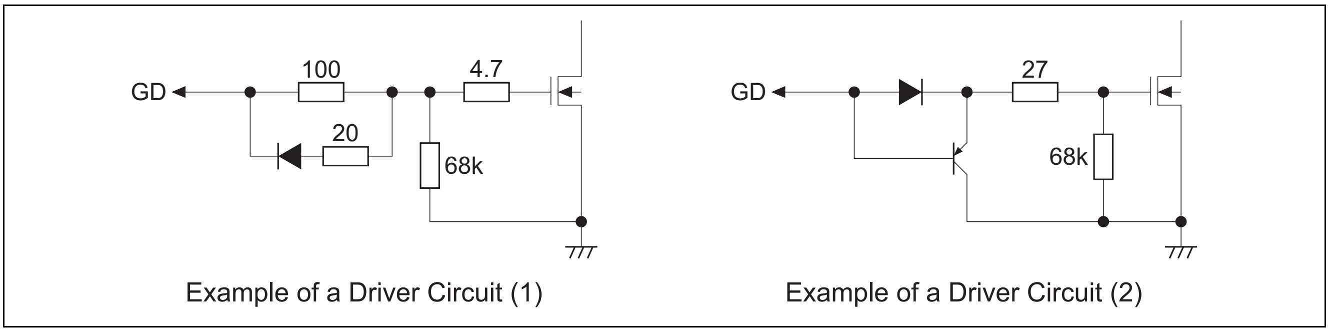


Figure 3

3.6 Protection

R2A20113A has the over voltage protection for PFC output voltage, feedback open loop protection, the over current protection, off time control function and so on.

3.6.1 Static Over Voltage Protection (S-OVP)

Static Over Voltage Protection stops an OUT signal when FB pin voltage reaches 1.08 × VFB (2.51 V typ).
A Power MOSFET turns off quickly and S-OVP keeps stopping an GD signal till FB pin voltage reaches 1.08 × VFB (2.51 V typ) – 100 mV.

3.6.2 Feedback Low Detection (FB-LOW)

The FeedBack LOW protection discharges COMP pin voltage during FB pin voltage is under 0.3 V.
Therefore an GD signal does not appears in this case.

3.6.3 Dynamic Over Voltage Function (D-OVP)

Dynamic Over Voltage Protection Function starts to decrease the On time of the MOSFET when FB pin voltage reaches 1.04 × VFB (2.51 V typ).
The Power MOSFET ON time is decreased gradually, so that, the audio noise, that occurs when the current of inductor stops suddenly, can be avoided.

3.6.4 Dynamic Under Voltage Function (D-UVP)

When the voltage of the FP-pin is less than 0.92 × VFB, R2A20113A starts to increase the On time of the MOSFET regardless of the COMP voltage. The maximum On time while D-UVP is working is twice as long as the On time at steady state.
This function is active when once the voltage of the FB-pin is more than 0.96 × VFB after the IC starts.

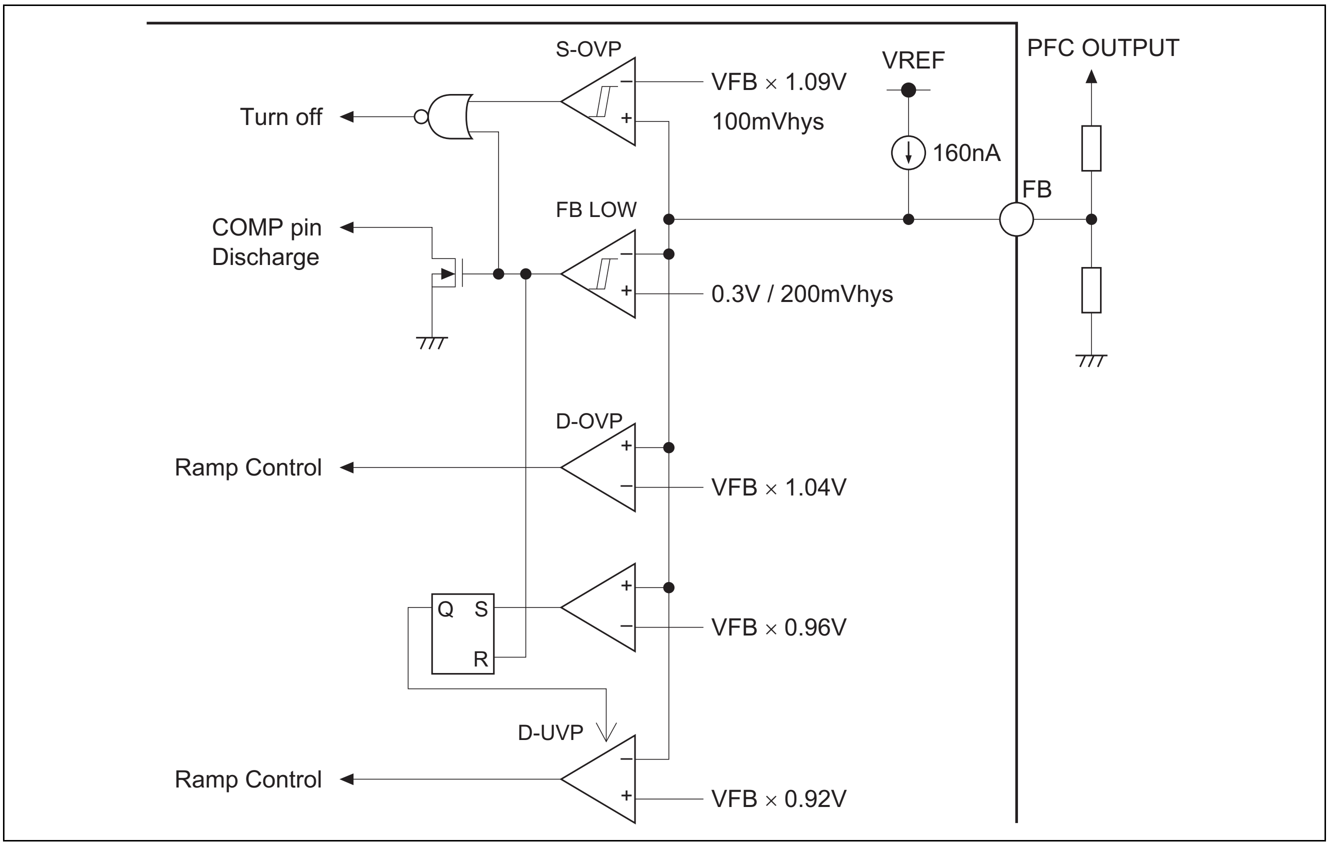


Figure 4

3.6.5 Over Current Protection (OCP)

This function defend Power MOSFET, boost inductor and boost Diode from over current.
OCP pin senses the each Power MOSFET source current by using an external sense resistor.
When OCP pin reaches –0.6V, an output is stopped with pulse-by-pulse.

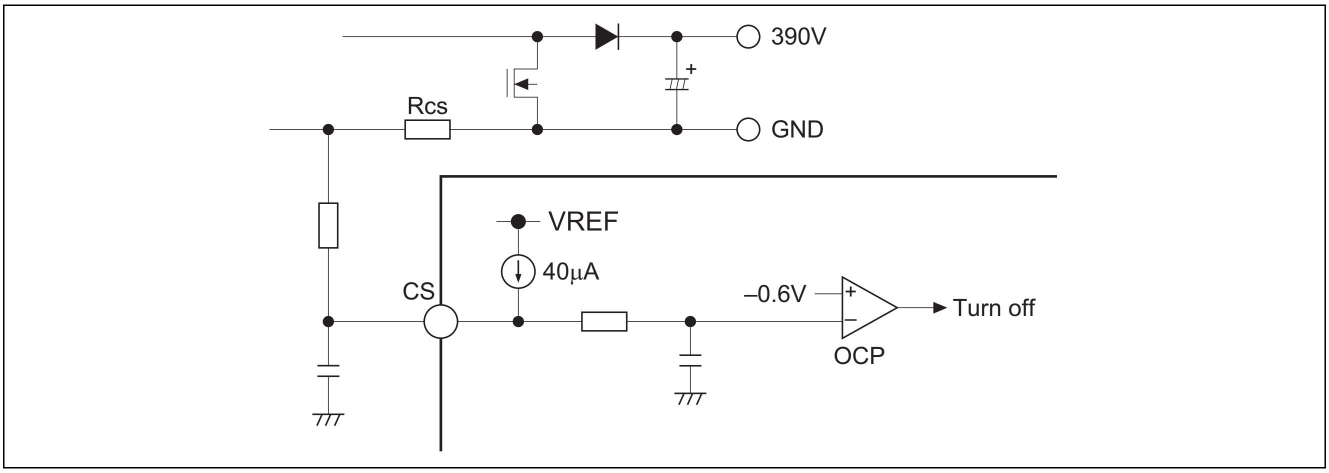


Figure 5

3.6.6 Off Time Control (Frequency Limit Function)

By masking ZCD signals for a certain period after the MOSFET shifts from On to Off, the frequency of the MOSFET switching is limited. So the decrease of the efficiency due to the MOSFET heating during the light load would be avoided.
The masking period is 1.4 µs (typ.).
ZCD signals are ignored during the masking period after the MOSFET shifts from On to Off. At the first signal of ZCD just after the masking period, the MOSFET is turned on.

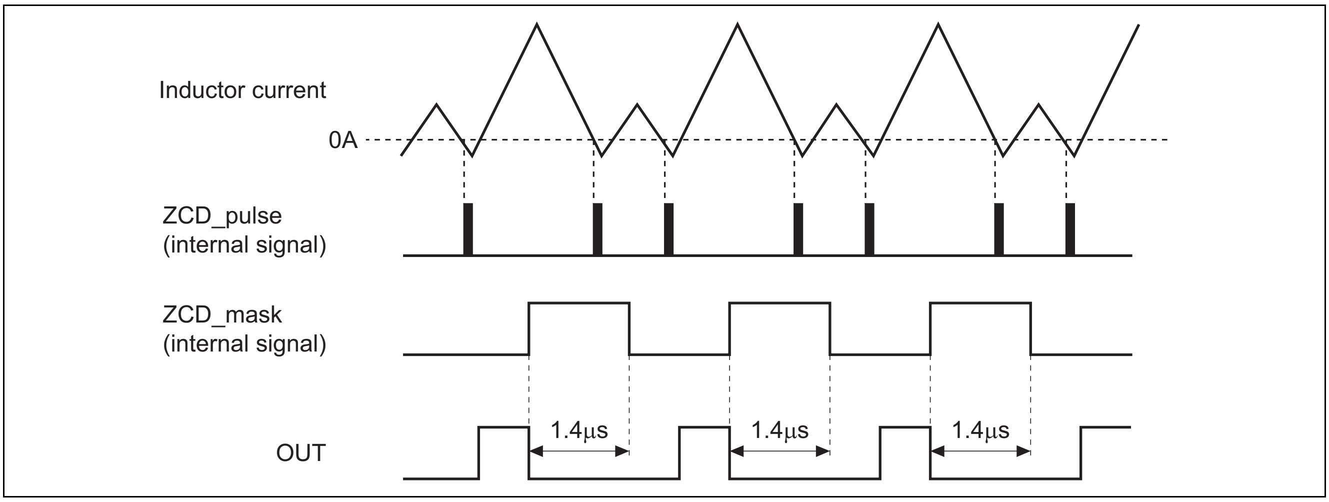


Figure 6 Example of Off Time Control

3.6.7 Restriction Function on Restart Mode

Although R2A20113A contains the function which turns on the MOSFET forcedly when there is no ZCD signal in a certain period, 150 μs (typ.), the IC stops the Restart mode in order to prevent the high current from flowing into the MOSFET under the situations as follows:

(Example 1) The case when the inrush current flows into the output capacitor through the boost inductor at the instance of turning on the AC input voltage.

(Example 2) The case when the peaks of the AC input voltage rectified by the diode bridge are larger than the total voltage of the PFC output voltage and the forward voltage of the boost diode.

In both examples, because the currents continue to flow into the boost inductors, the voltage of the CS-pin is negative. Under these situations like two examples above, R2A20113A stops the Restart mode.

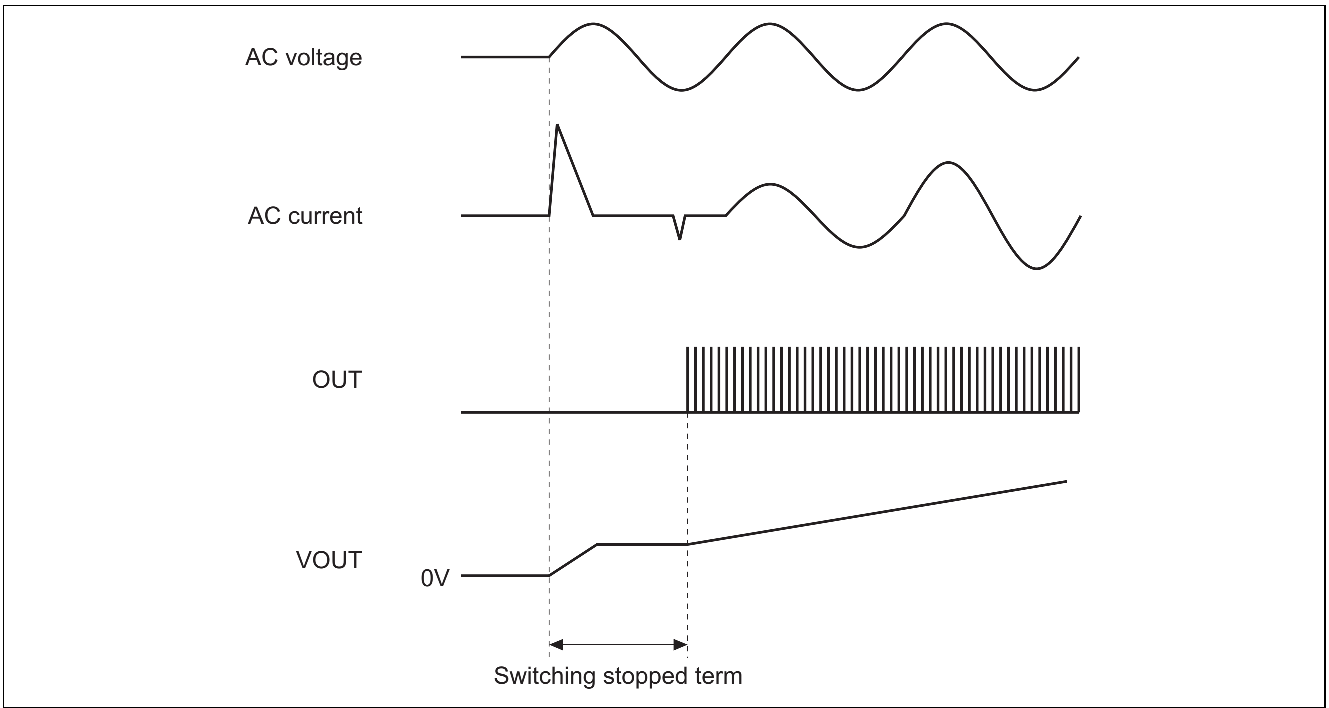


Figure 7 Example(1) Stop of the Switching Operation

4. Design Guide

4.1 Boost Inductor

The inductance of the boost inductor is determined by the output power and a minimum switching frequency.
A minimum switching frequency must be higher than 20 kHz which is audio frequency to avoid audio noise of the inductor or the input capacitor. The frequency is generally set to the frequency higher than 50 kHz.
The inductance of boost inductor is obtained by Equation 1.
Use the value around 0.9 as the conduction loss η.

$$L[H] = \frac{V_{ACLow}^2 \times [V_o - \sqrt{2} \times V_{ACLow}] \times \eta}{2 \times f_{SWLow} \times V_o^2 \times I_{omax}} \quad \cdots (1)$$

Vo [V]: PFC output voltage
V_{ACLow} [V]: Effective value of minimum input voltage
Iomax [A]: Maximum output current
f_{SWLow} [Hz]: Minimum switching frequency

4.2 Output Capacitance

The capacitance of the output capacitor for arbitrary hold-up time is expressed in the next equation.

$$C_o[F] \geq \frac{2 \times P_o \times t_{hold}}{V_o^2 - V_{omin}^2} \quad \cdots (2)$$

thold [s]: Hold-up time
Vomin [V]: Minimum output voltage

4.3 Power MOS FET and Boost Diode

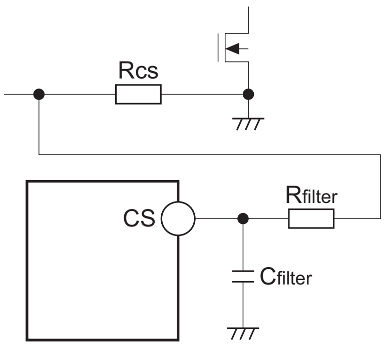
A peak current flowing on the Power MOSFET or the boost diode is expressed in the next equation. Use the value around 0.9 as the conduction loss η.

$$I_{Lpk}[A] = \frac{2\sqrt{2} \times P_o}{V_{ACLow} \times \eta} \quad \cdots (3)$$

4.4 Overcurrent-Detecting Resistor (Rcs)

RCS is obtained by Equation 4. Use the value around 0.9 as the conduction loss η.
RCS might be very small, so that care should be taken in the PCB pattern impedance.
And it is suggested that a CR filter of around 1MHz is put on the OCP pin to avoid a switching noise.
Also, use the value of 1.2 as the current-limiting factor β to allow a margin of 20% in the normal value of ILpk.

$$R_{cs}[\Omega] = \frac{0.6 \times V_{ACLow} \times \eta}{2\sqrt{2} \times P_o \times \beta} \quad \cdots (4)$$



Note: When Rcs becomes smaller, the voltage that is impressed to the terminal of CS becomes smaller. And then, it becomes easy for the restart operation to start at a high input voltage, and it causes the "sound bark", the audio noise of the inductor. This should be noted, when small value of Rcs is utilized to improve efficiency.
If you change the cutoff frequency of the filter, please set the resistance of Rfilter as a fixed value and adjust the capacitance of Cfilter. When the resistance of Rfilter is enlarged, it becomes easy for the restart operation to start.

4.5 The Resistance of RT

The maximum ON time (tonmax) is obtained from the following formula.
Use the value of around 0.9 as the conversion efficiency (the conduction loss) η.

$$Ton\ max[\mathrm{s}] = \frac{2 \times L \times Po}{VACLow^2 \times \eta} \quad \cdots (5)$$

Shown as figure 8, R2A20113A controls tonmax according to the resistance connected to the RT pin (RRT). By referring to figure 8, the resistance connected to the RT pin can be decided to achieve the tonmax calculated by the formula (5).

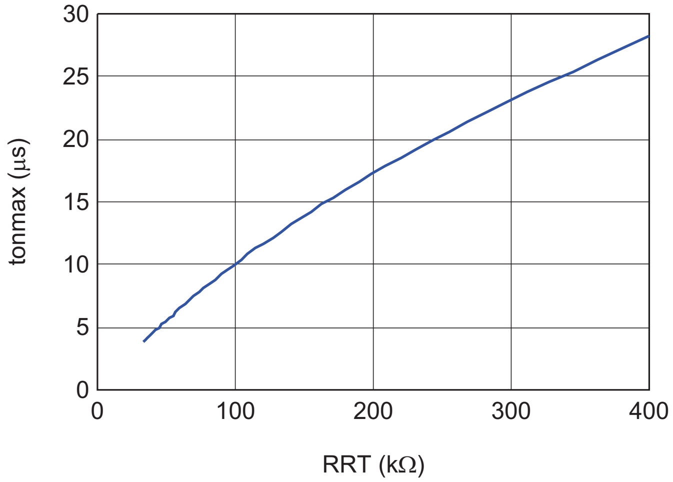


Figure 8 RRT–tonmax Characteristics

4.6 Soft Start Circuit and PFC OFF

If an over shoot of the PFC output or an audio noise of the inductor in start-up duration occurs and might be problems, an external soft start circuit should be added on the COMP pin.
Please refer to the figure 9(A) when you use the Q1 such that the tolerance of E-B reverse voltage is larger than the Vref voltage. Please refer to the figure 9(B) when you can not use the Q1 described above.
The soft start time is defined by CR time constant in figure 9(A) case. It is defined with charging time of COMP pin source current in figure 9(B). Though the soft start time should be decided and adjusted by the degrees of an over shoot and an audio noise level.
The operation of the PFC is stopped when the switch Q2 turns on and the COMP pin voltage becomes smaller than 1 V (typ).

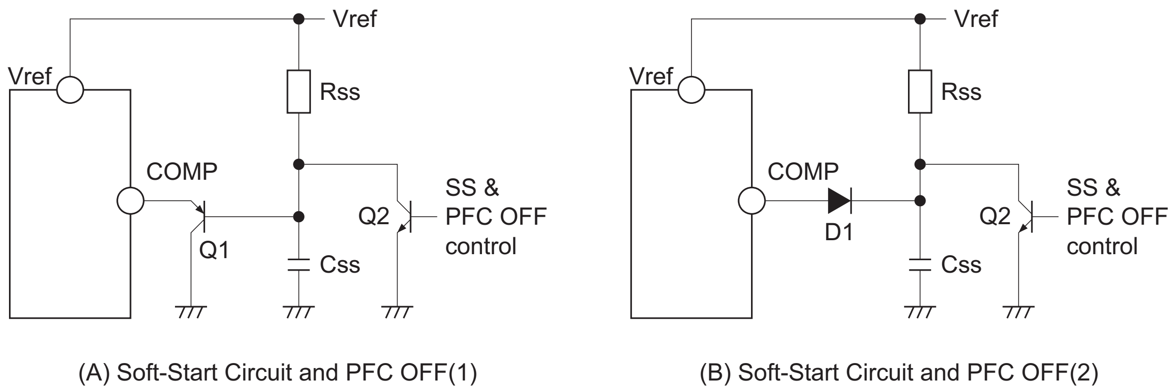
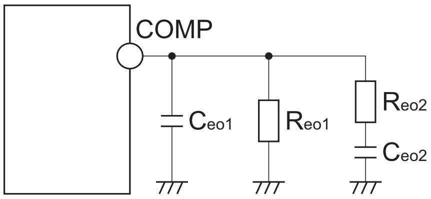


Figure 9

4.7 Frequency Characteristics of the Error Amplifier (gm Amplifier)

The error amplifier is a transconductance amplifier (gm amplifier). It does not need a feedback on input side. Therefore, it is possible to minimize influence on input circuit by a feedback circuit.
Gain of gm amplifier is calculated by product of transconductance and output impedance.
It is obtained by Equation 6, where Gm-v is tranceconductance of the gm amplifier and Rvo is an output resistor of the gm amplifier itself.
The overview of Gain-Frequency characteristics is shown in figure 10, in which the tendencies of the characteristics variation are illustrated when each parameter changes. Frequency characteristics of the amplifier is also shown in figure 11.

$$G_V = G_{m-v} \times \frac{1}{\dfrac{1}{R_{vo}} + \dfrac{1}{R_{eo1}} + j\omega C_{eo1} + \dfrac{1}{R_{eo2} + \dfrac{1}{j\omega C_{eo2}}}} \quad \cdots (6)$$



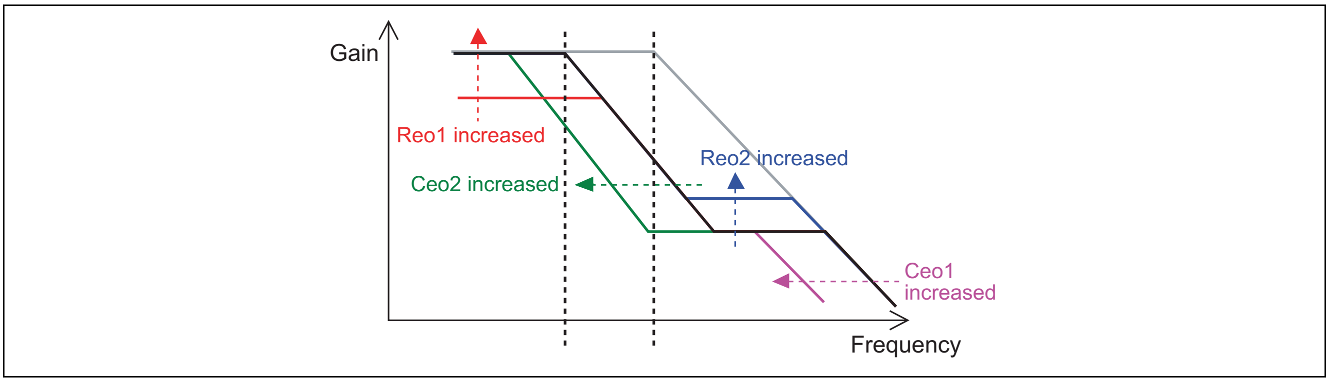


Figure 10 Overview of Gain–Frequency Characteristics

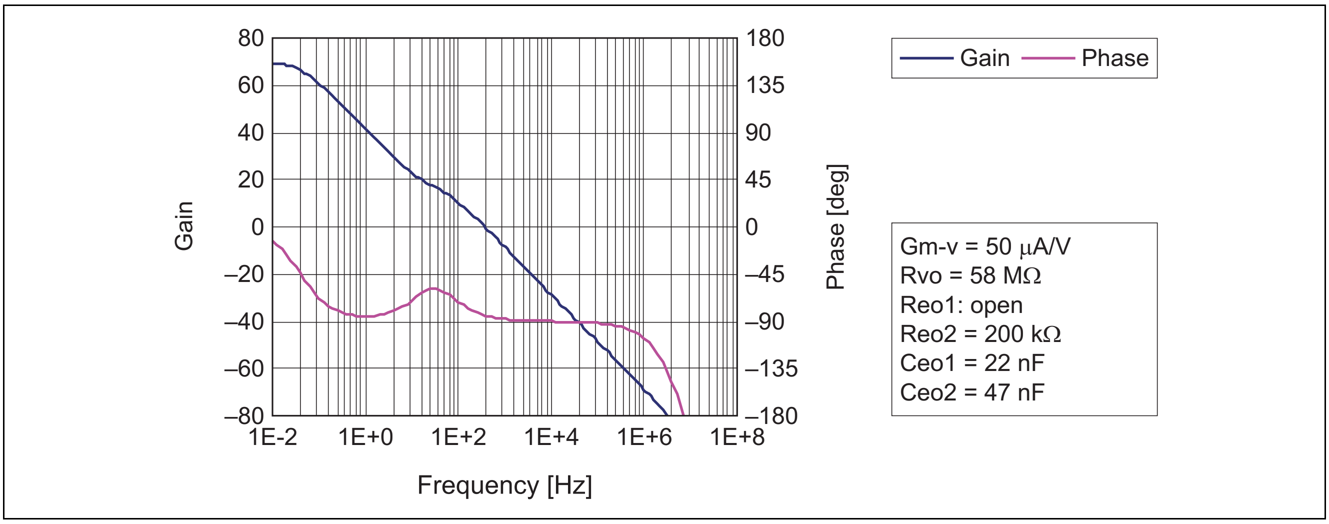


Figure 11 Frequency Characteristics of the Error Amplifier

4.8 About Abnormal Examination (1pin(FB) – 2pin(COMP) short)

Outline of operation:
It becomes voltage follower connection when 1pin (FB) and 2pin (COMP) are shorted, and the COMP operates to output 2.51 V. So, when 1pin and 2pin are shorted, the operation of the chip differs according to the state of the COMP voltage of normal operation: a) the COMP voltage is controlled by 2.51 V or more, b) the COMP voltage is controlled by 2.51 V or less.

- When the COMP voltage is controlled to keep 2.51 V or more (Low input voltage and heavy load)
  The output voltage of COMP decreases when the pins are shorted. And then ON time duration enough to keep the load power can not be obtained.
- When the COMP voltage is controlled to keep 2.51 V or less (High input voltage and light load)
  When the pins are shorted, the output voltage of the COMP is raised. And then ON time duration becomes longer then needed. The final voltage of PFC_OUT is obtained from the following formula.

$$PFC\_OUT_{short}[V] = (PFC\_OUT_{normal} \times 1.09) + (I_{comp} \times R_{fb}) \quad \cdots (7)$$

PFC_OUT(short):	The output voltage when the short-circuit between FB pin and COMP pin happens.
PFC_OUT(normal):	The voltage of PFC_OUT at normal operation
Icomp:	Sink current of the Error Amplifier (max 10 μA)
Rfb:	The resistance of the feedback resistor

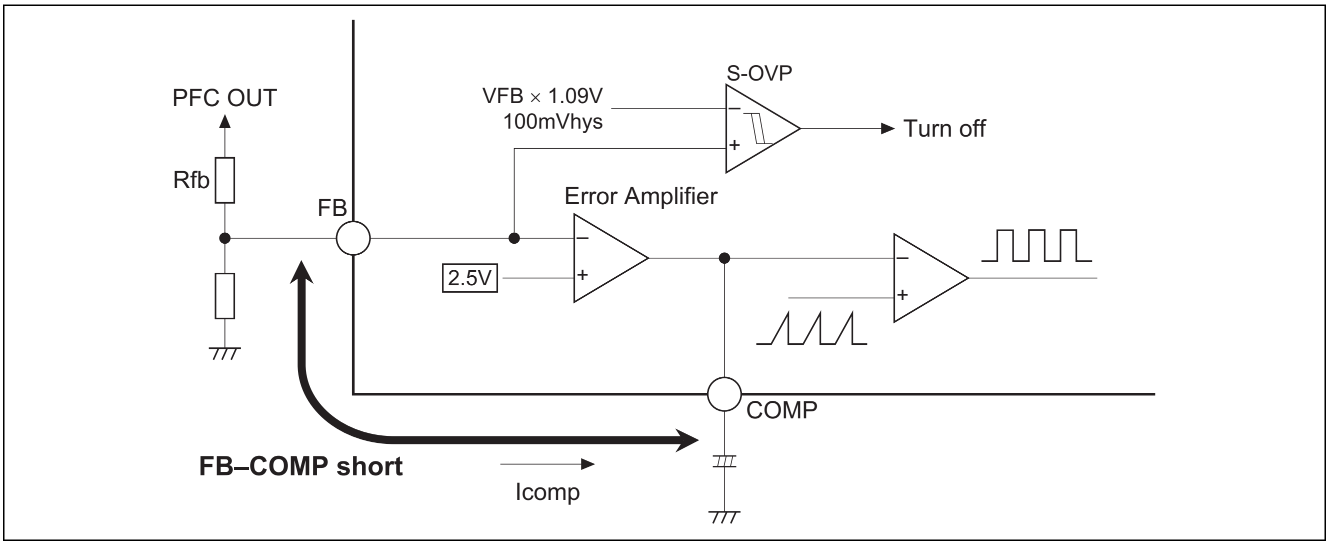
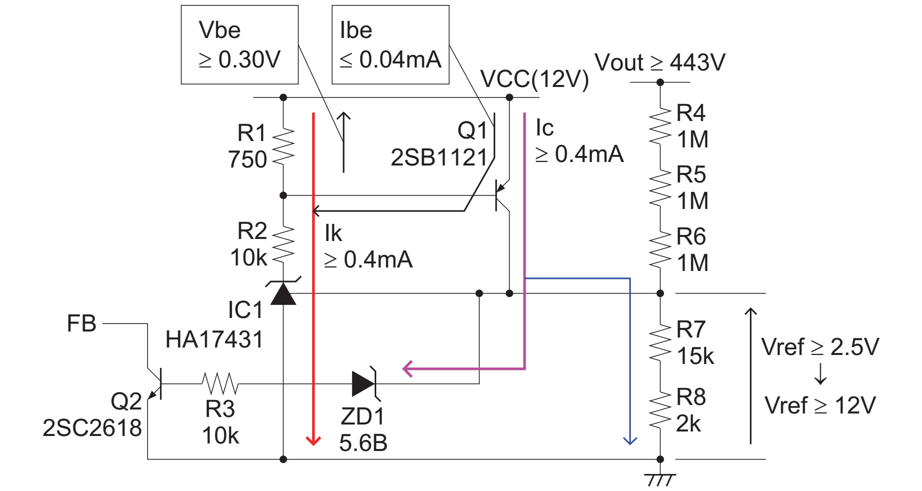


Figure 12

Countermeasure:
In case in which the feed-back resistor of the large resistance value is used between the output voltage and the FB-pin, or in case in which the output voltage is restricted at the lower voltage obtained by (7), the external circuit for the Over Voltage Protection (OVP) shown below should be prepared.
The PFC-OUT voltage rising can be prevented by this circuit depicted below when 1pin and 2pin are shorted.
When PFC output voltage (Vout) rises and exceeds 443 V (the OVP setting voltage), Vref becomes 2.5 V or more. And then, Ik increases rapidly by the characteristic of Shunt Regulator (IC1). So that, PNP transistor (Q1) is turned on, and Vref raises up near Vcc. As a result, zener diode (ZD1) is turned on and this makes the Q2 turn on and keep on hereafter, and then, the voltage of FB lowers to 0.5 V or less. So that, the PFC operation is stopped because of low voltage level of the FB.



Note: Ibe and Icare an example. The setting OVP voltage may change by variation and the temperature coefficient of hfeof Q1. Please evaluate it especially noting the value of R1 when you apply to an actual set.

Figure 13

5. Layout Pattern Guide

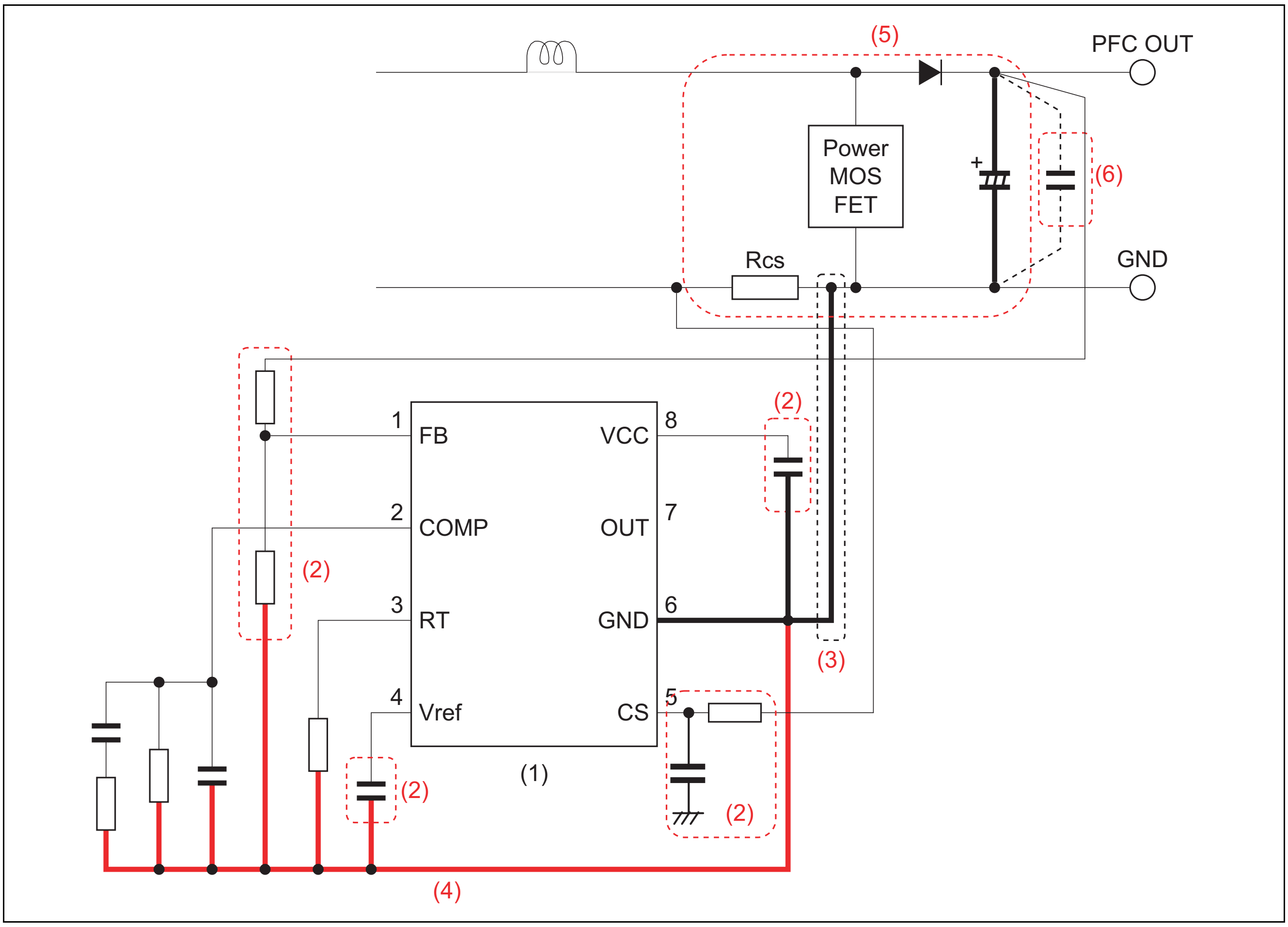


Figure 14

(1) Avoid switching noise by keeping the PFC IC as far as possible from high-voltage switching parts (power MOS FET, diode, and boost coil).
Take particular care to prevent noise radiation from the drain of the power MOS FET.

(2) To avoid the effects of radiated noise (to the extent this), place the filter on the CS pin and resistor on the FB pin as close to the IC as possible.
Also place the bypass capacitors for VCC and Vref as close to the IC as possible.
When the large value of the resistance, such as over 1 MΩ, is used in the FB line, the capacitor about 1000 pF should be used between FP pin and GND.

(3) Wire the GND line of the IC with a single thick pattern to the Rcs Resistor (Output side).

(4) Connect external components, the COMP, RT, and Vref pins to a common GND, and connect it to the GND pin of the IC with a single wiring.

(5) Keep pattern runs, on which current is discontinuous, as short as possible. In particular, it is effective to suppress overshooting of the drain voltage when the power MOS FET is turned off by ensuring a short distance between the drain and the anode of the boost diode.

(6) If a film capacitor is to be mounted to reduce switching ripple in the output voltage, insert it close to the diode. Use a film capacitor that has good high-frequency characteristics.

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Revision Record

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