RX113 Group, RX130 Group

Points of Difference Between RX113 Group and RX130 Group

Summary

This application note is intended as a reference for confirming the points of difference between the I/O registers of the RX113 Group and RX130 Group.

Target Device

RX130 Group 100-/64- pin versions

When using this application note with other Renesas MCUs, careful evaluation is recommended after making modifications to comply with the alternate MCU.

Contents

1. Comparison of Functions of RX113 Group and RX130 Group

A comparison of the functions of the RX113 Group and RX130 Group is provided below. For details of the functions, see 2, Comparative Overview of Functions, and 5, Reference Documents.

Table 1.1 is a comparative listing of the functions of the RX113 and RX130.

Table 1.1 Comparison of Functions of RX113 and RX130

Function	RX113	RX130
CPU	○	○
Operating mode	△	△
Address Space	△	△
Resets	△	△
Option-setting memory	△	△
Voltage detection circuit (LVDAa): RX113, (LVDAb): RX130	△	△
Clock generation circuit	△	△
Clock frequency accuracy measurement circuit (CAC)	○	○
Low power consumption function	△	△
Register write protection function	△	△
Exception Handling	○	○
Interrupt controller (ICUb)	△	△
Bus	△	△
Data transfer controller (DTCa)	○	○
Event link controller (ELC)	△	△
I/O ports	△	△
Multi-function pin controller (MPC)	△	△
Multi-function timer pulse unit 2 (MTU2a)	○	○
Port output enable 2 (POE2a)	○	○
8-bit timer (TMR)	△	△
Compare match timer (CMT)	△	△
Realtime clock (RTCA)	△	△
Low-power timer (LPT)	○	○
Independent watchdog timer (IWDTa)	○	○
USB2.0 Host/Function module	○	×
Serial communication interface (SCIe, SCIf): RX113, (SCIg, SCIh): RX130	△	△
IrDA interface	○	×
Remote control signal receiver (REMC)	×	○
I²C bus interface (RIIC): RX113, (RIICa): RX130	△	△
Serial sound interface (SSI)	○	×
Serial peripheral interface (RSPI): RX113, (RSPIa): RX130	△	△
CRC calculator (CRC)	○	○
LCD controller/driver (LCDC)	○	×
Capacitive touch sensing unit (CTSU): RX113, (CTSUa): RX130	△	△
12-bit A/D converter (S12ADb): RX113, (S12ADE): RX130	△	△
12-bit D/A converter (R12DAA): RX113, D/A converter (DAa): RX130	△	△
Temperature sensor (TEMPSA)	○	○
Comparator B (CMPBa)	○	○
Data operation circuit (DOC)	○	○
RAM	△	△
Flash memory (ROM)	△	△
Flash memory (E2 Data Flash)	○	○

Function	RX113	RX130
Package (LFQFP64/100 only)	△	△

Note: ○: Function implemented, ×: Function not implemented, △: Differences exist between implementation of function on RX113 and RX130.

2. Comparative Overview of Functions

This section lists points of difference between the peripheral functions of the RX113 and RX130 groups, comparing each function in overview and the registers of each function. Specifications implemented only on one group are shown in red, specifications that exist on both groups but with points of difference are shown in red for the RX130 Group, and specifications that exist on both groups are shown in black.

2.1 Operating Modes

Table 2.1 shows a comparative listing of the operating modes specifications.

Table 2.1 Comparative Listing of Operating Modes Specifications

Item	RX113	RX130
Operating mode	Single-chip mode	Single-chip mode
	Boot mode (USB interface)	—
	Boot mode (SCI interface)	Boot mode (SCI interface)
Mode pins	MD, UB#	MD

2.2 Address Space

Figure 2.1 shows the comparisons of memory maps.

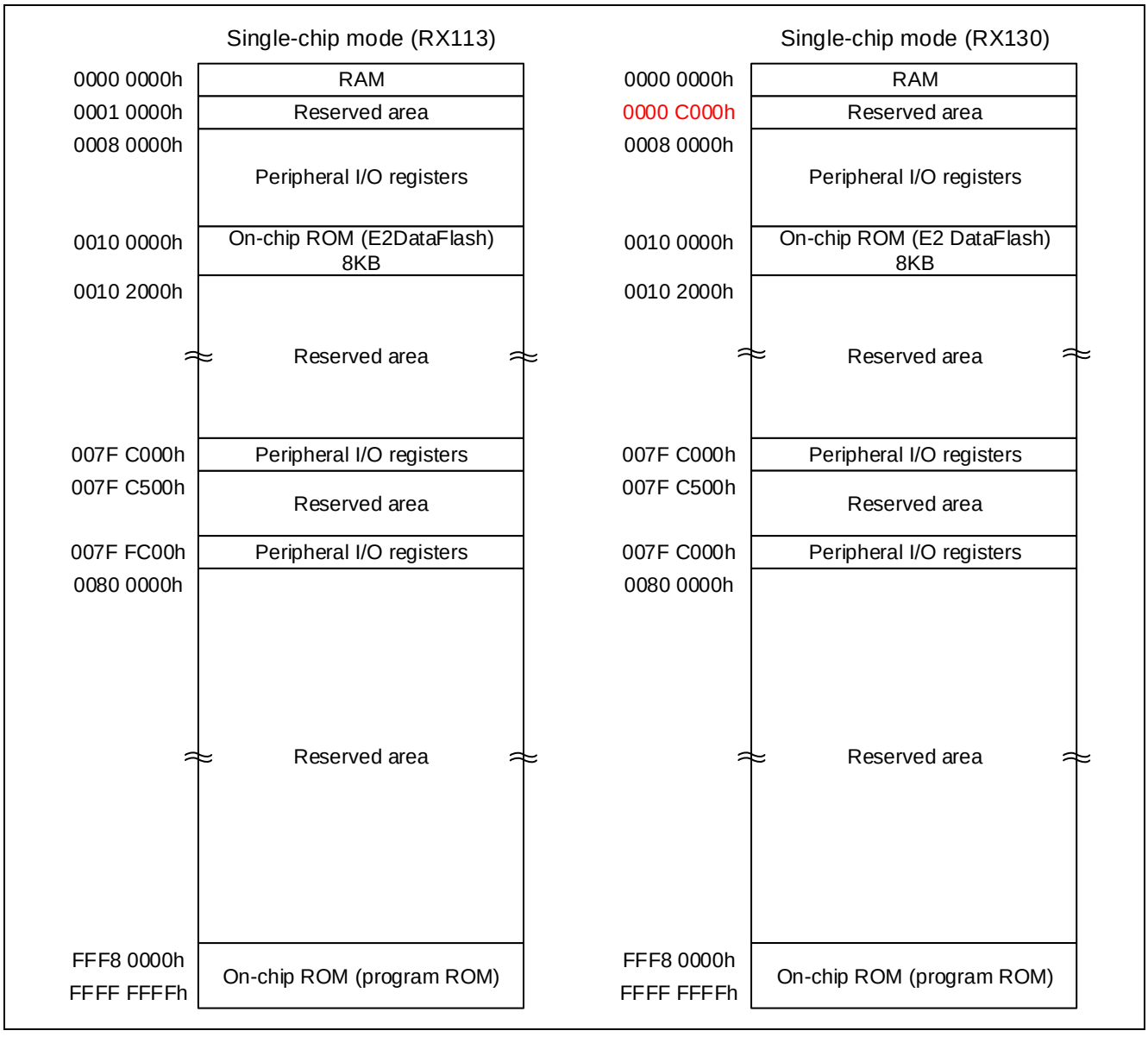

Figure 2.1 Memory Map in Each Operating Mode

2.3 Resets

Table 2.2 shows a comparative listing of the reset specifications, and Table 2.3 shows a comparative listing of the reset registers.

Table 2.2 Comparative Listing of Reset Specifications

Item	RX113	RX130
Name of reset	RES# pin reset	RES# pin reset
	Power-on reset	Power-on reset
	—	Voltage monitoring 0 reset
	Voltage monitoring 1 reset	Voltage monitoring 1 reset
	Voltage monitoring 2 reset	Voltage monitoring 2 reset
	Independent watchdog timer reset	Independent watchdog timer reset
	Software reset	Software reset

Table 2.3 Comparative Listing of Reset Register

Register	Bit	RX113	RX130
RSTSR0	LVD0RF	—	Voltage monitoring 0 reset detection flag

2.4 Option-Setting Memory

Table 2.4 shows a comparative listing of the option-setting memory registers, and Figure 2.2 shows a comparative of the option-setting memory.

Table 2.4 Comparative Listing of Option-Setting Memory Registers

Register	Bit	RX113	RX130
OFS1	STUPLVD1LVL [3:0]	Startup voltage monitoring 1 reset detection level select bits	—
	STUPLVD1REN	Startup voltage monitoring 1 reset enable bit	—
	FASTSTUP	b0	b3
	LVDAS	—	Voltage detection 0 circuit start bit
	VDSEL[1:0]	—	Voltage detection 0 level select bits

Note 1. Only the notation differs. The functionality is the same.

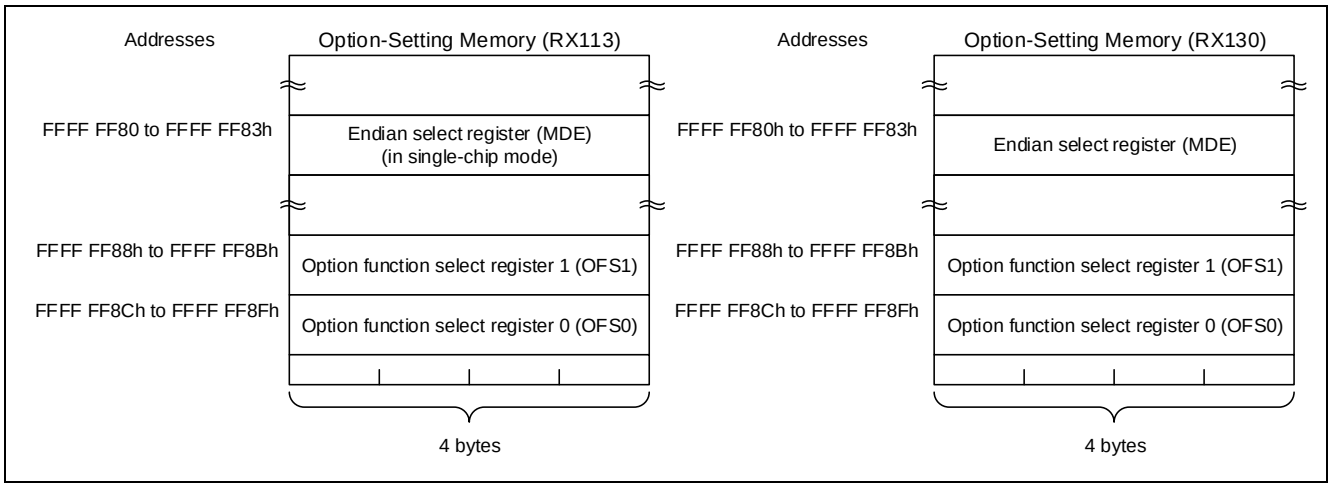

Figure 2.2 Comparative of Option-Setting Memory

2.5 Voltage Detection Circuit

Table 2.5 shows a comparative listing of the voltage detection circuit specifications, and Table 2.6 shows a comparative listing of the voltage detection circuit registers.

Table 2.5 Comparative Listing of Voltage Detection Circuit Specifications

		RX113			RX130		
Item		**Voltage Monitoring 0**	**Voltage Monitoring 1**	**Voltage Monitoring 2**	**Voltage Monitoring 0**	**Voltage Monitoring 1**	**Voltage Monitoring 2**
VCC monitoring	Monitored voltage	—	Vdet1	Vdet2	Vdet0	Vdet1	Vdet2
	Detection target	—	Voltage rises or falls past Vdet1.	Voltage rises or falls past Vdet2.	Voltage falls lower than Vdet0.	Voltage rises or falls past Vdet1.	Voltage rises or falls past Vdet2.
				The EXVCCINP2 bit in LVCMPCR can be used to select between VCC and the voltage input to the CMPA2 pin.			The EXVCCINP2 bit in LVCMPCR can be used to select between VCC and the voltage input to the CMPA2 pin.
	Detection voltage	—	Selectable from 10 levels using LVDLVLR.LVD1LVL[3:0] bits	Selectable from four levels using LVDLVLR.LVD2LVL[1:0] bits	Selectable from four levels using OFS1 register.	Selectable from 14 levels using LVDLVLR.LVD1LVL[3:0] bits.	Selectable from four levels using LVDLVLR.LVD2LVL[1:0] bits.
	Monitor flag	—	LVD1SR.LVD1MON flag: Monitors if higher or lower than Vdet1.	LVD2SR.LVD2MON flag: Monitors if higher or lower than Vdet2.	—	LVD1SR.LVD1MON flag: Monitors if higher or lower than Vdet1.	LVD2SR.LVD2MON flag: Monitors if higher or lower than Vdet2.
			LVD1SR.LVD1DET flag: Detects rise or fall past Vdet1.	LVD2SR.LVD2DET flag: Detects rise or fall past Vdet2.		LVD1SR.LVD1DET flag: Detects rise or fall past Vdet1.	LVD2SR.LVD2DET flag: Detects rise or fall past Vdet2.
Voltage detection processing	Reset	—	Voltage monitoring 1 reset	Voltage monitoring 2 reset	Voltage monitoring 0 reset	Voltage monitoring 1 reset	Voltage monitoring 2 reset
			Reset when Vdet1 > VCC: Selectable between CPU operation restarts a fixed period of time after VCC > Vdet1 and CPU operation restarts a fixed period of time after Vdet1 > VCC.	Reset when Vdet2 > VCC or CMPA2 pin voltage: Selectable between CPU operation restarts a fixed period of time after VCC or CMPA2 pin voltage > Vdet2 and CPU operation restarts a fixed period of time after Vdet2 > VCC or CMPA2 pin voltage.	Reset when Vdet0 > VCC: CPU operation restarts a fixed period of time after VCC > Vdet0.	Reset when Vdet1 > VCC: Selectable between CPU operation restarts a fixed period of time after VCC > Vdet1 and CPU operation restarts a fixed period of time after Vdet1 > VCC.	Reset when Vdet2 > VCC or CMPA2 pin voltage: Selectable between CPU operation restarts a fixed period of time after VCC or CMPA2 pin voltage > Vdet2 and CPU operation restarts a fixed period of time after Vdet2 > VCC or CMPA2 pin voltage.

Item		RX113 Voltage Monitoring 0	RX113 Voltage Monitoring 1	RX113 Voltage Monitoring 2	RX130 Voltage Monitoring 0	RX130 Voltage Monitoring 1	RX130 Voltage Monitoring 2
Voltage detection processing	Interrupt	—	Voltage monitoring 1 interrupt	Voltage monitoring 2 interrupt	—	Voltage monitoring 1 interrupt	Voltage monitoring 2 interrupt
			Selectable between non-maskable interrupt and interrupt.	Selectable between non-maskable interrupt and interrupt.		Selectable between non-maskable interrupt and interrupt.	Selectable between non-maskable interrupt and interrupt.
			Interrupt request generated both when Vdet1 > VCC and when VCC > Vdet1, or one or the other.	Interrupt request generated both when Vdet2 > VCC or CMPA2 pin voltage and when VCC or CMPA2 pin voltage > Vdet2, or one or the other.		Interrupt request generated both when Vdet1 > VCC and when VCC > Vdet1, or one or the other.	Interrupt request generated both when Vdet2 > VCC or CMPA2 pin voltage and when VCC or CMPA2 pin voltage > Vdet2, or one or the other.
Event link function		—	Available: Vdet1 pass-through detection event output	—	—	Available: Vdet1 pass-through detection event output	—

Table 2.6 Comparative Listing of Voltage Detection Circuit Registers

Register	Bit	RX113	RX130
LVDLVLR	LVD1LVL [3:0]	Voltage detection 1 level select bits (standard voltage during drop in voltage) b3 b0 0 1 0 0: 3.10 V 0 1 0 1: 3.00 V 0 1 1 0: 2.90 V 0 1 1 1: 2.79 V 1 0 0 0: 2.68 V 1 0 0 1: 2.58 V 1 0 1 0: 2.48 V 1 0 1 1: 2.06 V 1 1 0 0: 1.96 V 1 1 0 1: 1.86 V Do not set to values other than the above.	Voltage detection 1 level select bits (standard voltage during drop in voltage) b3 b0 0 0 0 0: 4.29 V 0 0 0 1: 4.14 V 0 0 1 0: 4.02 V 0 0 1 1: 3.84 V 0 1 0 0: 3.10 V 0 1 0 1: 3.00 V 0 1 1 0: 2.90 V 0 1 1 1: 2.79 V 1 0 0 0: 2.68 V 1 0 0 1: 2.58 V 1 0 1 0: 2.48 V 1 0 1 1: 2.20 V 1 1 0 0: 1.96 V 1 1 0 1: 1.86 V Do not set to values other than the above.
	LVD2LVL [1:0]	Voltage detection 2 level select bits (standard voltage during drop in voltage) b5 b4 0 0: 2.90 V 0 1: 2.60 V 1 0: 2.00 V 1 1: 1.80 V	Voltage detection 2 level select bits (standard voltage during drop in voltage) b5 b4 0 0: 4.29 V 0 1: 4.14 V 1 0: 4.02 V 1 1: 3.84 V

2.6 Clock Generation Circuit

Table 2.7 shows a comparative listing of the clock generation circuit specifications, and Table 2.8 shows a comparative listing of the clock generation circuit registers.

Table 2.7 Comparative Listing of Clock Generation Circuit Specifications

Item	RX113	RX130
Uses	• Generates the system clock (ICLK) supplied to the CPU, DTC, ROM, and RAM. • Generates the peripheral module clocks (PCLKB, PCLKD) supplied to the peripheral module clocks. Peripheral module clock PCLKD is used as the operating clock for S12AD, and peripheral module clock PCLKB is used as the operating clock for the modules other than S12AD. • Generates the FlashIF clock (FCLK) supplied to the FlashIF. • Generates the USB clock (UCLK) supplied to the USB. • Generates the CAC clock (CACCLK) supplied to the CAC. • Generates the RTC-dedicated sub clock (RTCSCLK) supplied to the RTC. • Generates the IWDT-dedicated clock (IWDTCLK) supplied to the IWDT. • Generates the LCD clock (LCDSRCCLK) supplied to the LCD. • Generates the SSI clock (SSISCK) supplied to the SSI. • Generates the LPT clock (LPTCLK) supplied to the LPT.	• Generates the system clock (ICLK) supplied to the CPU, DTC, ROM, and RAM. • Generates the peripheral module clocks (PCLKB, PCLKD) supplied to the peripheral module clocks. Peripheral module clock PCLKD is used as the operating clock for S12AD, and peripheral module clock PCLKB is used as the operating clock for the modules other than S12AD. • Generates the FlashIF clock (FCLK) supplied to the FlashIF. • Generates the CAC clock (CACCLK) supplied to the CAC. • Generates the RTC-dedicated sub clock (RTCSCLK) supplied to the RTC. • Generates the IWDT-dedicated clock (IWDTCLK) supplied to the IWDT. • Generates the LPT clock (LPTCLK) supplied to the LPT. • Generates the REMC clock (REMCLK) to be supplied to the REMC.
Operating frequencies	• ICLK: 32 MHz (max.) • PCLKB: 32 MHz (max.) • PCLKD: 32 MHz (max.) • FCLK: 1 MHz to 32 MHz (for programming and erasing the ROM and E2 DataFlash) 32 MHz (max.): (for reading from the E2 DataFlash) • UCLK: 48 MHz • CACCLK: Same frequency as each oscillator • RTCSCLK: 32.768 kHz • IWDTCLK: 15 kHz • LCDSRCCLK: Same as selected oscillator clock • LPTCLK: Same as selected oscillator clock	• ICLK: 32 MHz (max.) • PCLKB: 32 MHz (max.) • PCLKD: 32 MHz (max.) • FCLK: 1 MHz to 32 MHz (for programming and erasing the ROM and E2 DataFlash) 32 MHz (max.): (for reading from the E2 DataFlash) • CACCLK: Same frequency as each oscillator • RTCSCLK: 32.768 kHz • IWDTCLK: 15 kHz • LPTCLK: Same as selected oscillator clock • REMCLK: Same as selected oscillator clock

Item	RX113	RX130
Main clock oscillator	• Resonator frequency: 1 MHz to 20 MHz (VCC ≥ 2.4 V) 1 MHz to 8 MHz (VCC < 2.4 V) • External clock input frequency: 20 MHz (max.) • Connectable resonator or additional circuit: Ceramic resonator, crystal resonator • Connection pins: EXTAL, XTAL • Oscillation stop detection function: When oscillation stop of the main clock is detected, the system clock source is switched to LOCO, and MTU output can be forcedly driven to high-impedance.	• Resonator frequency: 1 MHz to 20 MHz (VCC ≥ 2.4 V) 1 MHz to 8 MHz (VCC < 2.4 V) • External clock input frequency: 20 MHz (max.) • Connectable resonator or additional circuit: Ceramic resonator, crystal resonator • Connection pins: EXTAL, XTAL • Oscillation stop detection function: When oscillation stop of the main clock is detected, the system clock source is switched to LOCO, and MTU output can be forcedly driven to high-impedance. • Drive capacity switching function
Sub-clock oscillator	• Resonator frequency: 32.768 kHz • Connectable resonator or additional circuit: crystal resonator • Connection pins: XCIN, XCOUT	• Resonator frequency: 32.768 kHz • Connectable resonator or additional circuit: crystal resonator • Connection pins: XCIN, XCOUT • Drive capacity switching function
PLL circuit	• Input clock source: Main clock • Input pulse frequency division ratio: Selectable from 1, 2, and 4 • Input frequency: 4 MHz to 8 MHz • Frequency multiplication ratio: Selectable within range from ×6, ×8 • Oscillation frequency: 32 MHz to 48 MHz (VCC ≥ 2.4 V)	• Input clock source: Main clock • Input pulse frequency division ratio: Selectable from 1, 2, and 4 • Input frequency: 4 MHz to 8 MHz • Frequency multiplication ratio: Selectable within range from ×4 to ×8 (increments of 0.5) • Oscillation frequency: 24 MHz to 32 MHz (VCC ≥ 2.4 V)
USB-dedicated PLL circuit	• Input clock source: Main clock • Input pulse frequency division ratio: Selectable from 1, 2, and 4 • Input frequency: 4 MHz, 8 MHz • Frequency multiplication ratio: Selectable within range from ×6, ×8 • Oscillation frequency: 48 MHz (VCC ≥ 2.4 V)	—
High-speed on-chip oscillator (HOCO)	Oscillation frequency: 32 MHz	Oscillation frequency: 32 MHz
Low-speed on-chip oscillator (LOCO)	Oscillation frequency: 4 kHz	Oscillation frequency: 4 MHz
IWDT-dedicated on-chip oscillator	Oscillation frequency: 15 kHz	Oscillation frequency: 15 kHz

Table 2.8 Comparative Listing of Clock Generation Circuit Registers

Register	Bit	RX113	RX130
PLLCR	STC[5:0]	Frequency multiplication factor setting bits b13 b8 0 0 1 0 1 1: ×6 0 0 1 1 1 1: ×8 Do not set to values other than the above.	Frequency multiplication factor setting bits b13 b8 0 0 0 1 1 1: ×4 0 0 1 0 0 0: ×4.5 0 0 1 0 0 1: ×5 0 0 1 0 1 0: ×5.5 0 0 1 0 1 1: ×6 0 0 1 1 0 0: ×6.5 0 0 1 1 0 1: ×7 0 0 1 1 1 0: ×7.5 0 0 1 1 1 1: ×8 Do not set to values other than the above.
UPLLCR	—	USB-dedicated PLL control register	—
UPLLCR2	—	USB-dedicated PLL control register 2	—
HOFCR	—	—	High-speed on-chip oscillator forced oscillation control register
OSCOVFSR	UPLOVF	USB-dedicated PLL clock oscillation stabilization flag 0: USB-dedicated PLL is stopped or not stabilized. 1: Oscillation is stable and the clock can be used as UCLK.	—
LCDSCLKCR	—	LCD source clock control register	—
LCDSCLKCR2	—	LCD source clock control register 2	—
HOCOWTCR	—	High-speed on-chip oscillator wait control register	—
CKOCR	RX113: CKOSEL[2:0] RX130: CKOSEL[3:0]	CLKOUT output source select bits b10 b8 0 0 0: LOCO clock 0 0 1: HOCO clock 0 1 0: Main clock 0 1 1: Sub-clock Do not set to values other than the above.	CLKOUT output source select bits b11 b8 0 0 0 0: LOCO clock 0 0 0 1: HOCO clock 0 0 1 0: Main clock 0 0 1 1: Sub-clock 0 1 0 0: PLL Do not set to values other than the above.
LOCOTRR	—	—	Low-speed on-chip oscillator trimming register
ILOCOTRR	—	—	IWDT-dedicated on-chip oscillator trimming register
HOCOTRRn (n = 0)	—	—	High-speed on-chip oscillator trimming register n

2.7 Low Power Consumption Functions

Table 2.9 shows a comparative listing of the low power consumption specifications, Table 2.10 to Table 2.12 shows a Comparative Listing of Entering and Exiting Low Power Consumption Modes and Operating States in Each Mode, and Table 2.13 shows a comparative listing of the low power consumption specifications.

Table 2.9 Comparative Listing of Low Power Consumption Functions Specifications

Item	RX113	RX130
Reduction of power consumption by clock switching	The frequency division ratio can be set independently for the system clock (ICLK), peripheral module clock (PCLKB), S12AD clock (PCLKD), and FlashIF clock (FCLK).	The frequency division ratio can be set independently for the system clock (ICLK), peripheral module clock (PCLKB), S12AD clock (PCLKD), and FlashIF clock (FCLK).
Module stop function	Each peripheral module can be stopped independently.	Each peripheral module can be stopped independently.
Function for transition to low power consumption mode	It is possible to transition to a low power consumption mode in which the CPU, peripheral modules, or oscillators are stopped.	It is possible to transition to a low power consumption mode in which the CPU, peripheral modules, or oscillators are stopped.
Low power consumption modes	• Sleep mode • Deep sleep mode • Software standby mode	• Sleep mode • Deep sleep mode • Software standby mode
Operating power reduction function	• Power consumption can be reduced in normal operation, sleep mode, and deep sleep mode by selecting an appropriate operating power consumption control mode according to the operating frequency and operating voltage. • Three operating power control modes are available — High-speed operating mode — Middle-speed operating mode — Low-speed operating mode	• Power consumption can be reduced in normal operation, sleep mode, and deep sleep mode by selecting an appropriate operating power consumption control mode according to the operating frequency and operating voltage. • Three operating power control modes are available — High-speed operating mode — Middle-speed operating mode — Low-speed operating mode

Table 2.10 Comparative Listing of Entering and Exiting Low Power Consumption Modes and Operating States in Each Mode (Sleep Mode)

Entering and Exiting Low Power Consumption Modes and Operating States	RX113	RX130
	Sleep Mode	Sleep Mode
Entry trigger	Control register + instruction	Control register + instruction
Exit trigger	Interrupt	Interrupt
After exiting from each mode, CPU begins from	Interrupt handling	Interrupt handling
Main clock oscillator	Operating possible	Operating possible
Sub-clock oscillator	Operating possible	Operating possible
High-speed on-chip oscillator	Operating possible	Operating possible
Low-speed on-chip oscillator	Operating possible	Operating possible
IWDT-dedicated on-chip oscillator	Operating possible	Operating possible
PLL	Operating possible	Operating possible
USB-dedicated PLL	Operating possible	—
CPU	Stopped (Retained)	Stopped (Retained)
RAM0 (0000 0000h to 0000 3FFFh)	Operating possible (Retained)	—
RAM0 (0000 0000h to 0000 BFFFh)	—	Operating possible (Retained)
DTC	Operating possible	Operating possible
Flash memory	Operating	Operating
Independent watchdog timer (IWDT)	Operating possible	Operating possible
Remote control signal receiver (REMC)	—	Operating possible
Realtime clock (RTC)	Operating possible	Operating possible
Low power timer (LPT)	Operating possible	Operating possible
Voltage detection circuit (LVD)	Operating possible	Operating possible
Power-on reset circuit	Operating	Operating
Peripheral modules	Operating possible	Operating possible
I/O ports	Operating	Operating
RTCOUT	Operating possible	Operating possible
CLKOUT	Operating possible	Operating possible
Comparator B	Operating possible	Operating possible
LCD controller/driver	Operating possible	—

Table 2.11 Comparative Listing of Entering and Exiting Low Power Consumption Modes and Operating States in Each Mode (Deep Sleep Mode)

Entering and Exiting Low Power Consumption Modes and Operating States	RX113	RX130
	Deep Sleep Mode	Deep Sleep Mode
Entry trigger	Control register + instruction	Control register + instruction
Exit trigger	Interrupt	Interrupt
After exiting from each mode, CPU begins from	Interrupt handling	Interrupt handling
Main clock oscillator	Operating possible	Operating possible
Sub-clock oscillator	Operating possible	Operating possible
High-speed on-chip oscillator	Operating possible	Operating possible
Low-speed on-chip oscillator	Operating possible	Operating possible
IWDT-dedicated on-chip oscillator	Operating possible	Operating possible
PLL	Operating possible	Operating possible
USB-dedicated PLL	Operating possible	—
CPU	Stopped (Retained)	Stopped (Retained)
RAM0 (0000 0000h to 0000 3FFFh)	Stopped (Retained)	—
RAM0 (0000 0000h to 0000 BFFFh)	—	Stopped (Retained)
DTC	Stopped (Retained)	Stopped (Retained)
Flash memory	Stopped (Retained)	Stopped (Retained)
Independent watchdog timer (IWDT)	Operating possible	Operating possible
Remote control signal receiver (REMC)	—	Operating possible
Realtime clock (RTC)	Operating possible	Operating possible
Low power timer (LPT)	Operating possible	Operating possible
Voltage detection circuit (LVD)	Operating possible	Operating possible
Power-on reset circuit	Operating	Operating
Peripheral modules	Operating possible	Operating possible
I/O ports	Operating	Operating
RTCOUT	Operating possible	Operating possible
CLKOUT	Operating possible	Operating possible
Comparator B	Operating possible	Operating possible
LCD controller/driver	Operating possible	—

Table 2.12 Comparative Listing of Entering and Exiting Low Power Consumption Modes and Operating States in Each Mode (Software Standby Mode)

Entering and Exiting Low Power Consumption Modes and Operating States	RX113	RX130
	Software Standby Mode	Software Standby Mode
Entry trigger	Control register + instruction	Control register + instruction
Exit trigger	Interrupt	Interrupt
After exiting from each mode, CPU begins from	Interrupt handling	Interrupt handling
Main clock oscillator	Stopped	Stopped
Sub-clock oscillator	Operating possible	Operating possible
High-speed on-chip oscillator	Stopped	Operating possible
Low-speed on-chip oscillator	Stopped	Stopped
IWDT-dedicated on-chip oscillator	Operating possible	Operating possible
PLL	Stopped	Stopped
USB-dedicated PLL	Stopped	—
CPU	Stopped (Retained)	Stopped (Retained)
RAM0 (0000 0000h to 0000 3FFFh)	Stopped (Retained)	—
RAM0 (0000 0000h to 0000 BFFFh)	—	Stopped (Retained)
DTC	Stopped (Retained)	Stopped (Retained)
Flash memory	Stopped (Retained)	Stopped (Retained)
Independent watchdog timer (IWDT)	Operating possible	Operating possible
Remote control signal receiver (REMC)	—	Operating possible
Realtime clock (RTC)	Operating possible	Operating possible
Low power timer (LPT)	Operating possible	Operating possible
Voltage detection circuit (LVD)	Operating possible	Operating possible
Power-on reset circuit	Operating	Operating
Peripheral modules	Stopped (Retained)	Stopped (Retained)
I/O ports	Retained	Retained
RTCOUT	Operating possible	Operating possible
CLKOUT	Operating possible	Operating possible
Comparator B	Operating possible	Operating possible
LCD controller/driver	Operating possible	—

Table 2.13 Comparative Listing of Low Power Consumption Function Registers

Register	Bit	RX113	RX130
MSTPCRA	MSTPA14	Compare match timer 1 (unit 1) module stop bit	—
	MSTPA18	12-bit D/A converter module stop bit	—
	MSTPA19	—	D/A converter module stop bit
MSTPCRB	MSTPB19	USB0 module stop bit	—
	MSTPB29	Serial communication interface 2 module stop bit	—
MSTPCRC	b15-b1	Reserved bits These bits are read as 1. The write value should be 1.	Reserved bits These bits are read as 0. The write value should be 0.
	MSTPC20	IrDA module stop bit	—
	MSTPC28	—	Remote control signal receiver 1 module stop bit
	MSTPC29	—	Remote control signal receiver 0 module stop bit
MSTPCRD	b7-b0	Reserved bits These bits are read as 1. The write value should be 1.	Reserved bits These bits are read as 0. The write value should be 0.
	MSTPD11	LCD controller module stop bit	—
	MSTPD15	Serial sound interface module stop bit	—

2.8 Register Write Protection Function

Table 2.14 shows a comparative overview of the register write protection function specifications, and Table 2.15 shows a comparative listing of the register write protection function registers.

Table 2.14 Comparative Overview of Register Write Protection Function Specifications

Item	RX113	RX130
PRCR0 bit	• Registers related to the clock generation circuit SCKCR, SCKCR3, PLLCR, PLLCR2, MOSCCR, SOSCCR, LOCOCR, ILOCOCR, HOCOCR, OSTDCR, OSTDSR, CKOCR, UPLLCR, UPLLCR2, LCDSCLKCR, LCDSCLKCR2	• Registers related to the clock generation circuit SCKCR, SCKCR3, PLLCR, PLLCR2, MOSCCR, SOSCCR, LOCOCR, ILOCOCR, HOCOCR, HOFCR, OSTDCR, OSTDSR, CKOCR, LOCOTRR, ILOCOTRR, HOCOTRR0
PRCR1 bit	• Registers related to the operating modes SYSCR1 • Registers related to the low power consumption functions SBYCR, MSTPCRA, MSTPCRB, MSTPCRC, MSTPCRD, OPCCR, RSTCKCR, SOPCCR • Registers related to the clock generation circuit MOFCR, MOSCWTCR • Software reset register SWRR	• Registers related to the operating modes SYSCR1 • Registers related to the low power consumption functions SBYCR, MSTPCRA, MSTPCRB, MSTPCRC, MSTPCRD, OPCCR, RSTCKCR, SOPCCR • Registers related to the clock generation circuit MOFCR, MOSCWTCR • Software reset register SWRR
PRCR2 bit	• Registers related to the clock generation circuit HOCOWTCR • Registers related to the low power timer LPTCR1, LPTCR2, LPTCR3, LPTPRD, LPCMR0, LPWUCR	• Registers related to the low power timer LPTCR1, LPTCR2, LPTCR3, LPTPRD, LPCMR0, LPWUCR
PRCR3 bit	• Registers related to the LVD LVCMPCR, LVDLVLR, LVD1CR0, LVD1CR1, LVD1SR, LVD2CR0, LVD2CR1, LVD2SR	• Registers related to the LVD LVCMPCR, LVDLVLR, LVD1CR0, LVD1CR1, LVD1SR, LVD2CR0, LVD2CR1, LVD2SR

Table 2.15 Comparative Listing of Register Write Protection Function Registers

Register	Bit	RX113	RX130
PRCR	PRC2	Protect bit 2 Enables writing to the registers related to the low power timer and the clock generation circuit.	Protect bit 2 Enables writing to the registers related to the low power timer.

2.9 Interrupt Controller

Table 2.16 shows a comparative listing of the interrupt controller specifications, and Table 2.17 shows a comparative listing of the interrupt controller registers.

Table 2.16 Comparative Listing of Interrupt Controller Specifications

Item		RX113 (ICUb)	RX130 (ICUb)
Interrupt	Peripheral function interrupts	• Interrupts from peripheral modules • Interrupt detection: Edge detection/level detection The detection method is fixed for each source of connected peripheral modules.	• Interrupts from peripheral modules • Interrupt detection: Edge detection/level detection The detection method is fixed for each source of connected peripheral modules.
	External pin interrupts	• Interrupts from pins IRQ0 to IRQ7 • Sources: 8 • Interrupt detection: One detection method among low level, falling edge, rising edge, and rising and falling edges can be set for each source. • Digital filter function: Supported	• Interrupts from pins IRQ0 to IRQ7 • Sources: 8 • Interrupt detection: One detection method among low level, falling edge, rising edge, and rising and falling edges can be set for each source. • Digital filter function: Supported
	Software interrupt	• Interrupt generated by writing to a register. • Source: 1	• Interrupt generated by writing to a register. • Source: 1
	Event link interrupt	The ELSR18I or ELSR19I interrupt is generated by an ELC event.	The ELSR8I or ELSR18I interrupt is generated by an ELC event.
	Interrupt priority level	Priority is specified by register settings.	Priority is specified by register settings.
	Fast interrupt function	Faster interrupt processing by the CPU can be specified only for a single interrupt source.	Faster interrupt processing by the CPU can be specified only for a single interrupt source.
	DTC control	The DTC can be activated by interrupt sources.	The DTC can be activated by interrupt sources.
Non-maskable interrupts	NMI pin interrupt	• Interrupt from the NMI pin • Interrupt detection: Falling edge/rising edge • Digital filter function: Supported	• Interrupt from the NMI pin • Interrupt detection: Falling edge/rising edge • Digital filter function: Supported
	Oscillation stop detection interrupt	Interrupt at oscillation stop detection	Interrupt at oscillation stop detection
	IWDT underflow/refresh error	Interrupt at an underflow of the down counter or at the occurrence of a refresh error	Interrupt at an underflow of the down counter or at the occurrence of a refresh error
	Voltage monitoring 1 interrupt	Voltage monitoring interrupt of voltage monitoring circuit 1 (LVD1)	Voltage monitoring interrupt of voltage monitoring circuit 1 (LVD1)
	Voltage monitoring 2 interrupt	Voltage monitoring interrupt of voltage monitoring circuit 2 (LVD2)	Voltage monitoring interrupt of voltage monitoring circuit 2 (LVD2)

Item	RX113 (ICUb)	RX130 (ICUb)
Return from low power consumption modes	• Sleep mode and deep sleep mode: Return is initiated by a non-maskable interrupt or any other interrupt source. • Software standby mode: Return is initiated by a non-maskable interrupt, interrupt IRQ0 to IRQ7, or RTC alarm/period interrupt.	• Sleep mode and deep sleep mode: Return is initiated by a non-maskable interrupt or any other interrupt source. • Software standby mode: Return is initiated by a non-maskable interrupt, interrupt IRQ0 to IRQ7, or RTC alarm/period interrupt.

Table 2.17 Comparative Listing of Interrupt Controller Register

Register	Bit	RX113 (ICUb)	RX130 (ICUb)
DTCERn	DTCE	DTC activation enable bit 0: DTC activation is disabled. 1: DTC activation is enabled.	DTC transfer request enable bit 0: The corresponding interrupt source is selected as the source of an interrupt to the CPU. 1: The corresponding interrupt source is selected as the DTC activation source.

2.10 Bus

Table 2.18 shows a comparative listing of the bus specifications.

Table 2.18 Comparative Listing of Bus Specifications

Item		RX113	RX130
CPU bus	Instruction bus	• Connected to the CPU (for instructions). • Connected to the on-chip memory (RAM and ROM). • Operates in synchronization with the system clock (ICLK).	• Connected to the CPU (for instructions). • Connected to the on-chip memory (RAM and ROM). • Operates in synchronization with the system clock (ICLK).
	Operand bus	• Connected to the CPU (for operand). • Connected to the on-chip memory (RAM and ROM). • Operates in synchronization with the system clock (ICLK).	• Connected to the CPU (for operand). • Connected to the on-chip memory (RAM and ROM). • Operates in synchronization with the system clock (ICLK).
Memory buses	Memory bus 1	Connected to the RAM.	Connected to the RAM.
	Memory bus 2	Connected to the ROM.	Connected to the ROM.
Internal main buses	Internal main bus 1	• Connected to the CPU. • Operates in synchronization with the system clock (ICLK).	• Connected to the CPU. • Operates in synchronization with the system clock (ICLK).
	Internal main bus 2	• Connected to the DTC. • Connected to the on-chip memory (RAM and ROM). • Operates in synchronization with the system clock (ICLK).	• Connected to the DTC. • Connected to the on-chip memory (RAM and ROM). • Operates in synchronization with the system clock (ICLK).
Internal peripheral buses	Internal peripheral bus 1	• Connected to peripheral modules (DTC, interrupt controller, and bus error monitoring section). • Operates in synchronization with the system clock (ICLK).	• Connected to peripheral modules (DTC, interrupt controller, and bus error monitoring section). • Operates in synchronization with the system clock (ICLK).
	Internal peripheral bus 2	• Connected to peripheral modules. • Operates in synchronization with the peripheral module clock (PCLKB).	• Connected to peripheral modules. • Operates in synchronization with the peripheral module clock (PCLKB, PCLKD).
	Internal peripheral bus 3	• Connected to peripheral modules (USB). • Operates in synchronization with the peripheral module clock (PCLKB).	• Connected to peripheral modules (Touch). • Operates in synchronization with the peripheral module clock (PCLKB).
	Internal peripheral bus 4	• Connected to the ROM (P/E) and E2 DataFlash memory. • Operates in synchronization with the FlashIF clock (FCLK).	• Connected to the ROM (P/E) and E2 DataFlash memory. • Operates in synchronization with the FlashIF clock (FCLK).

2.11 Event Link Controller

Table 2.19 shows a comparative listing of the event link controller specifications, Table 2.20 shows a comparative listing of the event link controller registers, and Table 2.21 shows a comparative listing of ELSRn register setting values.

Table 2.19 Comparative Listing of Event Link Controller Specifications

Item	RX113 (ELC)	RX130 (ELC)
Event link function	• 45 event signals can be directly connected to modules. • It is possible to specify that timer modules operate when an event is input. • Event link operation is possible for port B. Single-port: Event link operation can be enabled for a specified single bit in a port. Port group: Event link operation can be enabled for a group of specified bits within an 8-bit I/O port.	• 47 event signals can be directly connected to modules. • It is possible to specify that timer modules operate when an event is input. • Event link operation is possible for port B. Single-port: Event link operation can be enabled for a specified single bit in a port. Port group: Event link operation can be enabled for a group of specified bits within an 8-bit I/O port.
Low power consumption function	It is possible to specify the module stop state.	It is possible to specify the module stop state.

Table 2.20 Comparative Listing of Event Link Controller Register

Register	Bit	RX113	RX130
ELOPC	LPTMD[1:0]	—	LPT operation select bits

Table 2.21 Comparative Listing of ELSRn Register Setting Values

Setting Value	RX113	RX130	Event
32h	—	○	LPT compare match
34h	—	○	S12AD comparison conditions met
35h	—	○	S12AD comparison conditions not met
5Dh	○	—	LPT compare match

2.12 I/O Ports

Table 2.22 shows a Comparative Listing of I/O Port Specifications, Table 2.23 and Table 2.24 list points of difference between the I/O port functions (on 100-pin and 64-pin products, respectively), and Table 2.25 is a comparative listing of I/O port registers.

Table 2.22 Comparative Listing of I/O Port Specifications

	RX113		RX130	
Port Symbol	100 pin	64 pin	100 pin	64 pin
PORT0	P02, P04, P07	Not provided	P03 to P07	P03, P05
PORT1	P10 to P17	P14 to P17	P12 to P17	P14 to P17
PORT2	P20 to P27	P26, P27	P20 to P27	P26, P27
PORT3	P30 to P32, P35	P30 to P32, P35	P30 to P37	P30 to P32, P35 to P37
PORT4	P40 to P44, P46	P40 to P42	P40 to P47	P40 to P47
PORT5	P50 to P56	P54, P55	P50 to P55	P54, P55
PORT9	P90 to P92	Not provided	Not provided	Not provided
PORTA	PA0 to PA7	PA0, PA1, PA3, PA4, PA6	PA0 to PA7	PA0, PA1, PA3, PA4, PA6
PORTB	PB0 to PB7	PB0, PB1, PB3, PB5 to PB7	PB0 to PB7	PB0, PB1, PB3, PB5 to PB7
PORTC	PC0 to PC7	PC2 to PC7*1	PC0 to PC7	PC2 to PC7*1
PORTD	PD0 to PD4	PD0 to PD2	PD0 to PD7	Not provided
PORTE	PE0 to PE7	PE0 to PE7	PE0 to PE7	PE0 to PE5
PORTF	PF6, PF7	Not provided	Not provided	Not provided
PORTH	PH7	PH7	PH0 to PH3	PH0 to PH3
PORTJ	PJ0, PJ2, PJ3, PJ6, PJ7	PJ0, PJ2, PJ6, PJ7	PJ1, PJ3, PJ6, PJ7	PJ6, PJ7

Note 1. PC0 and PC1 are valid only when switching by the port switching register A.

Table 2.23 Comparative Listing of I/O Port Functions (100-Pin)

Item	Port Symbol	RX113	RX130
Input pull-up function	PORT0	P02, P04, P07	P03 to P07
	PORT1	P10 to P17	P12 to P17
	PORT2	P20 to P27	P20 to P27
	PORT3	P30 to P32	P30 to P34, P36, P37
	PORT4	—	P40 to P47
	PORT5	P50 to P56	P50 to P55
	PORTA	PA0 to PA7	PA0 to PA7
	PORTB	PB0 to PB7	PB0 to PB7
	PORTC	PC2 to PC7	PC0 to PC7
	PORTD	PD0 to PD4	PD0 to PD7
	PORTE	PE0 to PE7	PE0 to PE7
	PORTF	PF6, PF7	—
	PORTH	—	PH0 to PH3
	PORTJ	PJ0, PJ2, PJ3	PJ1, PJ3, PJ6, PJ7
Open-drain output function	PORT0	P02, P04, P07	—
	PORT1	P10 to P17	P12 to P17
	PORT2	P20 to P27	P20 to P23, P26, P27
	PORT3	P30 to P32	P30 to P34, P36, P37
	PORT5	P50 to P53, P56	—
	PORTA	PA0 to PA7	PA0 to PA7
	PORTB	PB0 to PB7	PB0 to PB7
	PORTC	PC2 to PC7	PC0 to PC7
	PORTD	—	PD0 to PD2
	PORTE	PE0 to PE7	PE0 to PE3
	PORTJ	PJ3	PJ3
Drive capacity switching function	PORT0	—	P03 to P07*1
	PORT1	—	P12 to P17
	PORT2	—	P20 to P27
	PORT3	—	P30 to P34, P36*1, P37*1
	PORT4	—	P40 to P47*1
	PORT5	—	P50 to P55
	PORTA	—	PA0 to PA7
	PORTB	—	PB0 to PB7
	PORTC	—	PC0 to PC7
	PORTD	—	PD0 to PD7
	PORTE	—	PE0 to PE7
	PORTH	—	PH0 to PH3
	PORTJ	—	PJ1, PJ3, PJ6*1, PJ7*1
5 V tolerant	PORT1	P16, P17	P12, P13, P16, P17
	PORTA	PA6	—
	PORTB	PB0	—

Note 1. Fixed to normal output

Table 2.24 Comparative Listing of I/O Port Functions (64-Pin)

Item	Port Symbol	RX113	RX130
Input pull-up function	PORT0	—	P03, P05
	PORT1	P14 to P17	P14 to P17
	PORT2	P26, P27	P26, P27
	PORT3	P30 to P32	P30 to P32, P35 to P37
	PORT4	—	P40 to P47
	PORT5	P54, P55	P54, P55
	PORTA	PA0, PA1, PA3, PA4, PA6	PA0, PA1, PA3, PA4, PA6
	PORTB	PB0, PB1, PB3, PB5 to PB7*1	PB0, PB1, PB3, PB5 to PB7*1*2
	PORTC	PC2 to PC7*1	PC0 to PC7*1*2
	PORTD	PD0 to PD2	—
	PORTE	PE0 to PE7	PE0 to PE5
	PORTH	—	PH0 to PH3
	PORTJ	PJ0, PJ2	PJ6, PJ7
Open-drain output function	PORT1	P14 to P17	P14 to P17
	PORT2	P26, P27	P26, P27
	PORT3	P30 to P32	P30 to P32, P36, P37
	PORTA	PA0, PA1, PA3, PA4, PA6	PA0, PA1, PA3, PA4, PA6
	PORTB	PB0, PB1, PB3, PB5 to PB7*1	PB0, PB1, PB3, PB5 to PB7*1*2
	PORTC	PC2 to PC7*1	PC0 to PC7*1*2
	PORTE	PE0 to PE7	PE0 to PE3
Drive capacity switching function	PORT0	—	P03, P05
	PORT1	—	P14 to P17
	PORT2	—	P26, P27
	PORT3	—	P30 to P32, P36, P37
	PORT4	—	P40 to P47
	PORT5	—	P54, P55
	PORTA	—	PA0, PA1, PA3, PA4, PA6
	PORTB	—	PB0, PB1, PB3, PB5 to PB7*1*2
	PORTC	—	PC0 to PC7*1*2
	PORTE	—	PE0 to PE5
	PORTH	—	PH0 to PH3
	PORTJ	—	PJ6, PJ7
5 V tolerant	PORT1	P16, P17	P12, P13, P16, P17
	PORTA	PA6	—
	PORTB	PB0	—

Note 1. On 80-pin (RX130 only) and 64-pin package products, pins PB6 and PC0, and PB7 and PC1 have multiplexed functions. These can be switched by making settings to the PSRA register. The pin functions conform to the settings of the selected port.

Note 2. On 48-pin package products, pins PB0 and PC0, PB1 and PC1, PB3 and PC2, and PB5 and PC3 have multiplexed functions. These can be switched by making settings to the PSRB register. The pin functions conform to the settings of the selected port.

Table 2.25 Comparative Listing of I/O Port Registers

Register	Bit	RX113	RX130
ODR0	B0, B1	Pm0 Output Type Select ● P20, P30, P50, PA0, PB0, PC0, PE0 b0 0: CMOS output 1: N-channel open-drain output b1 These bits are read as 0. The write value should be 0. ● P10 b1 b0 0 0: CMOS output 0 1: N-channel open-drain output 1 0: P-channel open-drain output 1 1: Setting prohibited.	Pm0 Output Type Select b0 0: CMOS output 1: N-channel open-drain output b1 These bits are read as 0. The write value should be 0.
ODR1	B0, B1	Pm4 Output Type Select ● P04, P24, PA4, PB4, PC4, PE4 b0 0: CMOS output 1: N-channel open-drain output b1 These bits are read as 0. The write value should be 0. ● P14 b1 b0 0 0: CMOS output 0 1: N-channel open-drain output 1 0: P-channel open-drain output 1 1: Setting prohibited.	Pm4 Output Type Select b0 0: CMOS output 1: N-channel open-drain output b1 These bits are read as 0. The write value should be 0.
PSRB	—	—	Port switching register B
DSCR	—	—	Drive capacity control register

2.13 Multi-Function Pin Controller

Table 2.26 shows a comparative listing of functions assigned to each multiplexed pin, and Table 2.27 shows a comparative listing of the multi-function pin controller registers.

Blue characters exist only in the RX113, and orange characters exist only in the RX130. "√" indicates pin implemented, "×" indicates pin not implemented, "-" indicates no assignment pin for function, Grey hatching indicates pin function not implemented.

Table 2.26 Comparative Listing of Functions Assigned to Each Multiplexed Pin

Module/Function	Pin Functions	Allocation Port	RX113		RX130	
			100 pin	64 pin	100 pin	64 pin
Interrupt	NMI (input)	P35	○	○	○	○
	IRQ0 (input)	P30	○	○	○	○
		PE0	○	○	-	-
		PD0	○	○	○	×
		PH1	-	-	○	○
	IRQ1 (input)	P31	○	○	○	○
		PE1	○	○	-	-
		PD1	○	○	○	×
		PH2	-	-	○	○
	IRQ2 (input)	P32	○	○	○	○
		PB0	○	○	-	-
		PC4	○	○	-	-
		P12	○	×	○	×
		PD2	○	○	○	×
	IRQ3 (input)	P27	○	○	-	-
		PE3	○	○	-	-
		PA6	○	○	-	-
		P13	○	×	○	×
		PD3	○	×	○	×
		P33	-	-	○	×
	IRQ4 (input)	P14	○	○	○	○
		PB1	○	○	○	○
		PE4	○	○	-	-
		PD4	○	×	○	×
		P34	-	-	○	×
	IRQ5 (input)	P15	○	○	○	○
		PA4	○	○	○	○
		PE5	○	○	○	○
		P56	○	×	-	-
		PD5	-	-	○	×
	IRQ6 (input)	P16	○	○	○	○
		PA3	○	○	○	○
		PE6	○	○	○	×
		P10	○	×	-	-
		PD6	-	-	○	×

Module/Function	Pin Functions	Allocation Port	RX113		RX130	
			100 pin	64 pin	100 pin	64 pin
Interrupt	IRQ7 (input)	P17	○	○	○	○
		PE2	○	○	○	○
		PE7	○	○	○	×
		P11	○	×	-	-
		PD7	-	-	○	×
Multi-function timer unit 2	MTIOC0A (input/output)	P14	○	○	-	-
		PB3	○	○	○	○
		PE3	○	○	-	-
		P04	○	×	-	-
		P34	-	-	○	×
	MTIOC0B (input/output)	P15	○	○	○	○
		PA1	○	○	○	○
		P13	○	×	○	×
	MTIOC0C (input/output)	P17	○	○	-	-
		P32	○	○	○	○
		PB0	○	○	-	-
		PB1	○	○	○	○
	MTIOC0D (input/output)	PA3	○	○	○	○
		P02	○	×	-	-
		P33	-	-	○	×
	MTIOC1A (input/output)	PE4	○	○	○	○
		P20	○	×	○	×
		P56	○	×	-	-
	MTIOC1B (input/output)	PA3	○	○	-	-
		PB5	○	○	○	○
		PE3	○	○	-	-
		P21	○	×	○	×
	MTIOC2A (input/output)	P26	○	○	○	○
		PA6	○	○	-	-
		PB5	○	○	○	○
		PE0	○	○	-	-
		P50	○	×	-	-
	MTIOC2B (input/output)	P27	○	○	○	○
		PA4	○	○	-	-
		PE5	○	○	○	○
		P53	○	×	-	-
	MTIOC3A (input/output)	P14	○	○	○	○
		P17	○	○	○	○
		PC7	○	○	○	○
		PE4	○	○	-	-
		PC1	○	×	○	×
		PF7	○	×	-	-
		PJ1	-	-	○	×

Module/Function	Pin Functions	Allocation Port	RX113		RX130	
			100 pin	64 pin	100 pin	64 pin
Multi-function timer unit 2	MTIOC3B (input/output)	P17	○	○	○	○
		PB3	○	○	-	-
		PB7	○	○	○	○
		PC5	○	○	○	○
		P22	○	×	○	×
	MTIOC3C (input/output)	P16	○	○	○	○
		PC6	○	○	○	○
		PJ3	○	×	○	×
		PC0	○	×	○	×
		PF6	○	×	-	-
	MTIOC3D (input/output)	P16	○	○	○	○
		PB6	○	○	○	○
		PC4	○	○	○	○
		P23	○	×	○	×
	MTIOC4A (input/output)	PA0	○	○	○	○
		PB3	○	○	○	○
		PE2	○	○	○	○
		P24	○	×	○	×
	MTIOC4B (input/output)	P30	○	○	○	○
		P54	○	○	○	○
		PC2	○	○	○	○
		PE3	○	○	○	○
		PD1	○	○	○	×
	MTIOC4C (input/output)	PB1	○	○	○	○
		PE1	○	○	○	○
		PE5	○	○	○	○
		P25	○	×	○	×
		P51	○	×	-	-
	MTIOC4D (input/output)	P31	○	○	○	○
		P55	○	○	○	○
		PC3	○	○	○	○
		PE4	○	○	○	○
		PD2	○	○	○	×
	MTIC5U (input)	PA4	○	○	○	○
		P11	○	×	-	-
		PD7	-	-	○	×
	MTIC5V (input)	PA6	○	○	○	○
		P10	○	×	-	-
		PD6	-	-	○	×
	MTIC5W (input)	PB0	○	○	○	○
		P56	○	×	-	-
		PD5	-	-	○	×

Module/Function	Pin Functions	Allocation Port	RX113		RX130	
			100 pin	64 pin	100 pin	64 pin
Multi-function timer unit 2	MTCLKA (input)	P14	○	○	○	○
		PA4	○	○	○	○
		PC6	○	○	○	○
		P24	○	×	○	×
	MTCLKB (input)	P15	○	○	○	○
		PA6	○	○	○	○
		PC7	○	○	○	○
		P25	○	×	○	×
	MTCLKC (input)	PA1	○	○	○	○
		PC4	○	○	○	○
		P22	○	×	○	×
	MTCLKD (input)	PA3	○	○	○	○
		PC5	○	○	○	○
		P23	○	×	○	×
Port output enable 2	POE0# (input)	PC4	○	○	○	○
		PA3	○	○	-	-
		P11	○	×	-	-
		PD7	-	-	○	×
	POE1# (input)	PB5	○	○	○	○
		P10	○	×	-	-
		PD6	-	-	○	×
	POE2# (input)	PA6	○	○	○	○
		P04	○	×	-	-
		P56	○	×	-	-
		P34	-	-	○	×
		PD5	-	-	○	×
	POE3# (input)	PB3	○	○	○	○
		PE0	○	○	-	-
		P02	○	×	-	-
		PD4	○	×	○	×
		P33	-	-	○	×
	POE8# (input)	P17	○	○	○	○
		P30	○	○	○	○
		PE3	○	○	○	○
		PD3	○	×	○	×
8-bit timer	TMO0 (output)	P22	○	×	○	×
		PB3	○	○	○	○
		PH1	-	-	○	○
	TMCI0 (input)	P21	○	×	○	×
		PB1	○	○	○	○
		PH3	-	-	○	○
	TMRI0 (input)	P20	○	×	○	×
		PA4	○	○	○	○
		PH2	-	-	○	○

Module/Function	Pin Functions	Allocation Port	RX113		RX130	
			100 pin	64 pin	100 pin	64 pin
8-bit timer	TMO1 (output)	P17	○	○	○	○
		P26	○	○	○	○
	TMCI1 (input)	P12	○	×	○	×
		P54	○	○	○	○
		PC4	○	○	○	○
	TMRI1 (input)	P24	○	×	○	×
		PB5	○	○	○	○
	TMO2 (output)	P16	○	○	○	○
		PC7	○	○	○	○
	TMCI2 (input)	P15	○	○	○	○
		P31	○	○	○	○
		PC6	○	○	○	○
	TMRI2 (input)	P14	○	○	○	○
		PC5	○	○	○	○
	TMO3 (output)	P13	○	×	○	×
		P32	○	○	○	○
		P55	○	○	○	○
	TMCI3 (input)	P04	○	×	-	-
		P27	○	○	○	○
		PA6	○	○	○	○
		P34	-	-	○	×
	TMRI3 (input)	P02	○	×	-	-
		P30	○	○	○	○
		P33	-	-	○	×
Serial communications interface	RXD0 (input)/ SMISO0 (input/output)/ SSCL0 (input/output)	P21	○	×	○	×
		P11	○	×	-	-
	TXD0 (output)/ SMOSI0 (input/output)/ SSDA0 (input/output)	P20	○	×	○	×
		P10	○	×	-	-
	SCK0 (input/output)	P22	○	×	○	×
		P12	○	×	-	-
	CTS0# (input)/ RTS0# (output)/ SS0# (input)	P23	○	×	○	×
		P13	○	×	-	-
	RXD1 (input)/ SMISO1 (input/output)/ SSCL1 (input/output)	P15	○	○	○	○
		P30	○	○	○	○
		PC6	○	○	-	-

Module/Function	Pin Functions	Allocation Port	RX113		RX130	
			100 pin	64 pin	100 pin	64 pin
Serial communications interface	TXD1 (output)/ SMOSI1 (input/output)/ SSDA1 (input/output)	P16	○	○	○	○
		P26	○	○	○	○
		PC7	○	○	-	-
		P56	○	×	-	-
	SCK1 (I/O)	P17	○	○	○	○
		P27	○	○	○	○
		PC5	○	○	-	-
	CTS1# (input)/ RTS1# (output)/ SS1# (input)	P14	○	○	○	○
		P31	○	○	○	○
	RXD2 (input)/ SMISO2 (input/output)/ SSCL2 (input/output)	P52	○	×		
	TXD2 (output)/ SMOSI2 (input/output)/ SSDA2 (input/output)	P50	○	×		
	SCK2 (input/output)	P51	○	×		
	CTS2# (input)/ RTS2# (output)/ SS2# (input)	P53	○	×		
	RXD5 (input)/ SMISO5 (input/output)/ SSCL5 (input/output)/ IRRXD5 (input)	PA3	○	○	○	○
		PC2	○	○	○	○
		PA2	○	×	○	×
	TXD5 (output)/ SMOSI5 (input/output)/ SSDA5 (input/output)/ IRTXD5 (output)	PA4	○	○	○	○
		PC3	○	○	○	○
	SCK5 (input/output)	PA1	○	○	○	○
		PC4	○	○	○	○
		PC1	○	×	○	×
	CTS5# (input)/ RTS5# (output)/ SS5# (input)	PA6	○	○	○	○
		PC0	○	×	○	×
	RXD6 (input)/ SMISO6 (input/output)/ SSCL6 (input/output)	P02	○	×	-	-
		P27	○	○	-	-
		PB0	○	○	○	○
		P33	-	-	○	×
		PD1	-	-	○	×

Module/Function	Pin Functions	Allocation Port	RX113		RX130	
			100 pin	64 pin	100 pin	64 pin
Serial communications interface	TXD6 (output)/ SMOSI6 (input/output)/ SSDA6 (input/output)	P07	○	×	-	-
		P26	○	○	-	-
		PB1	○	○	○	○
		P32	○	○	○	○
		PD0	-	-	○	×
	SCK6 (input/output)	P04	○	×	-	-
		PB3	○	○	○	○
		P34	-	-	○	×
		PD2	-	-	○	×
	CTS6# (input)/ RTS6# (output)/ SS6# (input)	P32	○	○	-	-
		PJ3	○	×	○	×
		PB2	○	×	○	×
	RXD8 (input)/ SMISO8 (input/output)/ SSCL8 (input/output)	PC6	○	○	○	×
		PA6	○	×	-	-
	TXD8 (output)/ SMOSI8 (input/output)/ SSDA8 (input/output)	PC7	○	○	○	×
		PA7	○	×	-	-
	SCK8 (input/output)	PC5	○	○	○	×
		PA5	○	×	-	-
	CTS8# (input)/ RTS8# (output)/ SS8# (input)	PC4	○	○	○	×
		PA4	○	×	-	-
	RXD9 (input)/ SMISO9 (input/output)/ SSCL9 (input/output)	PB6	○	○	○	×
		PE4	○	○	-	-
	TXD9 (output)/ SMOSI9 (input/output)/ SSDA9 (input/output)	PB7	○	○	○	×
		PE5	○	○	-	-
	SCK9 (input/output)	PB5	○	○	○	×
		PE3	○	○	-	-
	CTS9# (input)/ RTS9# (output)/ SS9# (input)	PB4	○	×	○	×
		PE0	○	○	-	-
	RXD12 (input)/ SMISO12 (input/output)/ SSCL12 (input/output)/ RXDX12 (input)	PE2	○	○	○	○
		P17	○	○	-	-
		P11	○	×	-	-

Module/Function	Pin Functions	Allocation Port	RX113		RX130	
			100 pin	64 pin	100 pin	64 pin
Serial communications interface	TXD12 (output)/ SMOSI12 (input/output)/ SSDA12 (input/output)/ TXDX12 (output)/ SIOX12 (input/output)	PE1	○	○	○	○
		P14	○	○	-	-
		P10	○	×	-	-
	SCK12 (input/output)	PE0	○	○	○	○
		P27	○	○	-	-
		P12	○	×	-	-
	CTS12# (input)/ RTS12# (output)/ SS12# (input)	PE3	○	○	○	○
		P13	○	×	-	-
I2C bus interface	SCL0 (input/output)	P16	○	○	○	○
		PB0	○	○	-	-
		P12	-	-	○	×
	SDA0 (input/output)	P17	○	○	○	○
		PA6	○	○	-	-
		P13	-	-	○	×
Serial peripheral interface	RSPCKA (input/output)	P15	○	○	-	-
		PB0	○	○	○	○
		PC5	○	○	○	○
		PE3	○	○	-	-
		P51	○	×	-	-
		PA5	-	-	○	×
	MOSIA (input/output)	P16	○	○	○	○
		PA6	○	○	○	○
		PE4	○	○	-	-
		PC6	○	○	○	○
		P50	○	×	-	-
	MISOA (input/output)	P17	○	○	○	○
		PC7	○	○	○	○
		PA3	○	○	-	-
		P52	○	×	-	-
		PE5	○	○	-	-
		PA7	-	-	○	×
	SSLA0 (input/output)	P14	○	○	-	-
		PA4	○	○	○	○
		PC4	○	○	○	○
		P53	○	×	-	-
	SSLA1 (output)	PA0	○	○	○	○
		PC0	○	×	○	×
	SSLA2 (output)	PA1	○	○	○	○
		PC1	○	×	○	×
	SSLA3 (output)	PC2	○	○	○	○

Module/Function	Pin Functions	Allocation Port	RX113		RX130	
			100 pin	64 pin	100 pin	64 pin
Serial peripheral interface	SSLA3 (output)	PA2	○	×	○	×
USB 2.0 host/function module	USB0_EXICEN (output)	PC6	○	○		
	USB0_VBUSEN (output)	P16	○	○		
		PC4	○	○		
		P26	○	○		
	USB0_OVRCURA (input)	P14	○	○		
		PB3	○	○		
	USB0_OVRCURB (input)	P16	○	○		
		PC7	○	○		
	USB0_ID (input)	PC5	○	○		
	USB0_VBUS (input)	P16	○	○		
	USB0_VBUS (input)	PC4	○	○		
Realtime clock	RTCOUT (output)	P16	○	○	○	○
		P32	○	○	○	○
		PB0	○	○	-	-
		PA1	○	○	-	-
12-bit A/D converter	AN000 (input)	P40	○	○	○	○
	AN001 (input)	P41	○	○	○	○
	AN002 (input)	P42	○	○	○	○
	AN003 (input)	P43	○	×	○	○
	AN004 (input)	P44	○	×	○	○
	AN005 (input)	P90	○	×	-	-
		P45	-	-	○	○
	AN006 (input)	P46	○	×	○	○
	AN007 (input)	P91	○	×	-	-
		P47	-	-	○	○
	AN008 (input)	PE0	○	○		
	AN009 (input)	PE1	○	○		
	AN010 (input)	PE2	○	○		
	AN011 (input)	PE3	○	○		
	AN012 (input)	PE4	○	○		
	AN013 (input)	PE5	○	○		
	AN014 (input)	PE6	○	○		
	AN015 (input)	PE7	○	○		
	AN016 (input)	PE0			○	○
	AN017 (input)	PE1			○	○
	AN018 (input)	PE2			○	○
	AN019 (input)	PE3			○	○
	AN020 (input)	PE4			○	○
	AN021 (input)	PE5			○	○
	AN022 (input)	PE6			○	×
	AN023 (input)	PE7			○	×
	AN024 (input)	PD0			○	×
	AN025 (input)	PD1			○	×

Module/Function	Pin Functions	Allocation Port	RX113		RX130	
			100 pin	64 pin	100 pin	64 pin
12-bit A/D converter	AN026 (input)	PD2			○	×
	AN027 (input)	PD3			○	×
	AN028 (input)	PD4			○	×
	AN029 (input)	PD5			○	×
	AN030 (input)	PD6			○	×
	AN031 (input)	PD7			○	×
	AN0021 (input)	P92	○	×		
	VREFH0 (input)	PJ6	○	○		
	VREFL0 (input)	PJ7	○	○		
	ADTRG0# (input)	P16	○	○	○	○
		P27	○	○	-	-
		PB0	○	○	-	-
		P25	○	×	○	×
		P07	○	×	○	×
12-bit D/A converter	DA0 (output)	PJ0	○	○	-	-
		P03	-	-	○	○
	DA1 (output)	PJ2	○	○	-	-
		P05	-	-	○	○
	VREFH	P41	○	○		
	VREFL	P42	○	○		
Clock	CLKOUT (output)	P15	○	○	-	-
		PC4	○	○	-	-
		PE3	-	-	○	○
		PE4	-	-	○	○
Clock frequency accuracy measurement circuit	CACREF (input)	P27	○	○	-	-
		PA0	○	○	○	○
		PC7	○	○	○	○
		P15	○	○	-	-
		PH0	-	-	○	○
Voltage detection circuit	CMPA2 (input)	P27	○	○	-	-
		PE4	-	-	○	○
Comparator B	CMPB0 (input)	PE1	○	○	○	○
	CVREFB0 (input)	PE2	○	○	○	○
	CMPOB0 (output)	PE7	○	○	-	-
		PE5	-	-	○	○
	CMPB1 (input)	PA3	○	○	○	○
	CVREFB1 (input)	PA4	○	○	○	○
	CMPOB1 (output)	PE5	○	○	-	-
		PB1	-	-	○	○
Serial sound interface	SSISCK0 (input/output)	PB5	○	○		
		PE0	○	○		
	SSIWS0 (input/output)	PB1	○	○		
		PE4	○	○		
	SSIRXD0 (input)	PB6	○	○		
		PE2	○	○		
	SSITXD0 (input)	PB7	○	○		
		PE1	○	○		

Module/Function	Pin Functions	Allocation Port	RX113		RX130	
			100 pin	64 pin	100 pin	64 pin
Serial sound interface	AUDIO_MCLK (input)	PB3	○	○		
		PE3	○	○		
LCD Controller/Drivers	COM0 (output)	PC5	○	○		
	COM1 (output)	PC4	○	○		
	COM2 (output)	PC3	○	○		
	COM3 (output)	PC2	○	○		
	SEG00 (output)	P13	○	×		
	SEG01 (output)	P12	○	×		
	SEG02 (output)	P11	○	×		
	SEG03 (output)	P10	○	×		
	SEG04 (output)	P56	○	×		
	SEG05 (output)	P53	○	×		
	SEG06 (output)	P52	○	×		
	SEG07 (output)	P51	○	×		
	SEG08 (output)	P50	○	×		
	SEG09 (output)	PC1	○	×		
	SEG10 (output)	PC0	○	×		
	SEG11/COM4 (output)	PB7	○	○		
	SEG12/COM5 (output)	PB6	○	○		
	SEG13/COM6 (output)	PB5	○	○		
	SEG14 (output)	PB4	○	×		
	SEG15/COM7 (output)	PB3	○	○		
	SEG16 (output)	PB2	○	×		
	SEG17 (output)	PB1	○	○		
	SEG18 (output)	PA7	○	×		
	SEG19 (output)	PA5	○	×		
	SEG20 (output)	PA4	○	○		
	SEG21 (output)	PA3	○	○		
	SEG22 (output)	PA2	○	×		
	SEG23 (output)	PA1	○	○		
	SEG24 (output)	PA0	○	○		
	SEG25 (output)	PF7	○	×		
	SEG26 (output)	PF6	○	×		
	SEG27 (output)	PE5	○	○		
	SEG28 (output)	PE4	○	○		
	SEG29 (output)	PE3	○	○		
	SEG30 (output)	PE2	○	○		
	SEG31 (output)	PE1	○	○		
	SEG32 (output)	PE0	○	○		
	SEG33 (output)	PE7	○	○		
	SEG34 (output)	PE6	○	○		
	SEG35 (output)	PD4	○	×		
	SEG36 (output)	PD3	○	×		
	SEG37 (output)	PD2	○	○		

Module/Function	Pin Functions	Allocation Port	RX113		RX130	
			100 pin	64 pin	100 pin	64 pin
LCD Controller/Drivers	SEG38 (output)	PD1	○	○		
	SEG39 (output)	PD0	○	○		
	CAPH (output)	P30	○	○		
	CAPL (output)	P31	○	○		
	VL1 (input/output)	P55	○	○		
	VL2 (input/output)	P54	○	○		
	VL3 (input/output)	PC7	○	○		
	VL4 (input/output)	PC6	○	○		
Capacitive touch sensing unit	TS0 (output)	P07	○	×		
	TS0 (input/output)	P32			○	○
	TS1 (output)	P04	○	×		
	TS1 (input/output)	P31			○	○
	TS2 (output)	P02	○	×	-	-
		P30	-	-	○	○
	TS3 (output)	PJ3	○	×	-	-
		P27	-	-	○	○
	TS4 (output)	P25	○	×	-	-
		P26	-	-	○	○
	TS5 (output)	P24	○	×	-	-
		P15	-	-	○	○
	TS6 (output)	P23	○	×	-	-
		P14	-	-	○	○
	TS7 (output)	P22	○	×	-	-
		PH3	-	-	○	○
	TS8 (output)	P21	○	×	-	-
		PH2	-	-	○	○
	TS9 (output)	P20	○	×	-	-
		PH1	-	-	○	○
	TS10 (output)	P27	○	×	-	-
		PH0	-	-	○	○
	TS11 (output)	P32	○	×	-	-
		P55	-	-	○	○
	TS12 (output)	P54			○	○
	TS13 (output)	PC7			○	○
	TS14 (output)	PC6			○	○
	TS15 (output)	PC5			○	○
	TS16 (output)	PC3			○	○
	TS17 (output)	PC2			○	○
	TS18 (output)	PB7			○	○
	TS19 (output)	PB6			○	○
	TS20 (output)	PB5			○	○
	TS21 (output)	PB4			○	×
	TS22 (output)	PB3			○	○
	TS23 (output)	PB2			○	×
	TS24 (output)	PB1			○	○
	TS25 (output)	PB0			○	○
	TS26 (output)	PA6			○	○

Module/Function	Pin Functions	Allocation Port	RX113		RX130	
			100 pin	64 pin	100 pin	64 pin
Capacitive touch sensing unit	TS27 (output)	PA5			○	×
	TS28 (output)	PA4			○	○
	TS29 (output)	PA3			○	○
	TS30 (output)	PA2			○	×
	TS31 (output)	PA1			○	○
	TS32 (output)	PA0			○	○
	TS33 (output)	PE4			○	○
	TS34 (output)	PE3			○	○
	TS35 (output)	PE2			○	○
	TSCAP (input/output)	P26	○	×		
	TSCAP (—)	PC4			○	○
Remote control signal receiver (REMC)	PMC0	P51			○	×
	PMC1	P52			○	×

Table 2.27 Comparative Listing of Multi-Function Pin Controller Registers

Register	Bit	RX113	RX130
P0nPFS	ASEL	—	Analog function select bit
P1nPFS	ISEL	Interrupt function select bit 0: Not used as IRQn input pin. 1: Used as IRQn input pin. P10: IRQ6 (100 pin) P11: IRQ7 (100 pin) P12: IRQ2 (100 pin) P13: IRQ3 (100 pin) P14: IRQ4 (100/64 pins) P15: IRQ5 (100/64 pins) P16: IRQ6 (100/64 pins) P17: IRQ7 (100/64 pins)	Interrupt function select bit 0: Not used as IRQn input pin. 1: Used as IRQn input pin. P12: IRQ2 (100/80 pins) P13: IRQ3 (100/80 pins) P14: IRQ4 (100/80/64/48 pins) P15: IRQ5 (100/80/64/48 pins) P16: IRQ6 (100/80/64/48 pins) P17: IRQ7 (100/80/64/48 pins)
P2nPFS	ISEL	Interrupt function select bit	—
	ASEL	Analog function select bit	—
P3nPFS	ISEL	Interrupt function select bit 0: Not used as IRQn input pin. 1: Used as IRQn input pin. P30: IRQ0 (100/64 pins) P31: IRQ1 (100/64 pins) P32: IRQ2 (100/64 pins)	Interrupt function select bit 0: Not used as IRQn input pin. 1: Used as IRQn input pin. P30: IRQ0 (100/80/64/48 pins) P31: IRQ1 (100/80/64/48 pins) P32: IRQ2 (100/80/64 pins) P33: IRQ3 (100 pin) P34: IRQ4 (100/80 pins)
P4nPFS	ASEL	Analog function select bit 0: Not used as an analog pin. 1: Used as an analog pin. P40: AN000 (100/64 pins) P41: AN001/VREFH (100/64 pins) P42: AN002/VREFL (100/64 pins) P43: AN003 (100 pin) P44: AN004 (100 pin) P46: AN006 (100 pin)	Analog function select bit 0: Not used as an analog pin. 1: Used as an analog pin. P40: AN000 (100/80/64/48 pins) P41: AN001 (100/80/64/48 pins) P42: AN002 (100/80/64/48 pins) P43: AN003 (100/80/64 pins) P44: AN004 (100/80/64 pins) P45: AN005 (100/80/64/48 pins) P46: AN006 (100/80/64/48 pins) P47: AN007 (100/80/64/48 pins)
P5nPFS	ISEL	Interrupt function select bit 0: Not used as IRQn input pin. 1: Used as IRQn input pin. P56: IRQ5 (100 pin)	—
P9nPFS	—	P9n pin function select registers	—
PAnPFS	ISEL	Interrupt function select bit 0: Not used as IRQn input pin. 1: Used as IRQn input pin. PA3: IRQ6 (100/64 pins) PA4: IRQ5 (100/64 pins) PA6: IRQ3 (100/64 pins)	Interrupt function select bit 0: Not used as IRQn input pin. 1: Used as IRQn input pin. PA3: IRQ6 (100/80/64/48 pins) PA4: IRQ5 (100/80/64/48 pins)
PBnPFS	ISEL	Interrupt function select bit 0: Not used as IRQn input pin. 1: Used as IRQn input pin. PB0: IRQ2 (100/64 pins) PB1: IRQ4 (100/64 pins)	Interrupt function select bit 0: Not used as IRQn input pin. 1: Used as IRQn input pin. PB1: IRQ4 (100/80/64/48 pins)

Register	Bit	RX113	RX130
PCnPFS	ISEL	Interrupt function select bit 0: Not used as IRQn input pin. 1: Used as IRQn input pin. PC4: IRQ2 (100/64 pins)	—
PDnPFS	ISEL	Interrupt function select bit 0: Not used as IRQn input pin. 1: Used as IRQn input pin. PD0: IRQ0 (100/64 pins) PD1: IRQ1 (100/64 pins) PD2: IRQ2 (100/64 pins) PD3: IRQ3 (100 pin) PD4: IRQ4 (100 pin)	Interrupt function select bit 0: Not used as IRQn input pin. 1: Used as IRQn input pin. PD0: IRQ0 (100/80 pins) PD1: IRQ1 (100/80 pins) PD2: IRQ2 (100/80 pins) PD3: IRQ3 (100 pin) PD4: IRQ4 (100 pin) PD5: IRQ5 (100 pin) PD6: IRQ6 (100 pin) PD7: IRQ7 (100 pin)
	ASEL	—	Analog function select bit 0: Not used as an analog pin. 1: Used as an analog pin. PD0: AN024 (100/80 pins) PD1: AN025 (100/80 pins) PD2: AN026 (100/80 pins) PD3: AN027 (100 pin) PD4: AN028 (100 pin) PD5: AN029 (100 pin) PD6: AN030 (100 pin) PD7: AN031 (100 pin)
PEnPFS	ISEL	Interrupt input function select bit 0: Not used as IRQn input pin. 1: Used as IRQn input pin. PE0: IRQ0 (100/64 pins) PE1: IRQ1 (100/64 pins) PE2: IRQ7 (100/64 pins) PE3: IRQ3 (100/64 pins) PE4: IRQ4 (100/64 pins) PE5: IRQ5 (100/64 pins) PE6: IRQ6 (100/64 pins) PE7: IRQ7 (100/64 pins)	Interrupt function select bit 0: Not used as IRQn input pin. 1: Used as IRQn input pin. PE2: IRQ7 (100/80/64/48 pins) PE5: IRQ5 (100/80/64 pins) PE6: IRQ6 (100 pin) PE7: IRQ7 (100 pin)

Register	Bit	RX113	RX130
PEnPFS	ASEL	PEn Analog function select bit 0: Not used as an analog pin. 1: Used as an analog pin. PE0: AN008 (100/64 pins) PE1: AN009/CMPB0 (100/64 pins) PE2: AN010/CVREFB0 (100/64 pins) PE3: AN011 (100/64 pins) PE4: AN012 (100/64 pins) PE5: AN013 (100/64 pins) PE6: AN014 (100/64 pins) PE7: AN015 (100/64 pins)	Analog function select bit 0: Not used as an analog pin. 1: Used as an analog pin. PE0: AN016 (100/80/64 pins) PE1: AN017, CMPB0 (100/80/64/48 pins) PE2: AN018, CVREFB0 (100/80/64/48 pins) PE3: AN019 (100/80/64/48 pins) PE4: AN020, CMPA2 (100/80/64/48 pins) PE5: AN021 (100/80/64 pins) PE6: AN022 (100 pin) PE7: AN023 (100 pin)
PFnPFS	—	PFn pin function select registers	—
PHnPFS	—	—	PHn pin function select registers
PJnPFS	ASEL	Analog function select bit 0: Not used as an analog pin. 1: Used as an analog pin. PJ0: DA0 (100/64 pins) PJ2: DA1 (100/64 pins)	Analog function select bit 0: Not used as an analog pin. 1: Used as an analog pin. PJ6: VREFH0 PJ7: VREFL0
		0: The AVCC0 pin is selected as the reference power supply pin for high-electric potential. 1: The VREFH0 pin is selected as the reference power supply pin for high-electric potential. PJ6: AVCC0/VREFH0 (100/64 pins)	
		0: The AVSS0 pin is selected as the reference power supply ground pin for low-electric potential. 1: The VREFL0 pin is selected as the reference power supply ground pin for low-electric potential. PJ7: AVSS0/VREFL0 (100/64 pins)	

2.14 8-Bit Timer

Table 2.28 shows a comparative overview of 8-bit timer specifications.

Table 2.28 Comparative Overview of 8-Bit Timer Specifications

Item	RX113 (TMR)	RX130 (TMR)
Count clocks	• Internal clock: PCLK/1, PCLK/2, PCLK/8, PCLK/32, PCLK/64, PCLK/1,024, PCLK/8,192 • External clock: external count clock	• Frequency-divided clock: PCLK/1, PCLK/2, PCLK/8, PCLK/32, PCLK/64, PCLK/1,024, PCLK/8,192 • External clock: external count clock
Number of channels	(8 bits × 2 channels) × 2 units	(8 bits × 2 channels) × 2 units
Compare match	• 8-bit mode (compare match A, compare match B) • 16-bit mode (compare match A, compare match B)	• 8-bit mode (compare match A, compare match B) • 16-bit mode (compare match A, compare match B)
Counter clear	Selectable among compare match A, compare match B, and external reset signal.	Selectable among compare match A, compare match B, and external reset signal.
Timer output	Output pulses with a user-defined duty cycle or PWM output	Output pulses with a user-defined duty cycle or PWM output
Cascading of two channels	• 16-bit count mode 16-bit timer using TMR0 for the upper 8 bits and TMR1 for the lower 8 bits (TMR2 for the upper 8 bits and TMR3 for the lower 8 bits) • Compare match count mode TMR1 can be used to count TMR0 compare matches (TMR3 can be used to count TMR2 compare matches).	• 16-bit count mode 16-bit timer using TMR0 for the upper 8 bits and TMR1 for the lower 8 bits (TMR2 for the upper 8 bits and TMR3 for the lower 8 bits) • Compare match count mode TMR1 can be used to count TMR0 compare matches (TMR3 can be used to count TMR2 compare matches).
Interrupt sources	Compare match A, compare match B, and overflow	Compare match A, compare match B, and overflow
Event link function (output)	Compare match A, compare match B, and overflow (TMR0 and TMR2)	Compare match A, compare match B, and overflow (TMR0 and TMR2)
Event link function (input)	Ability to perform one of three actions according to accepted event (1) Counter start (TMR0 and TMR2) (2) Event counter (TMR0 and TMR2) (3) Counter restart (TMR0 and TMR2)	Ability to perform one of three actions according to accepted event (1) Counter start (TMR0 and TMR2) (2) Event counter (TMR0 and TMR2) (3) Counter restart (TMR0 and TMR2)
DTC activation	The DTC can be activated by compare match A interrupts or compare match B interrupts.	The DTC can be activated by compare match A interrupts or compare match B interrupts.
Generation of baud rate clock for SCI	—	Generation of baud rate clock for SCI
Generation of receive clock for REMC	—	Generation of operating clock for remote control signal receiver (REMC)
Low power consumption function	It is possible to transition each unit to the module stop state for each unit.	It is possible to transition each unit to the module stop state.

2.15 Compare Match Timer

Table 2.29 shows a comparative overview of the compare match timer specification, and Table 2.30 shows a comparative listing of the compare match timer registers.

Table 2.29 Comparative Overview of Compare Match Timer Specifications

Item	RX113 (CMT)	RX130 (CMT)
Number of units	2 compare match timer (CMT) units (unit 0 and unit 1), each consisting of a 2-channel 16-bit timer, for a total of 4 channels	1 compare match timer (CMT) unit (unit 0), each consisting of a 2-channel 16-bit timer, for a total of 2 channels
Count clocks	Four frequency-divided clocks One clock from PCLK/8, PCLK/32, PCLK/128, and PCLK/512 can be selected for each channel.	Four frequency-divided clocks One clock from PCLK/8, PCLK/32, PCLK/128, and PCLK/512 can be selected for each channel.
Interrupt	A compare match interrupt can be requested for each channel.	A compare match interrupt can be requested for each channel.
Event link function (output)	Event signal output at CMT1 compare match	Event signal output at CMT1 compare match
Event link function (input)	• Support for linked operation of specified module • Support for CMT1 counter start, event counter, and count restart	• Support for linked operation of specified module • Support for CMT1 counter start, event counter, and count restart
Low power consumption function	It is possible to specify the module stop state for each unit.	It is possible to specify the module stop state.

Table 2.30 Comparative Listing of Compare Match Timer Registers

Register	Bit	RX113 (CMT)	RX130 (CMT)
CMSTR1	—	Compare match timer start register 1	—

2.16 Realtime Clock

Table 2.31 shows a comparative listing of the realtime clock registers.

Table 2.31 Comparative Listing of Realtime Clock Registers

Register	Bit	RX113 (RTCA)	RX130 (RTCc)
RCR3	RTCDV[2:0]	Sub-clock oscillator drive capacity control bits b3 b1 0 0 0: Medium drive capacity for low CL 0 0 1: High drive capacity for low CL 0 1 0: Low drive capacity for low CL 1 0 0: Drive capacity for standard CL Do not set to values other than the above.	Sub-clock oscillator drive capacity control bits b3 b1 0 0 0: Setting prohibited. 0 0 1: Drive capacity for low CL 0 1 0: Setting prohibited. 0 1 1: Setting prohibited. 1 0 0: Setting prohibited. 1 0 1: Setting prohibited. 1 1 0: Drive capacity for standard CL 1 1 1: Setting prohibited.

Note 1. Only the notation differs. The functionality is the same.

2.17 Serial Communication Interface

Table 2.32 and Table 2.33 show a comparative overview of the serial communication interface specifications, and Table 2.34 shows a comparative listing of the serial communication interface registers.

Table 2.32 Comparative Overview of Serial Communication Interface Specifications (SCIe: RX113, SCIg: RX130)

Item	RX113 (SCIe)	RX130 (SCIg)
Number of channels	7 channels (SCI0, SCI1, SCI2, SCI5, SCI6, SCI8, SCI9)	6 channels (SCI0, SCI1, SCI5, SCI6, SCI8, SCI9)
Serial communication modes	• Asynchronous • Clock synchronous • Smart card interface • Simple I²C bus • Simple SPI bus	• Asynchronous • Clock synchronous • Smart card interface • Simple I²C bus • Simple SPI bus
Transfer speed	Bit rate specifiable by on-chip baud rate generator.	Bit rate specifiable by on-chip baud rate generator.
Full-duplex communication	Transmitter: Continuous transmission possible using double-buffer configuration. Receiver: Continuous reception possible using double-buffer configuration.	Transmitter: Continuous transmission possible using double-buffer configuration. Receiver: Continuous reception possible using double-buffer configuration.
I/O pins	• SCI I/O pins (asynchronous mode and clock synchronous mode) SCK0, RXD0, TXD0, CTS0#/RTS0# SCK1, RXD1, TXD1, CTS1#/RTS1# SCK2, RXD2, TXD2, CTS2#/RTS2# SCK5, RXD5, TXD5, CTS5#/RTS5# SCK6, RXD6, TXD6, CTS6#/RTS6# SCK8, RXD8, TXD8, CTS8#/RTS8# SCK9, RXD9, TXD9, CTS9#/RTS9# • SCI I/O pins (simple I²C mode) SSCL0, SSDA0, SSCL1, SSDA1, SSCL2, SSDA2, SSCL5, SSDA5, SSCL6, SSDA6, SSCL8, SSDA8, SSCL9, SSDA9	• SCI I/O pins (asynchronous mode and clock synchronous mode) SCK0, RXD0, TXD0, CTS0#/RTS0# SCK1, RXD1, TXD1, CTS1#/RTS1# SCK5, RXD5, TXD5, CTS5#/RTS5# SCK6, RXD6, TXD6, CTS6#/RTS6# SCK8, RXD8, TXD8, CTS8#/RTS8# SCK9, RXD9, TXD9, CTS9#/RTS9# • SCI I/O pins (simple I²C mode) SSCL0, SSDA0, SSCL1, SSDA1, SSCL5, SSDA5, SSCL6, SSDA6, SSCL8, SSDA8, SSCL9, SSDA9

Item		RX113 (SCIe)	RX130 (SCIg)
I/O pins		• SCI I/O pins (simple SPI mode) SCK0, SMISO0, SMOSI0, SS0#, SCK1, SMISO1, SMOSI1, SS1#, SCK2, SMISO2, SMOSI2, SS2#, SCK5, SMISO5, SMOSI5, SS5#, SCK6, SMISO6, SMOSI6, SS6#, SCK8, SMISO8, SMOSI8, SS8#, SCK9, SMISO9, SMOSI9, SS9#	• SCI I/O pins (simple SPI mode) SCK0, SMISO0, SMOSI0, SS0#, SCK1, SMISO1, SMOSI1, SS1#, SCK5, SMISO5, SMOSI5, SS5#, SCK6, SMISO6, SMOSI6, SS6#, SCK8, SMISO8, SMOSI8, SS8#, SCK9, SMISO9, SMOSI9, SS9#
Data transfer		Selectable between LSB-first or MSB-first transfer.	Selectable between LSB-first or MSB-first transfer.
Interrupt sources		Transmit end, transmit data empty, receive data full, receive error, completion of generation of start condition, restart condition, or stop condition (simple I^2C mode)	Transmit end, transmit data empty, receive data full, receive error, completion of generation of start condition, restart condition, or stop condition (simple I^2C mode)
Low power consumption function		It is possible to transition each channel to the module stop state.	It is possible to transition each channel to the module stop state.
Synchronous mode	Data length	7 or 8 bits	7, 8, or 9 bits
	Transmission stop bits	1 or 2 bits	1 or 2 bits
	Parity	Even parity, odd parity, or no parity	Even parity, odd parity, or no parity
	Receive error detection	Parity, overrun, and framing errors	Parity, overrun, and framing errors
	Hardware flow control	The CTSn# and RTSn# pins can be used to control transmission and reception.	The CTSn# and RTSn# pins can be used to control transmission and reception.
	Start bit detection	Selectable between low level and falling edge.	Selectable between low level and falling edge.
	Break detection	When a framing error occurs, a break can be detected by reading the RXDn pin level directly.	When a framing error occurs, a break can be detected by reading the RXDn pin level directly.
	Clock source	An internal or external clock can be selected. Transfer rate clock input from the TMU can be used (SCI1 and SCI5).	An internal or external clock can be selected. Transfer rate clock input from the TMR can be used (SCI5 and SCI6).
	Double-speed mode	—	Baud rate generator double-speed mode is selectable.
	Multi-processor communication function	Serial communication among multiple processors	Serial communication among multiple processors
	Noise cancellation	The signal paths from input on the RXDn pins incorporate on-chip digital noise filters.	The signal paths from input on the RXDn pins incorporate on-chip digital noise filters.

Item		RX113 (SCIe)	RX130 (SCIg)
Clock synchronous mode	Data length	8 bits	8 bits
	Receive error detection	Overrun error	Overrun error
	Hardware flow control	The CTSn# and RTSn# pins can be used to control transmission and reception.	The CTSn# and RTSn# pins can be used to control transmission and reception.
Smart card interface mode	Error processing	An error signal can be transmitted automatically when a parity error is detected during reception.	An error signal can be transmitted automatically when a parity error is detected during reception.
		Data can be retransmitted automatically when an error signal is received during transmission.	Data can be retransmitted automatically when an error signal is received during transmission.
	Data type	Both direct convention and inverse convention are supported.	Both direct convention and inverse convention are supported.
Simple I^2C mode	Communication format	I^2C bus format	I^2C bus format
	Operating mode	Master (single-master operation only)	Master (single-master operation only)
	Transfer speed	Fast mode is supported.	Fast mode is supported.
	Noise canceler	The signal paths from input on the SSCLn and SSDAn pins incorporate on-chip digital noise filters, and the noise cancellation bandwidth is adjustable.	The signal paths from input on the SSCLn and SSDAn pins incorporate on-chip digital noise filters, and the noise cancellation bandwidth is adjustable.
Simple SPI mode	Data length	8 bits	8 bits
	Error detection	Overrun error	Overrun error
	SS input pin function	Applying a high-level signal to the SSn# pin causes the output pins to enter the high-impedance state.	Applying a high-level signal to the SSn# pin causes the output pins to enter the high-impedance state.
	Clock settings	Selectable among four clock phase and clock polarity settings.	Selectable among four clock phase and clock polarity settings.
Bit rate modulation function		—	On-chip baud rate generator output correction can reduce errors.
Event link function (SCI5 only)		Error (receive error, error signal detection) event output	Error (receive error, error signal detection) event output
		Receive data full event output	Receive data full event output
		Transmit data empty event output	Transmit data empty event output
		Transmit end event output	Transmit end event output

Table 2.33 Comparative Overview of Serial Communication Interface Specifications (SCIf: RX113, SCIh: RX130)

Item		RX113 (SCIf)	RX130 (SCIh)
Number of channels		1 channel (SCI12)	1 channels (SCI12)
Serial communication modes		• Asynchronous • Clock synchronous • Smart card interface • Simple I²C bus • Simple SPI bus	• Asynchronous • Clock synchronous • Smart card interface • Simple I²C bus • Simple SPI bus
Transfer speed		Bit rate specifiable by on-chip baud rate generator.	Bit rate specifiable by on-chip baud rate generator.
Full-duplex communication		Transmitter: Continuous transmission possible using double-buffer configuration. Receiver: Continuous reception possible using double-buffer configuration.	Transmitter: Continuous transmission possible using double-buffer configuration. Receiver: Continuous reception possible using double-buffer configuration.
I/O pins		• SCI I/O pins (asynchronous mode and clock synchronous mode) SCK12, RXD12, TXD12, CTS12#/RTS12# • SCI I/O pins (simple I²C mode) SSCL12, SSDA12 • SCI I/O pins (simple SPI mode) SCK12, SMISO12, SMOSI12, SS12# • SCI I/O pins (extended serial mode) RXDX12, TXDX12, SIOX12	• SCI I/O pins (asynchronous mode and clock synchronous mode) SCK12, RXD12, TXD12, CTS12#/RTS12# • SCI I/O pins (simple I²C mode) SSCL12, SSDA12 • SCI I/O pins (simple SPI mode) SCK12, SMISO12, SMOSI12, SS12# • SCI I/O pins (extended serial mode) RXDX12, TXDX12, SIOX12
Data transfer		Selectable between LSB-first or MSB-first transfer.	Selectable between LSB-first or MSB-first transfer.
Interrupt sources		Transmit end, transmit data empty, receive data full, receive error, completion of generation of start condition, restart condition, or stop condition (simple I²C mode)	Transmit end, transmit data empty, receive data full, receive error, completion of generation of start condition, restart condition, or stop condition (simple I²C mode)
Low power consumption function		It is possible to transition to the module stop state.	It is possible to transition to the module stop state.
Synchronous mode	Data length	7 or 8 bits	7, 8, or 9 bits
	Transmission stop bits	1 or 2 bits	1 or 2 bits
	Parity	Even parity, odd parity, or no parity	Even parity, odd parity, or no parity
	Receive error detection	Parity, overrun, and framing errors	Parity, overrun, and framing errors
	Hardware flow control	The CTSn# and RTSn# pins can be used to control transmission and reception.	The CTSn# and RTSn# pins can be used to control transmission and reception.
	Start bit detection	Selectable between low level and falling edge.	Selectable between low level and falling edge.

Item		RX113 (SCIf)	RX130 (SCIh)
Synchronous mode	Break detection	When a framing error occurs, a break can be detected by reading the RXDn pin level directly.	When a framing error occurs, a break can be detected by reading the RXDn pin level directly.
	Clock source	An internal or external clock can be selected. Transfer rate clock input from the MTU can be used (SCI12).	An internal or external clock can be selected. Transfer rate clock input from the MTU can be used (SCI12).
	Double-speed mode	—	Baud rate generator double-speed mode is selectable.
	Multi-processor communication function	Serial communication among multiple processors	Serial communication among multiple processors
	Noise cancellation	The signal paths from input on the RXDn pins incorporate on-chip digital noise filters.	The signal paths from input on the RXDn pins incorporate on-chip digital noise filters.
Clock synchronous mode	Data length	8 bits	8 bits
	Receive error detection	Overrun error	Overrun error
	Hardware flow control	The CTSn# and RTSn# pins can be used to control transmission and reception.	The CTSn# and RTSn# pins can be used to control transmission and reception.
Smart card interface mode	Error processing	An error signal can be transmitted automatically when a parity error is detected during reception.	An error signal can be transmitted automatically when a parity error is detected during reception.
		Data can be retransmitted automatically when an error signal is received during transmission.	Data can be retransmitted automatically when an error signal is received during transmission.
	Data type	Both direct convention and inverse convention are supported.	Both direct convention and inverse convention are supported.
Simple I^2C mode	Communication format	I^2C bus format	I^2C bus format
	Operating mode	Master (single-master operation only)	Master (single-master operation only)
	Transfer speed	Fast mode is supported.	Fast mode is supported.
	Noise canceler	The signal paths from input on the SSCLn and SSDAn pins incorporate on-chip digital noise filters, and the noise cancellation bandwidth is adjustable.	The signal paths from input on the SSCLn and SSDAn pins incorporate on-chip digital noise filters, and the noise cancellation bandwidth is adjustable.
Simple SPI mode	Data length	8 bits	8 bits
	Error detection	Overrun error	Overrun error
	SS input pin function	Applying a high-level signal to the SSn# pin causes the output pins to enter the high-impedance state.	Applying a high-level signal to the SSn# pin causes the output pins to enter the high-impedance state.
	Clock settings	Selectable among four clock phase and clock polarity settings.	Selectable among four clock phase and clock polarity settings.
Extended serial mode	Start frame transmission	• Output of the break field low width and generation of an interrupt on detection • Detection of bus collisions and the generation of interrupts on detection	• Output of the break field low width and generation of an interrupt on detection • Detection of bus collisions and the generation of interrupts on detection

Item		RX113 (SCIf)	RX130 (SCIh)
Extended serial mode	Start frame reception	• Output of the break field low width and generation of an interrupt on detection • Comparison of data in control fields 0 and 1 and generation of an interrupt when the two match • Two kinds of data for comparison (primary and secondary) can be set in control field 1. • A priority interrupt bit can be set in control field 1. • Support for handling of start frames that do not include a break field • Support for handling of start frames that do not include control field 0 • Function for measuring bit rates	• Output of the break field low width and generation of an interrupt on detection • Comparison of data in control fields 0 and 1 and generation of an interrupt when the two match • Two kinds of data for comparison (primary and secondary) can be set in control field 1. • A priority interrupt bit can be set in control field 1. • Support for handling of start frames that do not include a break field • Support for handling of start frames that do not include control field 0 • Function for measuring bit rates
	I/O control functions	• Selectable polarity for TXDX12 and RXDX12 signals • Ability to enable digital filter function for RXDX12 • Half-duplex operation employing RXDX12 and TXDX12 signals multiplexed on the same pin • Selectable timing for the sampling of data received through RXDX12 • Signals received on RXDX12 can be passed through to SCIe when the extended serial mode control section is off.	• Selectable polarity for TXDX12 and RXDX12 signals • Ability to enable digital filter function for RXDX12 • Half-duplex operation employing RXDX12 and TXDX12 signals multiplexed on the same pin • Selectable timing for the sampling of data received through RXDX12 • Signals received on RXDX12 can be passed through to SCIg when the extended serial mode control section is off.
	Timer function	Usable as a reloading timer	Usable as a reloading timer
Bit rate modulation function		—	On-chip baud rate generator output correction can reduce errors.

Table 2.34 Comparative Listing of Serial Communication Interface Registers

Register	Bit	RX113 (SCIe, SCIf)	RX130 (SCIg, SCIh)
RDRH	—	—	Receive data register H
RDRL	—	—	Receive data register L
RDRHL	—	—	Receive data register HL
TDRH	—	—	Transmit data register H
TDRL	—	—	Transmit data register L
TDRHL	—	—	Transmit data register HL
SMR	CHR	Character length bit (Valid only in asynchronous mode.) 0: Transmit/receive in 8-bit data length 1: Transmit/receive in 7-bit data length	Character length bit (Valid only in asynchronous mode.) Selects in combination with the SCMR.CHR1 bit. CHR1 CHR 0 0: Transmit/receive in 9-bit data length 0 1: Transmit/receive in 9-bit data length 1 0: Transmit/receive in 8-bit data length (initial value) 1 1: Transmit/receive in 7-bit data length
	CM	Communications mode bit 0: Asynchronous mode 1: Clock synchronous mode or simple SPI mode	Communications mode bit 0: Asynchronous mode or simple I²C mode 1: Clock synchronous mode or simple SPI mode
SCR	CKE[1:0]	Clock enable bits SCI0, SCI2, SCI6, SCI8, and SCI9 (Asynchronous mode) b1 b0 0 0: On-chip baud rate generator The SCKn pin functions as an I/O port. 0 1: On-chip baud rate generator A clock with the same frequency as the bit rate is output on the SCKn pin. 1 x: External clock Input a clock with a frequency 16 times the bit rate on SCKn pin. When the SEMR.ABCS bit is set to 1, input a clock with a frequency eight times the bit rate. (Clock synchronous mode) b1 b0 0 x: Internal clock The SCKn pin functions as the clock output pin. 1 x: External clock The SCKn pin functions as the clock input pin.	Clock enable bits SCI0, SCI1, SCI8, and SCI9 (Asynchronous mode) b1 b0 0 0: On-chip baud rate generator The SCKn pin functions as an I/O port. 0 1: On-chip baud rate generator A clock with the same frequency as the bit rate is output on the SCKn pin. 1 x: External clock Input a clock with a frequency 16 times the bit rate on SCKn pin. When the SEMR.ABCS bit is set to 1, input a clock with a frequency eight times the bit rate. (Clock synchronous mode) b1 b0 0 x: Internal clock The SCKn pin functions as the clock output pin. 1 x: External clock The SCKn pin functions as the clock input pin.

Register	Bit	RX113 (SCIe, SCIf)	RX130 (SCIg, SCIh)
SCR	CKE[1:0]	SCI1, SCI5, and SCI12 (Asynchronous mode) b1 b0 0 0: On-chip baud rate generator The SCKn pin functions as an I/O port. 0 1: On-chip baud rate generator A clock with the same frequency as the bit rate is output on the SCKn pin. 1 x: External clock or MTU clock • A clock with a frequency 16 times the bit rate should be input on the SCKn pin. When the SEMR.ABCS bit is set to 1, input a clock with a frequency 8 times the bit rate. • The MTU clock can be used. The SCKn pin is available for use as an I/O port according to the I/O port settings when the MTU clock is used. (Clock synchronous mode) b1 b0 0 x: Internal clock The SCKn pin functions as the clock output pin. 1 x: External clock The SCKn pin functions as the clock input pin.	SCI5, SCI6, and SCI12 (Asynchronous mode) b1 b0 0 0: On-chip baud rate generator The SCKn pin functions as an I/O port. 0 1: On-chip baud rate generator A clock with the same frequency as the bit rate is output on the SCKn pin. 1 x: External clock or TMR clock • A clock with a frequency 16 times the bit rate should be input on the SCKn pin. When the SEMR.ABCS bit is set to 1, input a clock with a frequency 8 times the bit rate. • The MTU clock can be used. The SCKn pin is available for use as an I/O port according to the I/O port settings when the MTU clock is used. (Clock synchronous mode) b1 b0 0 x: Internal clock The SCKn pin functions as the clock output pin. 1 x: External clock The SCKn pin functions as the clock input pin.
SCMR	CHR1	—	Character length bit 1 (Valid only in asynchronous mode.) Selects in combination with the SMR.CHR bit. CHR1 CHR 0 0: Transmit/receive in 9-bit data length 0 1: Transmit/receive in 9-bit data length 1 0: Transmit/receive in 8-bit data length (initial value) 1 1: Transmit/receive in 7-bit data length
MDDR	—	—	Modulation duty register
SEMR	ACS0	Asynchronous ModeClock Source Select 0: External clock input 1: Logical AND of two compare matches output from TMR (valid for SCI1,SCI5, and SCI12 only)	Asynchronous ModeClock Source Select 0: External clock input 1: Logical AND of two compare matches output from TMR (valid for SCI5,SCI6, and SCI12 only)
	BRME	—	Bit rate modulation enable bit

Register	Bit	RX113 (SCIe, SCIf)	RX130 (SCIg, SCIh)
	BGDM	—	Baud rate generator double-speed mode select bit
CR2	BCCS[1:0]	Bus collision detection clock select bits b5 b4 0 0: SCI base clock frequency 0 1: SCI base clock frequency divided by 2 1 0: SCI base clock frequency divided by 4 1 1: Do not set.	Bus collision detection clock select bits • When SEMR.BGDM = 0 or SEMR.BGDM = 1 and SMR.CKS[1:0] = a value other than 00b 0 0: SCI base clock 0 1: SCI base clock frequency divided by 2 1 0: SCI base clock frequency divided by 4 1 1: Do not set. • When SEMR.BGDM = 1 and SMR.CKS[1:0] = 00b b5 b4 0 0: SCI base clock frequency divided by 2 0 1: SCI base clock frequency divided by 4 1 0: Do not set. 1 1: Do not set.

2.18 I²C Bus Interface

Table 2.35 shows a comparative overview of the I²C bus interface registers.

Table 2.35 Comparative Overview of I²C Bus Interface Registers

Register	Bit	R1630 (RIIC)	RX130 (RIICa)
ICMR2	TMWE	TMWE timeout internal counter write enable bit	—
TMOCNTL	—	Timeout internal counter	—
TMOCNTU	—	Timeout internal counter	—

2.19 Serial Peripheral Interface

Table 2.36 shows a comparative overview of the serial peripheral interface specifications, and Table 2.37 shows a comparative overview of the serial peripheral interface registers.

Table 2.36 Comparative Overview of Serial Peripheral Interface Specifications

Item	RX113 (RSPI)	RX130 (RSPIa)
Number of channels	1 channel	1 channel
RSPI transfer functions	• Use of MOSI (master out/slave in), MISO (master in/slave out), SSL (slave select), and RSPCK (RSPI clock) signals allows serial communication through SPI operation (4-wire method) or clock synchronous operation (3-wire method). • Transmit-only operation is available. • Communication mode: Full-duplex or transmit-only can be selected. • Switching of the polarity of RSPCK is supported. • Switching of the phase of RSPCK is supported.	• Use of MOSI (master out/slave in), MISO (master in/slave out), SSL (slave select), and RSPCK (RSPI clock) signals allows serial communication through SPI operation (4-wire method) or clock synchronous operation (3-wire method). • Transmit-only operation is available. • Communication mode: Full-duplex or transmit-only can be selected. • Switching of the polarity of RSPCK is supported. • Switching of the phase of RSPCK is supported.
Data format	• Selectable between MSB-first and LSB-first. • Transfer bit length is selectable among 8, 9, 10, 11, 12, 13, 14, 15, 16, 20, 24, or 32 bits. • 128-bit transmit/receive buffers • Up to four frames can be transferred in one round of transmission/reception (with each frame consisting of up to 32 bits).	• Selectable between MSB-first and LSB-first. • Transfer bit length is selectable among 8, 9, 10, 11, 12, 13, 14, 15, 16, 20, 24, or 32 bits. • 128-bit transmit/receive buffers • Up to four frames can be transferred in one round of transmission/reception (with each frame consisting of up to 32 bits).
Bit rate	• In master mode, the on-chip baud rate generator generates RSPCK by frequency-dividing PCLK (the division ratio ranges from 2 to 4096). • In slave mode, the minimum PCLK clock divided by 8 can be input as RSPCK (the maximum frequency of RSPCK is PCLK divided by 8). Width at high level: 4 cycles of PCLK; width at low level: 4 cycles of PCLK	• In master mode, the on-chip baud rate generator generates RSPCK by frequency-dividing PCLK (the division ratio ranges from 2 to 4096). • In slave mode, the minimum PCLK clock divided by 8 can be input as RSPCK (the maximum frequency of RSPCK is PCLK divided by 8). Width at high level: 4 cycles of PCLK; width at low level: 4 cycles of PCLK
Buffer configuration	• The transmit and receive buffers have a double buffer configuration. • The transmit and receive buffers are each 128 bits in size.	• The transmit and receive buffers have a double buffer configuration. • The transmit and receive buffers are each 128 bits in size.
Error detection	• Mode fault error detection • Overrun error detection • Parity error detection	• Mode fault error detection • Overrun error detection • Parity error detection

Item	RX113 (RSPI)	RX130 (RSPIa)
SSL control function	• Four SSL pins (SSLA0 to SSLA3) for each channel • In single-master mode, SSLA0 to SSLA3 pins are output. • In multi-master mode: SSLA0 pin is input, and SSLA1 to SSLA3 pins are either output or unused. • In slave mode: SSLA0 pin is input, and SSLA1 to SSLA3 pins are unused. • Controllable delay from SSL output assertion to RSPCK operation (RSPCK delay) Setting range: 1 to 8 RSPCK cycles (set in RSPCK-cycle units) • Controllable delay from RSPCK stop to SSL output negation (SSL negation delay) Setting range: 1 to 8 RSPCK cycles (set in RSPCK-cycle units) • Controllable wait for next-access SSL output assertion (next-access delay) Setting range: 1 to 8 RSPCK cycles (set in RSPCK-cycle units) • SSL polarity-change function	• Four SSL pins (SSLA0 to SSLA3) for each channel • In single-master mode, SSLA0 to SSLA3 pins are output. • In multi-master mode: SSLA0 pin is input, and SSLA1 to SSLA3 pins are either output or unused. • In slave mode: SSLA0 pin is input, and SSLA1 to SSLA3 pins are unused. • Controllable delay from SSL output assertion to RSPCK operation (RSPCK delay) Setting range: 1 to 8 RSPCK cycles (set in RSPCK-cycle units) • Controllable delay from RSPCK stop to SSL output negation (SSL negation delay) Setting range: 1 to 8 RSPCK cycles (set in RSPCK-cycle units) • Controllable wait for next-access SSL output assertion (next-access delay) Setting range: 1 to 8 RSPCK cycles (set in RSPCK-cycle units) • SSL polarity-change function
Control in master transfer	• Transfers of up to eight commands can be performed sequentially in looped execution. • For each command, the following can be set: SSL signal value, bit rate, RSPCK polarity/phase, transfer data length, LSB/MSB-first, burst, RSPCK delay, SSL negation delay, and next-access delay • A transfer can be initiated by writing to the transmit buffer. • The MOSI signal value when SSL is negated can be specified.	• Transfers of up to eight commands can be performed sequentially in looped execution. • For each command, the following can be set: SSL signal value, bit rate, RSPCK polarity/phase, transfer data length, LSB/MSB-first, burst, RSPCK delay, SSL negation delay, and next-access delay • A transfer can be initiated by writing to the transmit buffer. • The MOSI signal value when SSL is negated can be specified. • RSPCK auto-stop function
Interrupt sources	Interrupt sources: • Receive buffer full interrupt • transmit buffer empty interrupt • RSPI error interrupt (mode fault, overrun, parity error) • RSPI idle interrupt (RSPI idle)	Interrupt sources: • Receive buffer full interrupt • transmit buffer empty interrupt • RSPI error interrupt (mode fault, overrun, parity error) • RSPI idle interrupt (RSPI idle)
Other functions	• Function for switching between CMOS output and open-drain output • Function for initializing the RSPI • Loopback mode function	• Function for switching between CMOS output and open-drain output • Function for initializing the RSPI • Loopback mode function
Low power consumption function	It is possible to specify the module stop state.	It is possible to specify the module stop state.

Table 2.37 Comparative Listing of Serial Peripheral Interface Registers

Register	Bit	RX113 (RSPI)	RX130 (RSPIa)
SPCR2	SCKASE	—	RSPCK auto-stop function enable bit

2.20 Capacitive Touch Sensing Unit

Table 2.38 shows a comparative overview of the capacitive touch sensing unit specifications, and Table 2.39 shows a comparative listing of the capacitive touch sensing unit registers.

Table 2.38 Comparative Overview of Capacitive Touch Sensing Unit Specifications

Item		RX113 (CTSU)	RX130 (CTSUa)
Operating clock		PCLK, PCLK/2, or PCLK/4	PCLK, PCLK/2, or PCLK/4
Pins	RX113: TS0 to TS11 RX130: TS0 to TS35	Electrostatic capacitance measurement pins (12 channels)	Electrostatic capacitance measurement pins (36 channels)
	TSCAP	Low-pass filter (LPF) connection pin	Low-pass filter (LPF) connection pin
Measurement modes	Self-capacitance single scan mode	Electrostatic capacitance on a channel is measured by the self-capacitance method.	Electrostatic capacitance on a channel is measured by the self-capacitance method.
	Self-capacitance multi-scan mode	Electrostatic capacitance on multiple channels is measured successively by the self-capacitance method.	Electrostatic capacitance on multiple channels is measured successively by the self-capacitance method.
	Mutual capacitance full scan mode	Electrostatic capacitance on multiple channels is measured successively by the mutual capacitance method.	Electrostatic capacitance on multiple channels is measured successively by the mutual capacitance method.
Noise prevention		Synchronous noise prevention, high-range noise prevention	Synchronous noise prevention, high-range noise prevention
Measurement start conditions		• Software trigger • External trigger (event input by the event link controller (ELC))	• Software trigger • External trigger (event input by the event link controller (ELC))

Table 2.39 Comparative Listing of Capacitive Touch Sensing Unit Registers

Register	Bit	RX113 (CTSU)	RX130 (CTSUa)
CTSUCR0	CTSUIOC	—	CTSU transmit pin control bit
	CTSUTXVSEL	—	CTSU transmission power supply select bit
CTSUMCH0	RX113: CTSUMCH0 [3:0] RX130: CTSUMCH0 [5:0]	CTSU measurement channel 0 bits • Self-capacitance single scan mode b3 b0 0 0 0 0: TS0 0 0 0 1: TS1 0 0 1 0: TS2 0 0 1 1: TS3 0 1 0 0: TS4 0 1 0 1: TS5 0 1 1 0: TS6 0 1 1 1: TS7 1 0 0 0: TS8 1 0 0 1: TS9 1 0 1 0: TS10 1 0 1 1: TS11 Other than above: Starting measurement operation (CTSUCR0.CTSUSTRT bit = 1) is prohibited after these bits are set. • Modes other than self-capacitance single scan b3 b0 0 0 0 0: TS0 0 0 0 1: TS1 0 0 1 0: TS2 0 0 1 1: TS3 0 1 0 0: TS4 0 1 0 1: TS5 0 1 1 0: TS6 0 1 1 1: TS7 1 0 0 0: TS8 1 0 0 1: TS9 1 0 1 0: TS10 1 0 1 1: TS11 1 1 1 1: Measurement is stopped.	CTSU measurement channel 0 bits • Self-capacitance single scan mode b5 b0 0 0 0 0 0 0: TS0 : : 1 0 0 0 1 1: TS35 Other than above: Starting measurement operation (CTSUCR0.CTSUSTRT bit = 1) is prohibited after these bits are set. • Modes other than self-capacitance single scan b5 b0 0 0 0 0 0 0: TS0 : : 1 0 0 0 1 1: TS35 1 1 1 1 1 1: Measurement is stopped.

Register	Bit	RX113 (CTSU)	RX130 (CTSUa)
CTSUMCH1	RX113: CTSUMCH1 [3:0] RX130: CTSUMCH1 [5:0]	CTSU measurement channel 1 bits b3 b0 0 0 0 0: TS0 0 0 0 1: TS1 0 0 1 0: TS2 0 0 1 1: TS3 0 1 0 0: TS4 0 1 0 1: TS5 0 1 1 0: TS6 0 1 1 1: TS7 1 0 0 0: TS8 1 0 0 1: TS9 1 0 1 0: TS10 1 0 1 1: TS11 1 1 1 1: Measurement is stopped.	CTSU measurement channel 1 bits b5 b0 0 0 0 0 0 0: TS0 : : 1 0 0 0 1 1: TS35 1 1 1 1 1 1: Measurement is stopped.
CTSUCHAC1	CTSUCHAC14	—	CTSU channel enable control 14 bit
	CTSUCHAC15	—	CTSU channel enable control 15 bit
	CTSUCHAC16	—	CTSU channel enable control 16 bit
	CTSUCHAC17	—	CTSU channel enable control 17 bit
CTSUCHAC2	—	—	CTSU channel enable control register 2
CTSUCHAC3	—	—	CTSU channel enable control register 3
CTSUCHAC4	—	—	CTSU channel enable control register 4
CTSUCHTRC1	CTSUCHTRC14	—	CTSU channel transmit/receive control 14 bit
	CTSUCHTRC15	—	CTSU channel transmit/receive control 15 bit
	CTSUCHTRC16	—	CTSU channel transmit/receive control 16 bit
	CTSUCHTRC17	—	CTSU channel transmit/receive control 17 bit
CTSUCHTRC2	—	—	CTSU channel transmit/receive control register 2
CTSUCHTRC3	—	—	CTSU channel transmit/receive control register 3
CTSUCHTRC4	—	—	CTSU channel transmit/receive control register 4
CTSUERRS	CTSUSPMD [1:0]	—	Calibration mode bits
	CTSUTSOD	—	TS pin fixed output bit
	CTSUDRV	—	Calibration setting bit 3
	CTSUTSOC	—	Calibration setting bit 7
CTSUTRMR	—	—	CTSU reference current calibration register

2.21 12-Bit A/D Converter

Table 2.40 shows a comparative overview of the 12-bit A/D converter specifications, and Table 2.41 shows a comparative listing of the 12-bit A/D converter registers.

Table 2.40 Comparative Overview of 12-Bit A/D Converter

Item	RX113 (S12ADb)	RX130 (S12ADE)
Number of units	1 unit	1 unit
Input channels	17 channels	24 channels
Extended analog function	Temperature sensor output, internal reference voltage	Temperature sensor output, internal reference voltage
A/D conversion method	Successive approximation method	Successive approximation method
Resolution	12 bits	12 bits
Conversion time	1.0 µs per channel (when operating with A/D conversion clock ADCLK = 32 MHz)	1.4 µs per channel (when operating with A/D conversion clock ADCLK = 32 MHz)
A/D conversion clock	Peripheral module clock PCLK and A/D conversion clock ADCLK can be set so that the division ratio is one of the following: PCLK: ADCLK division ratio = 1:1, 1:2, 1:4, 1:8, 2:1, 4:1 ADCLK is set using the clock generation circuit.	Peripheral module clock PCLK*1 and A/D conversion clock ADCLK*1 can be set so that the frequency ratio is one of the following: PCLK: ADCLK frequency ratio = 1:1, 1:2, 2:1, 4:1, 8:1 ADCLK is set using the clock generation circuit.
Data register	• For analog input: 17 data registers • One data register for each unit for A/D conversion data multiplexing in double trigger mode • For temperature sensor: One data register • For internal reference voltage: One data register • The results of A/D conversion are stored in 12-bit A/D data registers. • In addition mode, A/D conversion results are added and stored in A/D data registers as 14-bit data. • Duplication of A/D conversion data — A/D conversion data of one selected analog input channel is stored in A/D data register y when conversion is started by the first trigger and in the duplication register when started by the second trigger. — In single scan mode or group scan mode, duplication is available only when double trigger mode is enabled.	• For analog input: 24 data registers • One data register for each unit for A/D conversion data multiplexing in double trigger mode • For temperature sensor: One data register • For internal reference voltage: One data register • 1 register per unit for self-diagnostics • The results of A/D conversion are stored in 12-bit A/D data registers. • Output of A/D conversion results at 12-bit precision • The value obtained by adding up A/D-converted results is stored as a value (number of conversion accuracy bits + 2 bits/4 bits) in the A/D data registers in A/D-converted value addition mode. • Double trigger mode (selectable in single scan and group scan modes) • The first piece of A/D-converted analog-input data on one selected channel is stored in the data register for the channel, and the second piece is stored in the duplication register

Item	RX113 (S12ADb)	RX130 (S12ADE)
Operating mode	• Single scan mode: — A/D conversion is performed only once on the analog inputs of up To 17 user-selected channels. — A/D conversion is performed only once on the temperature sensor output. — A/D conversion is performed only once on the internal reference voltage. • Continuous scan mode: — A/D conversion is performed repeatedly on the analog inputs of up to 17 user-selected channels. • Group scan mode: — Up to 17 channels of analog input are divided between group A and group B, and A/D conversion is performed only once on all the channels in the selected group. — The scanning start conditions can be selected independently for group A and group B allowing conversion to start at a different time for each group.	• Single scan mode: — A/D conversion is performed only once on the analog inputs of up to 24 user-selected channels. — A/D conversion is performed only once on the temperature sensor output. — A/D conversion is performed only once on the internal reference voltage. • Continuous scan mode: — A/D conversion is performed repeatedly on the analog inputs of up to 24 user-selected channels. • Group scan mode: — Up to 24 user-selected channels of analog input are divided between group A and group B, and A/D conversion is performed only once on all the channels in the selected group. — The scanning start conditions (synchronous triggers) can be selected independently for group A and group B allowing conversion to start at a different time for each group. • Group scan mode (with group A priority control selected): — If a group A trigger is input when A/D conversion on group B is in progress, scanning of group B is stopped and scanning of group A starts. — Restart of A/D conversion on group B (rescan) after completion of A/D conversion on group A can be enabled.
A/D conversion start conditions	• Software trigger • Synchronous trigger Trigger by MTU or ELC • Asynchronous trigger A/D conversion can be triggered by the ADTRG0# pin.	• Software trigger • Synchronous trigger Conversion start is triggered by the multi-function timer pulse unit (MTU) and event link controller (ELC). • Asynchronous trigger A/D conversion can be started by the external trigger ADTRG0# pin.

Item	RX113 (S12ADb)	RX130 (S12ADE)
Functions	• Variable sampling state count • A/D-converted value adding mode • Double trigger mode (duplication of A/D conversion data)	• Variable sampling state count • Self-diagnostic function for 12-bit A/D converter • Selectable A/D-converted value adding mode or averaging mode • Analog input disconnection detection function (discharge function/ precharge function) • Double trigger mode (duplication of A/D conversion data) • A/D data register auto-clear function • Compare function (window A, window B) • Ring buffers (16) for compare function
Interrupt sources	• In modes other than double trigger mode and group scan mode, an A/D scan end interrupt request (S12ADI0) can be generated on completion of a single scan. • In double trigger mode, an A/D scan end interrupt request (S12ADI0) can be generated on completion of a double scan. • In group scan mode, a scan end interrupt request (S12ADI0) can be generated on completion of a group A scan. On completion of a group B scan a dedicated group B scan end interrupt request (GBADI) can be generated. • When double trigger mode is enabled in group scan mode, a scan end interrupt request (S12ADI0) can be generated on completion of two scans of group A. On completion of a group B scan a dedicated scan end interrupt request (GBADI) can be generated. • The or data transfer controller (DTC) can be activated by the S12ADI0 or GBADI interrupt.	• In modes other than double trigger mode and group scan mode, an A/D scan end interrupt request (S12ADI0) can be generated on completion of a single scan. • In double trigger mode, an A/D scan end interrupt request (S12ADI0) can be generated on completion of a double scan. • In group scan mode, a scan end interrupt request (S12ADI0) can be generated on completion of a group A scan. On completion of a group B scan a dedicated group B scan end interrupt request (GBADI) can be generated. • When double trigger mode is enabled in group scan mode, a scan end interrupt request (S12ADI0) can be generated on completion of two scans of group A. On completion of a group B scan a dedicated scan end interrupt request (GBADI) can be generated. • The data transfer controller (DTC) can be activated by the S12ADI0 or GBADI interrupt.

Item	RX113 (S12ADb)	RX130 (S12ADE)
Event link function	• In group scan mode an ELC event can be generated on completion of scans other than group B scan. • Scanning can be started by a trigger from the ELC.	• In group scan mode an ELC event can be generated on completion of scans other than group B scan. • An ELC event can be generated on completion of group B scan in group scan mode. • An ELC event can be generated at end of all scans. • Scanning can be started by a trigger from the ELC. • An ELC event can be generated according to the window compare function event conditions in single scan mode.
Reference voltage	• VREFH0, AVCC0, or the internal reference voltage can be selected as the high-side reference voltage. • VREFL0 or AVSS0 can be selected as the low-side reference voltage.	• VREFH0 or AVCC0 can be selected as the high-side reference voltage. • VREFL0 or AVSS0 can be selected as the low-side reference voltage.
Low power consumption function	It is possible to specify the module stop state.	It is possible to specify the module stop state.

Table 2.41 Comparative Listing of 12-Bit A/D Converter Registers

Register	Bit	RX113	RX130
ADDRy	AD[11:0]*1	12-bit A/D-converted value	A/D-converted value
	AD[13:0]*1	14-bit A/D-converted value addition result	Same-channel A/D-converted value addition result
ADDBLDR	AD[11:0]*1	12-bit A/D-converted value	A/D-converted value
	AD[13:0]*1	14-bit A/D-converted value addition result	Same-channel A/D-converted value addition result
ADTSDR	AD[11:0]*1	12-bit A/D-converted value	A/D-converted value
	AD[13:0]*1	14-bit A/D-converted value addition result	Same-channel A/D-converted value addition result
ADOCDR	AD[11:0]*1	12-bit A/D-converted value	A/D-converted value
	AD[13:0]*1	14-bit A/D-converted value addition result	Same-channel A/D-converted value addition result
ADRD	—	—	A/D self-diagnostic data register
ADCSR	DBLANS [4:0]	A/D conversion data duplication channel select bits	Double trigger channel select bits
	ADHSC	A/D conversion mode select bit 0: Normal conversion 1: High-speed conversion	A/D conversion select bit 0: High-speed conversion 1: Low-current conversion
ADANSA	—	A/D channel select register A	—
ADANSA0	—	—	A/D channel select register A0
ADANSA1	ANSA1[5]	A/D conversion channel 21 select bit	—
	ANSA100 to ANSA115	—	A/D conversion channel select bits
ADANSB	—	A/D channel select register B	—
ADANSB0	—	—	A/D channel select register B0
ADANSB1	ANSB1[5]	A/D conversion channel 21 select bit	—
	ANSB100 to ANSB115	—	A/D conversion channel select bits
ADADS	—	A/D-converted value addition mode select register	—
ADADS0	—	—	A/D-converted value addition/ average channel select register 0
ADADS1	ADS1[5]	A/D conversion channel 21 select bit	—
	ADS100 to ADS115	—	A/D-converted value addition/ average channel select bits
ADADC	RX113: ADC[1:0] RX130: ADC[2:0]	Addition count select bits	Addition count select bits
	AVE	—	Average mode enable bit

Register	Bit	RX113	RX130
ADCER	ACE	Automatic clearing enable bit	A/D data register automatic clearing enable bit
	DIAGVAL [1:0]	—	Self-diagnostic conversion voltage select bits
	DIAGLD	—	Self-diagnostic mode select bit
	DIAGM	—	Self-diagnostic enable bit
ADSTRGR	RX113: TRSB[3:0] RX130: TRSB[5:0]	A/D conversion start trigger for group B select bits	A/D conversion start trigger for group B select bits
	RX113: TRSA[3:0] RX130: TRSA[5:0]	A/D conversion start trigger select bits	A/D conversion start trigger select bits
ADEXICR	TSSAD	Temperature sensor output A/D-converted value addition select bit 0: Temperature sensor output A/D-converted value addition is not selected. 1: Temperature sensor output A/D-converted value addition is selected.	Temperature sensor output A/D-converted value addition/average mode select bit 0: Temperature sensor output A/D-converted value addition/ average mode is not selected. 1: Temperature sensor output A/D-converted value addition/ average mode is selected.
	OCSAD	Internal reference voltage A/D-converted value addition select bit 0: Internal reference voltage A/D-converted value addition is not selected. 1: Internal reference voltage A/D-converted value addition is selected.	Internal reference voltage A/D-converted value addition/average mode select bit 0: Internal reference voltage A/D-converted value addition/ average mode is not selected. 1: Internal reference voltage A/D-converted value addition/ average mode is selected.
	TSS	Temperature sensor output A/D conversion select bit	—
	OCS	Internal reference voltage A/D-conversion select bit	—
	TSSA	—	Temperature sensor output A/D conversion select bit
	OCSA	—	Internal reference voltage A/D-conversion select bit
ADSSTRn	SST[7:0]	Sampling time setting bits	—
ADDISCR	—	—	A/D disconnection detection controller
ADELCCR	—	—	A/D event link control register
ADGSPCR	—	—	A/D group scan priority control register
ADCMPCR	—	—	A/D comparison function control register
ADCMPANSR0	—	—	A/D comparison function window A channel select register 0
ADCMPANSR1	—	—	A/D comparison function window A channel select register 1

Register	Bit	RX113	RX130
ADCMPANSER	—	—	A/D comparison function window A extended input select register
ADCMPLR0	—	—	A/D comparison function window A compare condition setting register 0
ADCMPLR1	—	—	A/D comparison function window A compare condition setting register 1
ADCMPLER	—	—	A/D comparison function window A extended input compare condition setting register
ADCMPDR0	—	—	A/D comparison function window A lower level setting register
ADCMPDR1	—	—	A/D comparison function window A upper level setting register
ADCMPSR0	—	—	A/D comparison function window A channel status register 0
ADCMPSR1	—	—	A/D comparison function window A channel status register 1
ADCMPSER	—	—	A/D comparison function window A extended input channel status register
ADHVREFCNT	HVREFDIS	High-side reference voltage discharge bit	—
	CSVSEL	High-potential reference voltage select bits	—
	HVSEL[1:0]	—	High-potential reference voltage select bits
	LVSEL	—	Low-potential reference voltage select bit
	ADSLP	—	Sleep bit
ADWINMON	—	—	A/D comparison function window A/B status monitor register
ADCMPBNSR	—	—	A/D comparison function window B channel select register
ADWINLLB	—	—	A/D comparison function window B lower level setting register
ADWINULB	—	—	A/D comparison function window B upper level setting register
ADCMPBSR	—	—	A/D comparison function window B channel status register
ADBUFn	—	—	A/D data storage buffer register n
ADBUFEN	—	—	A/D data storage buffer enable register
ADBUFPTR	—	—	A/D data storage buffer pointer register

Note 1. The number of usable bits differs according to the setting conditions.

2.22 D/A Converter

Table 2.42 shows a comparative overview of the D/A converter specifications, and Table 2.43 shows a comparative listing of the D/A converter registers.

Table 2.42 Comparative Overview of D/A Converter Specifications

Item	RX113 (12- Bit D/A Converter (R12DAA))	RX130 (D/A Converter (DAa))
Resolution	12 bits	8 bits
Output channel	2 channels	2 channels
Measure against mutual interference between analog modules	Measure against interference between D/A and A/D conversion: D/A converted data update timing is controlled by the 12-bit A/D converter synchronous D/A conversion enable input signal output by the 12-bit A/D converter. Degradation of 12-bit A/D conversion accuracy caused by interference is reduced by controlling the D/A converter inrush current generation timing with the enable signal.	Measure against interference between D/A and A/D conversion: D/A converted data update timing is controlled by the 12-bit A/D converter synchronous D/A conversion enable input signal output by the 12-bit A/D converter. Degradation of 8-bit A/D conversion accuracy caused by interference is reduced by controlling the D/A converter inrush current generation timing with the enable signal.
Low power consumption function	It is possible to transition to the module stop state.	It is possible to transition to the module stop state.
Event link function (input)	Ability to activate DA0 by event signal input	Ability to activate DA0 by event signal input

Table 2.43 Comparative Listing of D/A Converter Registers

Register	Bit	RX113 (12- Bit D/A Converter (R12DAA))	RX130 (D/A Converter (DAa))
DADRm) (m = 0, 1)	—	D/A Data Register m ● DADPR.DPSEL bit = 0 (data is flush with the right end of the register) Data placement : b11 to b0 ● DADPR.DPSEL bit = 1 (data is flush with the left end of the register) Data placement : b15 to b4	D/A Data Register m ● DADPR.DPSEL bit = 0 (data is flush with the right end of the register) Data placement : b7 to b0 ● DADPR.DPSEL bit = 1 (data is flush with the left end of the register) Data placement : b15 to b8
DAADSCR	DAADST	D/A A/D synchronous conversion bit 0: 12-bit D/A converter operation is not synchronized with 12-bit A/D converter operation. (Measures against interference between D/A and A/D conversion are disabled.) 1: 12-bit D/A converter operation is synchronized with 12-bit A/D converter operation. (Measures against interference between D/A and A/D conversion are enabled.)	D/A A/D synchronous conversion bit 0: 8-bit D/A converter operation is not synchronized with 12-bit A/D converter operation. (Measures against interference between D/A and A/D conversion are disabled.) 1: 8-bit D/A converter operation is synchronized with 12-bit A/D converter operation. (Measures against interference between D/A and A/D conversion are enabled.)
DAVREFCR	—	D/A VREF control register	—

2.23 RAM

Table 2.44 shows a comparative overview of the RAM specifications.

Table 2.44 Comparative Overview of RAM

Item	RX113	RX130
RAM capacity	Maximum 64 KB	Maximum 48 KB
RAM address	0000 0000h to 0000 7FFFh (32 KB) 0000 0000h to 0000 FFFFh (64 KB)	0000 0000h to 0000 27FFh (10 KB) 0000 0000h to 0000 3FFFh (16 KB) 0000 0000h to 0000 7FFFh (32 KB) 0000 0000h to 0000 BFFFh (48 KB)
Access	• Single-cycle access is possible for both reading and writing. • The RAM can be enabled or disabled.	• Single-cycle access is possible for both reading and writing. • The RAM can be enabled or disabled.
Low power consumption function	It is possible to specify the module stop state.	It is possible to specify the module stop state.

2.24 Flash Memory (ROM)

Table 2.45 shows a comparative overview of the flash memory specifications.

Table 2.45 Comparative Overview of Flash Memory Specifications

Item	RX113	RX130
Memory space	• User area: Maximum 512 KB • Data area: 8 KB • Extra area: Stores the start-up area information, access window information, and unique ID.	• User area: Maximum 512 KB • Data area: 8 KB • Extra area: Stores the start-up area information, access window information, and unique ID.
Software commands	• The following commands are implemented: Program, blank check, block erase, unique ID read • The following commands are implemented for programming the extra area: Program start-up area information, program access window information	• The following commands are implemented: Program, blank check, block erase, unique ID read • The following commands are implemented for programming the extra area: Program start-up area information, program access window information
Value after erase	• ROM: FFh • E2 DataFlash: FFh	• ROM: FFh • E2 DataFlash: FFh
Interrupt	An interrupt (FRDYI) is generated upon completion of software command processing or forced stop processing.	An interrupt (FRDYI) is generated upon completion of software command processing or forced stop processing.
On-board programming	Boot mode (SCI interface) • Channel 1 of the serial communications interface (SCI1) is used for asynchronous serial communication. • The user area and data area are rewritable. Boot mode (FINE interface) • The FINE is used. • The user area and data area are rewritable. Boot mode (USB interface) • Channel 0 of the USB 2.0 Function (USB0) module is used. • The user area and data area are rewritable. • The flash memory can be rewritten in self-powered or bus-powered mode. • A personal computer can be connected using only a USB cable. Self-programming (single-chip mode) • The user area and data area are rewritable using a flash rewrite routine in a user program.	Boot mode (SCI interface) • Channel 1 of the serial communications interface (SCI1) is used for asynchronous serial communication. • The user area and data area are rewritable. Boot mode (FINE interface) • The FINE is used. • The user area and data area are rewritable. Self-programming (single-chip mode) • The user area and data area are rewritable using a flash rewrite routine in a user program.
Off-board programming	The user area and data area are rewritable using a flash programmer compatible with the MCU.	The user area and data area are rewritable using a flash programmer compatible with the MCU.

Item	RX113	RX130
ID code protect	• Connection with the serial programmer can be enabled or disabled using ID codes in boot mode. • Connection with an on-chip debugging emulator can be enabled or disabled using ID codes.	• Connection with the serial programmer can be enabled or disabled using ID codes in boot mode. • Connection with an on-chip debugging emulator can be enabled or disabled using ID codes.
Start-up program protection function	This function is used to safely rewrite blocks 0 to 15.	This function is used to safely rewrite blocks 0 to 15.
Area protection	This function enables rewriting of only the specified range in the user area and disables rewriting of the other blocks during self-programming.	This function enables rewriting of only the specified range in the user area and disables rewriting of the other blocks during self-programming.
Background operation (BGO) function	Programs in the ROM can be executed while rewriting the E2 DataFlash.	Programs in the ROM can be executed while rewriting the E2 DataFlash.

2.25 Package (LFQFP64/100 only)

There are some differences in the outline drawing of the LFQFP64, LFQFP100 package, so please be careful when designing the board.

For details, refer to Design Guide for Migration between RX Family: Differences in Package External form (R01AN4591EJ).

Table 2.46 Comparison of package codes

Item	RX113	RX130
64 pin LFQFP	PLQP0064KB-A	PLQP0064KB-C
100 pin LFQFP	PLQP0100KB-A	PLQP0100KB-B

3. Comparison of Pin Functions

Table 3.1 and Table 3.2 list only the points of differences for the pins of the RX113 Group and RX130 Groups (100-pin LFQFP and 64-pin LFQFP, respectively). Items implemented only on one group are shown in blue. Items implemented on both groups with no points of difference are shown in black.

For details, see User's Manual: Hardware, listed in 5, Reference Documents.

Table 3.1 Points of Difference for Pins (100-Pin LFQFP Package)

LFQFP 100-Pin No.	RX113	RX130
1	P04/MTIOC0A/POE2#/TMCI3/SCK6/TS1	P06
2	PJ0/DA0	P03/DA0
3	P02/MTIOC0D/POE3#/TMRI3/RXD6/SMISO6/SSCL6/TS2	P04
4	PJ3/MTIOC3C/CTS6#/RTS6#/SS6#/TS3	PJ3/MTIOC3C/CTS6#/RTS6#/SS6#
5	P25/MTIOC4C/MTCLKB/TS4/ADTRG0#	VCL
6	P24/MTIOC4A/MTCLKA/TMRI1/TS5	PJ1/MTIOC3A
7	P23/MTIOC3D/MTCLKD/CTS0#/RTS0#/SS0#/TS6	MD/FINED
8	P22/MTIOC3B/MTCLKC/TMO0/SCK0/TS7	XCIN
9	P21/MTIOC1B/TMCI0/RXD0/SMISO0/SSCL0/TS8	XCOUT
10	P20/MTIOC1A/TMRI0/TXD0/SMOSI0/SSDA0/TS9	RES#
11	P27/MTIOC2B/TMCI3/SCK12/SCK1/RXD6/SMISO6/SSCL6/TS10/IRQ3/ADTRG0#/CACREF/CMPA2	XTAL/P37
12	P26/MTIOC2A/TMO1/TXD1/SMOSI1/SSDA1/USB0_VBUSEN/TXD6/SMOSI6/SSDA6/TSCAP	VSS
13	P30/MTIOC4B/POE8#/TMRI3 RXD1/SMISO1/SSCL1/CAPH/IRQ0	EXTAL/P36
14	P31/MTIOC4D/TMCI2/CTS1#/RTS1#/SS1#/CAPL/IRQ1	VCC
15	MD/FINED	P35/NMI
16	RES#	P34/MTIOC0A/TMCI3/POE2#/SCK6/IRQ4
17	XCOUT	P33/MTIOC0D/TMRI3/POE3#/RXD6/SMISO6/SSCL6/IRQ3
18	XCIN/PH7	P32/MTIOC0C/TMO3/TXD6/SMOSI6/SSDA6/TS0/IRQ2/RTCOUT
19	UPSEL/P35/NMI	P31/MTIOC4D/TMCI2/CTS1#/RTS1#/SS1#/TS1/IRQ1
20	XTAL	P30/MTIOC4B/POE8#/TMRI3/RXD1/SMISO1/SSCL1/TS2/IRQ0
21	EXTAL	P27/MTIOC2B/TMCI3/SCK1/TS3
22	VCL	P26/MTIOC2A/TMO1/TXD1/SMOSI1/SSDA1/TS4
23	VSS	P25/MTIOC4C/MTCLKB/ADTRG0#
24	VCC	P24/MTIOC4A/MTCLKA/TMRI1
25	P32/MTIOC0C/RTCOUT/TMO3/TXD6/SMOSI6/SSDA6/CTS6#/RTS6#/SS6#/TS11/IRQ2	P23/MTIOC3D/MTCLKD/CTS0#/RTS0#/SS0#

LFQFP 100-Pin No.	RX113	RX130
26	P17/MTIOC0C/MTIOC3A/MTIOC3B/ POE8#/TMO1/SCK1/MISOA/SDA0/RXD12/ RXDX12/SMISO12/SSCL12/IRQ7	P22/MTIOC3B/MTCLKC/TMO0/SCK0
27	P16/MTIOC3C/MTIOC3D/RTCOUT/TMO2/ TXD1/SMOSI1/SSDA1/MOSIA/SCL0/USB0 _VBUS/USB0_VBUSEN/USB0_OVRCURB/ IRQ6/ADTRG0#	P21/MTIOC1B/TMCI0/RXD0/SMISO0/SSC L0
28	P15/MTIOC0B/MTCLKB/TMCI2/RXD1/SMI SO1/SSCL1/RSPCKA/IRQ5/CLKOUT/CAC REF	P20/MTIOC1A/TMRI0/TXD0/SMOSI0/SSD A0
29	UB#/P14/MTIOC0A/MTIOC3A/MTCLKA/TM RI2/CTS1#/RTS1#/SS1#/SSLA0/TXD12/TX DX12/SIOX12/SMOSI12/SSDA12/USB0_O VRCURA/IRQ4	(5 V tolerant)/P17/MTIOC3A/MTIOC3B/ TMO1/POE8#/SCK1/MISOA/SDA/IRQ7
30	VCC_USB	(5 V tolerant)/P16/MTIOC3C/MTIOC3D/ TMO2/TXD1/SMOSI1/SSDA1/MOSIA/SCL/I RQ6/RTCOUT/ADTRG0#
31	USB0_DM	P15 MTIOC0B/MTCLKB/TMCI2/RXD1/ SMISO1/SSCL1/TS5/IRQ5
32	USB0_DP	P14 MTIOC3A/MTCLKA/TMRI2/CTS1#/ RTS1#/SS1#/TS6/IRQ4
33	VSS_USB	(5 V tolerant)/P13/MTIOC0B/TMO3/SDA/ IRQ3
34	P13/MTIOC0B/TMO3/CTS12#/RTS12#/SS1 2#/CTS0#/RTS0#/SS0#/SEG00/IRQ3	(5 V tolerant)/P12/TMCI1/SCL/IRQ2
35	P12/TMCI1/SCK12/SCK0/SEG01/IRQ2	PH3/TMCI0/TS7
36	P11/MTIC5U/POE0#/RXD12/RXDX12/SMI SO12/SSCL12/RXD0/SMISO0/SSCL0/SEG 02/IRQ7	PH2/TMRI0/TS8/IRQ1
37	P10/MTIC5V/POE1#/TXD12/TXDX12/SIOX 12/SMOSI12/SSDA12/TXD0/SMOSI0/SSD A0/SEG03/IRQ6	PH1/TMO0/TS9/IRQ0
38	P56/MTIOC1A/MTIC5W/POE2#/TXD1/SMO SI1/SSDA1/SEG04/IRQ5	PH0/TS10/CACREF
39	P53/MTIOC2B SSLA0/CTS2#/RTS2#/SS2#/SEG05	P55/MTIOC4D/TMO3/TS11
40	P52/MISOA/RXD2/SMISO2/SSCL2/SEG06	P54/MTIOC4B/TMCI1/TS12
41	P51/MTIOC4C/RSPCKA/SCK2/SEG07	P53
42	P50/MTIOC2A/MOSIA/TXD2/SMOSI2/SSD A2/SEG08	P52/PMC1
43	P55/MTIOC4D/TMO3/VL1	P51/PMC0
44	P54/MTIOC4B/TMCI1/VL2	P50
45	PC7/MTIOC3A/MTCLKB/TMO2/TXD1/SMO SI1/SSDA1/MISOA/TXD8/SMOSI8/SSDA8/ USB0_OVRCURB/VL3/CACREF	PC7/MTIOC3A/MTCLKB/TMO2/MISOA/TX D8/SMOSI8/SSDA8/TS13/CACREF
46	PC6/MTIOC3C/MTCLKA/TMCI2/RXD1/SMI SO1/SSCL1/MOSIA/RXD8/SMISO8/SSCL8 /USB0_EXICEN/VL4	PC6/MTIOC3C/MTCLKA/TMCI2/MOSIA/RX D8/SMISO8/SSCL8/TS14
47	PC5/MTIOC3B/MTCLKD/TMRI2/SCK1/RSP CKA/SCK8/USB0_ID/COM0	PC5/MTIOC3B/MTCLKD/TMRI2/RSPCKA/ SCK8/TS15

LFQFP 100-Pin No.	RX113	RX130
48	PC4/MTIOC3D/MTCLKC/POE0#/TMCI1/SSLA0/CTS8#/RTS8#/SS8#/SCK5/USB0_VBUSEN/USB0_VBUS/COM1/IRQ2/CLKOUT	PC4/MTIOC3D/MTCLKC/POE0#/TMCI1/SSLA0/CTS8#/RTS8#/SS8#/SCK5/TSCAP
49	PC3/MTIOC4D/TXD5/SMOSI5/SSDA5/IRTXD5/COM2	PC3/MTIOC4D/TXD5/SMOSI5/SSDA5/TS16
50	PC2/MTIOC4B/RXD5/SMOSI5/SSCL5/IRRXD5/SSLA3/COM3	PC2/MTIOC4B/RXD5/SMISO5/SSCL5/SSLA3/TS17
51	PC1/MTIOC3A/SCK5/SSLA2/SEG09	PC1/MTIOC3A/SCK5/SSLA2
52	PC0/MTIOC3C/CTS5#/RTS5#/SS5#/SSLA1/SEG10	PC0/MTIOC3C/CTS5#/RTS5#/SS5#/SSLA1
53	PB7/MTIOC3B/TXD9/SMOSI9/SSDA9/SSITXD0/SEG11/COM4	PB7/MTIOC3B/TXD9/SMOSI9/SSDA9/TS18
54	PB6/MTIOC3D/RXD9/SMISO9/SSCL9/SSIRXD0/SEG12/COM5	PB6/MTIOC3D/RXD9/SMISO9/SSCL9/TS19
55	PB5/MTIOC1B/MTIOC2A/POE1#/TMRI1/SCK9/SSISCK0/SEG13/COM6	PB5/MTIOC1B/MTIOC2A/POE1#/TMRI1/SCK9/TS20
56	PB4/CTS9#/RTS9#/SS9#/SEG14	PB4/CTS9#/RTS9#/SS9#/TS21
57	PB3/MTIOC0A/MTIOC3B/MTIOC4A/POE3#/TMO0/SCK6/AUDIO_MCLK/USB0_OVRCURA/SEG15/COM7	PB3/MTIOC0A/MTIOC4A/POE3#/TMO0/SCK6/TS22
58	PB2/CTS6#/RTS6#/SS6#/SEG16	PB2/CTS6#/RTS6#/SS6#/TS23
59	PB1/MTIOC0C/MTIOC4C/TMCI0 TXD6/SMOSI6/SSDA6/SSIWS0/SEG17/IRQ4	PB1/MTIOC0C/MTIOC4C/TMCI0 TXD6/SMOSI6/SSDA6/TS24/IRQ4/CMPOB1
60	VCC	VCC
61	PB0/MTIOC0C/MTIC5W/RTCOUT/SCL0/RSPCKA/RXD6/SMISO6/SSCL6/IRQ2/ADTRG0#	PB0/MTIC5W/RSPCKA/RXD6/SMISO6/SSCL6/TS25
62	VSS	VSS
63	PA6/MTIC5V/MTCLKB/MTIOC2A/POE2#/TMCI3/CTS5#/RTS5#/SS5#/SDA0/MOSIA/RXD8/SMISO8/SSCL8/IRQ3	PA7/MISOA
64	PA7/TXD8/SMOSI8/SSDA8/SEG18	PA6/MTIC5V/MTCLKB/TMCI3/POE2#/CTS5#/RTS5#/SS5#/MOSIA/TS26
65	PA5/SCK8/SEG19	PA5/RSPCKA/TS27
66	PA4/MTIOC2B/MTIC5U/MTCLKA/TMRI0/TXD5/SMOSI5/SSDA5/IRTXD5/SSLA0/CTS8#/RTS8#/SS8#/SEG20/IRQ5/CVREFB1	PA4/MTIC5U/MTCLKA/TMRI0/TXD5/SMOSI5/SSDA5/SSLA0/TS28/IRQ5/CVREFB1
67	PA3/MTIOC0D/MTIOC1B/MTCLKD/POE0#/RXD5/SMISO5/SSCL5/IRRXD5/MISOA/SEG21/IRQ6/CMPB1	PA3/MTIOC0D/MTCLKD/RXD5/SMISO5/SSCL5/TS29/IRQ6/CMPB1
68	PA2/RXD5/SMISO5/SSCL5/IRRXD5/SSLA3/SEG22	PA2/RXD5/SMISO5/SSCL5/SSLA3/TS30
69	PA1/MTIOC0B/MTCLKC/RTCOUT/SCK5/SSLA2/SEG23	PA1/MTIOC0B/MTCLKC/SCK5/SSLA2/TS31
70	PA0/MTIOC4A/SSLA1/SEG24/CACREF	PA0/MTIOC4A/SSLA1/TS32/CACREF
71	PF7/MTIOC3A/SEG25	PE7/IRQ7/AN023
72	PF6/MTIOC3C/SEG26	PE6/IRQ6/AN022
73	PE5/MTIOC2B/MTIOC4C/MISOA/TXD9/SMOSI9/SSDA9/SEG27/IRQ5/AN013/CMPOB1	PE5/MTIOC2B/MTIOC4C/IRQ5/AN021/CMPOB0

LFQFP 100-Pin No.	RX113	RX130
74	PE4/MTIOC1A/MTIOC3A/MTIOC4D/MOSIA/RXD9/SMISO9/SSCL9/SSIWS0/SEG28/IRQ4/AN012	PE4/MTIOC1A/MTIOC4D/TS33/AN020/CMPA2/CLKOUT
75	PE3/MTIOC0A/MTIOC1B/MTIOC4B/POE8#/CTS12#/RTS12#/SS12#/RSPCKA/SCK9/AUDIO_MCLK/SEG29/IRQ3/AN011	PE3/MTIOC4B/POE8#/CTS12#/RTS12#/SS12#/TS34/AN019/CLKOUT
76	PE2/MTIOC4A/RXD12/RXDX12/SMISO12/SSCL12/SSIRXD0/SEG30/IRQ7/AN010/CVREFB0	PE2/MTIOC4A/RXD12/RXDX12/SMISO12/SSCL12/TS35/IRQ7/AN018/CVREFB0
77	PE1/MTIOC4C/TXD12/TXDX12/SIOX12/SMOSI12/SSDA12/SSITXD0/SEG31/IRQ1/AN009/CMPB0	PE1/MTIOC4C/TXD12/TXDX12/SIOX12/SMOSI12/SSDA12/AN017/CMPB0
78	PE0/MTIOC2A/POE3#/SCK12/CTS9#/RTS9#/SS9#/SSISCK0/SEG32/IRQ0/AN008	PE0/SCK12/AN016
79	PE7/SEG33/IRQ7/AN015/CMPOB0	PD7/MTIC5U/POE0#/IRQ7/AN031
80	PE6/SEG34/IRQ6/AN014	PD6/MTIC5V/POE1#/IRQ6/AN030
81	PD4/POE3#/SEG35/IRQ4	PD5/MTIC5W/POE2#/IRQ5/AN029
82	PD3/POE8#/SEG36/IRQ3	PD4/POE3#/IRQ4/AN028
83	PD2/MTIOC4D/SEG37/IRQ2	PD3/POE8#/IRQ3/AN027
84	PD1/MTIOC4B/SEG38/IRQ1	PD2/MTIOC4D/SCK6/IRQ2/AN026
85	PD0/SEG39/IRQ0	PD1/MTIOC4B/RXD6/SMISO6/SSCL6/IRQ1/AN025
86	P92/AN021	PD0/TXD6/SMOSI6/SSDA6/IRQ0/AN024
87	P91/AN007	P47/AN007
88	P46/AN006	P46/AN006
89	P90/AN005	P45/AN005
90	P44/AN004	P44/AN004
91	P43/AN003	P43/AN003
92	VREFL/P42/AN002	P42/AN002
93	VREFH/P41/AN001	P41/AN001
94	VREFL0/PJ7	VREFL0/PJ7
95	P40/AN000	P40/AN000
96	VREFH0/PJ6	VREFH0/PJ6
97	AVSS0	AVCC0
98	AVCC0	P07/ADTRG0#
99	P07/TXD6/SMOSI6/SSDA6/TS0/ADTRG0#	AVSS0
100	PJ2/DA1	P05/DA1

Table 3.2 Points of Difference for Pins (64-Pin LFQFP Package)

LFQFP 64-Pin No.	RX113	RX130
1	PJ0/DA0	P03
2	P27/MTIOC2B/TMCI3/SCK1/SCK12/RXD6/SMISO6/SSCL6/IRQ3/CMPA2/CACREF/ADTRG0#	VCL
3	P26/MTIOC2A/TMO1/TXD1/SMOSI1/SSDA1/USB0_VBUSEN/TXD6/SMOSI6/SSDA6	MD/FINED
4	P30/MTIOC4B/POE8#/TMRI3/RXD1/SMISO1/SSCL1/CAPH/IRQ0	XCIN
5	P31/MTIOC4D/TMCI2/CTS1#/RTS1#/SS1#/CAPL/IRQ1	XCOUT
6	MD/FINED	RES#
7	RES#	XTAL/P37
8	XCOUT	VSS
9	XCIN/PH7	EXTAL/P36
10	UPSEL/P35/NMI	VCC
11	XTAL	P35/NMI
12	EXTAL	P32/MTIOC0C/TMO3/TXD6/SMOSI6/SSDA6/TS0/IRQ2/RTCOUT
13	VCL	P31/MTIOC4D/TMCI2/CTS1#/RTS1#/SS1#/TS1/IRQ1
14	VSS	P30/MTIOC4B/TMRI3/POE8#/RXD1/SMISO1/SSCL1/TS2/IRQ0
15	VCC	P27/MTIOC2B/TMCI3/SCK1/TS3
16	P32/MTIOC0C/RTCOUT/TMO3/TXD6/SMOSI6/SSDA6/CTS6#/RTS6#/SS6# IRQ2	P26/MTIOC2A/TMO1/TXD1/SMOSI1/SSDA1/TS4
17	P17/MTIOC0C/MTIOC3A/MTIOC3B/POE8#/TMO1/SCK1/MISOA/SDA0/RXD12/RXDX12/SMISO12/SSCL12/IRQ7	(5 V tolerant)/P17/MTIOC3A/MTIOC3B/TMO1/POE8#/SCK1/MISOA/SDA/IRQ7
18	P16/MTIOC3C/MTIOC3D/TMO2/TXD1/SMOSI1/SSDA1/MOSIA/SCL0/USB0_VBUS/USB0_VBUSEN/USB0_OVRCURB/IRQ6/RTCOUT/ADTRG0#	(5 V tolerant)/P16/MTIOC3C/MTIOC3D/TMO2/TXD1/SMOSI1/SSDA1/MOSIA/SCL/IRQ6/RTCOUT/ADTRG0#
19	P15/MTIOC0B/MTCLKB/TMCI2/RXD1/SMISO1/SSCL1/RSPCKA/IRQ5/CLKOUT/CACREF	P15/MTIOC0B/MTCLKB/TMCI2/RXD1/SMISO1/SSCL1/TS5/IRQ5
20	UB#/P14/MTIOC0A/MTIOC3A/MTCLKA/TMRI2/CTS1#/RTS1#/SS1#/SSLA0/TXD12/TXDX12/SIOX12/SMOSI12/SSDA12/USB0_OVRCURA/IRQ4	P14/MTIOC3A/MTCLKA/TMRI2/CTS1#/RTS1#/SS1#/TS6/IRQ4
21	VCC_USB	PH3/TMCI0/TS7
22	USB0_DM	PH2/TMRI0/TS8/IRQ1
23	USB0_DP	PH1/TMO0/TS9/IRQ0
24	VSS_USB	PH0/TS10/CACREF
25	P55/MTIOC4D/TMO3/VL1	P55/MTIOC4D/TMO3/TS11
26	P54/MTIOC4B/TMCI1/VL2	P54/MTIOC4B/TMCI1/TS12
27	PC7/MTIOC3A/MTCLKB/TMO2/TXD1/SMOSI1/SSDA1/MISOA/TXD8/SMOSI8/SSDA8/USB0_OVRCURB/VL3/CACREF	PC7/MTIOC3A/TMO2/MTCLKB/MISOA/TS13/CACREF

LFQFP 64-Pin No.	RX113	RX130
28	PC6/MTIOC3C/MTCLKA/TMCI2/RXD1/SMISO1/SSCL1/MOSIA/RXD8/SMISO8/SSCL8/USB0_EXICEN/VL4	PC6/MTIOC3C/MTCLKA/TMCI2/MOSIA/TS14
29	PC5/MTIOC3B/MTCLKD/TMRI2/SCK1/RSPCKA/SCK8/USB0_ID/COM0	PC5/MTIOC3B/MTCLKD/TMRI2/RSPCKA/TS15
30	PC4/MTIOC3D/MTCLKC/POE0#/TMCI1/SSLA0/CTS8#/RTS8#/SS8#/SCK5/USB0_VBUSEN/USB0_VBUS/COM1/IRQ2/CLKOUT	PC4/MTIOC3D/MTCLKC/TMCI1/POE0#/SCK5/SSLA0/TSCAP
31	PC3/MTIOC4D/TXD5/SMOSI5/SSDA5/IRTXD5/COM2	PC3/MTIOC4D/TXD5/SMOSI5/SSDA5/TS16
32	PC2/MTIOC4B/RXD5/SMISO5/SSCL5/SSLA3/IRRXD5/COM3	PC2/MTIOC4B/RXD5/SMISO5/SSCL5/SSLA3/TS17
33	PB7/PC1/MTIOC3B/TXD9/SMOSI9/SSDA9/SSITXD0/SEG11/COM4	PB7/PC1/MTIOC3B/TS18
34	PB6/PC0/MTIOC3D/RXD9/SMOSI9/SSCL9/SSIRXD0/SEG12/COM5	PB6/PC0/MTIOC3D/TS19
35	PB5/MTIOC2A/MTIOC1B/POE1#/TMRI1/SCK9/SSISCK0/SEG13/COM6	PB5/MTIOC2A/MTIOC1B/TMRI1/POE1#/TS20
36	PB3/MTIOC0A/MTIOC3B/MTIOC4A/POE3#/TMO0/SCK6/AUDIO_MCLK/USB0_OVRCURA/SEG15/COM7	PB3/MTIOC0A/MTIOC4A/TMO0/POE3#/SCK6/TS22
37	PB1/MTIOC0C/MTIOC4C/TMCI0/TXD6/SMOSI6/SSDA6/SSIWS0/SEG17/IRQ4	PB1/MTIOC0C/MTIOC4C/TMCI0/TXD6/SMOSI6/SSDA6/TS24/IRQ4/CMPOB1
38	VCC	VCC
39	PB0/MTIC5W/MTIOC0C/RTCOUT/SCL0/RSPCKA/RXD6/SMOSI6/SSCL6/IRQ2/ADTRG0#	PB0/MTIC5W/RXD6/SMISO6/SSCL6/RSPCKA/TS25
40	VSS	VSS
41	PA6/MTIC5V/MTCLKB/MTIOC2A/POE2#/TMCI3/CTS5#/RTS5#/SS5#/SDA0/MOSIA/IRQ3	PA6/MTIC5V/MTCLKB/TMCI3/POE2#/CTS5#/RTS5#/SS5#/MOSIA/TS26
42	PA4/MTIC5U/MTCLKA/MTIOC2B/TMRI0/TXD5/SMOSI5/SSDA5/IRTXD5/SSLA0/SEG20/IRQ5/CVREFB1	PA4/MTIC5U/MTCLKA/TMRI0/TXD5/SMOSI5/SSDA5/SSLA0/TS28/IRQ5/CVREFB1
43	PA3/MTIOC0D/MTCLKD/MTIOC1B/POE0#/RXD5/SMISO5/SSCL5/IRRXD5/MISOA/SEG21/IRQ6/CMPB1	PA3/MTIOC0D/MTCLKD/RXD5/SMISO5/SSCL5/TS29/IRQ6/CMPB1
44	PA1/MTIOC0B/MTCLKC/RTCOUT/SCK5/SSLA2/SEG23	PA1/MTIOC0B/MTCLKC/SCK5/SSLA2/TS31
45	PA0/MTIOC4A/SSLA1/SEG24/CACREF	PA0/MTIOC4A/SSLA1/TS32/CACREF
46	PE5/MTIOC4C/MTIOC2B/MISOA/TXD9/SMOSI9/SSDA9/SEG27/IRQ5/AN013/CMPOB1	PE5/MTIOC4C/MTIOC2B/IRQ5/AN021/CMPOB0
47	PE4/MTIOC4D/MTIOC1A/MTIOC3A/MOSIA/RXD9/SMISO9/SSCL9/SSIWS0/SEG28/IRQ4/AN012	PE4/MTIOC4D/MTIOC1A/TS33/AN020/CMPA2/CLKOUT
48	PE3/MTIOC0A/MTIOC1B/MTIOC4B/POE8#/CTS12#/RTS12#/SS12#/RSPCKA/SCK9/AUDIO_MCLK/SEG29/IRQ3/AN011	PE3/MTIOC4B/POE8#/CTS12#/RTS12#/SS12#/TS34/AN019/CLKOUT
49	PE2/MTIOC4A/RXD12/RXDX12/SMISO12/SSCL12/RXDX12/SSIRXD0/SEG30/IRQ7/AN010/CVREFB0	PE2/MTIOC4A/RXD12/RXDX12/SMISO12/SSCL12/TS35/IRQ7/AN018/CVREFB0

LFQFP 64-Pin No.	RX113	RX130
50	PE1/MTIOC4C/TXD12/TXDX12/SIOX12/SMOSI12/SSDA12/SSITXD0/SEG31/IRQ1/AN009/CMPB0	PE1/MTIOC4C/TXD12/TXDX12/SIOX12/SMOSI12/SSDA12/AN017/CMPB0
51	PE0/MTIOC2A/POE3#/SCK12/CTS9#/RTS9#/SS6#/SSISCK0/SEG32/IRQ0/AN008	PE0/SCK12/AN016
52	PE7/SEG33/IRQ7/AN015/CMPOB0	P47/AN007
53	PE6/SEG34/IRQ6/AN014	P46/AN006
54	PD2/MTIOC4D/SEG37/IRQ2	P45/AN005
55	PD1/MTIOC4B/SEG38/IRQ1	P44/AN004
56	PD0/SEG39/IRQ0	P43/AN003
57	VREFL/P42/AN002	P42/AN002
58	VREFH/P41/AN001	P41/AN001
59	VREFL0/PJ7	VREFL0/PJ7
60	P40/AN000	P40/AN000
61	VREFH0/PJ6	VREFH0/PJ6
62	AVSS0	AVCC0
63	AVCC0	P05/DA1
64	PJ2/DA1	AVSS0

4. Notes on Migration

A number of points should be borne in mind regarding the differences between the RX113 Group and RX130 Group. Points related to operating voltage range are covered in 4.1, Operating Voltage Range, points related to hardware in 4.2, Key Points Regarding Pin Design, and points related to software in 4.3, Key Points Regarding Functional Design. Note that the descriptions below refer to the 100-pin versions of the products.

4.1 Operating Voltage Range

4.1.1 Power Supply Voltage

The RX113 Group and RX130 Group have different power supply voltage ranges.

Table 4.1 shows a comparative listing of the power supply voltage ranges.

Table 4.1 Comparison of Power Supply Voltage Range Specifications

Item	RX113	RX130
VCC (USB not used)	1.8 V to 3.6 V*1*2	1.8 V to 5.5 V*1
VCC (USB used)	3.0 V to 3.6 V*1*2	—
AVCC0	1.8 V to 3.6 V	1.8 V to 5.5 V
VREFH0	1.8 V to AVCC0	1.8 V to AVCC0
VREFH	1.8 V to AVCC0	—
VCC_USB	Same potential as VCC	—

Note 1. When VCC ≥ 2.0 V, AVCC0 and VCC may be set independently within the usable range. When VCC < 2.0 V, AVCC0 = VCC.

Note 2. The following restrictions apply to the voltage of pins PJ0 and PJ2 and to VCC and AVCC0.
When using the 12-bit D/A converter: Port J0 and J2 pin voltage (D/A output voltage) ≤ VCC
When in use as general ports: VCC ≤ AVCC0

4.2 Key Points Regarding Pin Design

The functions that are implemented on both the RX113 Group and RX130 Group are compatible with each other. However, there are differences in the layouts of the pin functions. Refer to section 3, Comparison of Pin Functions, and RX130 Group User's Manual: Hardware when designing the system board.

4.2.1 USB Pins

The VCC_USB pin, VSS_USB pin, USB0_VBUS pin, USB0_VBUSEN pin, USB0_OVRCURA pin, USB0_OVRCURB pin, USB0_EXICEN pin, USB0_ID pin, USB0_DM pin, USB0_DP pin, and USBc function exist on RX113 Group MCUs but not on RX130 Group MCUs.

4.2.2 Resonator Connection Pins

When the main clock is not used on the RX130 Group, the EXTAL and XTAL pins can be used as general ports P36 and P37. When using these pins as general ports, be sure to stop the main clock (MOSCCR.MOSTP = 1). However, do not use the EXTAL and XTAL pins as general ports P36 and P37 in a system that uses the main clock.

When the main clock is used, do not set P36 and P37 to output.

The EXTAL and XTAL pins cannot be used as general ports on the RX113 Group.

When input an external clock, pay attention to the connection destination of the external clock input.

Connect to the XTAL terminal when using the RX113 group, and to the EXTAL terminal when using the RX130 group.

4.2.3 A/D Converter Analog Input Pins

Eight channels, using pins AN008 to AN015, exist on RX130 Group MCUs but not on RX113 Group MCUs.

Fifteen channels, using pins AN016 to AN020 pin and pins AN022 to AN031, exist on RX113 Group MCUs but not on RX130 Group MCUs.

4.2.4 D/A Converter Analog Input Pins

The VREFH and VREFL pins exist on RX113 Group MCUs but not on RX130 Group MCUs.

On the RX113 Group the AVCC0 and VCC voltages may be set individually, subject to the following restrictions:

- When using pins PJ0 and PJ2 as D/A converter output pins, the D/A converter's output voltage should not be higher than the VCC voltage.
- When using pins PJ0 and PJ2 as I/O ports, the VCC voltage should not be higher than the AVCC0 voltage.
- The above restrictions do not apply when the PJ0 and PJ2 pins are not used.

4.2.5 Mode Setting Pins

The P14/UB# pin and boot mode (USB interface) exist on RX113 Group MCUs but not on RX130 Group MCUs.

Table 4.2 lists the correspondences between the mode setting pin settings and the operating modes.

The key points regarding the mode setting pins are common to products with 100-pin, 80-pin, 64-pin, and 48-pin packages.

Table 4.2 Mode Setting Pins and Operating Modes

Mode Setting Pins		Operating Mode	
MD	**UB#**	**RX113**	**RX130**
High	—	Single-chip mode	
Low	—	—	Boot mode (SCI interface)
Low	Low	Boot mode (USB interface)	—
Low	High or open	Boot mode (SCI interface)	—

4.2.6 General I/O Ports

Ports P03, P05, P06, P33, P34, P36, P37, P45, P47, PD5 to PD7, PH0 to PH3, and PJ1 do not exist on RX113 Group MCUs.

Ports P02, P10, P11, P56, P90 to P92, PF6, PF7, PH7, PJ0, and PJ2 do not exist on RX130 Group MCUs.

When migrating, use other general I/O ports.

Special care is called for regarding ports P40 to P44, P46, P90 to P92, PJ6, and PJ7 on the RX113 Group and ports P03 to P07, P40 to P47, PJ6, and PJ7 on the RX130 Group as these are AVCC-dependent I/O ports. If any of these pins will not be used, set each unused pin to input and either connect it to AVCC via a resistor (pull-up) or to AVSS via a resistor (pull-down). Alternatively, unused pins may be set to output and left open.

If the unused pins are set to output and left open, they will nevertheless be in the input state immediately after a reset. While in the input state the voltage level of these pins is undefined, possibly resulting in an increase in the power supply current.

4.3 Key Points Regarding Functional Design

Software that runs on RX113 Group MCUs is highly compatible with software that runs on RX130 Group MCUs. Nevertheless, there are differences in areas such as operation timing and electrical characteristics, so careful evaluation is necessary.

Points to be borne in mind when designing software, with regard to differences in function settings on RX113 Group and RX130 Group MCUs, are described below.

For points of difference in modules and functions, refer to section 2, Comparative Overview of Functions. When applying the information contained in this application note, careful evaluation is necessary.

4.3.1 Option-Setting Memory

Option function select register 0 (OFS0) and option function select register 1 (OFS1) in the flash memory are implemented differently on RX113 Group MCUs and RX130 Group MCUs. Appropriate changes must be made to setting values when adapting software.

For points of difference, refer to 2.3, Option-Setting Memory. For details, refer to the User's Manual: Hardware for each group listed in section 5. Reference Documents.

4.3.2 Operating Modes

Boot mode (USB interface) is implemented on RX113 Group MCUs but not on RX130 Group MCUs.

4.3.3 Clock Generation Circuit

The RX113 Group has a USB-dedicated PLL circuit but the RX130 Group has no such circuit. There are also differences in the multiplication factors and oscillation frequencies that can be selected for the PLL circuit on the RX113 Group and RX130 Group.

Table 4.3 lists the differences in the multiplication factors and oscillation frequencies.

Table 4.3 PLL Circuit Multiplication Factors and Oscillation Frequencies.

Item	RX113	RX130
Multiplication factors	×6, ×8	×4 to ×8 (increments of 0.5)
Oscillation frequencies	32 MHz to 48 MHz (VCC ≥ 2.4V)	24 MHz to 32 MHz (VCC ≥ 2.4 V)

For points of difference, refer to 2.5, Clock Generation Circuit. For details, refer to the User's Manual: Hardware for each group listed in section 5. Reference Documents.

4.3.4 Serial Communication Interface

When using the RTS function in asynchronous mode on the RX130 Group, stopping reception requires one PCLK clock cycle from when the SCR.RE bit is cleared to 0 until the RTS signal generator stops.

When reading the RDR (or RDRL) register after clearing the RE bit to 0, it is necessary to confirm that the value of the RE bit is 0 before reading the RDR (or RDRL) register to prevent these two processes from being performed consecutively.

For points of difference, refer to 2.17, Serial Communication Interface. For details, refer to the User's Manual: Hardware for each group listed in section 5. Reference Documents.

4.3.5 I²C Bus Interface

On the RX113 Group, when using the timeout detection function while the internal reference clock select bits (ICMR1.CKS[2:0]) are set to a value other than 000b, it is necessary to set the TMWE timeout internal counter write enable bit (ICMR2.TMWE) to “writing enabled” and to initialize the timeout internal counter (TMOCNTL and TMOCNTU).

For points of difference, refer to 2.18, I²C Bus Interface. For details, refer to the User’s Manual: Hardware for each group listed in section 5. Reference Documents.

4.3.6 12-Bit A/D Converter

The functionality of the 12-bit A/D converter has been enhanced on the RX130 Group so that more I/O registers can be used with it. In addition, software that uses the eight channels on pins AN008 to AN015 on the RX113 Group should be changed to use suitable channels among the expanded range of 16 channels on pins AN016 to AN031 (100-pin products), or the six channels on pins AN016 to AN021 (64-pin products), on the RX130 Group.

Some bits in the ADSSTRn registers do not exist on the RX113 Group, and the setting values used for the sampling time setting bits (SST[7:0]) differ on the RX130 Group.

When an asynchronous or synchronous trigger is selected as the A/D conversion start condition, the procedure for stopping A/D conversion differs on the RX113 Group and RX130 Group. On the RX113 Group, the ADCSR.ADST bit should be cleared to 0 (A/D conversion stop) after ADCSR.TRGE has been cleared to 0 and a software trigger selected as the condition for starting A/D conversion. The procedure to be followed on the RX130 Group is shown in the flowchart below.

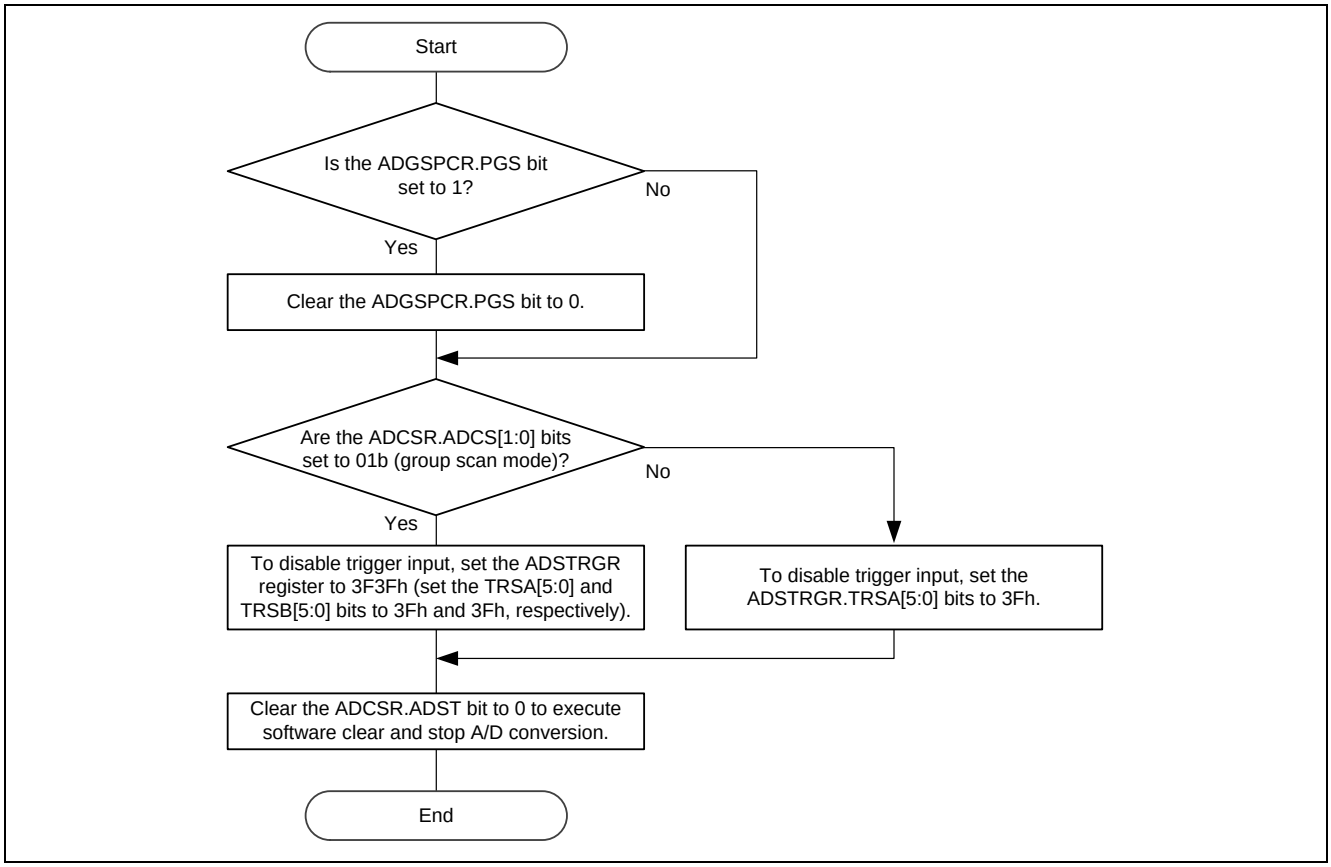

Figure 4.1 Setting Flowchart of Software Clearing Using ADCSR.ADST Bit

For points of difference, refer to 2.21, 12-Bit A/D Converter. For details, refer to the User’s Manual: Hardware for each group listed in section 5. Reference Documents.

5. Reference Documents

User's Manual: Hardware

RX113 Group, User's Manual: Hardware Rev.1.10 (R01UH0448EJ0110)
RX130 Group User's Manual: Hardware Rev.3.00 (R01UH0560EJ0300)
(The latest version can be downloaded from the Renesas Electronics website.)

Application Note

Points of Difference Between RX130 Group and RX230/RX231 Group (R01AN3067EJ)
Design Guide for Migration between RX Family: Differences in Package External (R01AN4591EJ)
(The latest version can be downloaded from the Renesas Electronics website.)

Technical Update/Technical News

(The technical updates issued after each referenced user manual are not reflected in this application note, so obtain latest version from the Renesas Electronics website.)

Revision History

Rev.	Date	Description	
		Page	Summary
1.00	Nov. 22, 2018	–	First edition issued
1.10	May. 8, 2019	Whole	Correspondence for 512KB of RX130 Confirmed the contents of the description again (Addition of description mistake etc.)
		6	Add memory map comparison of address space
		8	Add area comparison of option setting memory
		16	Add Comparative Listing of Entering and Exiting Low Power Consumption Modes and Operating States in Each Mode
		31	Add Comparative Listing of Functions Assigned to Each Multiplexed Pin
		75	Add differences in package external form

General Precautions in the Handling of Microprocessing Unit and Microcontroller Unit Products

The following usage notes are applicable to all Microprocessing unit and Microcontroller unit products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Precaution against Electrostatic Discharge (ESD)

   A strong electrical field, when exposed to a CMOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop the generation of static electricity as much as possible, and quickly dissipate it when it occurs. Environmental control must be adequate. When it is dry, a humidifier should be used. This is recommended to avoid using insulators that can easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors must be grounded. The operator must also be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions must be taken for printed circuit boards with mounted semiconductor devices.
2. Processing at power-on

   The state of the product is undefined at the time when power is supplied. The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the time when power is supplied. In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the time when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the time when power is supplied until the power reaches the level at which resetting is specified.
3. Input of signal during power-off state

   Do not input signals or an I/O pull-up power supply while the device is powered off. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Follow the guideline for input signal during power-off state as described in your product documentation.
4. Handling of unused pins

   Handle unused pins in accordance with the directions given under handling of unused pins in the manual. The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of the LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible.
5. Clock signals

   After applying a reset, only release the reset line after the operating clock signal becomes stable. When switching the clock signal during program execution, wait until the target clock signal is stabilized. When the clock signal is generated with an external resonator or from an external oscillator during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Additionally, when switching to a clock signal produced with an external resonator or by an external oscillator while program execution is in progress, wait until the target clock signal is stable.
6. Voltage application waveform at input pin

   Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between V_{IL} (Max.) and V_{IH} (Min.) due to noise, for example, the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between V_{IL} (Max.) and V_{IH} (Min.).
7. Prohibition of access to reserved addresses

   Access to reserved addresses is prohibited. The reserved addresses are provided for possible future expansion of functions. Do not access these addresses as the correct operation of the LSI is not guaranteed.
8. Differences between products

   Before changing from one product to another, for example to a product with a different part number, confirm that the change will not lead to problems. The characteristics of a microprocessing unit or microcontroller unit products in the same group but having a different part number might differ in terms of internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

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