Application Note

Adjustable Analog Sine/Square Wave Oscillator

AN-CM-324

Abstract

This application note describes how to design and build an adjustable, encoder-controlled, two-range sine / square wave oscillator.

The application note comes complete with a design file that can be found in the Reference section.

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1 Terms and Definitions

ACMP   Analog Comparator
GPO   General Purpose Output
IC   Integrated Circuit
I/O   Input / Output
OPAMP   Operational Amplifier

2 References

For related documents and software, please visit:

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Download our free GreenPAK Designer software [1] to open the .gp files [2] and view the proposed circuit design. Use the GreenPAK development tools [3] to freeze the design into your own customized IC in a matter of minutes. Find out more in a complete library of application notes [4] featuring design examples as well as explanations of features and blocks within the Dialog IC.

[1] GreenPAK Designer Software, Software Download, and User Guide
[2] AN-CM-324-GP Adjustable Analog Sine/ Square Wave Oscillator.gp, GreenPAK Design File
[3] GreenPAK Development Tools, GreenPAK Development Tools Webpage
[4] GreenPAK Application Notes, GreenPAK Application Notes Webpage
[5] SLG47004 Datasheet
[6] AN-CM-320 Potentiometer Controlled by an Encoder

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3   Introduction

This application note describes how to design and build an adjustable, encoder-controlled, two-range sine / square wave oscillator using the SLG47004 IC.

To design a simple analog sine wave oscillator (using Wien Bridge topology) a single OPAMP is required, see Figure 1. But to design a fully functional device with extra features many more active and passive components are needed. Figure 2 shows a schematic diagram of the OPAMP oscillator with the following features:

- Wide range adjustable frequency

- Two speeds of setting the frequency. Fast dial – for quick, and slow dial – for precision frequency set up

- Two range output frequency 15 Hz to 1.6 kHz and 430 Hz to 36 kHz

- Sine wave with an additional square wave output

- All controls using a single encoder with a built-in button

- Very low power consumption suitable for 3xLR44 batteries operation

- Extremely low power consumption in Off state (0.8 uA) eliminating the need for a physical switch (**Note 1**)

- Using single SLG47004 IC
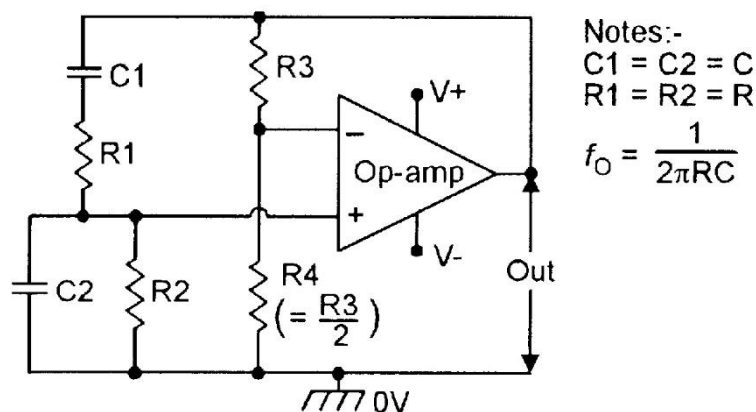
Figure 1: Basic Wien Bridge Sinewave Oscillator

Note 1: Some encoders may have one of the pins closed to the common in a steady-state, which will cause an extra current through the pull-up resistor even when the device is off. In this case, the current consumption in the off-state will be about 9.5 uA, which is also negligible.

Note 2: The device has no power-on indicator. If needed, it can be added by using an external transistor and a low-power LED.
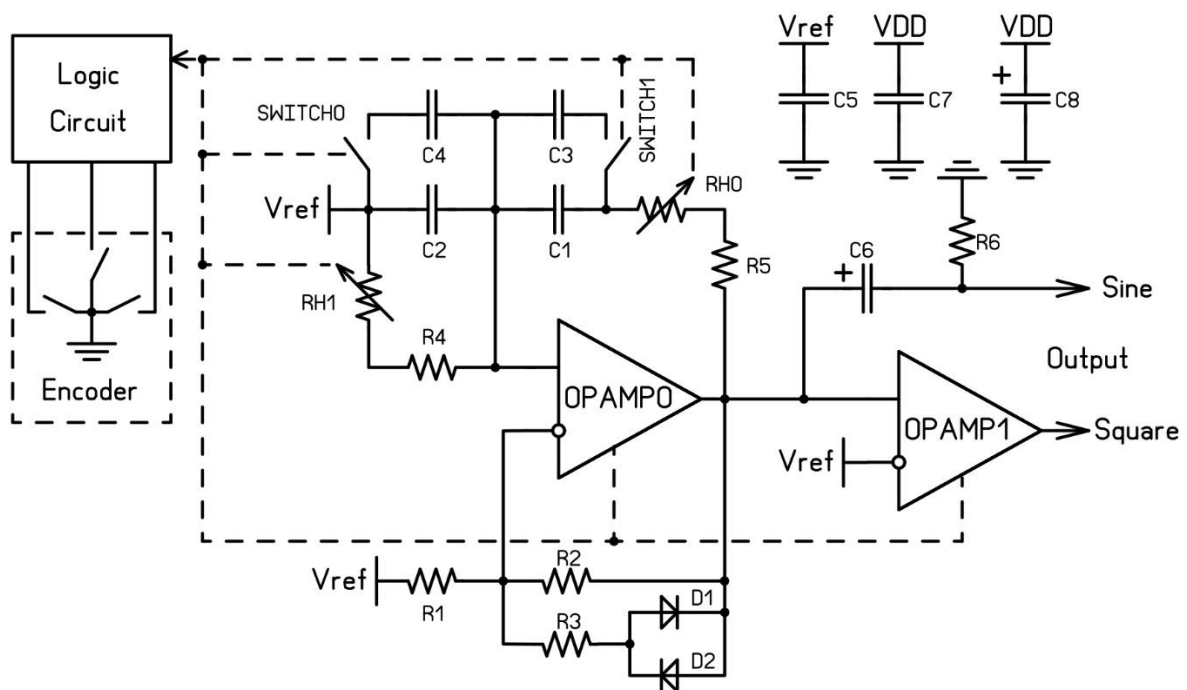
Figure 2: Adjustable, Encoder-controlled, Two-range Sine/Square Wave Oscillator Circuit

4   Design Operation

4.1   Schematic Design

As previously mentioned, only one chip is used in this design. The SLG47004 IC combines all necessary analog and digital macrocells in a tiny 3 x 3 mm STQFN-24 package. See Figure 3 for a complete schematic diagram in the GreenPAK Designer project.

Analog Part

This project uses nearly all analog macrocells within the IC. The central part plays the OPAMP0 as it is the oscillator itself. Its circuit represents a heavily modified Wien Bridge Sinewave Oscillator. The main issue with the Wien Bridge Oscillator is instability. The OPAMP's gain should be exactly 2 otherwise it won't start oscillating or it will go overdrive and the output sine wave will be distorted. This requires using precision resistors that are setting the gain (R1 and R2), and even then temperature and voltage fluctuation along with the OPAMP's imperfections may cause unstable oscillation. To overcome this problem a soft-clipping circuit R3D1D2 was added. It softly limits the gain and adds temperature stability not distorting the output waveform.

The digital rheostats RH0 and RH1 are used to adjust the frequency. Their resistance varies according to digital code from the control circuit and together with resistors R4 and R5, capacitors C1 and C2 (or C1+C3 and C2+C4) set the frequency.

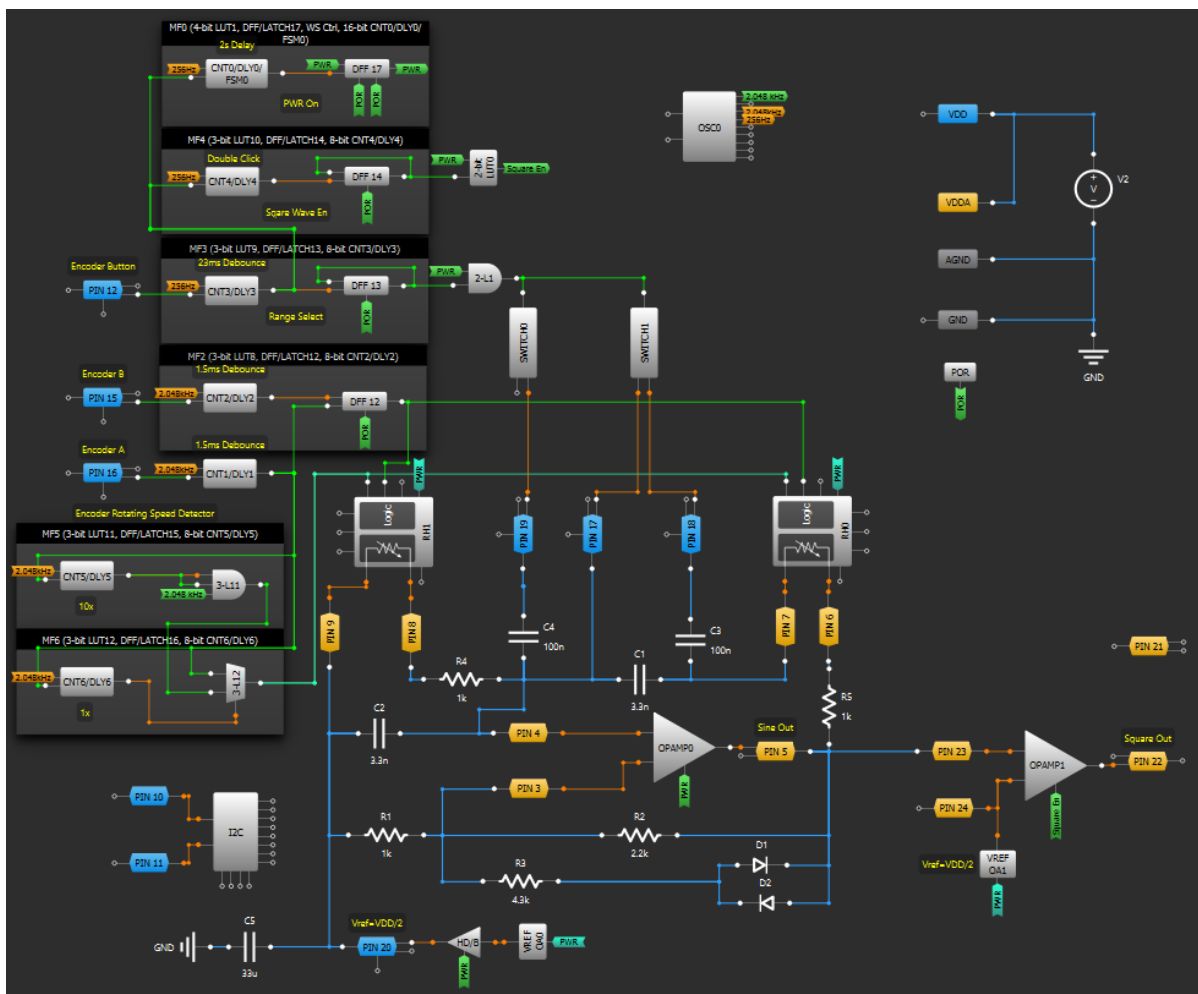## Adjustable Analog Sine/Square Wave Oscillator

Figure 3: Adjustable, Encoder-controlled, Two-range Sine/Square Wave Oscillator Project

Analog switches SWITCH0 and SWITCH1 serve to switch between two frequency ranges. When they are in Off state the capacitors C3 and C4 are disconnected from the circuit and the oscillator operates in the second range (450 Hz to 43 kHz). When the switches are in On state the capacitors C3 and C4 are connected in parallel to the capacitors C1 and C2 accordingly. This causes the oscillator to operate in the first frequency range (15 Hz to 1.4 kHz).

As a voltage reference, the VREF OA0 is used. It is configured to VDD/2 and output through the HD/B buffer to the PIN 20.

OPAMP1 is configured as the ACMP and is used to convert generated sine wave to a square wave. It has its own voltage reference, also configured to VDD/2 and connected to the inverting input.

Digital Part

All clocking in this design is done with a single low-power 2.048 kHz oscillator OSC0. It's the only macrocell that remains operational when the device is powered off. Nevertheless, the quiescent current in an off state is less than 1 uA, which allows connecting batteries directly to the chip not using any mechanical on/off switch.

The design uses several Counter/delays. The CNT3/DLY3 is configured as a 23 ms delay and is used as a button debounce. Together with the DFF13 and LUT1 (configured as logic AND), it controls analog switches SWITCH0 and SWITCH1. Thus, a single short push of the encoder button selects the frequency generation range.

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The CNT4/DLY4 is configured as a frequency detect with a period of 500 ms, so it reacts on at least two button pushes during 500 ms. Together with the DFF14 and LUT0, it switches on/off the square wave output.

The CNT0/DLY0 is configured as a 2-second delay and together with the DFF17, it serves as a power switch. So, when the encoder button is pressed and held for more than 2 seconds, it powers on/off all analog macrocells.

The CNT1/DLY1 and CNT2/DLY2 are configured as a 1.5 ms delay and serve as an encoder debounce. CNT2/DLY2 and DFF12 work as a detector of the encoder rotation direction and force rheostat's counter to count up or down. Meanwhile, both rheostats clock signal goes from CNT1/DLY1 through the Encoder Rotating Speed Detector built of CNT5/DLY5, LUT11, CNT6/DLY6, and LUT12.

The CNT5/DLY5 is configured as a 5 ms One Shot. For every encoder click, it generates a single pulse of approximately 5 ms. Those pulses then go to IN2 and IN1 inputs of the LUT11 (configured as logic AND), at the same time, the clock pulses (2.048 kHz) go to IN3 input. As a result, the package of 10 pulses is formed on its output.

The CNT6/DLY6 is configured as a Frequency Detect with a period of 40 ms. It detects the rotating speed of the encoder and with the help of the multiplexer (LUT12) outputs single or 10 pulses for every encoder click to the CLK input of both rheostats. So, when the user rotates the encoder slowly, every click equals one pulse, equals one bit, resulting in rheostat increasing or decreasing (depending on rotating direction) its current resistance by approximately 100 Ohm for precision frequency setting. Otherwise, when the rotating speed is high enough, every click equals 10 pulses, equals 10 bits, thus the rheostats will change their resistance by 10 steps for fast frequency sweep.

4.2 Typical Performance

Table 1. Typical Characteristics at VDD = 4.5V, T = 25 °C, No Load

Parameter	Description	Range	Output frequency, Hz	Typ	Unit
IDD	Current consumption, square wave off	1	15	0.69	mA
			1500	0.82	mA
		2	430	0.67	mA
			36000	0.73	mA
	Current consumption, square wave on	1	15	1.80	mA
			1500	1.33	mA
		2	430	1.12	mA
			36000	2.22	mA
Vsine (RMS)	Sine wave output voltage, RMS	1	15	0.90	V
			1500	0.86	V

		2	430	0.73	V
			36000	0.58	V
Vsine (p-p)	Sine wave output voltage, peak-to-peak	1	15	2.48	V
			1500	2.44	V
		2	430	2.08	V
			36000	1.72	V
Vsq (p-p)	Square wave output voltage, peak-to-peak	1	15	4.5	V
			1500	4.5	V
		2	430	4.5	V
			36000	4.5	V
Dt	Square wave duty cycle	1	15	53.0	%
			1500	50.0	%
		2	430	50.4	%
			36000	50.0	%

The oscilloscope screenshots of the Sine / Square wave oscillator are shown in Figure 4 through Figure 9.
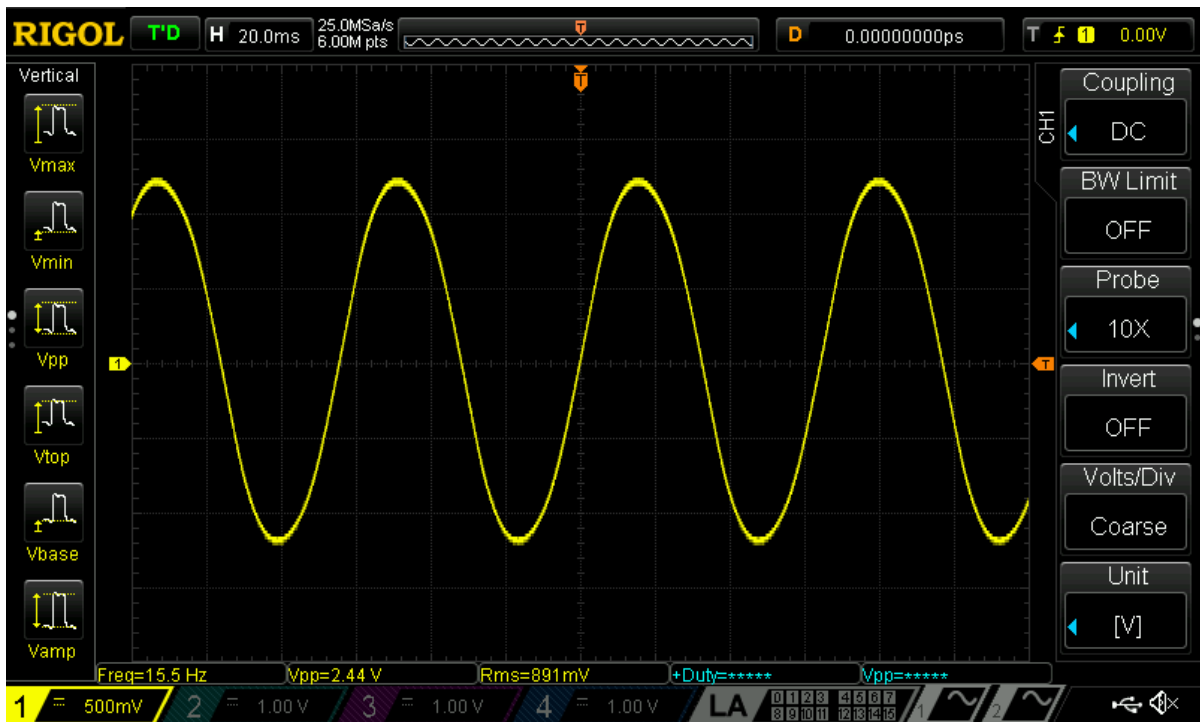
Adjustable Analog Sine/Square Wave Oscillator

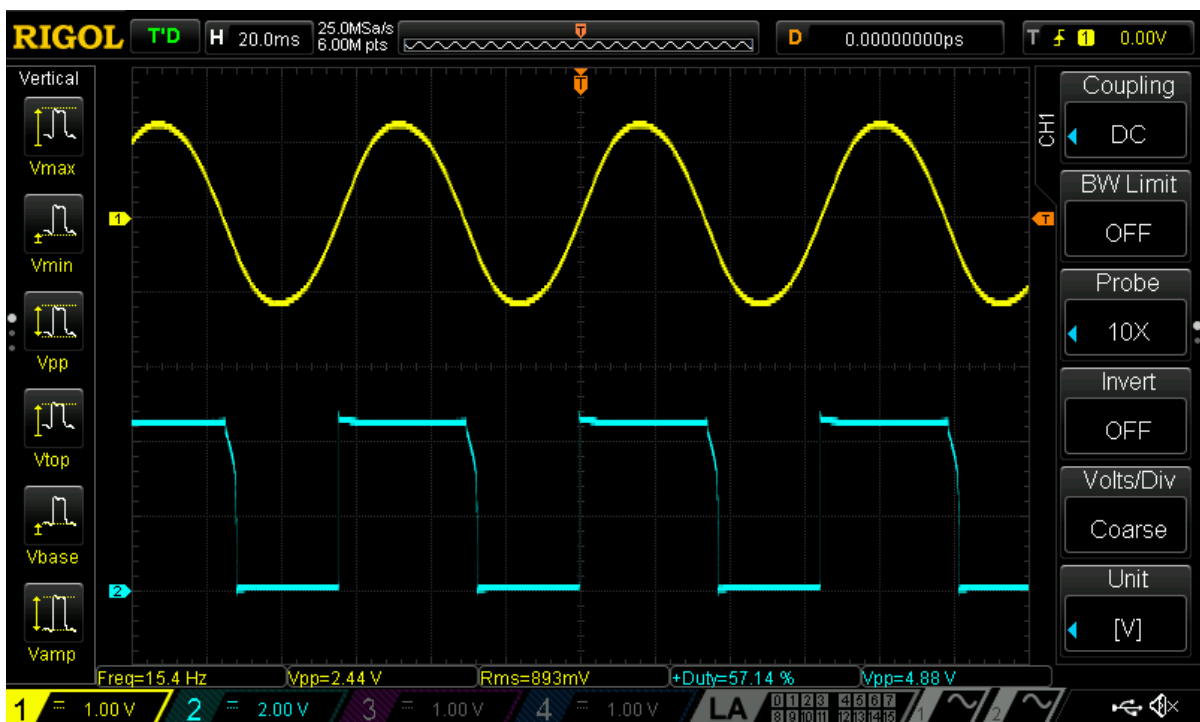**Figure 4: First Range, Sine Wave Output, Min. Frequency**

Figure 5: First Range, Sine and Square Wave Output, Min. Frequency
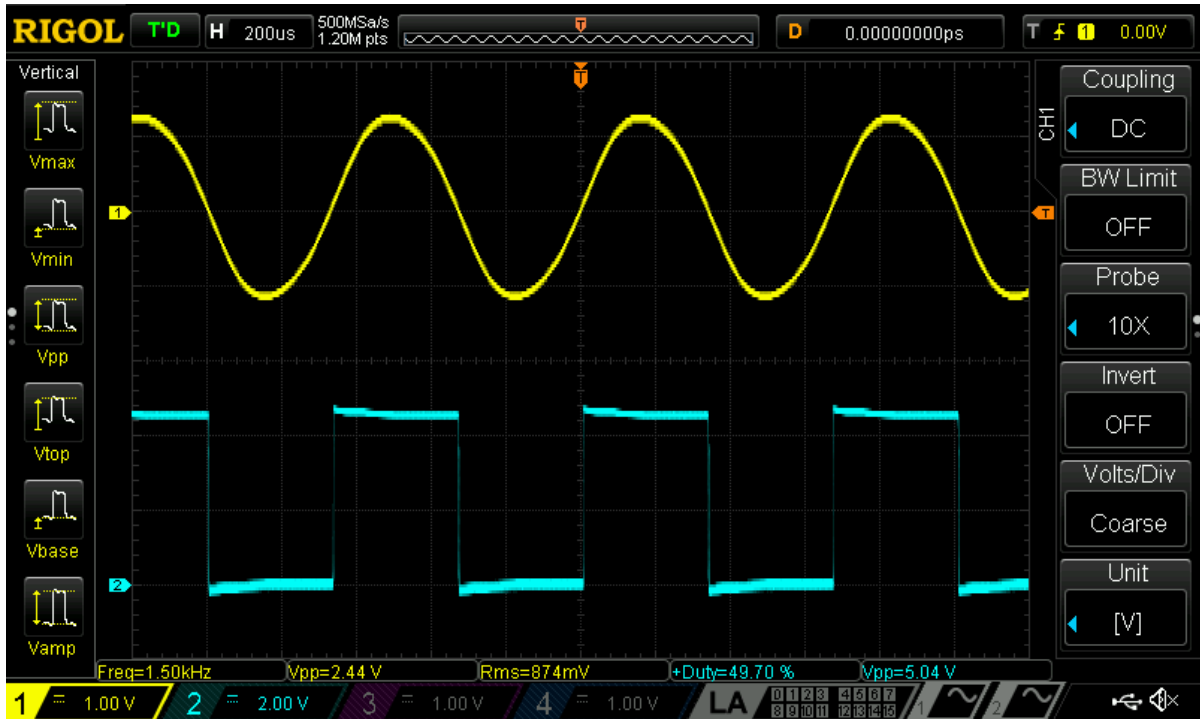
Adjustable Analog Sine/Square Wave Oscillator

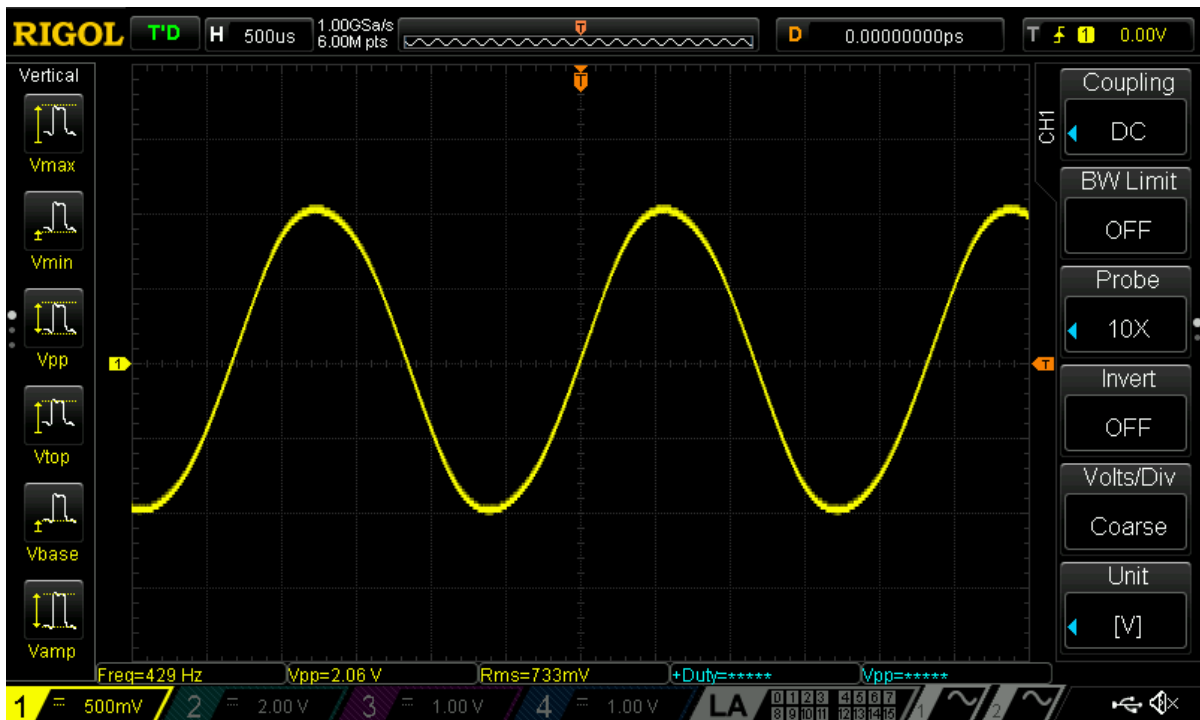**Figure 6: First Range, Sine and Square Wave Output, Max. Frequency**

Figure 7: Second Range, Sine Wave Output, Min. Frequency

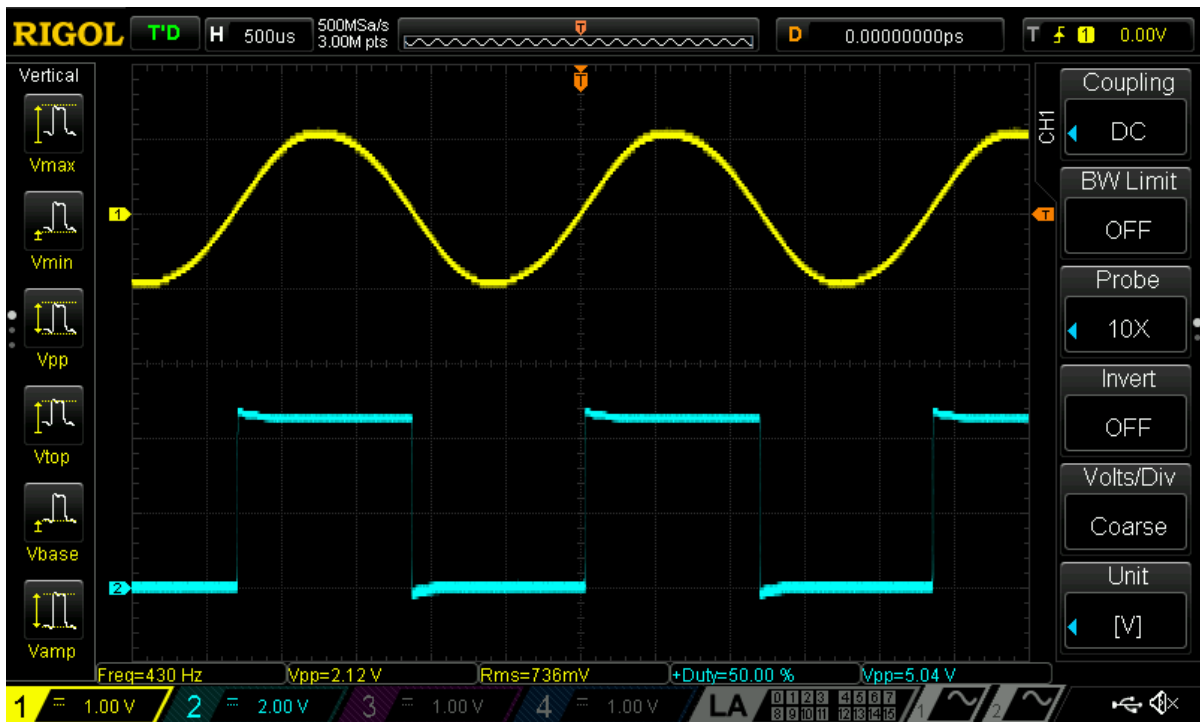## Adjustable Analog Sine/Square Wave Oscillator

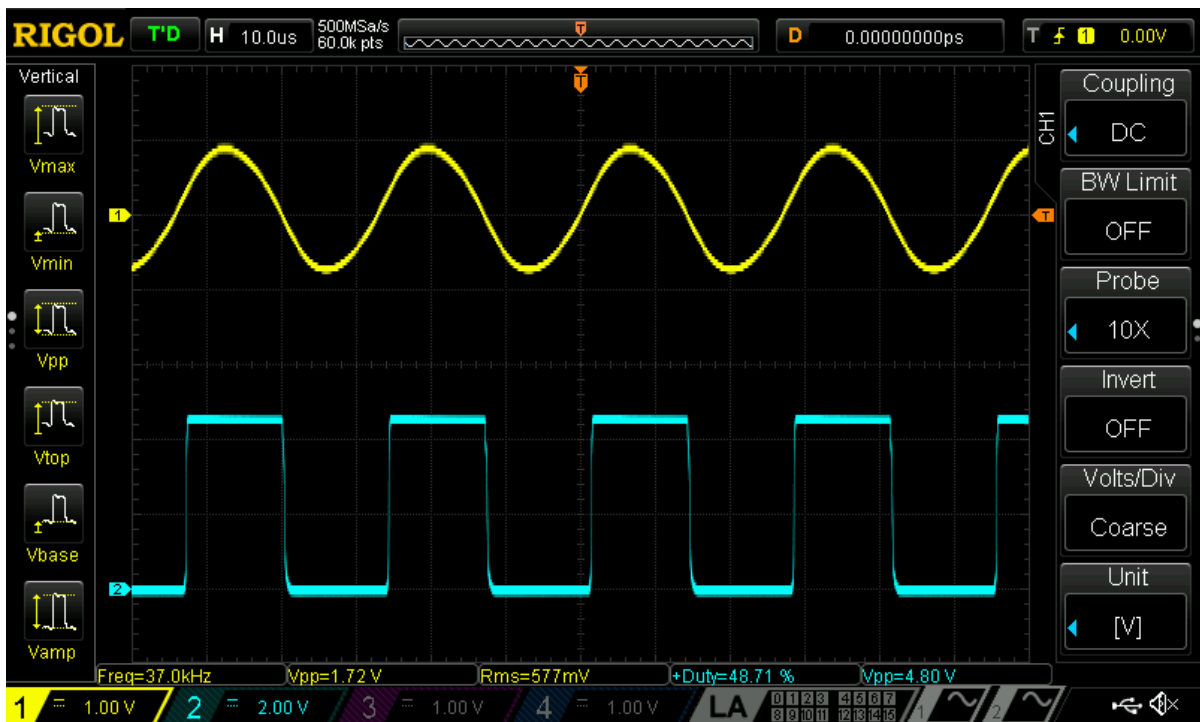**Figure 8: Second Range, Sine and Square Wave Output, Min. Frequency**

Figure 9: Second Range, Sine and Square Wave Output, Max. Frequency

Adjustable Analog Sine/Square Wave Oscillator

4.3   Macrocell Configuration

OSC0 Settings: default.

I2C Settings: default.

Table 2: PIN settings

Properties	PIN 3 to 9, and 17 to 24	PIN 10 and 11	PIN 12, 15, and 16
I/O selection	Analog input/output	Digital input	Digital input
Input mode OE=0	Analog input/output	Digital in without Schmitt trigger	Digital in with Schmitt trigger
Output mode OE=1	Analog input/output	None	None
Resistor	Floating	Floating	Pull Up
Resistor value	Floating	Floating	1M

*Note: although PIN 21 is not in use, it is recommended to set it to **Analog input/output** or connect it to the ground externally.*

Table 3: OPAMP Settings

Properties	ACMP0H	ACMP1H
Mode	OpAmp mode	ACMP mode
Bandwidth Selection	8 MHz	8 MHz
Charge Pump	Enable CP	Enable CP
Supporting Blocks On/Off	Follows OpAmp	Follows OpAmp
Vref connection	Disconnected	To IN-
Vref	VDDA*(32 / 64)	VDDA*(32 / 64)

Table 4: Vref Settings

Properties	VREF OPAMP0	VREF OPAMP1
Enable selection	From matrix	From matrix
Register enable	Vref enable	Vref enable
Input voltage selection	VDDA	VDDA
Output selection	VDDA*(32 / 64)	VDDA*(32 / 64)

Table 5: HD Buffer Settings

Properties	HD Buffer
Power up source	From matrix
Power up register	Disable
Input	VREF OPAMP0
Output	PIN 20 (GPIO6)

Table 6: Digital Rheostat Settings

Properties	RH0	RN1
Mode	None	Rheostat
Charge Pump Enable	From matrix	From matrix
Charge Pump Clock	Auto selection	Auto selection
Auto-Trim	Disable	Disable
Active level for UP/DOWN	Up when HIGH	Up when HIGH
Resistance (initial data)	512	512
UP/DOWN source	Ext. (From matrix)	Ext. (From matrix)
Clock	Ext. Clock (From matrix)	Ext. Clock (From matrix)

Table 7: Analog Switch Settings

Properties	SWITCH0	SWITCH1
Mode	Analog Switch	Analog Switch
Big PMOS control	By Matrix	--
Big NMOS control	--	By Matrix
Small NMOS enable	Disable	--
Small PMOS enable	--	Disable
Half Bridge Dead Time Select	Bypass	Bypass

Table 8: LUT Settings

IN2	IN1	IN0	2-bit LUT0	2-bit LUT1	3-bit LUT11 (MF5)	3-bit LUT12 (MF6)
0	0	0	0	0	0	Multiplexer
0	0	1	0	0	0	

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IN2	IN1	IN0	2-bit LUT0	2-bit LUT1	3-bit LUT11 (MF5)	3-bit LUT12 (MF6)
0	1	0	1	0	0	
0	1	1	0	1	0	
1	0	0	--	--	0	
1	0	1	--	--	0	
1	1	0	--	--	0	
1	1	1	--	--	1	

Table 9: DFF Settings

Properties	DFF12	DFF13	DFF14	DFF17
Mode	DFF	DFF	DFF	DFF
nSET/nRESET option	nRESET	nRESET	nRESET	None
Initial polarity	Low	Low	Low	Low
Q output polarity	Non-inverted (Q)	Inverted (nQ)	Inverted (nQ)	Inverted (nQ)

Table 10: CNT/DLY Settings

Properties	16-bit CNT0/DLY 0/FSM0 (MF0)	8-bit CNT1/DLY 1 (MF1)	8-bit CNT2/DLY 2 (MF2)	8-bit CNT3/DLY 3 (MF3)	8-bit CNT4/DLY 4 (MF4)	8-bit CNT5/DLY 5 (MF5)	8-bit CNT6/DLY 6 (MF6)
Type	CNT/DLY	--	--	--	--	--	--
Multi-function mode	--	CNT/DLY	--	--	--	--	--
Mode	Delay	Delay	Delay	Delay	Frequency detect	One shot	Frequency detect
Counter data	511	2	2	5	127	10	81
Edge select	Falling	Both	Both	Rising	Falling	Rising	Rising
DLY IN init. value	Bypass the initial	Bypass the initial	Bypass the initial	Bypass the initial	Bypass the initial	Bypass the initial	Bypass the initial
Output polarity	Inverted (nOUT)	Non-inverted (OUT)	Non-inverted (OUT)	Non-inverted (OUT)	Non-inverted (OUT)	Non-inverted (OUT)	Non-inverted (OUT)
Mode signal sync.	Bypass	Bypass	Bypass	Bypass	Bypass	Bypass	Bypass
Clock	OSC0 / 8	OSC0	OSC0	OSC0 / 8	OSC0 / 8	OSC0	OSC0

4.4 PCB Layout

The PCB was designed using the easyeda.com service. See the full schematic diagram, PCB design, and PCB 3D model in Figures 10 and 11. The size of the board is 25 x 34 mm. Figure 12 shows the photo of the prototype.
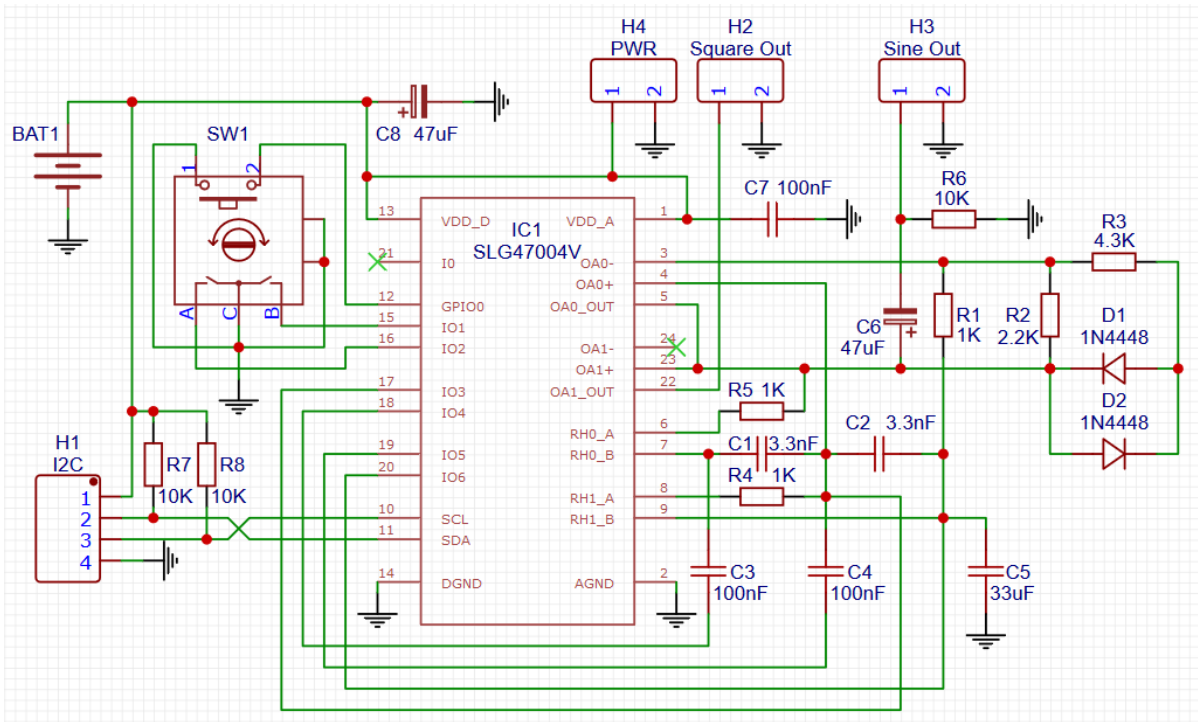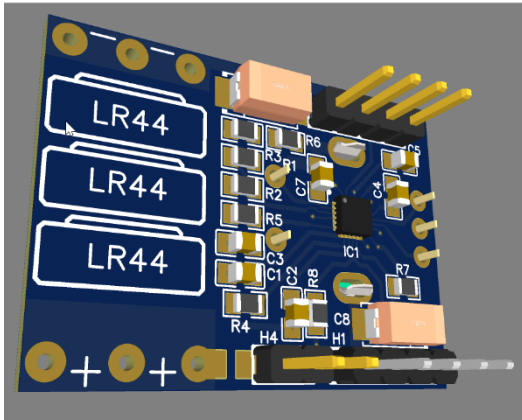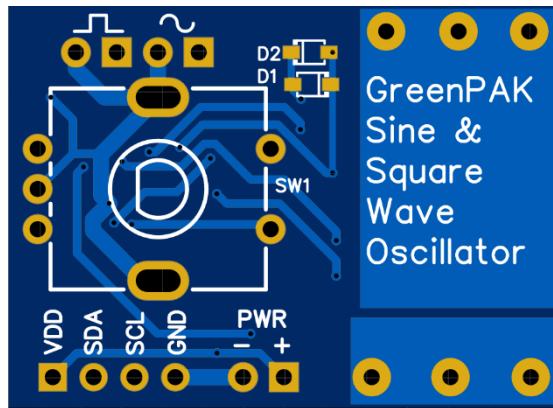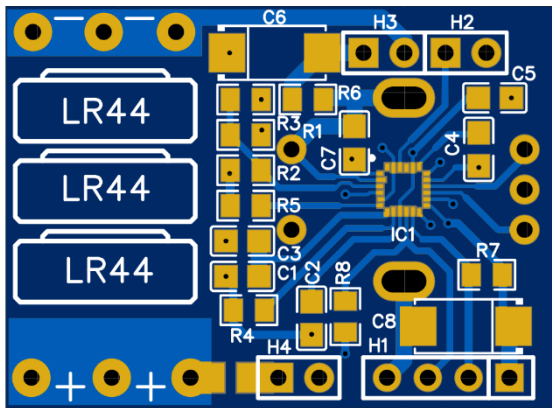
Adjustable Analog Sine/Square Wave Oscillator

Figure 10: Full Schematic Diagram

Bottom Side

Top Side

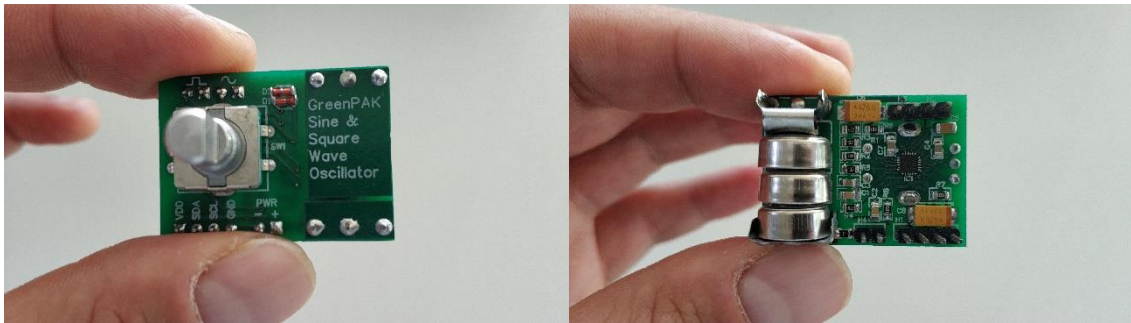**Figure 11: PCB Design and 3D Model**

Figure 12: Prototype Photo

4.5   Software Simulation

The GreenPAK Designer has the ability to simulate the design. To do that, a simplified circuit was designed, see Figure 13. The results of the simulation are shown in Figures 14 and 15.
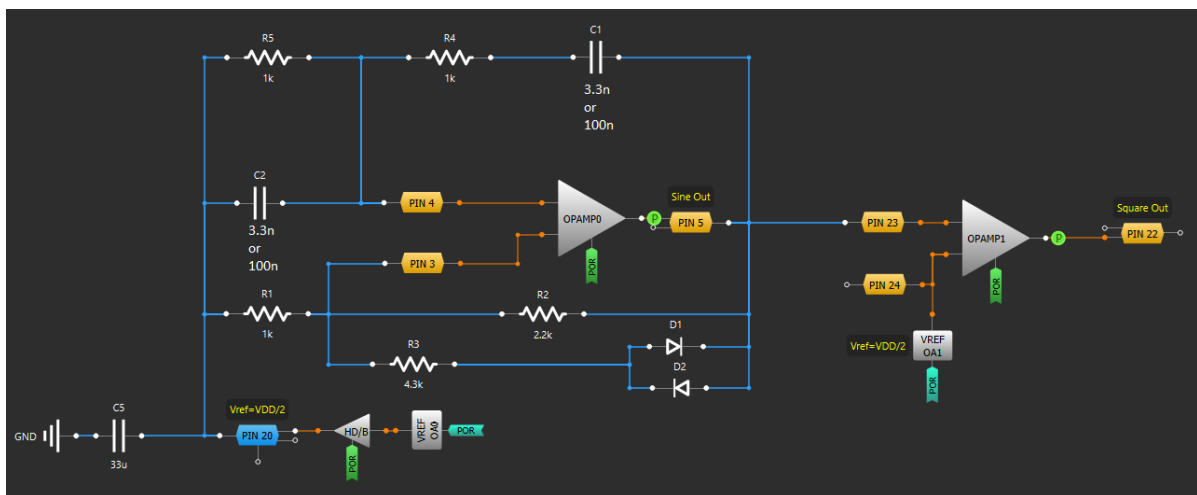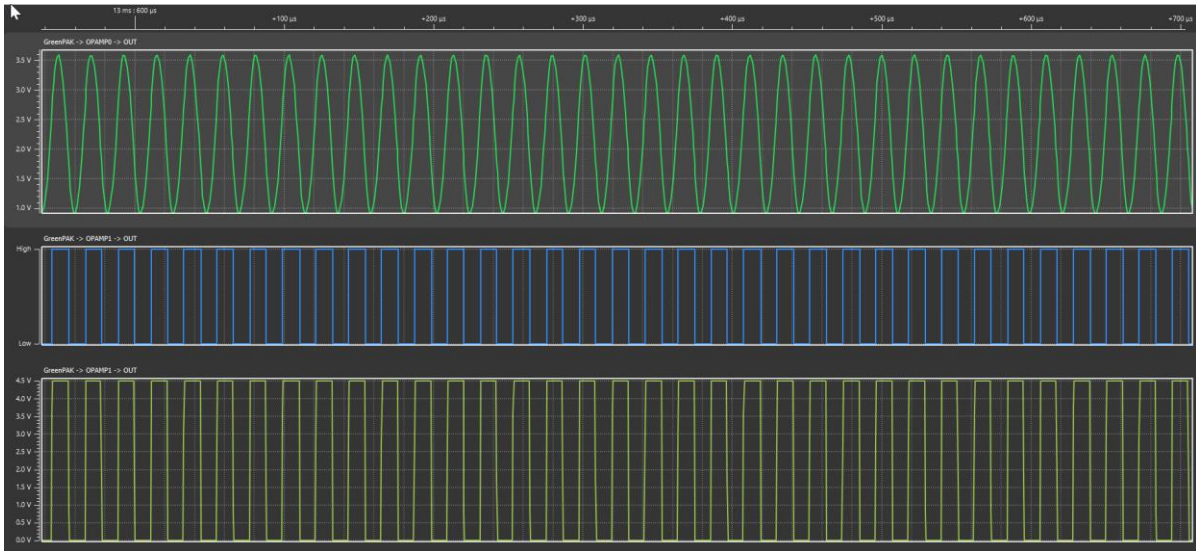

Figure 13: Simplified Circuit Design

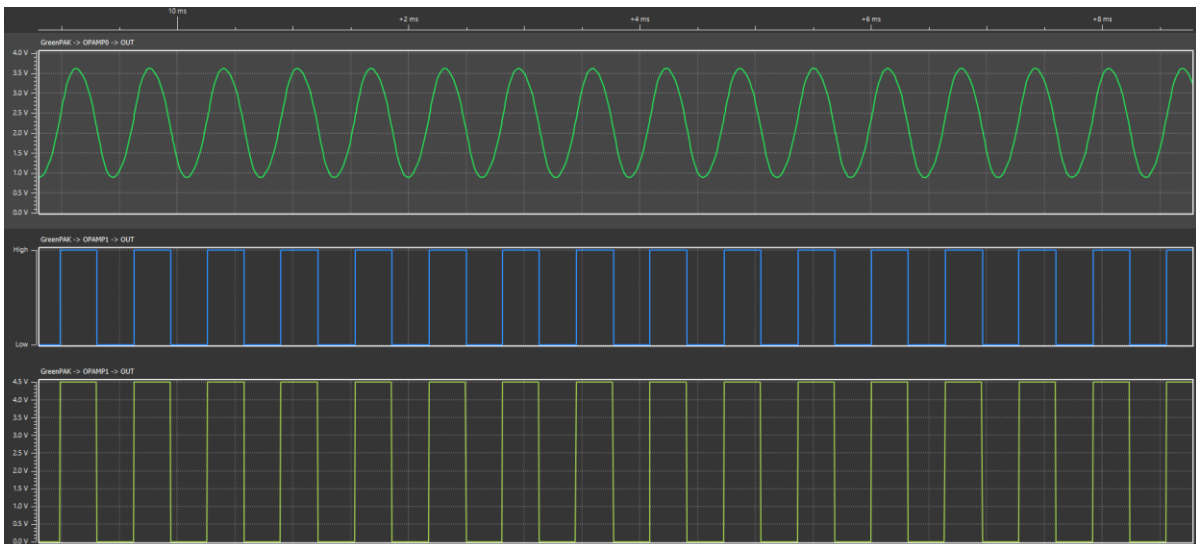**Figure 14: Simulation Results. C1 = C2 = 3.3n**

Figure 15: Simulation Results. C1 = C2 = 100n

5   Conclusions

As can be seen, designing and building an adjustable, encoder-controlled, two-range sine / square wave oscillator using the OPAMP PAK is very easy. The SLG47004 turned out to be the perfect IC for the design containing all necessary analog and digital macrocells. The design shown in this document is one of many versions of the device that can be built based on the SLG47004. There are some unused macrocells that can be used to design additional functions. And vise versa, if some features are not required, they can be easily deleted from the design.

Revision History

Revision	Date	Description
1.0	07-Oct-2021	Initial Version

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