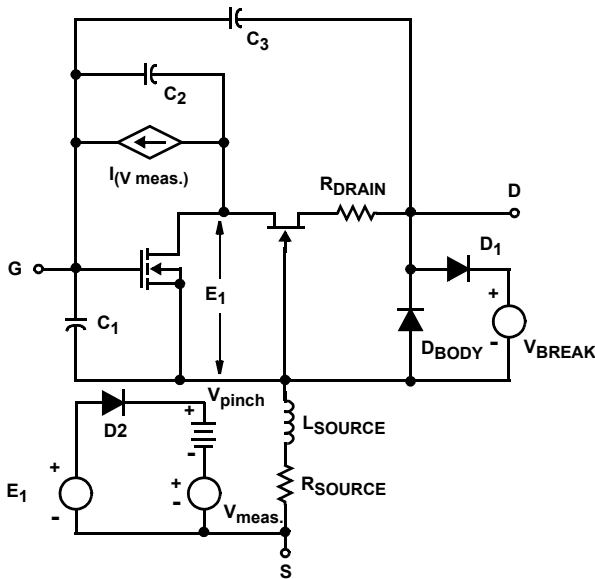


A Spice-2 Subcircuit Representation For Power MOSFETs Using Empirical Methods

**Abstract**

An accurate power-MOSFET model is not widely available for CAD circuit simulation. This work provides a subcircuit model which is compatible with SPICE-2 software and MOSFET terminal measurements. SPICE-2 is the circuit simulation package of choice for this work because of its universal availability, despite its inherent limitations. These limitations are circumvented through circuit means.

This effort models power-MOSFET terminal behavior consistent with SPICE-2 limitations; hence it will differ from the physical model as suggested by Wheatley, et al<sup>1</sup>, Ronan et al<sup>2</sup> and others. We feel we have advanced prior efforts<sup>3</sup> particularly in areas of third-quadrant operations, avalanche-mode simulation, switching waveforms and diode recovery waveforms.



**FIGURE 1. SPICE-2 SUBCIRCUIT FOR POWER MOSFET SIMULATION**

NOTE: If the JFET source voltage,  $E_1$ , is very low relative to its  $V_{PINCH}$  voltage, the JFET is in a highly conductive state, tightly coupling  $C_2$  to the JFET drain. However, as the voltage  $E_1$  approaches  $V_{PINCH}$ , the JFET operates in a constant-current mode, thereby permitting a much faster drain slew rate, which is determined primarily by  $C_3$ .

**Discussion**

The subcircuit shown in Figure 1 is described in Table 1. All passive circuit elements are constants. The very-high-gain JFET is used to simulate the dual-slope drain voltage vs time switching curve common to the power MOSFET.<sup>1,2</sup>

If  $E_1$  exceeds  $V_{PINCH}$ , errors will exist in the turn-on waveforms. The  $C_2$  discharge current-controlled current source remedies this situation in conjunction with the subcircuit containing  $D_2$ . The  $D_2$  ideality factor was set at 0.03 to assure that  $E_1$  minus  $V_{PINCH}$  does not exceed several millivolts.

The body diode cannot be properly modeled by the JFET gate-drain diode, hence  $D_{BODY}$ . Conditions of Table 1 assure that most third-quadrant current flow is via  $D_{BODY}$ . Avalanche breakdown is more accurately modeled by the clamp circuit containing  $D_1$ .

Table 1 in combination with Figures 2, 3, 4 and 5 provides the required empirical inputs. Table 2 lists the preferred algorithm for parameter extraction.

**TABLE 1. EMPIRICAL INPUTS**

MOSFET	Enhancement mode; $W = L = 1\mu\text{m}$ ; $K_P$ (Figure 2); $V_{TO}$ (Figure 2); $C's = 0$ ; $I_{DSO} = 1E-12$
JFET	Depletion mode; areas factor = 1; $B = 100K_P$ (Figure 2); $V_{TO} = V_{PINCH}$ (Figure 5); $C's = \text{diode lifetime} = R_{SERIES} = 0$ ; diode ideality factor = 1.0, $I_{DSO} = 1E-20$
BODY DIODE	$I_S$ from Figure 4; Ideality Factor = 1.0; R from Figure 4 (must be very much greater than $R_D$ ); C (from $C_{OSS}$ ); lifetime = best fit to $T_{RR}$
$D_1$	$I_S = \text{arbitrary}$ ; C = lifetime = 0; ideality factor = best low-current fit; R = best high-current fit
$D_2$	$I_S = 1E-8$ ; C = lifetime = R = 0; ideality factor = 0.03
$R_S$	Figure 2.
$R_{DRAIN}$	Figure 3
$L_S$	Approximately $(5L) \ln(4L/d)$ nH; L and d are source wire inches.
$V_{PINCH}$	$V_{TO}$ of JFET.
$V_{BRK}$	Avalanche voltage.
$C_1$	From Figure 5.
$C_2$	Maximum from Figure 5.
$C_3$	Minimum from Figure 5.

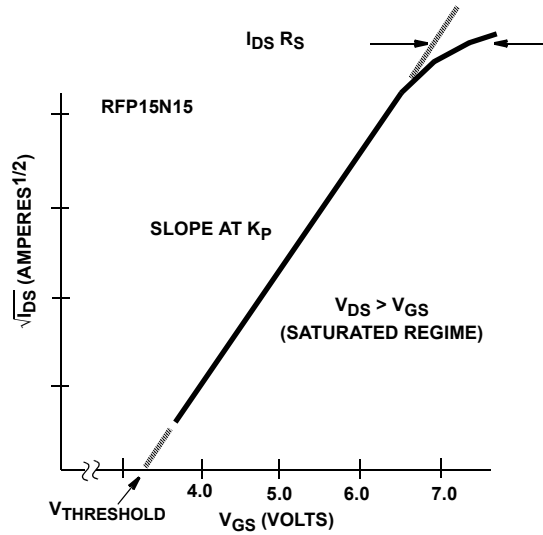


FIGURE 2. SQUARE ROOT OF DRAIN CURRENT VS GATE VOLTAGE DEFINES  $V_{THRESHOLD}$ ,  $K_P$  AND  $R_S$

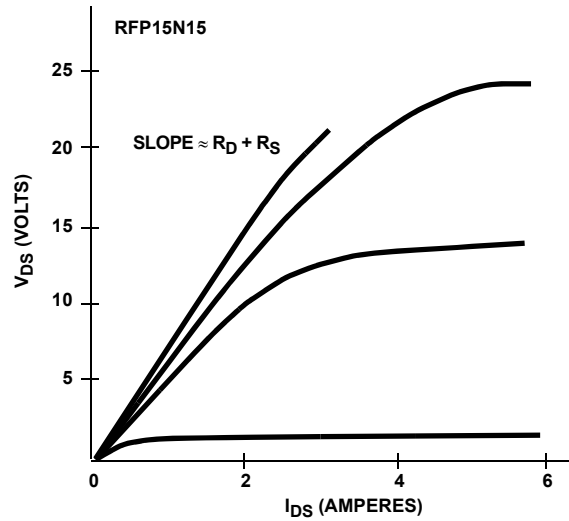


FIGURE 3. DRAIN CURRENT VS DRAIN VOLTAGE WITH CONSTANT GATE VOLTAGE DEFINES "ON" RESISTANCE

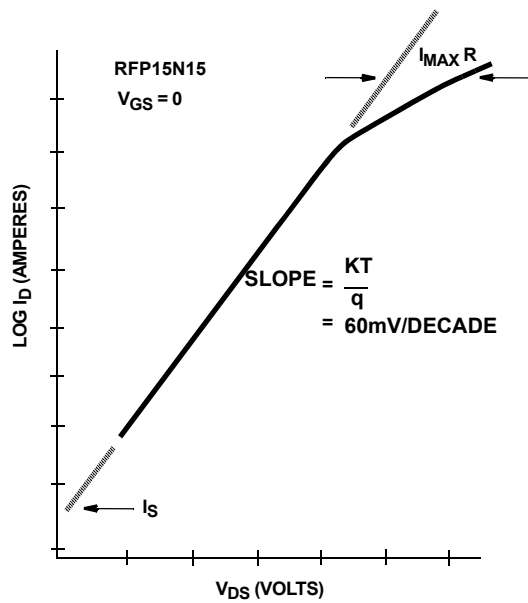


FIGURE 4. THIRD-QUADRANT OPERATION DEFINES  $I_S$  AND  $R$  OF DIODE  $D_{BODY}$

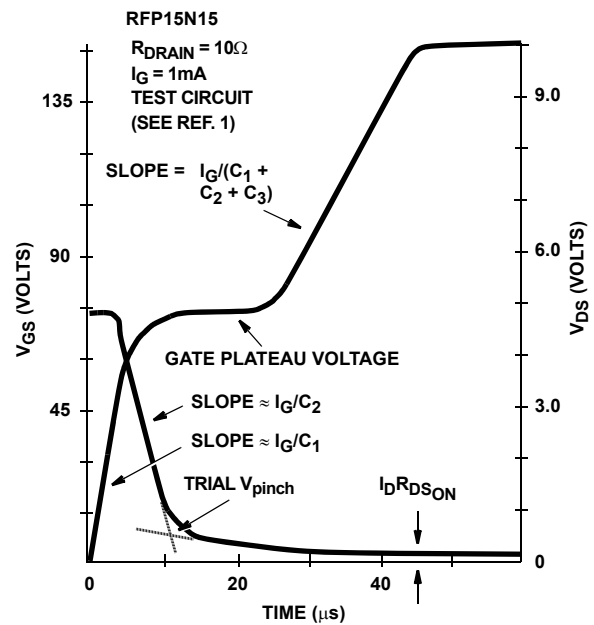


FIGURE 5. DRAIN AND GATE VOLTAGE VS TIME DETERMINE  $C_1$ ,  $C_2$ ,  $C_3$  AND  $V_{PINCH}$ .

TABLE 2. PREFERRED ALGORITHM FOR PARAMETER EXTRACTION

1. Determine  $K_P$  of lateral MOS
2. Determine  $V_{TH}$  of lateral MOS
3. Determine  $C_1$
4. Determine  $C_1 + C_2 + C_3$
5. Determine  $R_{DS}$
6. Assign  $B$  of JFET =  $100 \times K_P$  of lateral MOS
7. Use trial  $V_{PINCH}$
8. Use  $C_2$  (Maximum),  $C_3$  (Minimum) are curve-fit  $C$ 's
9. Adjust  $V_{PINCH}$  to fix gate voltage plateau

## Results

Figure 6 and Figure 7 compare measured static data to calculated transfer curves and output curves. Calculated static-output curves are shown in Figure 8 and Figure 9 for third-quadrant range, including avalanche. Calculated switching data is compared to measured switching curves<sup>1,2</sup> in Figure 10 and Figure 11. Calculated body-diode recovery curves are shown in Figure 12.

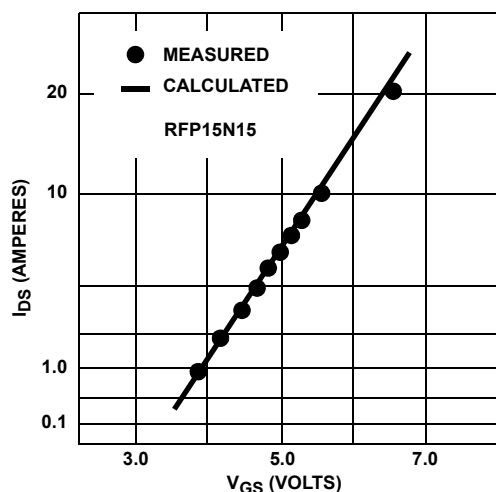


FIGURE 6. DRAIN CURRENT VS GATE VOLTAGE (NOTE SQUARE ROOT SCALE) - MEASURED CURVE VS CALCULATED POINTS

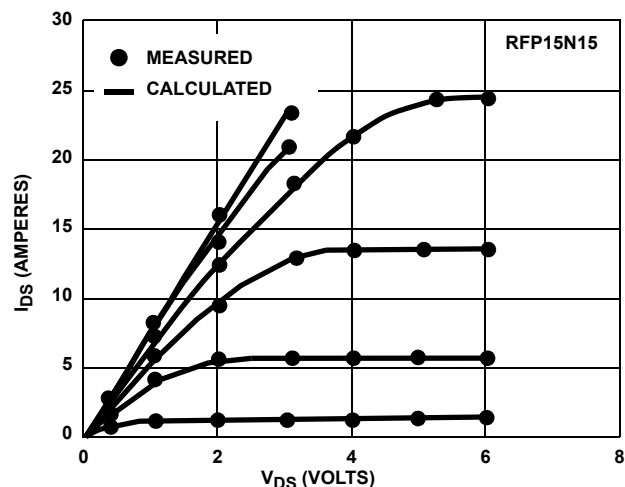


FIGURE 7. DRAIN CURRENT VS DRAIN VOLTAGE FOR CONSTANT VALUES OF GATE VOLTAGE - MEASURED CURVES VS CALCULATED POINTS

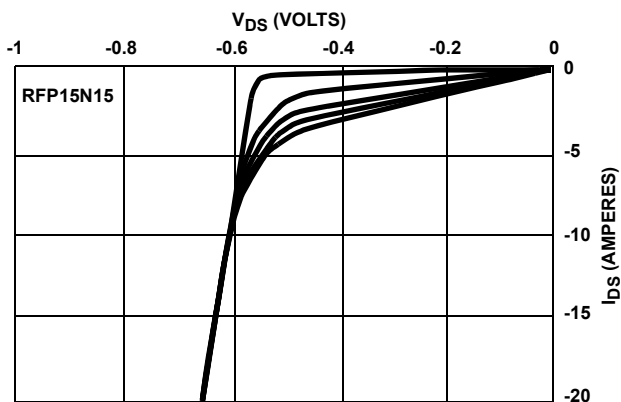


FIGURE 8. THIRD-QUADRANT DRAIN CURRENT VS DRAIN VOLTAGE WITH CONSTANT POSITIVE GATE VOLTAGE (CALCULATED)

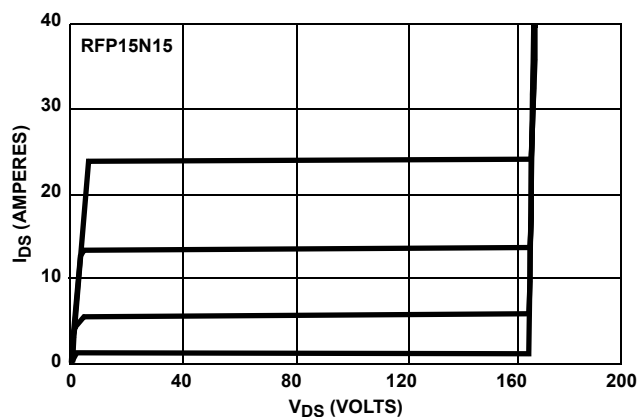


FIGURE 9. FIRST-QUADRANT DRAIN CURRENT VS DRAIN VOLTAGE,  $V_{GS} = \text{CONSTANT}$ . NOTE AVALANCHE BREAKDOWN (CALCULATED)

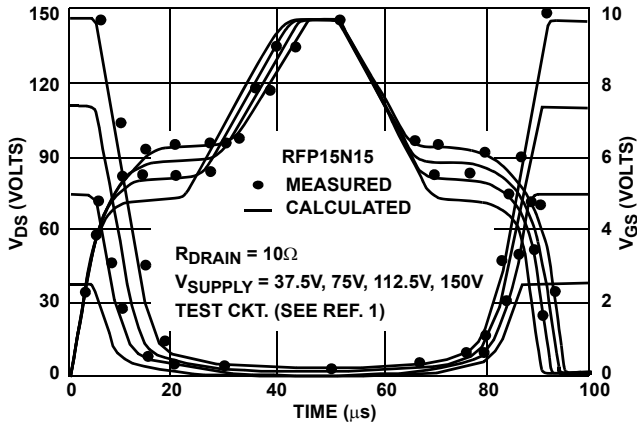


FIGURE 10. DRAIN AND GATE VOLTAGE VS TIME FOR CONSTANT GATE CIRCUIT - MEASURED CURVES VS CALCULATED POINTS

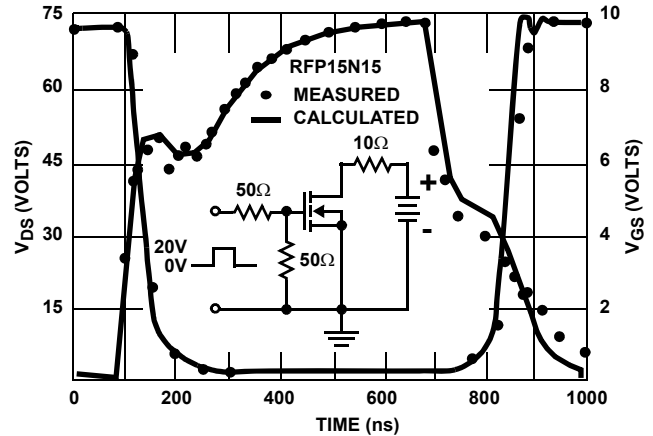


FIGURE 11. DRAIN AND GATE VOLTAGE VS TIME FOR STANDARD SWITCHING CIRCUIT - MEASURED CURVES VS CALCULATED POINTS

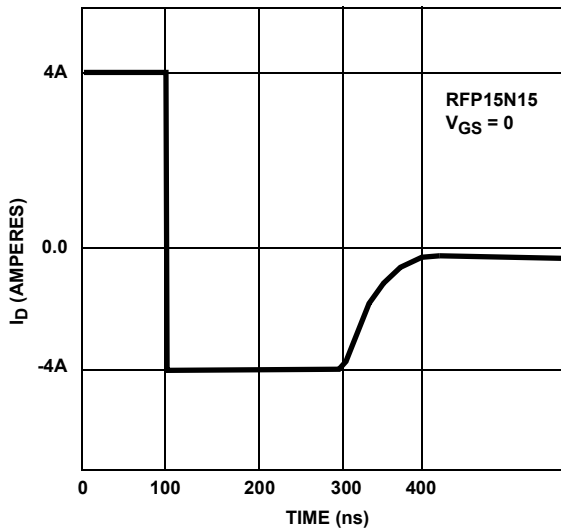


FIGURE 12. THIRD-QUADRANT DIODE - RECOVERY VS TIME CURVE (CALCULATED)

## Conclusion

An equivalent-circuit model for power-MOSFETs, that is suitable for use with the SPICE CAD program, has been demonstrated. The model is compatible with all versions of SPICE presently available without modification to the program's internal code. The model addresses static and dynamic behavior of first and third-quadrant operation, including avalanche breakdown, and is empirical in nature. All necessary input parameters may be inferred from data sheets or simple terminal measurements.

Excellent agreement has been obtained between measured and simulated results.

## References

- [1] Wheatley Jr., C. F. and Ronan Jr., H. R., "Switching Waveforms of the L<sup>2</sup>FET: A 5-Volt Gate-Drive Power MOSFET," Power Electronic Specialists Conference Record, June 1984, p. 238
- [2] Ronan Jr., H. R. and Wheatley Jr., C. F., "Power MOSFET Switching Waveforms: A New Insight," Proceedings of Powercon II, April 1984, p. C-3
- [3] Nienhaus, H. A., Bowers, J. C., and Herren Jr., P. C., "A High Power MOSFET Computer Model," Power Conversion International, January 1982, p 65

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