GreenPAK Macro Circuit RS flip flop with Reset priority

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Introduction

RS flip flop or SR flip flop — is a circuit that keeps its previous state when both inputs are LOW, and changes its state when one of the inputs (Set or Reset) is HIGH.

If Set input goes HIGH, Output will go HIGH, and if Reset goes HIGH the Output will go LOW. In a classic cross coupled logic gate circuit, the output is undetermined when both inputs are HIGH. The design presented in this application note assigns priority to RS to solve that limitation.

RS flip flop circuit design

The RS flip flop circuit is presented in Figure1. In this realization it consists of two latch blocks, outputs of which are connected with the respective opposite blocks' CK inputs. Set and Reset signals are input on the latches' D input. PINs and latches properties are shown in Figure 2 and Figure 3.

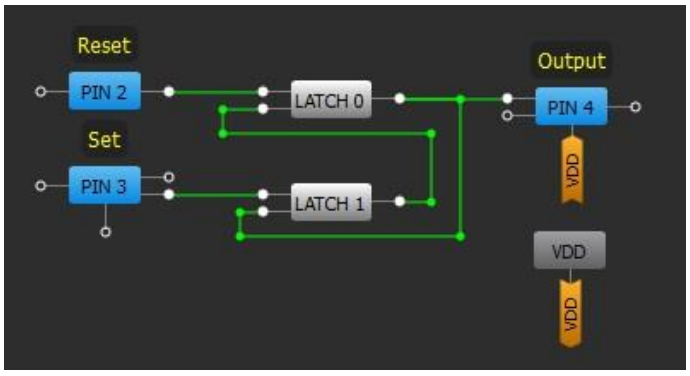

Figure 1. RS flip flop circuit design

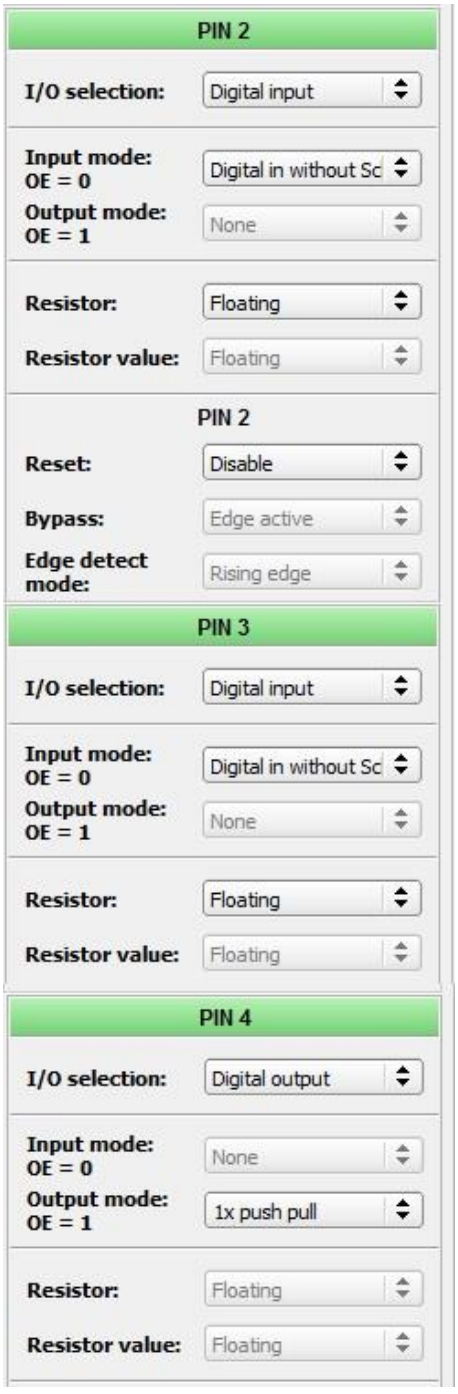

Figure 2. PINs configuration

Figure 3. Latches configuration

RS flip flop circuit analysis

When a pulse comes from Set, the LATCH1 is not latched, because latches' outputs are inverted and LATCH0 initial polarity is HIGH. At this moment LATCH1 Q becomes LOW and LATCH0 Q – HIGH.

When a pulse comes from Reset, LATCH0 Q goes LOW and LATCH1 Q – HIGH, that provides reset function.

In this design, Reset input has higher priority than Set, which means that regardless of which signal comes first: Set or Reset, at the moment when these both inputs are HIGH Output will always stay LOW (See figure 4).

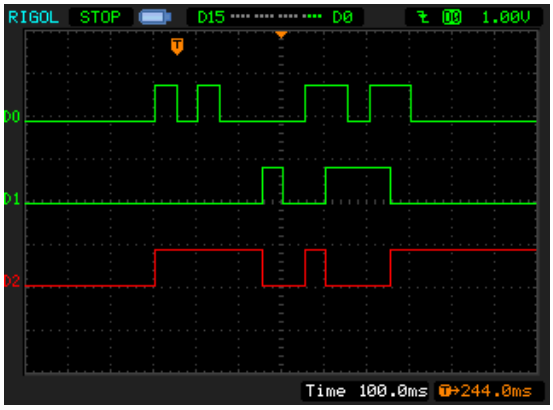

Figure 4. RS flip flop functional diagram

D0 –PIN#3 (Set); D1 – PIN#2 (Reset); D2 – PIN#4 (Output)

Conclusion

Using only two Latch blocks of GreenPAK silicon it is possible to create a circuit that functions as a RS flip flop with priority. This circuit is apt to be most useful in complicated designs where state machines are used.

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