[Notes]
RX Family
RSCI Module Firmware Integration Technology,
RX Driver Package

R20TS0766ES0100
Rev.1.00
Oct. 16, 2021

Outline

When using the products in the title, note the following point.

1. Notes on default Transfer Data Direction in asynchronous mode

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1.1 Applicable Products

(1) RSCI module Firmware Integration Technology (RSCI FIT module)

The applicable revision numbers and document numbers are as follows.

Table 1.1 RSCI FIT module applicable products

Revision number of the RSCI FIT module	Document number
Rev.1.00	R01AN5759ES0100

(2) RX Driver Package

The RSCI FIT module in (1) is also included in the RX Driver Package.
The product names and revision numbers of the applicable RX Driver Package and the revision numbers of the RSCI FIT module are as follows.

Table 1.2 Products which include the RSCI FIT module

RX Driver Package product name	RX Driver Package revision number	Document number	Revision number of the included RSCI FIT module
RX Family RX Driver Package Ver.1.31	Rev.1.31	R01AN5975xx0131	Rev.1.00

1.2 Applicable Devices

RX671 groups

1.3 Details and Conditions

In asynchronous mode initialization, R_RSCI_Open() will initialize Transfer Data Direction Select bit (DDIR) to '0' where MSB of data will be transmitted/received first. If the other connected device (such as Personal Computer) expects LSB data to be received/ transmitted first, then the data received will be incorrect at both ends.

The following illustrates how this happens:

R_RSCI_Open() will be called to initialize that required channel. Below shows the asynchronous mode code snippets :

```
rsci_err_t R_RSCI_Open(uint8_t const chan, rsci_mode_t const mode, rsci_cfg_t * const p_cfg,
                       void (* const p_callback)(void *p_args), rsci_hdl_t * const    p_hdl)
{
    …
    rsci_init_register(g_rsci_handles[chan]);
    …
    #if (RSCI_CFG_ASYNC_INCLUDED)
        /* Casting rsci_cfg_t type to rsci_uart_t type is valid */
        err = rsci_init_async(g_rsci_handles[chan], (rsci_uart_t *)p_cfg, &priority);
    #endif
    …
}
```

In rsci_init_register(), regardless of the value of hdl passed into this function, DDIR bit is always set to '0', where MSB of data will be transmitted/received first :

```
void rsci_init_register(rsci_hdl_t const hdl)
{
    …
    hdl->rom->regs->SCR3.BIT.DDIR = 0;
    …
}
```

1.4 Workaround

To set LSB to be transmitted/received first in asynchronous mode, make the following change:

Before modification

```
void rsci_init_register(rsci_hdl_t const hdl)
{
    …
    hdl->rom->regs->SCR3.BIT.DDIR = 0;
    …
}
```

After modification

```
void rsci_init_register(rsci_hdl_t const hdl)
{
    …
    hdl->rom->regs->SCR3.BIT.DDIR = 1;
    …
}
```

1.5 Schedule for Fixing the Problem

Change to LSB as default in asynchronous mode, will be fixed in Rev.1.10.

Revision History

Rev.	Date	Description	
		Page	Summary
1.00	Oct.16.21	-	First edition issued

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