# RL78/I1D
## Low Power Consuming Intermittent Operation of ADC Using DTC IAR


### Abstract

This application note explains low power consuming intermittent operation of ADC using DTC.


### Target Device

RL78/I1D

When using this application note with other Renesas MCUs, careful evaluation is recommended after making modifications to comply with the alternate MCU.

Contents

# 1. Specifications

This application note explains A/D conversion using the DTC and the A/D converter controlled by low power consuming operation, especially the STOP mode and SNOOZE mode.

The 8-bit interval timer (hereinafter referred to as 8-bit IT) is used to count periods of A/D conversion, P57 is applied to control the power supply (ON/OFF) of sensors, ELC is used to turn on OPAMP, the 12-bit interval timer (hereinafter called 12-bit IT) is used to count the stabilization wait time after the sensor is powered ON and DOC is used to judged of end of processing.

The A/D converter operates in the hardware trigger wait mode using the SNOOZE mode. As the hardware trigger, interrupts (INTIT) of the 12-bit interval timer are set.

The DTC uses two types of interrupts as activation factor; underflow interrupt of the 8-bit interval timer and A/D conversion end interrupt. The 8-bit interval timer underflow interrupt causes data transfer to the P5 register to start power supply to sensors, and transfers data to the ITMC register by chain transfer to start count of the 12-bit interval timer. The A/D conversion end interrupt transfers the ADCR register value to RAM, stops providing power supply to sensors by data transfer to the P5 register, transfers A/D conversion result to the DOC and judges the threshold value by the DOC. If above threshold value, releasing the STOP mode.

Table 1.1 shows peripheral functions used and their applications. Figure 1.1 shows an overview of operation. Figure 1.2 and Figure 1.3 illustrate the time charts.

**Table 1.1 Peripheral Functions Used and Their Applications**

| Peripheral function | Application |
|---|---|
| P137 | -Starts processing |
| 8-bit interval timer | - Counts periods of A/D conversion<br>- Functions as operational amplifier operation start trigger |
| DTC | Executes the following operations by 8-bit interval timer interrupts<br>- Sets high output to P57 (starts power supply to sensors)<br>- Starts count of the 12-bit interval timer (sensor stabilization wait time)<br>Executes the following operations by A/D conversion end interrupts<br>- Stores the A/D conversion result to RAM<br>- Sets low output to P57 (stops power supply to sensors)<br>- Sets the AWC bit again when the SNOOZE mode is shifted to STOP mode<br>- Stops the 12-bit interval timer count<br>- Transfers A/D conversion result to the DOC ( for determine releasing the STOP mode ) |
| P57 | Controls sensor power supply (ON/OFF) |
| 12-bit interval timer | Counts the stabilization wait time of sensors |
| ADC | Converts analog signal input levels of P17/ANI7 pins |
| Operational amplifiers (AMP0,1) | Amplify the analog input signal |
| Data operation circuit (DOC) | Determines to release the STOP mode<br>(releases the STOP mode by interrupts in DOC data addition mode) |

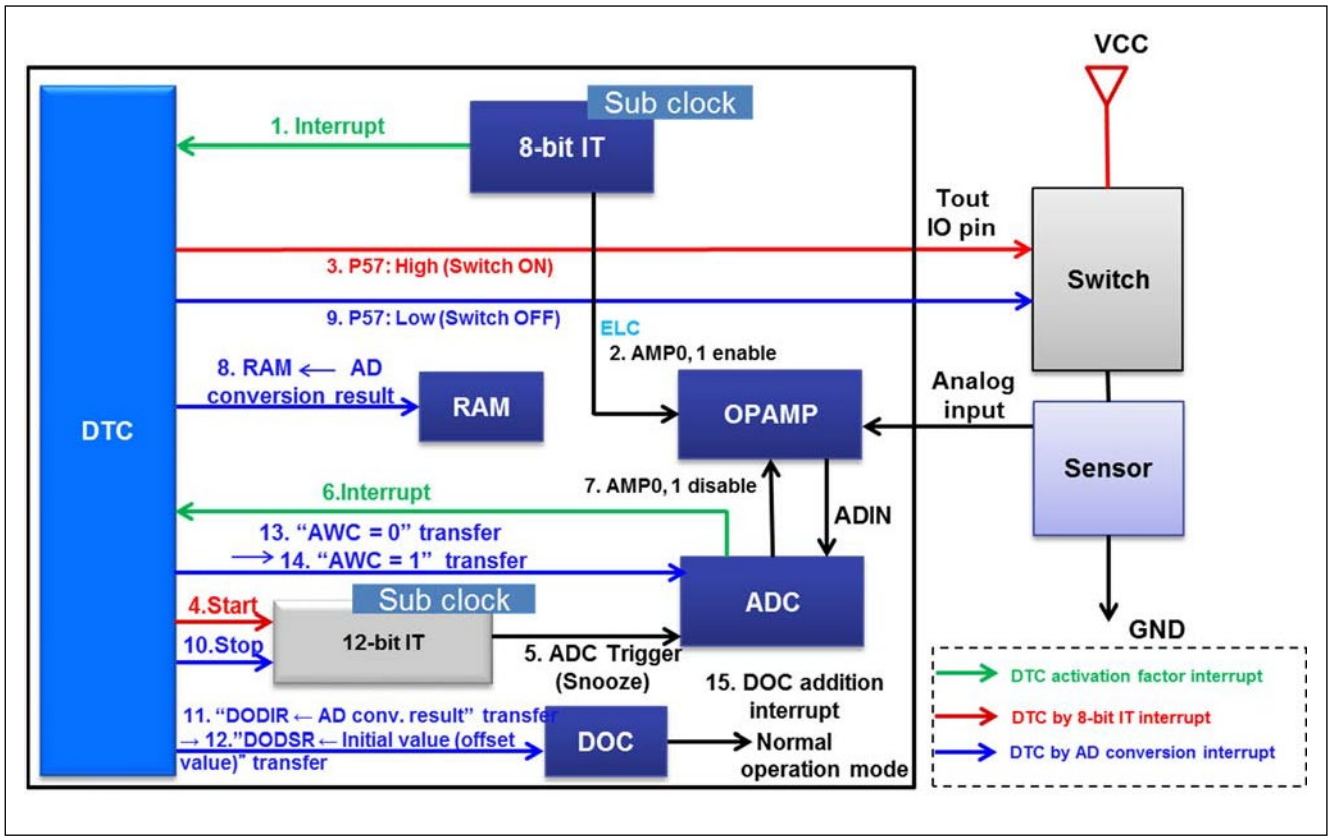


**Figure 1.1 Overview of Low Power Consuming Intermittent Operation of ADC Using DTC**

Note

1. In the above figure, when a low level is input, the switch is turned OFF (power supply to the sensor stops), and when a high level is input, the switch is turned ON (power supply to the sensor starts).

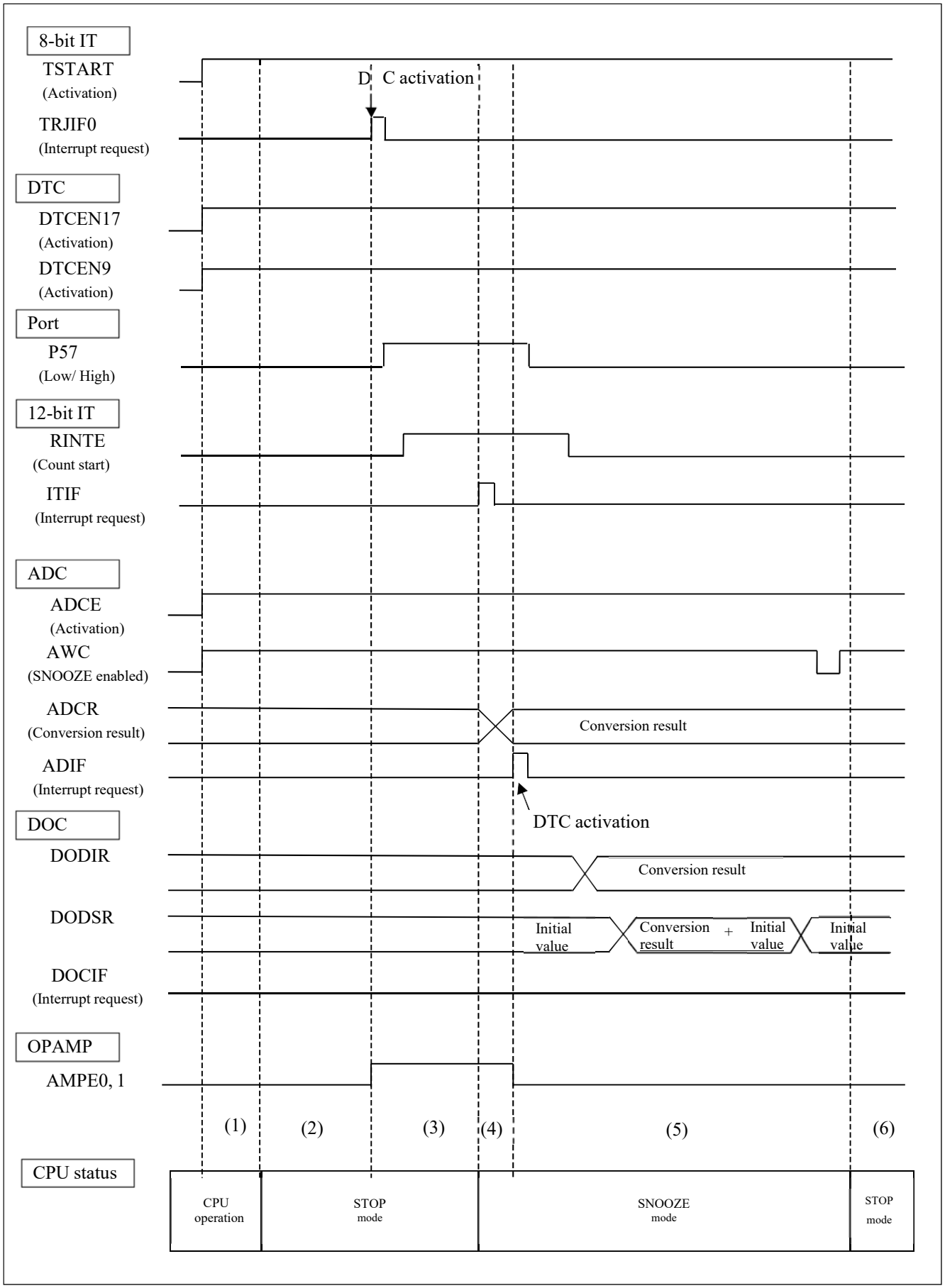


**Figure 1.2 Time Chart of Low Power Consuming Intermittent Operation of ADC Using DTC (STOP Mode Continued)**

1. Initial setting of the peripheral functions to be used is performed and count of the 8-bit interval timer is started.
2. When a low level is detected from P137, the CPU enters the STOP mode.
3. The operational amplifiers AMP0 and 1 are activated by an underflow interrupt of the 8-bit interval timer as trigger. At the same time, the DTC is activated and by transferring data to the P5 register, P57 is set to high output. By chain-transferring data to the ITMC register, count of the 12-bit interval timer is started.
4. The 12-bit interval timer interrupt (hardware trigger of the A/D converter) starts A/D conversion in the SNOOZE mode.
5. An A/D conversion end interrupt activates the DTC, and by transfers data to the P5 register and P57 is set to low output. By chain transfers, the 12-bit interval timer is set to be stopped. In addition, by transferring the A/D conversion result to the DOC and the AWC bit is set again.
6. When the DOC operation result is not larger than “FFFFH” upon the threshold value determination, a data operation circuit interrupt is not generated, and the mode is switched from the SNOOZE mode to the STOP mode.

After that, the procedures 3 to 6 are repeated.

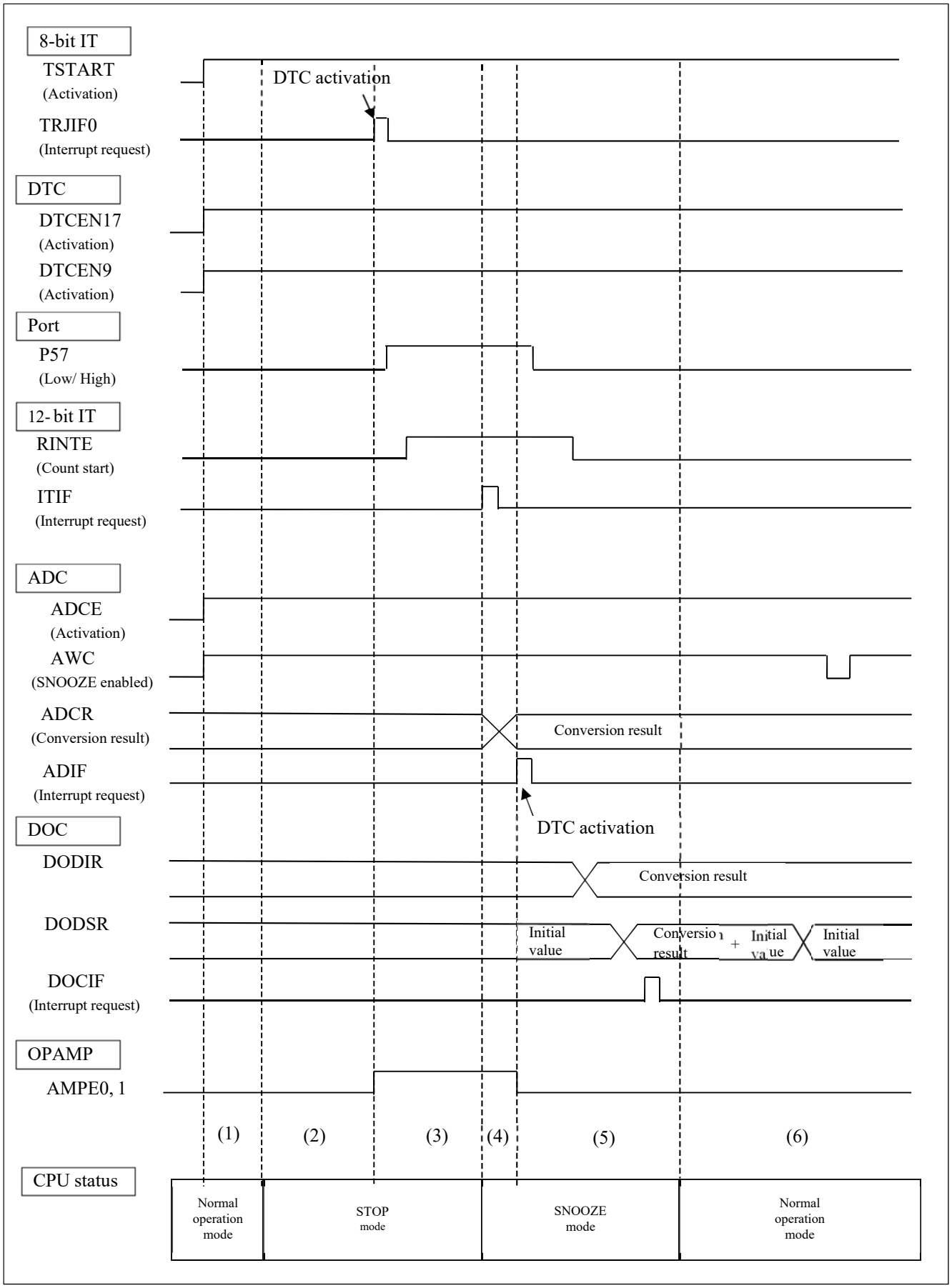


**Figure 1.3 Time Chart of Low Power Consuming Intermittent Operation of ADC Using DTC (STOP Mode Released)**

1. Initial setting of the peripheral functions to be used is performed and count of the 8-bit interval timer is started.
2. When a low level is detected from P137, the CPU enters the STOP mode.
3. The operational amplifiers AMP0 and 1 are activated by an underflow interrupt of the 8-bit interval timer as trigger. At the same time, the DTC is activated, and by transferring data to the P5 register, P57 is set to high output. By chain-transferring data to the ITMC register, count of the 12-bit interval timer is started.
4. The 12-bit interval timer interrupt (hardware trigger of the A/D converter) starts the A/D conversion in the SNOOZE mode.
5. An A/D conversion end interrupt activates the DTC, and by transfers data to the P5 register and P57 is set to low output. By chain transfers, the 12-bit interval timer is set to be stopped. In addition, by transferring the AD conversion result to the DOC, and the AWC bit is set again.
6. When the DOC operation result is larger than “FFFFH” upon the threshold value determination, a data operation circuit interrupt is generated.And the mode is switched from the SNOOZE mode to normal mode.
   Peripheral functions used for data operation circuit interrupt servicing are reset.

After that, the procedures 2 to 6 are repeated.

## 2. Operation Confirmation Conditions

The sample code accompanying this application note has been run and confirmed under the conditions below.

**Table 2.1 Operation Confirmation Conditions**

| Item | Description |
|---|---|
| Microcontroller used | RL78/I1D (R5F117GCG) |
| Operating frequency | ● High-speed on-chip oscillator clock: 24 MHz<br>● CPU/peripheral hardware clock: 24 MHz<br>● Subsystem clock: 32.768 KHz |
| Operating voltage | 3.3 V (operation possible from 3.1 to 3.6 V)<br>LVD operation (VLVI): Reset mode<br>(3.02 V at the rising edge or 2.96 V at the falling edge) |
| Integrated development environment (IAR) | IAR Systems<br>IAR Embedded Workbench for Renesas RL78 V4.21.3 |
| C compiler (IAR) | IAR Systems<br>IAR C/C++ Compiler for Renesas RL78 V4.21.3.2447 |
| Board used | RL78/I1D CPU board (RTE5117GC0TGB00000R) |

## 3. Related Application Notes

The application notes related to this document are shown below. Please refer to them as well.

RL78/G13 Initialization (R01AN0451E) Application Note

RL78/G13 A/D Converter (R01AN0452E) Application Note

RL78/G14 How to Use the DTC for the RL78/G14 (R01AN0861E) Application Note

RL78/G14 Transferring A/D Conversion Result Using the DTC (R01AN0863E) Application Note

RL78/G13 A/D Converter (SNOOZE Mode) (R01AN1464E) Application Note

RL78/I1D Low Power Consuming Intermittent Operation of ADC Using DTC (R01AN2231E) Application Note

# 4. Hardware

## 4.1 Hardware Example

Figure 4.1 shows hardware configuration used in this application note.

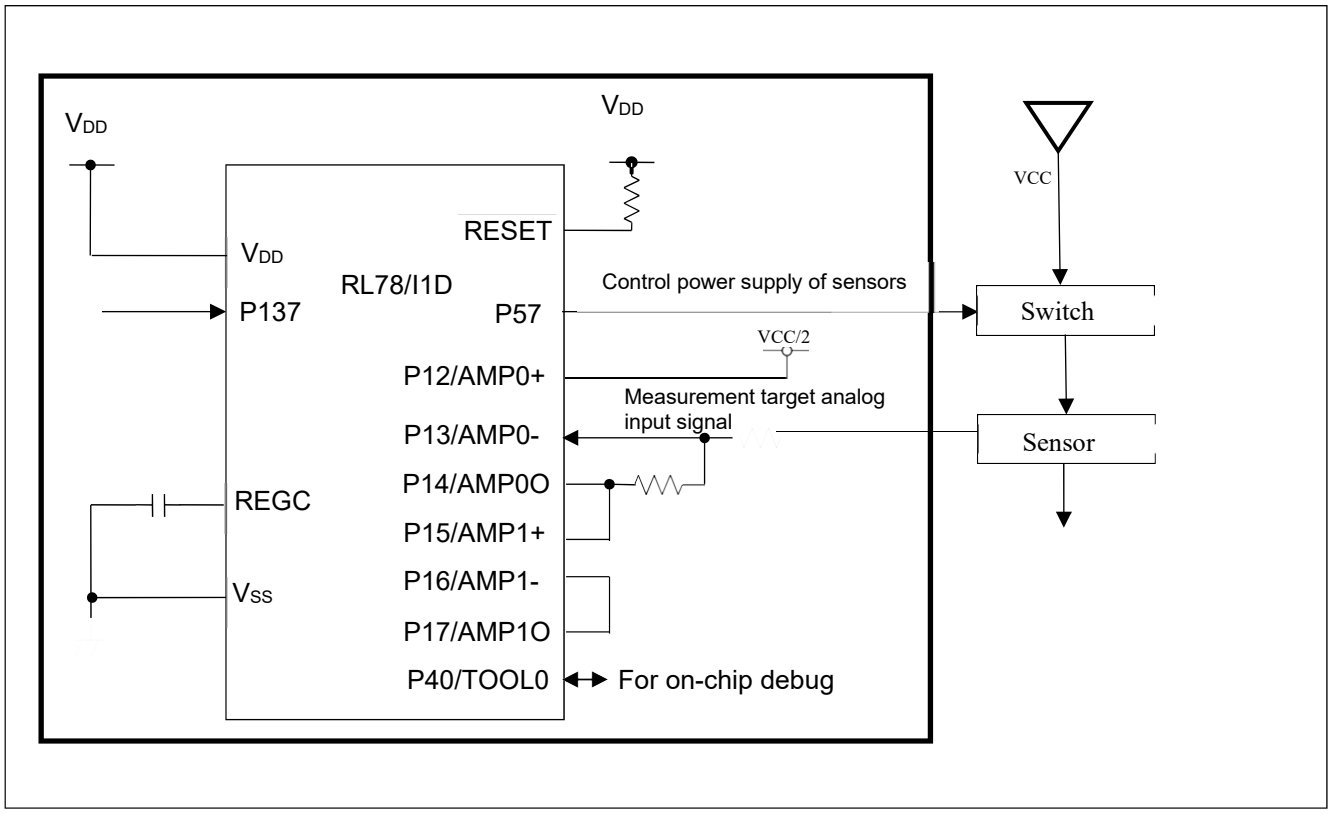


**Figure 4.1 Hardware Configuration Example**

Notes

1. The above figure is simplified to show an overview of the hardware connection. When designing application circuits, make sure to handle unused pins appropriately to satisfy the electrical characteristics (connect input only ports independently to either $V_{DD}$ or $V_{SS}$ via resistors).
2. Make sure to set $V_{DD}$ greater than the reset release voltage ($V_{LVI}$) specified by the LVD.

## 4.2 Pins Used

Table 4.1 lists the pins used and their functions.

**Table 4.1 Pins Used and Their Functions**

| Pin name | I/O | Function |
|---|---|---|
| P57 | Output | Sensor power supply control<br>High: sensor power supply ON<br>Low: sensor power supply OFF |
| P137 | Input | Switch input port (processing start) |
| P12/AMP0+ | Input | Operational amplifier 0 (+side) input |
| P13/AMP0- | Input | Operational amplifier 0 (-side) input |
| P14/AMP0O | Input | Operational amplifier 0 output |
| P15/AMP1+ | Input | Operational amplifier 1 (+side) input |
| P16/AMP1- | Input | Operational amplifier 1 (-side) input |
| P17/AMP1O (ANI7) | Input | Operational amplifier 1 output, A/D converter analog input port |

# 5. Software

## 5.1 Operation Overview

In this application note, A/D conversion is performed by using the DTC and the A/D converter controlled by low power consuming operation, especially the STOP mode and SNOOZE mode.

The 8-bit interval timer is used as activation trigger of the operational amplifier 1 and 0. It is also used to count periods of A/D conversion. P57 is applied to control the power supply (ON/OFF) of sensors. The 12-bit interval timer is used to count the stabilization wait time after the sensor power ON.

The A/D converter operates in the hardware trigger wait mode using the SNOOZE mode. As the hardware trigger, interrupts of the 12-bit interval timer (INTIT) are set.

The DTC uses two types of interrupts as activation factor; underflow interrupt of the 8-bit interval timer and A/D conversion end interrupt. The 8-bit interval timer underflow interrupt activates the operational amplifiers 0 and 1. At the same time, it causes data transfer to the P5 register by the DTC to start power supply to sensors, and transfers data to the ITMC register by chain transfer to start count of the 12-bit interval timer. The A/D conversion end interrupt stops the operational amplifier 0 and 1. Simultaneously, the conversion result is transferred to RAM by the DTC, and data is transferred to the P5 register by chain transfer to stop providing power supply to sensors. In addition, the 12-bit interval timer is stopped, the threshold value is determined by transferring AD conversion result to the DOC, and the AWC bit is reset.

The specific procedures are described below (1) to (20).

(1) Perform initial setting of the ports.

<Setting condition>

- Set P57 to low output and turn the sensor power supply OFF.

(2) Perform initial setting of the CPU.

<Setting conditions>

- Select the high-speed on-chip oscillator as the main system clock.
- Select the XT1 oscillator as the subsystem clock.

(3) Perform initial setting of the 12-bit interval timer.

<Setting condition>

- Set the interval time to 125 ms.

(4) Perform initial setting of the 8-bit interval timer.

<Setting conditions>

- Set the operation mode of the 8-bit interval timer to timer mode.
- Set the timer value to 1000 ms.

(5) Perform initial setting of the A/D converter.

<Setting conditions>

- Set the select mode in A/D conversion channel selection.
- Set the one-shot conversion mode as A/D conversion operation mode.
- Set the hardware trigger wait mode as A/D conversion start condition.
- Set the 12-bit interval timer interrupt signal (INTIT) as hardware trigger signal.
- Set P17/ANI7 pins to analog input.

(6) Perform initial setting of the operational amplifiers.

<Setting conditions>

- Set P12 to P17 to the analog mode.
- Set P12 to P17 to ‘input’.
- Enable wait for ELC.
- Set to the high-speed mode for operation mode.
- Select the ELC and A/D trigger mode for operational amplifier activation/stop trigger.
- Set the operational amplifier ELC trigger 0 as activation trigger of the operational amplifier units 0 and 1.

(7) Perform initial setting of the DTC.

<Setting conditions>

- Setting of DTCT0 (Transferring data at address 0xFFD00 to the P5 register)
  - Set the transfer source address: 0xFD00.
  - Set the transfer destination address: 0xFF05 (P5).
  - Select the 8-bit data size.
  - Enable chain transfers (DTCT1).
  - Set the 8-bit interval timer underflow as activation factor.
  - Set the number of DTC data transfers to once.
  - Set the repeat mode.

- Setting of DTCT1 (Transferring data at address 0xFFD04 to the ITMC register)
  - Set the transfer source address: 0xFD04.
  - Set the transfer destination address: 0xFF90(ITMC).
  - Select the 16-bit data size.
  - Disable chain transfers.
  - Set the number of DTC data transfers to once.
- Setting of DTCT2 (Transferring data of the ADCR register to the address 0xFFC00)
  - Set the transfer source address: 0xFF1E(ADCR).
  - Set the transfer destination address: 0xFC00.
  - Select the 16-bit data size.
  - Enable chain transfers (DTCT3).
  - Set the A/D conversion end as activation factor.
  - Set the number of DTC data transfers to 4 times.
  - Set the repeat mode.

- Setting of DTCT3 (Transferring data at address 0xFFD02 to the P5 register)
  - Set the transfer source address: 0xFD02.
  - Set the transfer destination address: 0xFF05(P5).
  - Select the 8-bit data size.
  - Enable chain transfers (DTCT4).
  - Set the number of DTC data transfers to 4 times.
- Setting of DTCT4 (Transferring data at address 0xFFD06 to the ITMC register)
  - Set the transfer source address: 0xFD06.
  - Set the transfer destination address: 0xFF90(ITMC).
  - Select the 16-bit data size.
  - Enable chain transfers (DTCT5).
  - Set the number of DTC data transfers to 4 times.

- Setting of DTCT5 (Transferring data of the ADCR register to the DODIR register)
  - Set the transfer source address: 0xFF1E(ADCR).
  - Set the transfer destination address: 0x0512(DODIR).
  - Select the 16-bit data size.
  - Enable chain transfers (DTCT6).
  - Set the number of DTC data transfers to 4 times.
- Setting of DTCT6 (Transferring data at address 0xFFD0C to the DODSR register)
  - Set the transfer source address: 0xFD0C.
  - Set the transfer destination address: 0x0514(DODSR).
  - Select the 16-bit data size.
  - Enable chain transfers (DTCT7).
  - Set the number of DTC data transfers to 4 times.
- Setting of DTCT7 (Transferring data at address 0xFFD08 to the ADM2 register)
  - Set the transfer source address: 0xFD08.
  - Set the transfer destination address: 0x0010(ADM2).
  - Select the 8-bit data size.
  - Enable chain transfers (DTCT8).
  - Set the number of DTC data transfers to 4 times.
- Setting of DTCT8 (Transferring data at address 0xFFD0A to the ADM2 register)
  - Set the transfer source address: 0xFD0A.
  - Set the transfer destination address: 0x0010(ADM2).
  - Select the 8-bit data size.
  - Disable chain transfers.
  - Set the number of DTC data transfers to 4 times.

(8) Perform initial setting of the ELC.

<Setting condition>

- Set the peripheral function to link in ELSELR10 (channel 00 of the 8-bit interval timer) to the operational amplifier 0 (the operational amplifier ELC trigger 0).

(9) Perform initial setting of the DOC.

<Setting conditions>

- Set the threshold value to determine the transition to the normal operation mode to the DODSR register as initial value.
- Enable the data operation circuit interrupt.
- Set to the data addition mode.

(10) Perform initial setting for main processing.

<Setting conditions>

- Set the variable g_dtc_gpio_p57_on to “0x 80” (P57 = High).
- Set the variable g_dtc_gpio_p57_off to “0x00” (P57 = Low).
- Set the variable g_dtc_it_start to the OR of the ITMC register (count value) and “0x8000U” (activation enabled).
- Set the variable g_dtc_it_stop to “0x0000U” (operation stopped).
- Set the variable g_dtc_adc_awc_clear to “0x00U” (AWC bit = 0).
- Set the variable g_dtc_adc_awc_set to “0x04U” (AWC bit =1).
- Set the variable g_dtc_doc_dodsr_value to the initial setting value of the DODSR register.
- Set the variable g_dtc_adc_adinput[0] to [3] to “0x0000”.

(11) Executes the following operations when a low level is detected from P137.

(12) Activate the DTC.

<Setting conditions>

- Set the DTCEN16 bit in the DTCEN1 register to “1” (Activation enabled).
- Set the DTCEN26 bit in the DTCEN2 register to “1” (Activation enabled).

(13) Set the A/D converter to SNOOZE mode in order to set the A/D conversion wait status.

- Set the ADCE bit in the ADM0 register to “1” (Enable A/D voltage comparator operation) to wait for A/D conversion.
- Set the AWC bit in the ADM2 register to “1” (The SNOOZE mode function is used.).

(14) Set the operational amplifier units 0 and 1 to enable to wait for the ELC.

<Setting condition>

- Set the bits AMPE0 and AMPE1 in the AMPC register to “1” (Wait for ELC is enabled).

(15) Start the 8-bit interval timer count.

<Setting condition>

- Set the TSTART00 bit in the TRTCR0 register to “1” (Count starts).

(16) The CPU shifts to the STOP mode.

(17) An 8-bit interval timer underflow interrupt is generated and the ELC activates the operational amplifiers 0 and 1. At the same time, the DTC is activated and starts data transfers. Chain transfer is enabled here, and the DTC performs the following two transfers.

- The DTC transfers the data at address 0xFFD00 (1 byte) to address 0xFFF05 (in the P5 register).
- The DTC transfers the data at address 0xFFD04 (2 bytes) to address 0xFFF90 (in the ITMC register).

(18) A 12-bit interval timer interrupt is generated and A/D conversion is started in the SNOOZE mode.

(19) An A/D conversion end interrupt is generated and the operational amplifiers 0 and 1 stop. At the same time, the DTC is activated and starts data transfers. Chain transfer is enabled here, and the DTC performs the following seven transfers.

- The DTC transfers the data at address 0xFFF1E (in the ADCR register) (2 bytes) to address 0xFFC00.
- The DTC transfers the data at address 0xFFD02 (1 byte) to address 0xFFF05 (in the P5 register).
- The DTC transfers the data at address 0xFFD06 (2 bytes) to address 0xFFF90 (in the ITMC register).
- The DTC transfers the data at address 0xFFF1E (in the ADCR register) (2 bytes) to address 0xF0512 (in the DODIR register).
- The DTC transfers the data at address 0xFFD0C (2 bytes) to address 0xF0514 (in the DODSR register).
- The DTC transfers the data at address 0xFFD08 (1 byte) to address 0xF0010 (in the ADM2 register).
- The DTC transfers the data at address 0xFFD0A (1 byte) to address 0xF0010 (in the ADM2 register).

(20) In case that an overflow occurs in the result of addition with the DODSR register when the data is transferred to the DODIR register, the operation mode returns to the normal operation mode and the procedure goes back to (11) after a data operation circuit interrupt is generated.
Without the overflow, the operation mode returns to the STOP mode and the procedure goes back to (16) after the DTC transfers the data.

Note

1. For notes on using devices, refer to the RL78/I1D User's Manual: Hardware.

## 5.2 Option Byte Settings

Table 5.1 lists the option byte settings.

**Table 5.1 Option Byte Settings**

| Address | Setting value | Contents |
|---|---|---|
| 000C0H/010C0H | 11101111B | Stops the watchdog timer<br>(Counting is stopped when a reset is released.) |
| 000C1H/010C1H | 01110111B | Sets the LVD in reset mode<br>Detection voltage: 3.02 V at the rising edge, 2.96 V at the falling edge |
| 000C2H/010C2H | 11100000B | Sets the HOCO clock to 24 MHz in HS mode. |
| 000C3H/010C3H | 10000100B | Enables on-chip debugging<br>Erases data of flash memory in case of failures in authenticating on-chip debug security ID. |

## 5.3 Constant

Table 5.2 lists the constant used in the sample code.

**Table 5.2 Constant Used in the Sample Code**

| Constant name | Setting value | Content |
|---|---|---|
| R_DOC_OFFSET | 0xF482 | Initial setting value of the data operation circuit |

## 5.4 Variables

Table 5.3 lists the global variables.

**Table 5.3 Global Variables**

| Type | Variable Name | Contents | Function Used |
|---|---|---|---|
| uint8_t | g_dtc_gpio_p57_on | Setting value of P57 (High) | main () |
| uint8_t | g_dtc_gpio_p57_off | Setting value of P57 (Low) | main () |
| uint16_t | g_dtc_it_start | Enables activation of the 12-bit interval timer | main () |
| uint16_t | g_dtc_it_stop | Stops operation of the 12-bit interval timer | main () |
| uint8_t | g_dtc_adc_awc_clear | Setting value to release the SNOOZE mode function | main () |
| uint8_t | g_dtc_adc_awc_set | Setting value to use the SNOOZE mode function | main () |
| uint16_t | g_dtc_doc_dodsr_value | Threshold value to transit to normal mode (Data operation circuit offset value) | main () |
| uint16_t | g_dtc_adc_adinput[5] | Result value of A/D conversion end | R_MAIN_UserInit() |

## 5.5 Functions

Table 5.4 lists functions.

**Table 5.4 List of Functions**

| Function name | Outline |
|---|---|
| hdwinit | Initial setting |
| R_Systeminit | Initial setting of the peripheral functions |
| R_CGC_Create | Initial setting of the CPU |
| R_PORT_Create | Initial setting of the ports |
| R_ADC_Create | Initial setting of the A/D converter |
| R_IT_Create | Initial setting of the 12-bit interval timer |
| R_IT8Bit0_Channel0_Create | Initial setting of the 8-bit interval timer |
| R_DTC_Create | Initial setting of the DTC |
| R_ELC_Create | Initial setting of the ELC |
| R_DOC_Create | Initial setting of the DOC |
| R_OPAMP_Create | Initial setting of the operational amplifiers |
| main | Main processing |
| R_MAIN_UserInit | Main initial setting |
| R_DTCD0_Start | DTC0 activation |
| R_DTCD2_Start | DTC2 activation |
| R_ADC_Set_SnoozeOn | A/D converter’s SNOOZE function start |
| R_ADC_Set_OperationOn | A/D voltage comparator operation start |
| R_IT8BIT0_CHANNEL0_Start | 8-bit interval timer count start |
| R_ADC_Set_SnoozeOff | A/D converter’s SNOOZE function stop |
| r_doc_interrupt | Data operation circuit interrupt servicing |
| R_ADC_Set_OperationOff | A/D conversion disabling |
| R_DTCD0_Stop | DTC0 stop |
| R_DTCD2_Stop | DTC2 stop |
| R_IT8BIT0_CHANNEL0_Stop | 8-bit interval timer count stop |
| R_OPAMP0_Start | Operational amplifier 0 operation start |
| R_OPAMP1_Start | Operational amplifier 1 operation start |
| R_DOC_ClearFlag | Data operation circuit flag clear |

## 5.6 Function Specifications

This part describes function specifications of the sample code.

[Function name] hdwinit

| | |
|---|---|
| Outline | Initial setting |
| Header | None |
| Declaration | void hdwinit(void) |
| Description | This function is used for initial setting of peripheral functions. |
| Arguments | None |
| Return value | None |
| Remarks | None |

[Function name] R_Systeminit

| | |
|---|---|
| Outline | Initial setting of the peripheral functions |
| Header | None |
| Declaration | void R_Systeminit(void) |
| Description | This function is used for initial setting of peripheral functions used in this application note. |
| Arguments | None |
| Return value | None |
| Remarks | None |

[Function name] R_PORT_Create

| | |
|---|---|
| Outline | Initial setting of the ports |
| Header | r_cg_port.h |
| Declaration | void R_PORT_Create(void) |
| Description | This function is used for initial setting of ports. |
| Arguments | None |
| Return value | None |
| Remarks | None |

[Function name] R_CGC_Create

| | |
|---|---|
| Outline | Initial setting of the CPU |
| Header | r_cg_cgc.h |
| Declaration | void R_CGC_Create(void) |
| Description | This function is used for initial setting of the CPU. |
| Arguments | None |
| Return value | None |
| Remarks | None |

[Function name] R_ADC_Create

| | |
|---|---|
| Outline | Initial setting of the A/D converter |
| Header | r_cg_adc.h |
| Declaration | void R_ADC_Create(void) |
| Description | This function is used for initial setting to use the A/D converter in the hardware trigger wait mode (select mode, one-shot conversion mode). |
| Arguments | None |
| Return value | None |
| Remarks | None |

[Function name] R_IT_Create

| | |
|---|---|
| Outline | Initial setting of the 12-bit interval timer |
| Header | r_cg_it.h |
| Declaration | void R_IT_Create(void) |
| Description | This function is used for initial setting of the 12-bit interval timer. |
| Arguments | None |
| Return value | None |
| Remarks | None |

[Function name] R_IT8Bit0_Channel0_Create

| | |
|---|---|
| Outline | Initial setting of the 8-bit interval timer |
| Header | r_cg_it8bit.h |
| Declaration | void R_IT8Bit0_Channel0_Create (void) |
| Description | This function is used for initial setting of the 8-bit timer in timer mode. |
| Arguments | None |
| Return value | None |
| Remarks | None |

[Function name] R_DTC_Create

| | |
|---|---|
| Outline | Initial setting of the DTC |
| Header | r_cg_dtc.h |
| Declaration | void R_DTC_Create(void) |
| Description | This function is used for initial setting of the DTC. |
| Arguments | None |
| Return value | None |
| Remarks | None |

[Function name] R_ELC_Create

| | |
|---|---|
| Outline | Initial setting of the ELC |
| Header | r_cg_elc.h |
| Declaration | void R_ELC_Create (void) |
| Description | This function is used for initial setting of the ELC. |
| Arguments | None |
| Return value | None |
| Remarks | None |

[Function name] R_DOC_Create

| | |
|---|---|
| Outline | Initial setting of the DOC |
| Header | r_cg_doc.h |
| Declaration | void R_DOC_Create (void) |
| Description | This function is used for initial setting of the DOC. |
| Arguments | None |
| Return value | None |
| Remarks | None |

[Function name] R_OPAMP_Create

| | |
|---|---|
| Outline | Initial setting of the operational amplifiers |
| Header | r_cg_opamp.h |
| Declaration | void R_OPAMP_Create (void) |
| Description | This function is used for initial setting of the operational amplifiers. |
| Arguments | None |
| Return value | None |
| Remarks | None |

[Function name] main

| | |
|---|---|
| Outline | Main processing |
| Header | None |
| Declaration | void main(void) |
| Description | This function is used for main processing. |
| Arguments | None |
| Return value | None |
| Remarks | None |

[Function name] R_MAIN_UserInit

| | |
|---|---|
| Outline | Main initial setting |
| Header | None |
| Declaration | void R_MAIN_UserInit(void) |
| Description | This function is used for main initial setting. |
| Arguments | None |
| Return value | None |
| Remarks | None |

[Function name] R_DTCD0_Start

| | |
|---|---|
| Outline | DTC0 activation |
| Header | r_cg_dtc.h |
| Declaration | void R_DTCD0_Start(void) |
| Description | This function is used for setting to enable DTC0 activation. |
| Arguments | None |
| Return value | None |
| Remarks | None |

[Function name] R_DTCD2_Start

| | |
|---|---|
| Outline | DTC2 activation |
| Header | r_cg_dtc.h |
| Declaration | void R_DTCD2_Start(void) |
| Description | This function is used for setting to enable DTC2 activation. |
| Arguments | None |
| Return value | None |
| Remarks | None |

[Function name] R_ADC_Set_SnoozeOn

| | |
|---|---|
| Outline | A/D converter's SNOOZE function start |
| Header | r_cg_adc.h |
| Declaration | void R_ADC_Set_SnoozeOn(void) |
| Description | This function is used for setting to start the SNOOZE mode function of the A/D converter. |
| Arguments | None |
| Return value | None |
| Remarks | None |

[Function name] R_ADC_Set_OperationOn

| | |
|---|---|
| Outline | A/D voltage comparator operation start |
| Header | r_cg_adc.h |
| Declaration | void R_ADC_Set_OperationOn (void) |
| Description | This function is used for setting to start A/D conversion. |
| Arguments | None |
| Return value | None |
| Remarks | None |

[Function name] R_IT8BIT0_CHANNEL0_Start

| | |
|---|---|
| Outline | 8-bit interval timer count start |
| Header | r_cg_it8bit.h |
| Declaration | void R_TMR_RJ0_Start (void) |
| Description | This function is used for setting to enable activation of the 8-bit interval timer. |
| Arguments | None |
| Return value | None |
| Remarks | None |

[Function name] r_doc_interrupt

| | |
|---|---|
| Outline | Data operation circuit interrupt servicing |
| Header | r_cg_doc.h |
| Declaration | void r_doc_interrupt(void) |
| Description | This function is used to initialize the peripheral functions when data operation circuit interrupts are generated. |
| Arguments | None |
| Return value | None |
| Remarks | None |

[Function name] R_ADC_Set_SnoozeOff

| | |
|---|---|
| Outline | A/D converter’s SNOOZE function stop |
| Header | r_cg_adc.h |
| Declaration | void R_ADC_Set_SnoozeOff(void) |
| Description | This function is used for setting to stop the SNOOZE mode of the A/D converter. |
| Arguments | None |
| Return value | None |
| Remarks | None |

[Function name] R_ADC_Set_OperationOff

| | |
|---|---|
| Outline | A/D conversion disabling |
| Header | r_cg_adc.h |
| Declaration | void R_ADC_Set_OperationOff (void) |
| Description | This function is used to disable A/D conversion. |
| Arguments | None |
| Return value | None |
| Remarks | None |

[Function name] R_DTCD0_Stop

| | |
|---|---|
| Outline | DTC0 stop |
| Header | r_cg_dtc.h |
| Declaration | void R_DTCD0_Stop (void) |
| Description | This function is used for setting to stop the DTC0. |
| Arguments | None |
| Return value | None |
| Remarks | None |

[Function name] R_DTCD2_Stop

| | |
|---|---|
| Outline | DTC2 stop |
| Header | r_cg_dtc.h |
| Declaration | void R_DTCD2_Stop (void) |
| Description | This function is used for setting to stop the DTC2. |
| Arguments | None |
| Return value | None |
| Remarks | None |

[Function name] R_IT8BIT0_CHANNEL0_Stop

| | |
|---|---|
| Outline | 8-bit interval timer count stop |
| Header | r_cg_it8bit.h |
| Declaration | void R_IT8BIT0_CHANNEL0_Stop (void) |
| Description | This function is used to stop the 8-bit interval timer. |
| Arguments | None |
| Return value | None |
| Remarks | None |

[Function name] R_DOC_ClearFlag

| | |
|---|---|
| Outline | Data operation circuit flag clear |
| Header | r_cg_doc.h |
| Declaration | void R_ R_DOC_ClearFlag (void) |
| Description | This function is used to clear the data operation circuit flag (the DOPCF bit). |
| Arguments | None |
| Return value | None |
| Remarks | None |

## 5.7 Flowcharts

Figure 5.1 shows an overall flow of the sample code.

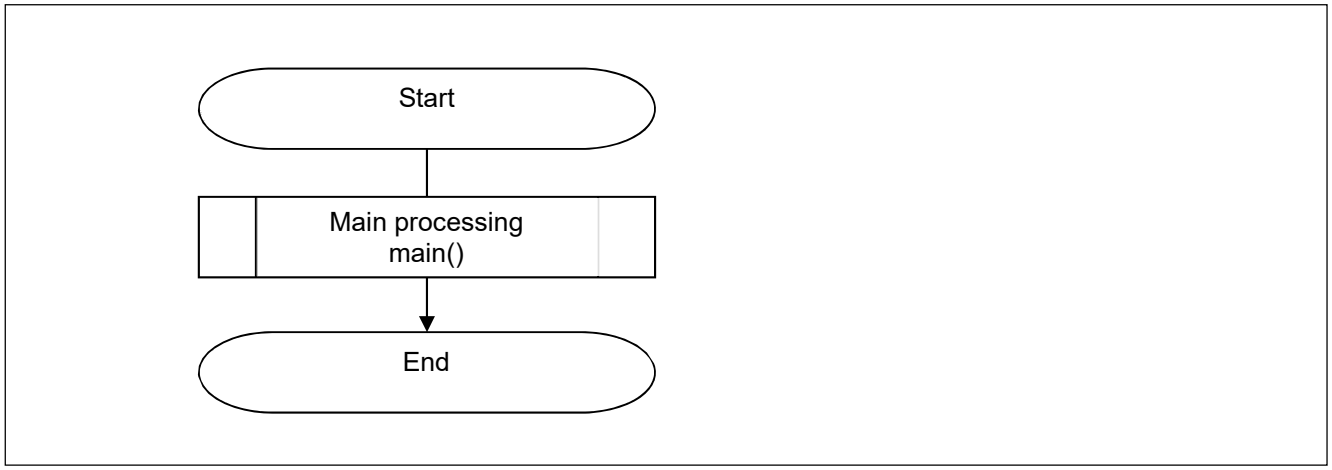


**Figure 5.1 Overall Flow**

### 5.7.1 Initialization

Figure 5.2 is a flowchart for initial setting.

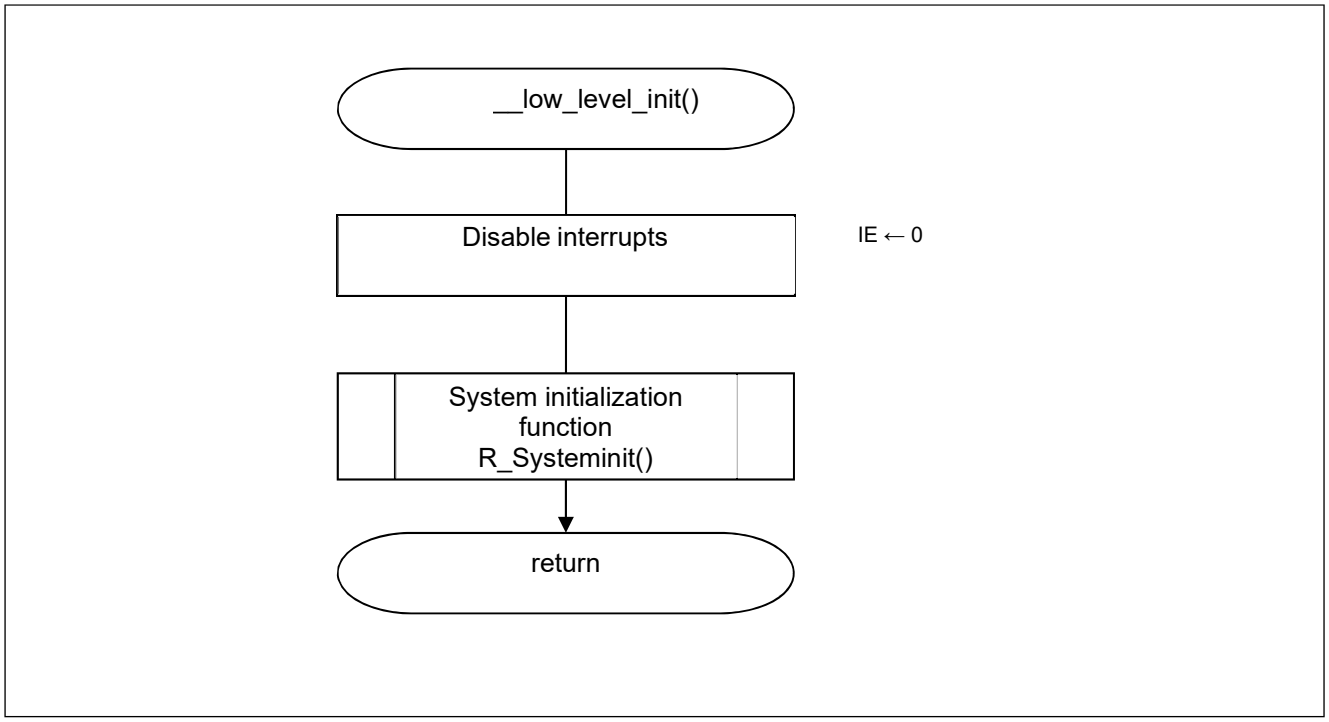


**Figure 5.2 Initial Setting**

### 5.7.2 Peripheral Function Initialization

Figure 5.3 shows a flowchart of initial setting of peripheral functions.

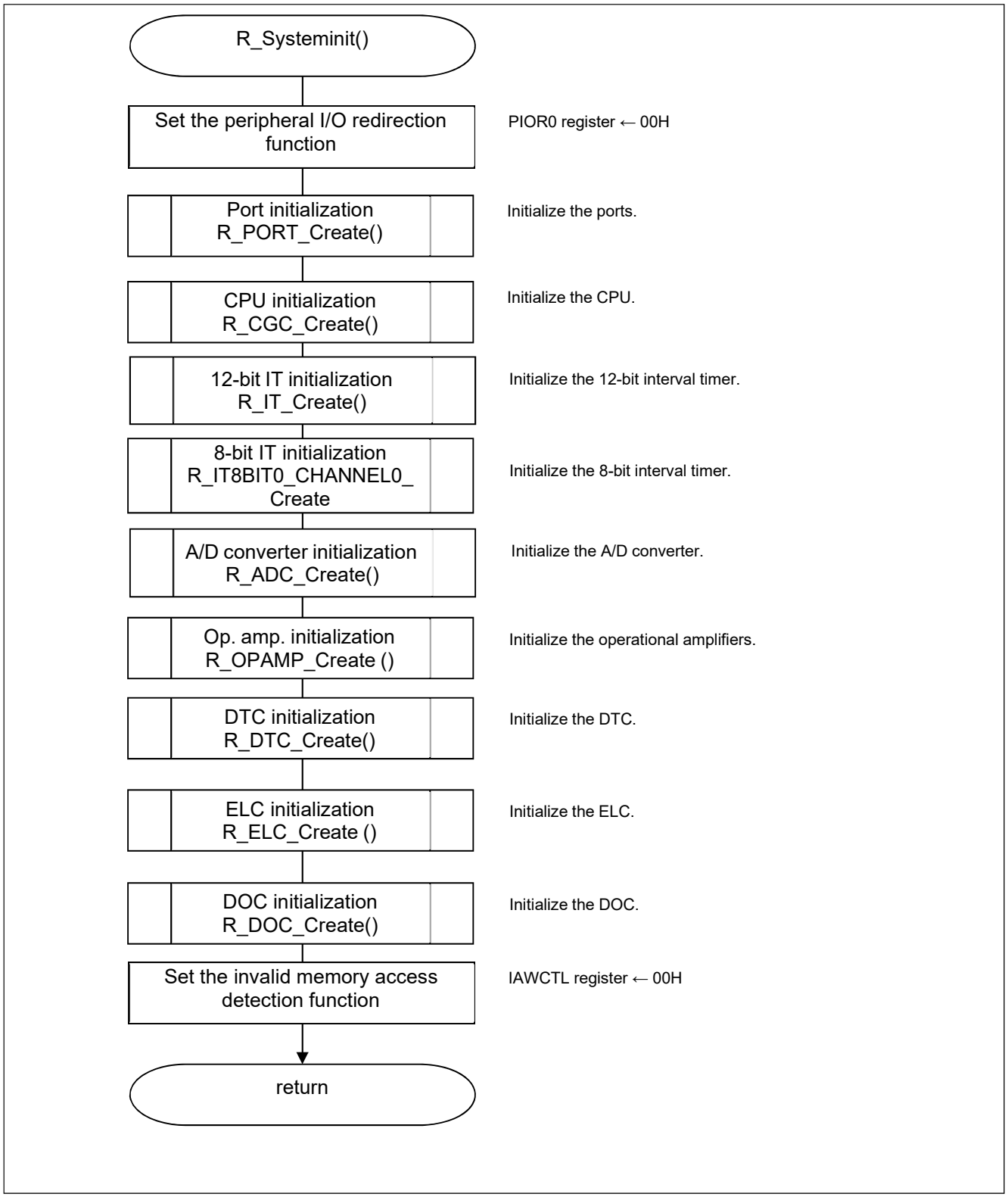


**Figure 5.3 Initial Setting of the Peripheral Functions**

### 5.7.3 Port Initialization

Figure 5.4 is a flowchart for initial setting of ports.

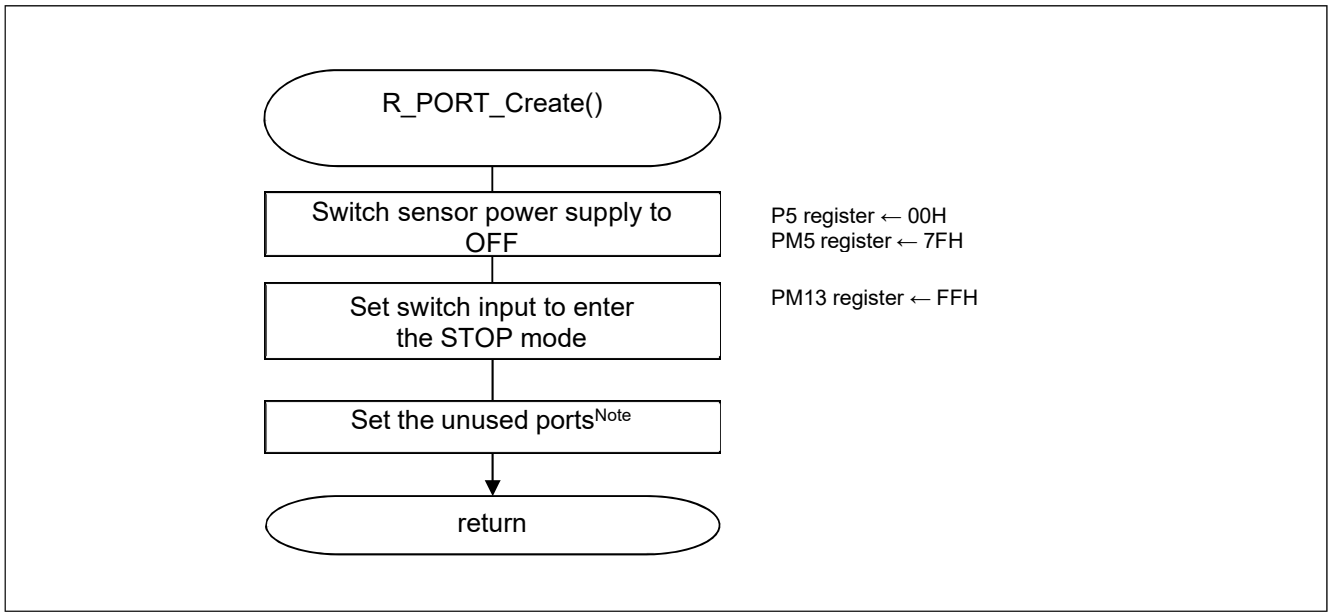


**Figure 5.4 Initial Setting of the Ports**

Note
1. Refer to the section entitled "Flowcharts" in RL78/G13 Initialization Application Note (R01AN0451E) for the configuration of the unused ports.

Caution
1. Provide proper treatment for unused pins so that their electrical specifications are met. Connect each of any unused input-only ports to VDD or VSS via a separate resistor.

### 5.7.4 CPU Initialization

Figure 5.5 is a flowchart for initial setting of the CPU.

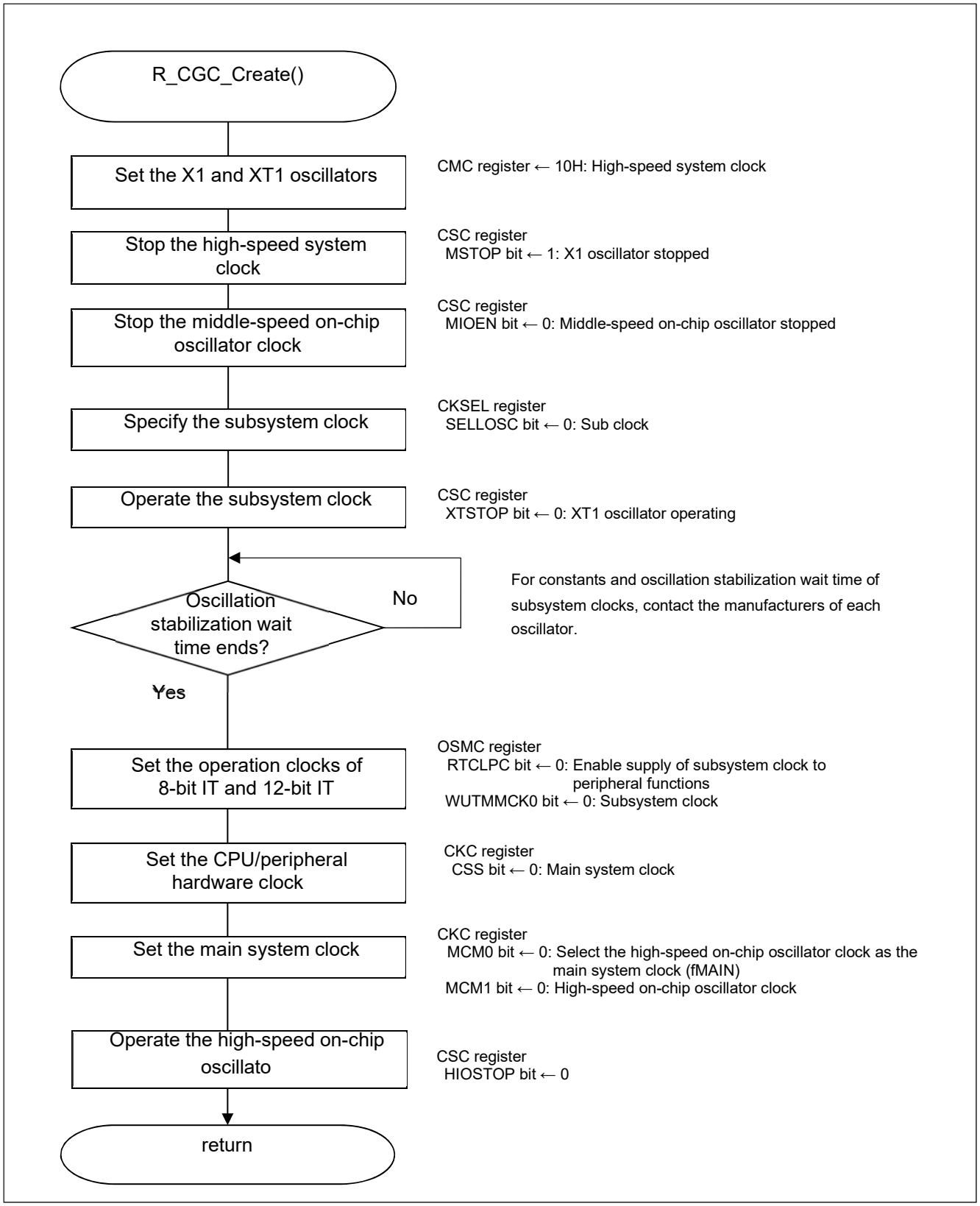


**Figure 5.5 Initial Setting of the CPU**

### X1 and XT1 oscillators setting

- Clock operation mode control register (CMC)

Set the high-speed system clock pin operation mode to input port mode.

Set the subsystem clock pin operation mode to low power consumption oscillation of the XT1 oscillator oscillation mode.

Symbol: CMC

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| EXCLK | OSCSEL | EXCLKS | OSCSELS | 0 | AMPHS1 | AMPHS0 | AMPH |
| **0** | **0** | **0** | **1** | x | **0** | **0** | **0** |

Bits 7 and 6

| EXCLK | OSCSEL | High-speed system clock pin operation mode | X1/P121 pin | X2/EXCLK/P122 pin |
|---|---|---|---|---|
| **0** | **0** | **Input mode** | **Input port** | |
| 0 | 1 | X1 oscillation mode | Crystal/ceramic resonator connection | |
| 1 | 0 | Input port mode | Input port | |
| 1 | 1 | External clock input mode | Input port | Input port |

Bits 5 and 4

| EXCLKS | OSCSELS | Subsystem clock pin operation mode | XT1/P123 pin | XT2/EXCLKS/P124 pin |
|---|---|---|---|---|
| 0 | 0 | Input port mode | Input port | |
| **0** | **1** | **XT1 oscillation mode** | **Crystal resonator connection** | |
| 1 | 0 | Input port mode | Input port | |
| 1 | 1 | External clock input mode | Input port | External clock input |

Bits 2 and 1

| AMPHS1 | AMPHS0 | XT1 oscillator oscillation mode selection |
|---|---|---|
| **0** | **0** | **Low power consumption oscillation (default)** |
| 0 | 1 | Normal oscillation |
| 1 | 0 | Ultra-low power consumption oscillation |
| 1 | 1 | Setting prohibited |

Bit 0

| AMPH | Control of X1 clock oscillation frequency |
|---|---|
| 0 | 1 MHz ≤ fX ≤ 10 MHz |
| **1** | **10 MHz < fX ≤ 20 MHz** |

Clock operation control setting

- Clock operation status control register (CSC)
  Operate the XT1 oscillator and high-speed on-chip oscillator.
  Stop the X1 oscillator and middle-speed on-chip oscillator.

Symbol: CSC

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| MSTOP | XTSTOP | 0 | 0 | 0 | 0 | MIOEN | HIOSTOP |
| **1** | **0** | x | x | x | x | **0** | **0** |

Bit 7

| MSTOP | High-speed system clock operation control | | |
|---|---|---|---|
| | X1 oscillation mode | External clock input mode | Input port mode |
| 0 | X1 oscillator operating | External clock from EXCLK pin is valid | **Input port** |
| **1** | X1 oscillator stopped | External clock from EXCLK pin is invalid | |

Bit 6

| XTSTOP | Subsystem clock operation control | | |
|---|---|---|---|
| | XT1oscillation mode | External clock input mode | Input port mode |
| **0** | **XT1 oscillator operating** | External clock from EXCLKS pin is valid | Input port |
| 1 | XT1 oscillator stopped | External clock from EXCLKS pin is invalid | |

Bit 1

| MIOEN | Middle-speed on-chip oscillator clock operation control |
|---|---|
| **0** | **Middle-speed on-chip oscillator stopped** |
| 1 | Middle-speed on-chip oscillator operating |

Bit 0

| HIOSTOP | High-speed on-chip oscillator clock operation control |
|---|---|
| **0** | **High-speed on-chip oscillator operating** |
| 1 | High-speed on-chip oscillator stopped |

### Subsystem clock setting

- Subsystem clock select register (CKSEL)

Select the sub clock as the subsystem clock.

Symbol: CKSEL

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | SELLOSC |
| x | x | x | x | x | x | x | **0** |

Bit 0

| SELLOSC | Selection of sub clock/low-speed on-chip oscillator clock |
|---|---|
| **0** | **Sub clock** |
| 1 | Low-speed on-chip oscillator clock |

### Operation clock setting for 8-bit and 12-bit interval timers

- Subsystem clock supply mode control register (OSMC)

Enable supply of subsystem clock to peripheral functions in STOP mode.

Select the subsystem clock as operation clock of the 8-bit interval timer and 12-bit interval timer.

Symbol: OSMC

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| RTCLPC | 0 | 0 | WUTMMCK0 | 0 | 0 | 0 | 0 |
| **0** | x | x | **0** | x | x | x | x |

Bit 7

| RTCLPC | Setting in STOP mode or HALT mode while subsystem clock is selected as CPU clock |
|---|---|
| **0** | **Enables supply of subsystem clock to peripheral functions** |
| 1 | Stops supply of subsystem clock to peripheral functions other than the real-time clock, 12-bit interval timer, 8-bit interval timer, and clock output/buzzer output controller |

Bit 4

| WUTMMCK0 | Selection of operation clock for real-time clock, frequency measurement circuit, 12-bit interval timer, 8-bit interval timer, and clock output/buzzer output controller |
|---|---|
| **0** | **Subsystem clock** |
| 1 | Low-speed on-chip oscillator clock |

System clock control setting

- System clock control register (CKC)

Select the high-speed on-chip oscillator clock as the CPU/peripheral hardware clock.

Symbol: CKC

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| CLS | CSS | MCS | MCM0 | 0 | 0 | MCS1 | MCM1 |
| x | **0** | x | x | x | x | **0** | **0** |

Bit 6

| CSS | Selection of CPU/peripheral hardware clock (fCLK) |
|---|---|
| **0** | **Main system clock (fMAIN)** |
| 1 | Subsystem clock (fSUB) |

Bit 1

| MCM0 | Main system clock (fMAIN) operation control |
|---|---|
| **0** | **Selects the high-speed on-chip oscillator clock (fIH) as the main system clock (fMAIN)** |
| 1 | Selects the high-speed system clock (fMX) as the main system clock (fMAIN) |

Bit 0

| MCM1 | Main on-chip oscillator clock (fOCO) operation control |
|---|---|
| **0** | **High-speed on-chip oscillator clock** |
| 1 | Middle-speed on-chip oscillator clock |

### 5.7.5 12-bit Interval Timer Initialization

Figure 5.6 is a flow chart for initial setting of the 12-bit interval timer.

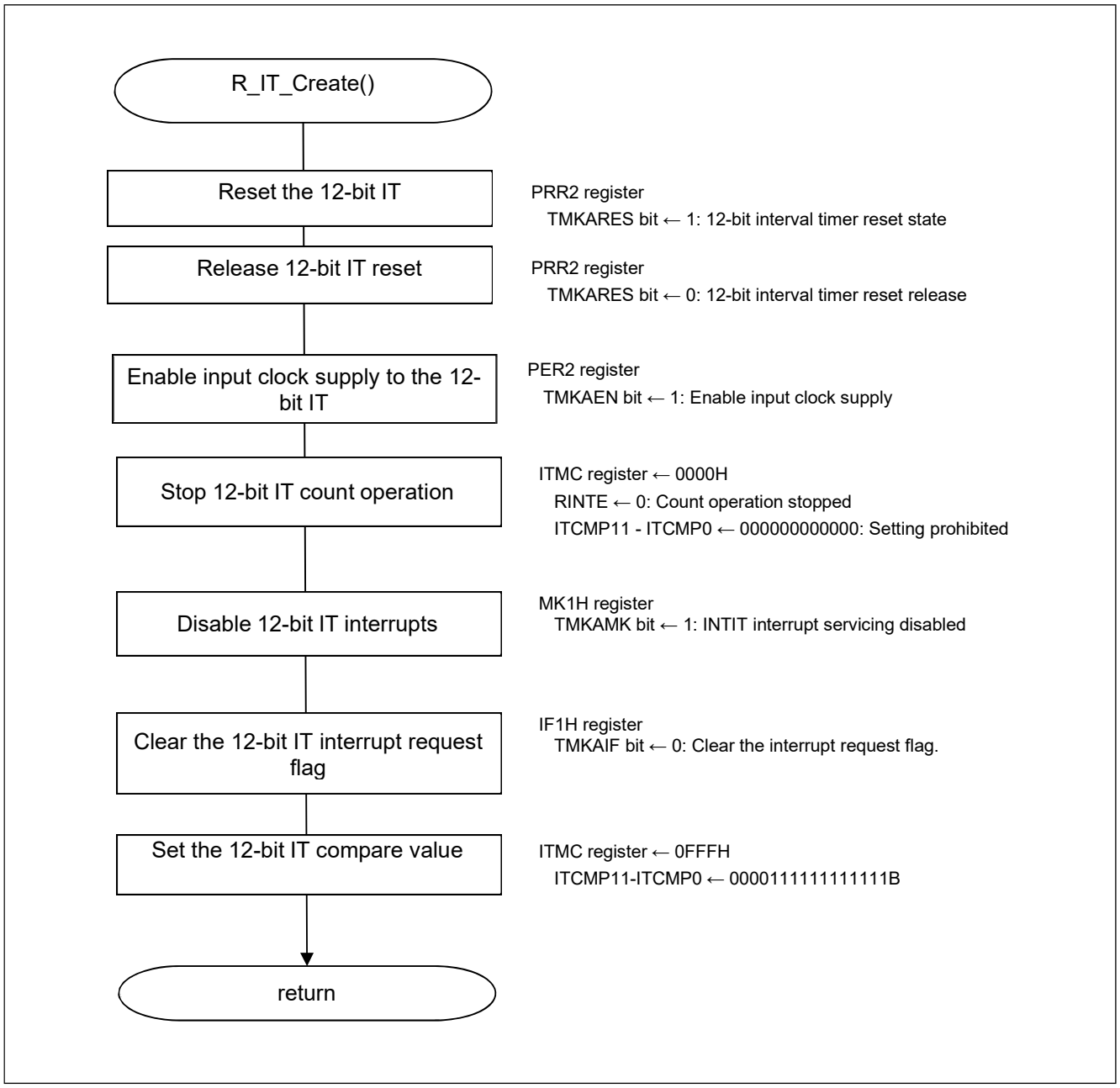


**Figure 5.6 Initial Setting of the 12-bit Interval Timer**

12-bit interval timer reset

- Peripheral reset control register 2 (PRR2)

Reset the 12-bit interval timer.

Symbol: PRR2

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| TMKARES | 0 | DOCRES | 0 | 0 | 0 | 0 | 0 |
| **1** | x | x | x | x | x | x | x |

Bit 7

| TMKARES | Reset control of 12-bit interval timer |
|---|---|
| 0 | 12-bit interval timer reset release |
| **1** | **12-bit interval timer reset state** |

12-bit interval timer reset release

- Peripheral reset control register 2 (PRR2)

Release the 12-bit interval timer reset state.

Symbol: PRR2

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| TMKARES | 0 | DOCRES | 0 | 0 | 0 | 0 | 0 |
| **0** | x | x | x | x | x | x | x |

Bit 7

| TMKARES | Reset control of 12-bit interval timer |
|---|---|
| **0** | **12-bit interval timer reset release** |
| 1 | 12-bit interval timer reset state |

### 12-bit interval timer clock supply start

- Peripheral enable register 2 (PER2)
  Start the 12-bit interval timer clock supply.

Symbol: PER2

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| TMKAEN | FMCEN | DOCEN | 0 | 0 | 0 | 0 | 0 |
| **1** | x | x | x | x | x | x | x |

Bit 7

| TMKAEN | Control of 12-bit interval timer input clock supply |
|---|---|
| 0 | Stops input clock supply. |
| **1** | **Enables input clock supply.** |

### 12-bit interval timer interrupt setting

- Interrupt request flag register (IF1H)
  Clear the interrupt request flag.
- Interrupt mask flag register (MK1H)
  Disable interrupt servicing.

Symbol: IF1H

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| 0 | DOCIF | CMPIF1 | CMPIF0 | KRIF | TMKAIFI | RTCIF | ADIF |
| x | x | x | x | x | **0** | x | x |

Bit 2

| TMKAIF | Interrupt request flag |
|---|---|
| **0** | **No interrupt request signal is generated.** |
| 1 | Interrupt request is generated, interrupt request status |

Symbol: MK1H

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| 0 | DOCMK | CMPMK1 | CMPMK0 | KRMK | TMKAMK | RTCMK | ADMK |
| x | x | x | x | x | **1** | x | x |

Bit 2

| TMKAMK | Interrupt servicing control |
|---|---|
| 0 | Interrupt servicing enabled |
| **1** | **Interrupt servicing disabled** |

Setting of the 12-bit interval timer count operation and compare value

- 12-bit interval timer control register (ITMC)

  Stop the 12-bit interval timer count operation.

  Set a compare value.

  Symbol: ITMC

| 15 | 14 | 13 | 12 | 11 - 0 |
|---|---|---|---|---|
| RINTE | 0 | 0 | 0 | ITCMP 11 - ITCMP 0 |
| **0** | x | x | x | **111111111111** |

Bit 15

| RINTE | 12-bit interval timer operation control |
|---|---|
| **0** | **Count operation stopped** |
| 1 | Count operation started |

Bits 11 to 0

| ITCMP11 - ITCMP0 | Fixed-cycle interrupt (INTRTC) selection |
|---|---|
| 001H | **Generates a fixed-cycle interrupt (count clock cycles x (ITCMP setting + 1)).** |
| • • • | |
| **FFFH** | |
| 000H | Setting prohibited |

### 5.7.6 8-bit Interval Timer Initialization

Figure 5.7 shows a flowchart for initial setting of the 8-bit interval timer.

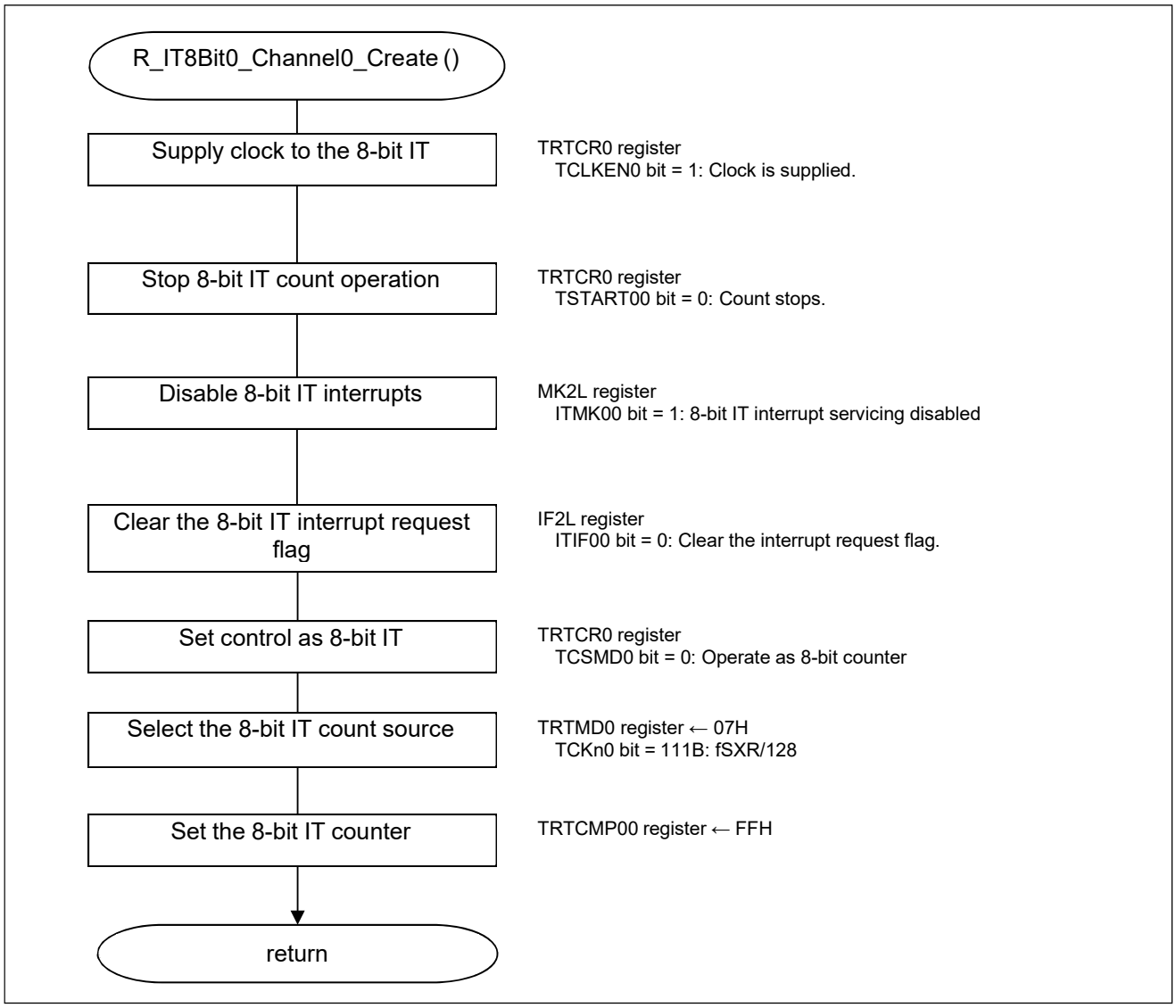


**Figure 5.7 Initial Setting of the 8-bit Interval Timer**

8-bit interval timer control setting

- 8-bit interval timer control register 0 (TRTCR0)
  Start clock supply as 8-bit counter.

Symbol: TRTCR0

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| TCSMD0 | 0 | 0 | TCLKEN0 | 0 | TSTART01 | 0 | TSTART00 |
| **0** | x | x | **1** | x | x | x | **0** |

Bit 7

| TCSMD0 | Mode selection |
|---|---|
| **0** | **Operates as 8-bit counter** |
| 1 | Operates as 16-bit counter (channel 0 and channel 1 are connected) |

Bit 4

| TCLKEN0 | 8-bit interval timer clock enable |
|---|---|
| 0 | Clock is stopped. |
| **1** | **Clock is supplied.** |

Bit 0

| TSTART00 | 8-bit interval timer 0 count start |
|---|---|
| **0** | **Count stops.** |
| 1 | Count starts. |

8-bit interval timer interrupt setting

- Interrupt mask flag register (MK2L)
  Disable interrupt servicing.
- Interrupt request flag register (IF2L)
  Clear the interrupt request flag.

Symbol: MK2L

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| FLMK | 0 | 0 | 0 | ITMK11 | ITMK10 | ITMK01 | ITMK00 |
| x | x | x | x | x | x | x | **1** |

Bit 0

| ITMK00 | Interrupt servicing control |
|---|---|
| 0 | Interrupt servicing enabled |
| **1** | **Interrupt servicing disabled** |

Symbol: IF2L

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| FLIF | 0 | 0 | 0 | ITIF11 | ITIF10 | ITIF01 | ITIF00 |
| x | x | x | x | x | x | x | **0** |

Bit 0

| ITIF00 | Interrupt request flag |
|---|---|
| **0** | **No interrupt request signal is generated.** |
| 1 | Interrupt request is generated, interrupt request status |

Note
1. For details on register settings, refer to RL78/I1D User's Manual: Hardware.

8-bit interval timer count source setting

- 8-bit interval timer division register 0 (TRTMD0)
  Set a counter value.

Symbol: TRTMD0

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| 0 | TCK01 | | | 0 | TCK00 | | |
| x | x | x | x | x | **111** | | |

Bit 2 to bit 0

| TCK00 | | | 8-bit interval timer 0 division selection |
|---|---|---|---|
| Bit 2 | Bit 1 | Bit 0 | |
| 0 | 0 | 0 | fSXR or fIL |
| 0 | 0 | 1 | fSXR/2 or fIL/2 |
| 0 | 1 | 0 | fSXR/4 or fIL/4 |
| 0 | 1 | 1 | fSXR/8 or fIL/8 |
| 1 | 0 | 0 | fSXR/16 or fIL/16 |
| 1 | 0 | 1 | fSXR/32 or fIL/32 |
| 1 | 1 | 0 | fSXR/64 or fIL/64 |
| **1** | **1** | **1** | **fSXR/128 or fIL/128** |

8-bit interval timer count value setting

- 8-bit interval timer compare register 00 (TRTCMP00)
  Set a count value.

Symbol: TRTCMP00

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** |

Bit 7 to bit 0

| Function |
|---|
| **8-bit counter** |

Note
1. For details on register settings, refer to RL78/I1D User's Manual: Hardware.

### 5.7.7 A/D Converter Initialization

Figure 5.8 shows a flowchart for initial setting of the A/D converter.

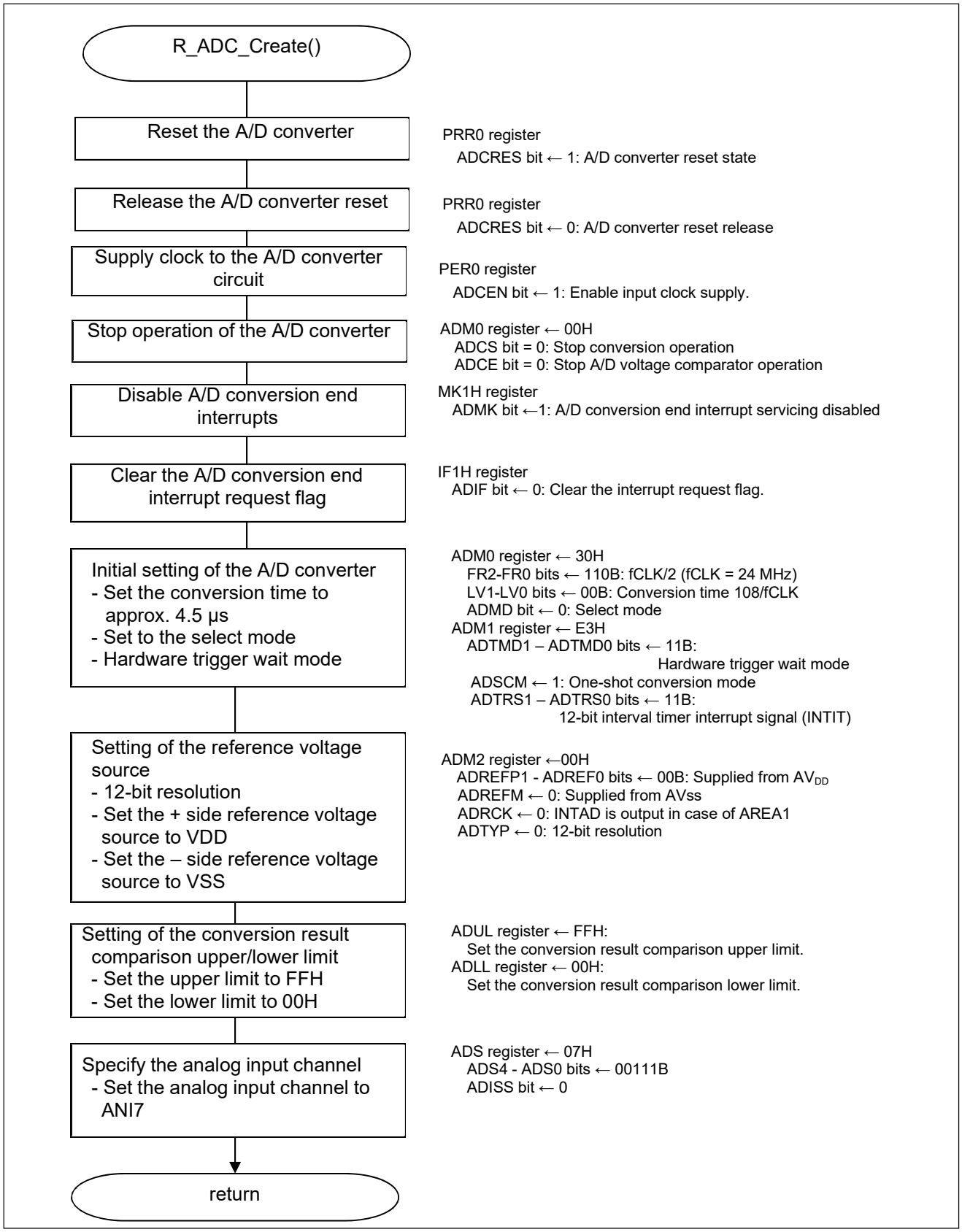


**Figure 5.8 Initial Setting of the A/D Converter**

### A/D converter reset

- Peripheral reset control register 0 (PRR0)
  Reset the A/D converter.

Symbol: PRR0

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| 0 | 0 | ADCRES | 0 | 0 | SAU0RES | 0 | 0 |
| x | x | **1** | x | x | x | x | x |

Bit 5

| ADCRES | Reset control of A/D converter |
|---|---|
| 0 | A/D converter reset release |
| **1** | **A/D converter reset state** |

### A/D converter reset release

- Peripheral reset control register 0 (PRR0)
  Release the A/D converter reset state.

Symbol: PRR0

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| 0 | 0 | ADCRES | 0 | 0 | SAU0RES | 0 | 0 |
| x | x | **0** | x | x | x | x | x |

Bit 5

| ADCRES | A/D converter reset control |
|---|---|
| **0** | **A/D converter reset release** |
| 1 | A/D converter reset state |

A/D converter clock supply start

- Peripheral enable register 0 (PER0)
  Start clock supply to the A/D converter.

Symbol: PER0

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| RTCEN | 0 | ADCEN | 0 | 0 | SAU0EN | 0 | TAU0EN |
| x | x | **1** | x | x | x | x | x |

Bit 5

| ADCEN | Control of A/D converter input clock supply |
|---|---|
| 0 | Stops input clock supply. |
| **1** | **Enables input clock supply.** |

A/D conversion end interrupt setting

- Interrupt mask flag register (MK1H)
  Disable interrupt servicing.
- Interrupt request flag register (IF1H)
  Clear the interrupt request flag.

Symbol: MK1H

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| 0 | DOCMK | CMPMK1 | CMPMK0 | KRMK | TMKAMK | RTCMK | ADMK |
| x | x | x | x | x | x | x | **1** |

Bit 0

| ADMK | Interrupt servicing control |
|---|---|
| 0 | Interrupt servicing enabled |
| **1** | **Interrupt servicing disabled** |

Symbol: IF1H

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| 0 | DOCIF | CMPIF1 | CMPIF0 | KRIF | TMKIF | RTCIF | ADIF |
| x | x | x | x | x | x | x | **0** |

Bit 0

| ADIF | Interrupt request flag |
|---|---|
| **0** | **No interrupt request signal is generated.** |
| 1 | Interrupt request is generated, interrupt request status |

### Setting of A/D conversion time and operation mode

- A/D converter mode register 0 (ADM0)
  Control A/D conversion operation.
  Specify the A/D conversion channel selection mode.

Symbol: ADM0

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| ADCS | ADMD | FR2 | FR1 | FR0 | LV1 | LV0 | ADCE |
| **0** | **0** | **1** | **1** | **0** | **0** | **0** | **0** |

Bit 7

| ADCS | A/D conversion operation control |
|---|---|
| **0** | **Stops conversion operation** |
| 1 | Enables conversion operation |

Bit 6

| ADMD | Specification of the A/D conversion channel selection mode |
|---|---|
| **0** | **Select mode** |
| 1 | Scan mode |

Bits 5 to 1

| ADM0 | | | | | Mode | Conversion time selection | | | | | Conversion clock ($f_{AD}$) |
|---|---|---|---|---|---|---|---|---|---|---|---|
| FR2 | FR1 | FR0 | LV1 | LV2 | | $f_{CLK}$ = 1 MHz | $f_{CLK}$ = 4 MHz | $f_{CLK}$ = 8 MHz | $f_{CLK}$ = 16 MHz | $f_{CLK}$ = 24 MHz | |
| 0 | 0 | 0 | **0** | **0** | **Standard 1** | Setting prohibited | Setting prohibited | Setting prohibited | Setting prohibited | 72 µs | $f_{CLK}/32$ |
| 0 | 0 | 1 | | | | | | | 54 µs | 36 µs | **$f_{CLK}/16$** |
| 0 | 1 | 0 | | | | | | 54 µs | 27 µs | 18 µs | $f_{CLK}/8$ |
| 0 | 1 | 1 | | | | | | 40.5 µs | 20.25 µs | 13.5 µs | $f_{CLK}/6$ |
| 1 | 0 | 0 | | | | | | 33.75 µs | 16.875 µs | 11.25 µs | $f_{CLK}/5$ |
| 1 | 0 | 1 | | | | | 54 µs | 27 µs | 13.5 µs | 9 µs | $f_{CLK}/4$ |
| **1** | **1** | **0** | | | | | 27 µs | 13.5 µs | 6.75 µs | **4.5 µs** | **$f_{CLK}/2$** |
| 1 | 1 | 1 | | | | 54 µs | 13.5 µs | 6.75 µs | 3.375 µs | Setting prohibited | $f_{CLK}/1$ |
| 0 | 0 | 0 | 0 | 1 | Standard 2 | Setting prohibited | Setting prohibited | Setting prohibited | Setting prohibited | 88 µs | $f_{CLK}/32$ |
| 0 | 0 | 1 | | | | | | | 66 µs | 44 µs | **$f_{CLK}/16$** |
| 0 | 1 | 0 | | | | | | 66 µs | 33 µs | 22 µs | $f_{CLK}/8$ |
| 0 | 1 | 1 | | | | | | 49.5 µs | 24.75 µs | 16.5 µs | $f_{CLK}/6$ |
| 1 | 0 | 0 | | | | | | 41.25 µs | 20.625 µs | 13.75 µs | $f_{CLK}/5$ |
| 1 | 0 | 1 | | | | | 66 µs | 33 µs | 16.5 µs | 11 µs | $f_{CLK}/4$ |
| 1 | 1 | 0 | | | | | 33 µs | 16.5 µs | 8.25 µs | 5.5 µs | $f_{CLK}/2$ |
| 1 | 1 | 1 | | | | 66 µs | 16.5 µs | 8.25 µs | 4.125 µs | Setting prohibited | $f_{CLK}/1$ |

Bit 0

| ADCE | A/D voltage comparator operation control |
|---|---|
| **0** | **Stops A/D voltage comparator operation** |
| 1 | Enables A/D voltage comparator operation |

A/D conversion trigger mode setting

- A/D converter mode register 1 (ADM1)
  Select an A/D conversion trigger mode.
  Set an A/D conversion operation mode.
  Select a hardware trigger signal.

Symbol: ADM1

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| ADTMD1 | ADTMD0 | ADSCM | 0 | 0 | 0 | ADTRS1 | ADTRS0 |
| **1** | **1** | **1** | x | x | x | **1** | **1** |

Bits 7 and 6

| ADTMD1 | ADTMD0 | Selection of the A/D conversion trigger mode |
|---|---|---|
| 0 | x | Software trigger mode |
| 1 | 0 | Hardware trigger no-wait mode |
| **1** | **1** | **Hardware trigger wait mode** |

Bit 5

| ADSCM | Specification of the A/D conversion operation mode |
|---|---|
| 0 | Sequential conversion mode |
| **1** | **One-shot conversion mode** |

Bits 1 and 0

| ADTRS1 | ADTRS0 | Selection of the hardware trigger signal |
|---|---|---|
| 0 | 0 | End of timer channel 01 count or capture interrupt signal (INTTM01) |
| 0 | 1 | Setting prohibited |
| 1 | 0 | Real-time clock interrupt signal (INTRTC) |
| **1** | **1** | **12-bit interval timer interrupt signal (INTIT)** |

### Reference voltage source setting

- A/D converter mode register 2 (ADM2)
  Select the + side reference voltage source of the A/D converter.
  Select the - side reference voltage source of the A/D converter.
  Check the upper limit and lower limit conversion result values.
  Specify the SNOOZE mode function.
  Select the A/D conversion resolution.

Symbol: ADM2

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| ADREFP1 | ADREFP0 | ADREFM | 0 | ADRCK | AWC | 0 | ADYTP |
| **0** | **0** | **0** | x | **0** | **0** | **0** | **0** |

Bits 7 and 6

| ADREFP1 | ADREFP0 | Selection of the + side reference voltage source of the A/D converter |
|---|---|---|
| **0** | **0** | **Supplied from $AV_{DD}$** |
| 0 | 1 | Supplied from $AV_{REFP}$/ANI0 |
| 1 | 0 | Supplied from the internal reference voltage (1.45 V) |
| 1 | 1 | Setting prohibited |

Bit 5

| ADREFM | Selection of the - side reference voltage source of the A/D converter |
|---|---|
| **0** | **Supplied from $AV_{SS}$** |
| 1 | Supplied from $AV_{REFM}$/ANI1 |

Bit 3

| ADRCK | Checking the upper limit and lower limit conversion result values |
|---|---|
| **0** | **The A/D conversion end interrupt request signal (INTAD) is output when the ADLL register ≤ the ADCR register ≤ the ADUL register (AREA1).** |
| 1 | The A/D conversion end interrupt request signal (INTAD) is output when the ADCR register < the ADLL register (AREA2) or the ADUL register < the ADCR register (AREA3). |

Bit 2

| AWC | Specification of the SNOOZE mode |
|---|---|
| **0** | **The SNOOZE mode function is not used.** |
| 1 | The SNOOZE mode function is used. |

Bit 0

| ADTYP | Selection of the A/D conversion resolution |
|---|---|
| **0** | **12-bit resolution** |
| 1 | 8-bit resolution |

### Conversion result comparison upper/lower limit setting

- Conversion result comparison upper limit setting register (ADUL)
- Conversion result comparison lower limit setting register (ADLL)

Set the conversion result comparison upper/lower limit.

Symbol: ADUL

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| ADUL7 | ADUL6 | ADUL5 | ADUL4 | ADUL3 | ADUL2 | ADUL1 | ADUL0 |
| **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** |

Symbol: ADLL

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| ADLL7 | ADLL6 | ADLL5 | ADLL4 | ADLL3 | ADLL2 | ADLL1 | ADLL0 |
| **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |

Input channel specification

- Analog input channel specification register (ADS)
  Specify the input channel of the analog voltage to be A/D converted.

Symbol: ADS

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| ADISS | 0 | 0 | ADS4 | ADS3 | ADS2 | ADS1 | ADS0 |
| **0** | x | x | **0** | **0** | **1** | **1** | **1** |

Bits 7, 4 to 0

| ADISS | ADS4 | ADS3 | ADS2 | ADS1 | ADS0 | Analog input channel | Input source |
|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 | 0 | ANI0 | P10/ANI0/AVREFP pin |
| 0 | 0 | 0 | 0 | 0 | 1 | ANI1 | P11/ANI1/AVREFM pin |
| 0 | 0 | 0 | 0 | 1 | 0 | ANI2 | P12/ANI2 pin |
| 0 | 0 | 0 | 0 | 1 | 1 | ANI3 | P13/ANI3 pin |
| 0 | 0 | 0 | 1 | 0 | 0 | ANI4 | P14/ANI4 pin |
| 0 | 0 | 0 | 1 | 0 | 1 | ANI5 | P15/ANI5 pin |
| 0 | 0 | 0 | 1 | 1 | 0 | ANI6 | P16/ANI6 pin |
| 0 | 1 | 0 | 0 | 0 | 1 | ANI17 | P02/ANI17 pin |
| **0** | **0** | **0** | **1** | **1** | **1** | **ANI7** | **P17/ANI7 pin** |
| 0 | 0 | 1 | 0 | 0 | 0 | ANI8 | P25/ANI8 pin |
| 0 | 0 | 1 | 0 | 0 | 1 | ANI9 | P24/ANI9 pin |
| 0 | 0 | 1 | 0 | 1 | 0 | ANI10 | P23/ANI10 pin |
| 0 | 0 | 1 | 0 | 1 | 1 | ANI11 | P22/ANI11 pin |
| 0 | 0 | 1 | 1 | 0 | 0 | ANI12 | P21/ANI12 pin |
| 0 | 0 | 1 | 1 | 0 | 1 | ANI13 | P20/ANI13 pin |
| 0 | 1 | 0 | 0 | 0 | 0 | ANI16 | P02/ANI16 pin |
| 0 | 1 | 0 | 0 | 0 | 1 | ANI17 | P03/ANI17 pin |
| 0 | 1 | 0 | 1 | 1 | 0 | ANI18 | P04/ANI18 pin |
| 1 | 0 | 0 | 0 | 0 | 0 | — | Temperature sensor output voltage |
| 1 | 0 | 0 | 0 | 0 | 1 | — | Internal reference voltage output (1.45 V) |
| Other than the above | | | | | | Setting prohibited | |

### 5.7.8 Operational Amplifier Initialization

Figure 5.9 is a flowchart for initial setting of the operational amplifiers.

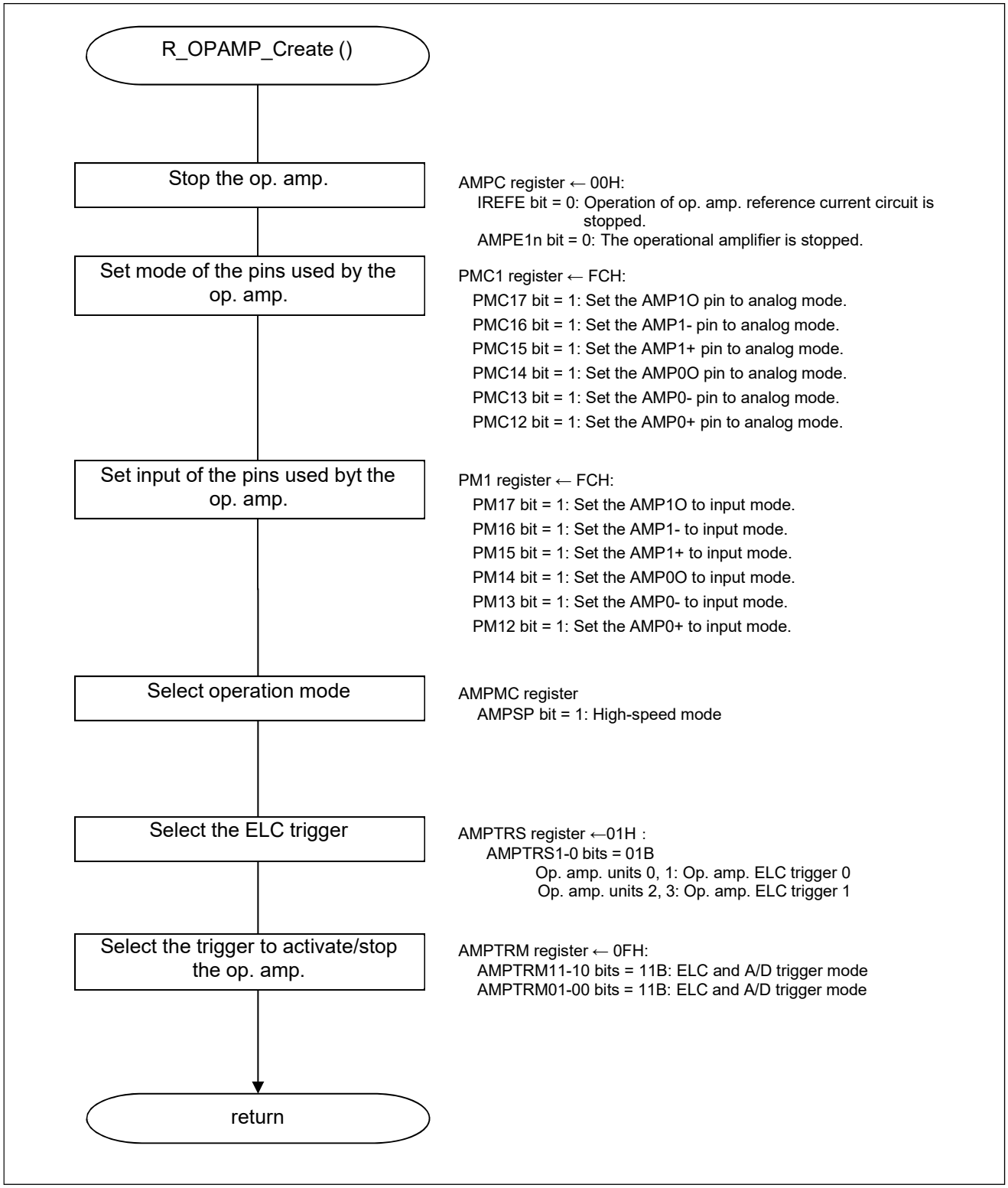


**Figure 5.9 Initial Setting of the Operational Amplifiers**

Operational amplifier stop

- Operational amplifier control register (AMPC)
  Stop the operational amplifiers.

Symbol: AMPC

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| IREFE | 0 | 0 | 0 | AMPE3 | AMPE2 | AMPE1 | AMPE0 |
| **0** | x | x | x | **0** | **0** | **0** | **0** |

Bit 7

| IREFE | Operation control of operational amplifier reference current circuit |
|---|---|
| **0** | **Operational amplifier reference current circuit is stopped.** |
| 1 | Operation of operational amplifier reference current circuit is enabled. |

Bits 3 to 0

| AMPEn | Operation control of operational amplifier |
|---|---|
| **0** | **Operation amplifier is stopped.** |
| 1 | Software trigger mode: Operation of operational amplifier is enabled.<br>ELC trigger mode or ELC and A/D trigger mode: Wait for ELC is enabled. |

### Mode setting of pins used for the operational amplifier

- Port mode control register 0 (PMC1)
  Set the pins to be used for the operational amplifiers to analog input.

Symbol: PMC1

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| PMC17 | PMC16 | PMC15 | PMC14 | PMC13 | PMC12 | PMC11 | PMC10 |
| **1** | **1** | **1** | **1** | **1** | **1** | x | x |

Bits 7 to 0

| PMC1n | Pmn pin digital I/O/analog input selection (n = 0 to 7) |
|---|---|
| 0 | Digital I/O (alternate function other than analog input) |
| **1** | **Analog input** |

### Input setting of pins used for the operational amplifier

- Port mode register 0 (PM1)
  Set the pins to be used for the operational amplifiers to input mode.

Symbol: PM1

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| PM17 | PM16 | PM15 | PM14 | PM13 | PM12 | PM11 | PM10 |
| **1** | **1** | **1** | **1** | **1** | **1** | x | x |

Bits 7 to 0

| PM1n | Pmn pin I/O mode selection (n = 0 to 7) |
|---|---|
| 0 | Output mode (the pin functions as an output port (output buffer on)) |
| **1** | **Input mode (the pin functions as an input port (output buffer off))** |

### Operation mode setting of the operational amplifier

- Operational amplifier mode control register (AMPMC)
  Set the operational amplifiers to high-speed mode.

Symbol: AMPMC

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| AMPSP | 0 | 0 | 0 | AMPPC3 | AMPPC2 | AMPPC1 | AMPPC0 |
| **1** | x | x | x | x | x | x | x |

Bit 7

| AMPSP | Operation mode selection (common to all units) |
|---|---|
| 0 | Low-power mode (Low-speed mode) |
| **1** | **High-speed mode** |

ELC trigger selection

- Operational amplifier ELC trigger select register (AMPTRS)
  Set the operational amplifier ELC trigger.

Symbol: AMPTRS

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 | 0 | AMPTRS1 | AMPTRS0 |
| x | x | x | x | x | x | **0** | **1** |

Bits 1 to 0

| AMPTRS1 | AMPTRS0 | ELC trigger selection |
|---|---|---|
| 0 | 0 | Operational amplifier unit 0: Operational amplifier ELC trigger 0<br>Operational amplifier unit 1: Operational amplifier ELC trigger 1<br>Operational amplifier unit 2: Operational amplifier ELC trigger 2<br>Operational amplifier unit 3: Operational amplifier ELC trigger 3 |
| **0** | **1** | **Operational amplifier unit 0: Operational amplifier ELC trigger 0**<br>**Operational amplifier unit 1: Operational amplifier ELC trigger 0**<br>**Operational amplifier unit 2: Operational amplifier ELC trigger 1**<br>**Operational amplifier unit 3: Operational amplifier ELC trigger 1** |
| 1 | 0 | Setting prohibited |
| 1 | 1 | Operational amplifier unit 0: Operational amplifier ELC trigger 0<br>Operational amplifier unit 1: Operational amplifier ELC trigger 0<br>Operational amplifier unit 2: Operational amplifier ELC trigger 0<br>Operational amplifier unit 3: Operational amplifier ELC trigger 0 |

Operational amplifier activation/stop trigger selection

- Operational amplifier trigger mode control register (AMPTRM)
  Set activation/stop of the operational amplifiers.

Symbol: AMPTRM

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| AMPTRM31 | AMPTRM30 | AMPTRM21 | AMPTRM20 | AMPTRM11 | AMPTRM10 | AMPTRM01 | AMPTRM00 |
| x | x | x | x | **1** | **1** | **1** | **1** |

Bits 3 to 0

| AMPTRMn1 | AMPTRMn0 | Operational amplifier function activation/stop trigger control |
|---|---|---|
| 0 | 0 | Software trigger mode<br>• The operational amplifier can be activated/stopped by setting the AMPC register.<br>• The operational amplifier cannot be activated by an ELC trigger.<br>• The operational amplifier cannot be controlled by an A/D conversion end trigger. |
| 0 | 1 | ELC trigger mode<br>• The operational amplifier can be set to wait for an ELC trigger or stopped by setting the AMPC register.<br>• The operational amplifier can be activated by an ELC trigger.<br>• The operational amplifier cannot be controlled by an A/D conversion end trigger. |
| 1 | 0 | Setting prohibited |
| **1** | **1** | **ELC and A/D trigger mode**<br>**• The operational amplifier can be set to wait for an ELC trigger or stopped by setting the AMPC register.**<br>**• The operational amplifier can be activated by an ELC trigger.**<br>**• The operational amplifier can be stopped by an A/D conversion end trigger.** |

Remark n: Unit number (n = 0, 1, 2, 3)

### 5.7.9 DTC Initialization

Figure 5.10 to Figure 5.12 show a flowchart for initial setting of the DTC.

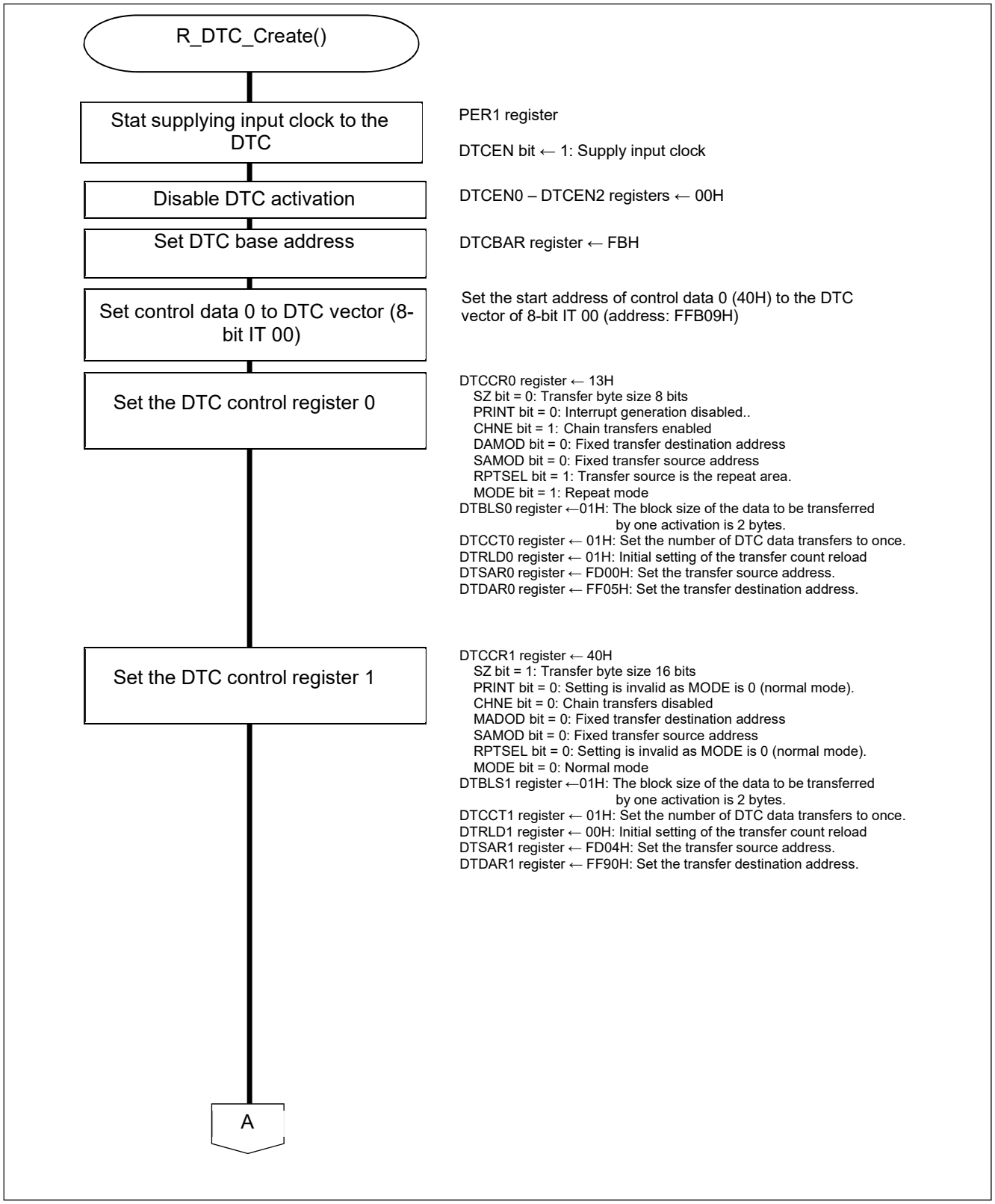


**Figure 5.10 Initial Setting of the DTC (1)**

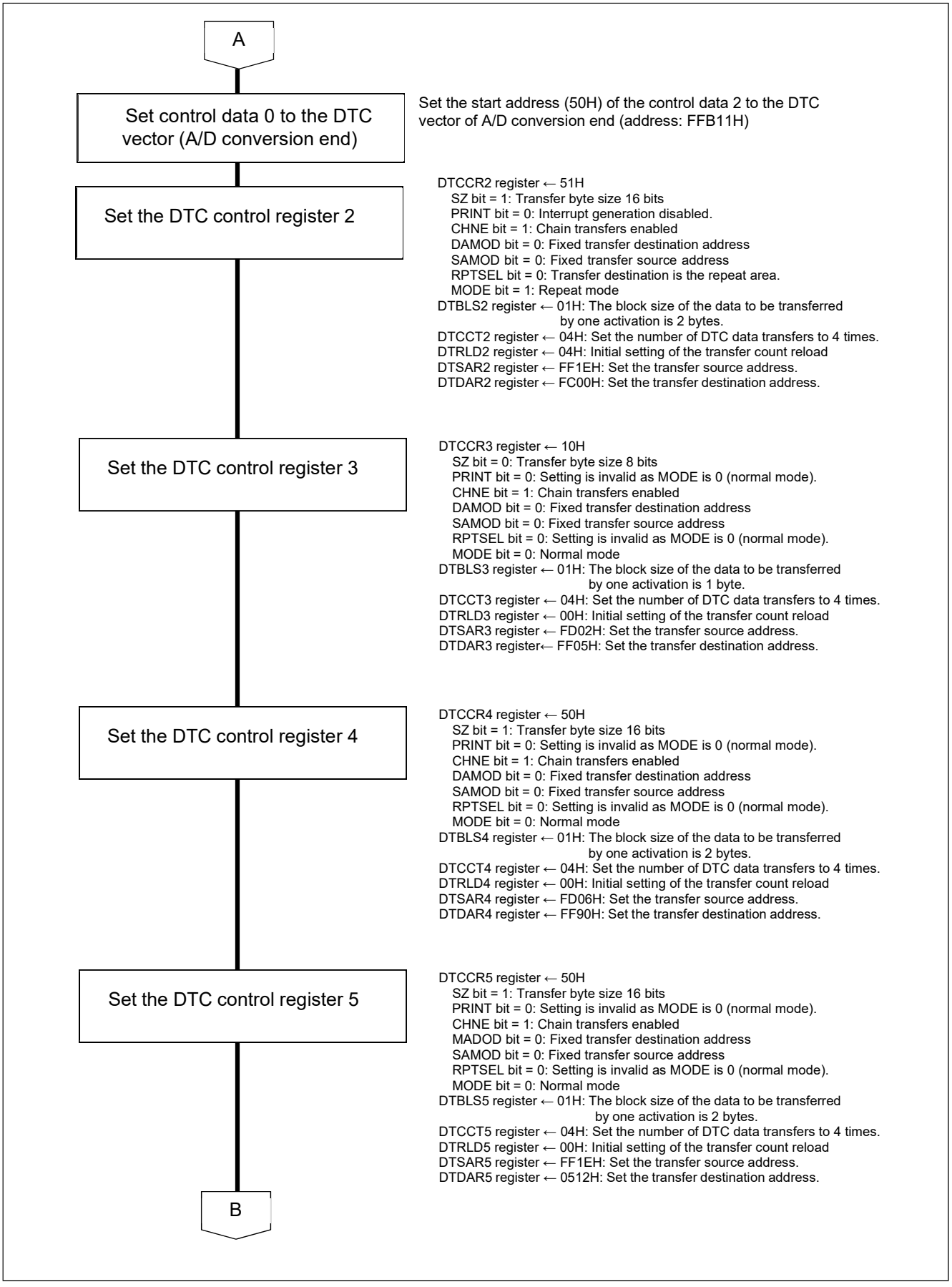


**Figure 5.11 Initial Setting of the DTC (2)**

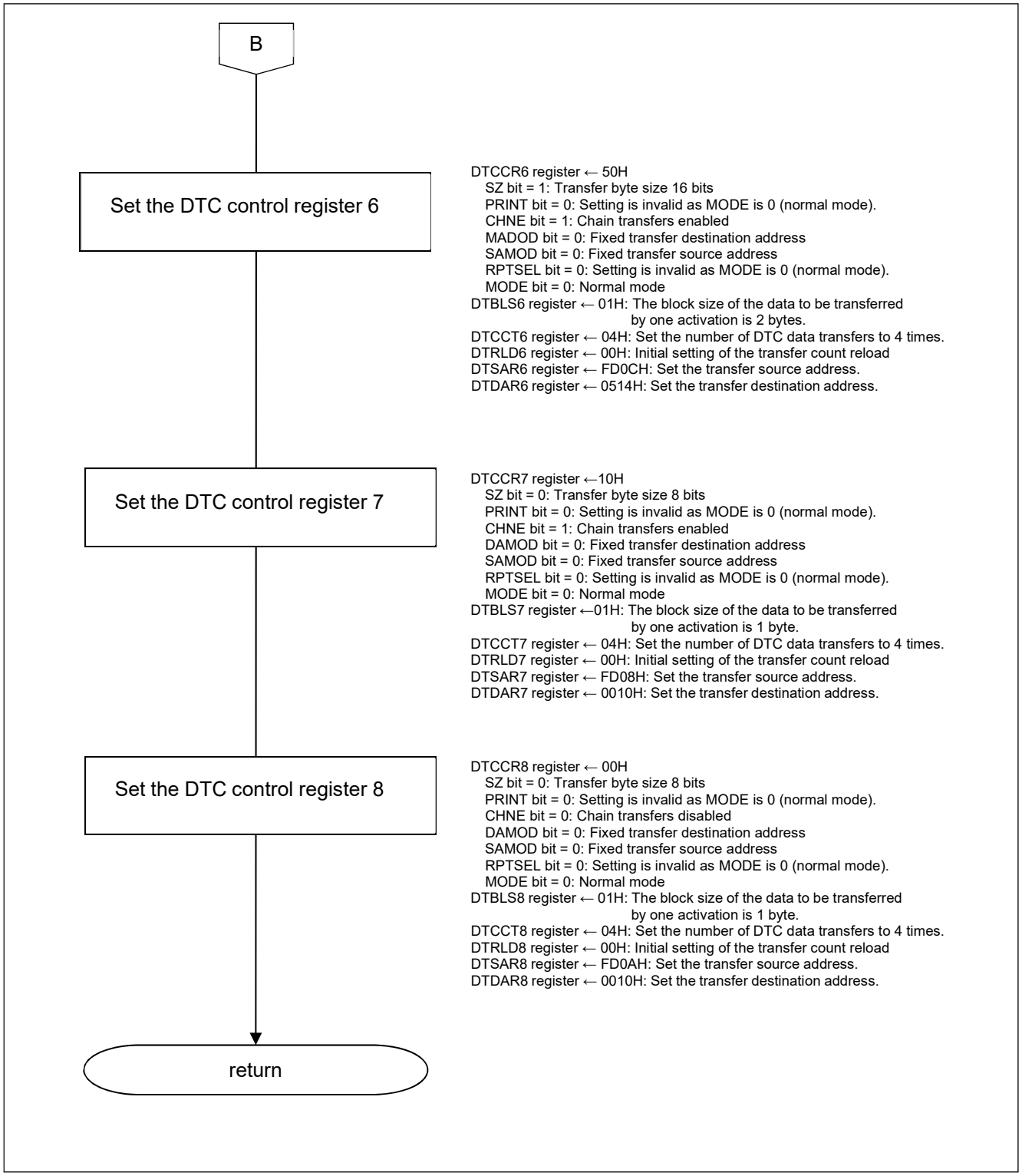


**Figure 5.12 Initial Setting of the DTC (3)**

DTC clock supply start

- Peripheral enable register 1 (PER1)

Start clock supply to DTC.

Symbol: PER1

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| 0 | 0 | CMPEN | 0 | DTCEN | 0 | 0 | 0 |
| x | x | x | x | **1** | x | x | x |

Bit 3

| DTCEN | Control of DTC input clock |
|---|---|
| 0 | Stops input clock supply. |
| **1** | **Supplies input clock.** |

DTC activation disabling

- DTC activation enable register I (DTCENi) (I = 0 to 2)

Disable DTC activation.

Symbol: DTCENi

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| DTCENi7 | DTCENi6 | DTCENi5 | DTCENi4 | DTCENi3 | DTCENi2 | DTCENi1 | DTCENi0 |
| **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |

Bit 7 to bit 0 (The below table shows the format of the bit 7 as an example. (The formats of the bits 7 to 0 are same.))

| DTCENi7 | DTC activation enable i7 |
|---|---|
| **0** | **Activation disabled** |
| 1 | Activation enabled |

DTC base address

- DTC base address register (DTCBAR)

Set the DTC base address to “FBH”.

Symbol: DTCBAR

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| DTCBAR7 | DTCBAR6 | DTCBAR5 | DTCBAR4 | DTCBAR3 | DTCBAR2 | DTCBAR1 | DTCBAR0 |
| **1** | **1** | **1** | **1** | **1** | **0** | **1** | **1** |

DTC control register 0 setting

- DTC control register 0 (DTCCR0)

Set to 8 bits (data size), chain transfer enabled, and repeat mode (transfer mode).

Symbol: DTCCR0

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| 0 | SZ | RPTINT | CHNE | DAMOD | SAMOD | RPTSEL | MODE |
| **-** | **0** | **0** | **1** | **0** | **0** | **1** | **1** |

Bit 6

| SZ | Data size selection |
|---|---|
| **0** | **8 bits** |
| 1 | 16 bits |

Bit 5

| RPTINT | Enabling/disabling repeat mode interrupts |
|---|---|
| **0** | **Interrupt generation disabled** |
| 1 | Interrupt generation enabled |
| The setting of the RPTINT bit is invalid when the MODE bit is 0 (normal mode). | |

Bit 4

| CHNE | Enabling/disabling chain transfers |
|---|---|
| 0 | Chain transfers disabled |
| **1** | **Chain transfers enabled** |
| Set the CHNE bit in the DTCCR23 register to 0 (chain transfers disabled). | |

Bit 3

| DAMOD | Transfer destination address control |
|---|---|
| **0** | **Fixed** |
| 1 | Incremented |
| The setting of the DAMOD bit is invalid when the MODE bit is 1 (repeat mode) and the RPTSEL bit is 0 (transfer destination is the repeat area). | |

Bit 2

| SAMOD | Transfer source address control |
|---|---|
| 0 | Fixed |
| 1 | Incremented |
| **The setting of the SAMOD bit is invalid when the MODE bit is 1 (repeat mode) and the RPTSEL bit is 1 (transfer source is the repeat area).** | |

Bit 1

| RPTSEL | Repeat area selection |
|---|---|
| 0 | Transfer destination is the repeat area. |
| **1** | **Transfer source is the repeat area.** |

Bit 0

| MODE | Transfer mode selection |
|---|---|
| 0 | Normal mode |
| **1** | **Repeat mode** |

DTC control register 1 setting

- DTC control register 1 (DTCCR1)

Set to 16 bits (data size), chain transfers disabled, and normal mode (transfer mode).

Symbol: DTCCR1

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| 0 | SZ | RPTINT | CHNE | DAMOD | SAMOD | RPTSEL | MODE |
| **-** | **1** | **0** | **0** | **0** | **0** | **0** | **0** |

Bit 6

| SZ | Data size selection |
|---|---|
| 0 | 8 bits |
| **1** | **16 bits** |

Bit 5

| RPTINT | Enabling/disabling repeat mode interrupts |
|---|---|
| 0 | Interrupt generation disabled |
| 1 | Interrupt generation enabled |
| **The setting of the RPTINT bit is invalid when the MODE bit is 0 (normal mode).** | |

Bit 4

| CHNE | Enabling/disabling chain transfers |
|---|---|
| **0** | **Chain transfers disabled** |
| 1 | Chain transfers enabled |
| Set the CHNE bit in the DTCCR23 register to 0 (chain transfers disabled). | |

Bit 3

| DAMOD | Transfer destination address control |
|---|---|
| **0** | **Fixed** |
| 1 | Incremented |
| The setting of the DAMOD bit is invalid when the MODE bit is 1 (repeat mode) and the RPTSEL bit is 0 (transfer destination is the repeat area). | |

Bit 2

| SAMOD | Transfer source address control |
|---|---|
| **0** | **Fixed** |
| 1 | Incremented |
| The setting of the SAMOD bit is invalid when the MODE bit is 1 (repeat mode) and the RPTSEL bit is 1 (transfer source is the repeat area). | |

Bit 1

| RPTSEL | Repeat area selection |
|---|---|
| 0 | Transfer destination is the repeat area. |
| 1 | Transfer source is the repeat area. |
| **The setting of the RPTSEL bit is invalid when the MODE bit is 0 (normal mode).** | |

Bit 0

| MODE | Transfer mode selection |
|---|---|
| **0** | **Normal mode** |
| 1 | Repeat mode |

DTC control register 2 setting

- DTC control register 2 (DTCCR2)

Set to 8 bits (data size), chain transfers enabled, and repeat mode (transfer mode).

Symbol: DTCCR2

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| 0 | SZ | RPTINT | CHNE | DAMOD | SAMOD | RPTSEL | MODE |
| **-** | **1** | **0** | **1** | **0** | **0** | **0** | **1** |

Bit 6

| SZ | Data size selection |
|---|---|
| 0 | 8 bits |
| **1** | **16 bits** |

Bit 5

| RPTINT | Enabling/disabling repeat mode interrupts |
|---|---|
| **0** | **Interrupt generation disabled** |
| 1 | Interrupt generation enabled |
| The setting of the RPTINT bit is invalid when the MODE bit is 0 (normal mode). | |

Bit 4

| CHNE | Enabling/disabling chain transfers |
|---|---|
| 0 | Chain transfers disabled |
| **1** | **Chain transfers enabled** |
| Set the CHNE bit in the DTCCR23 register to 0 (chain transfers disabled). | |

Bit 3

| DAMOD | Transfer destination address control |
|---|---|
| 0 | Fixed |
| 1 | Incremented |
| **The setting of the DAMOD bit is invalid when the MODE bit is 1 (repeat mode) and the RPTSEL bit is 0 (transfer destination is the repeat area).** | |

Bit 2

| SAMOD | Transfer source address control |
|---|---|
| **0** | **Fixed** |
| 1 | Incremented |
| The setting of the SAMOD bit is invalid when the MODE bit is 1 (repeat mode) and the RPTSEL bit is 1 (transfer source is the repeat area). | |

Bit 1

| RPTSEL | Repeat area selection |
|---|---|
| **0** | **Transfer destination is the repeat area.** |
| 1 | Transfer source is the repeat area. |
| The setting of the RPTSEL bit is invalid when the MODE bit is 0 (normal mode). | |

Bit 0

| MODE | Transfer mode selection |
|---|---|
| 0 | Normal mode |
| **1** | **Repeat mode** |

DTC control register 3 setting

- DTC control register 3 (DTCCR3)
- Set to 8 bits (data size), chain transfers enabled, and normal mode (transfer mode).

Symbol: DTCCR3

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| 0 | SZ | RPTINT | CHNE | DAMOD | SAMOD | RPTSEL | MODE |
| **-** | **0** | **0** | **1** | **0** | **0** | **0** | **0** |

Bit 6

| SZ | Data size selection |
|---|---|
| **0** | **8 bits** |
| 1 | 16 bits |

Bit 5

| RPTINT | Enabling/disabling repeat mode interrupts |
|---|---|
| 0 | Interrupt generation disabled |
| 1 | Interrupt generation enabled |
| **The setting of the RPTINT bit is invalid when the MODE bit is 0 (normal mode).** | |

Bit 4

| CHNE | Enabling/disabling chain transfers |
|---|---|
| 0 | Chain transfers disabled |
| **1** | **Chain transfers enabled** |
| Set the CHNE bit in the DTCCR23 register to 0 (chain transfers disabled). | |

Bit 3

| DAMOD | Transfer destination address control |
|---|---|
| **0** | **Fixed** |
| 1 | Incremented |
| The setting of the DAMOD bit is invalid when the MODE bit is 1 (repeat mode) and the RPTSEL bit is 0 (transfer destination is the repeat area). | |

Bit 2

| SAMOD | Transfer source address control |
|---|---|
| **0** | **Fixed** |
| 1 | Incremented |
| The setting of the SAMOD bit is invalid when the MODE bit is 1 (repeat mode) and the RPTSEL bit is 1 (transfer source is the repeat area). | |

Bit 1

| RPTSEL | Repeat area selection |
|---|---|
| 0 | Transfer destination is the repeat area. |
| 1 | Transfer source is the repeat area. |
| **The setting of the RPTSEL bit is invalid when the MODE bit is 0 (normal mode).** | |

Bit 0

| MODE | Transfer mode selection |
|---|---|
| **0** | **Normal mode** |
| 1 | Repeat mode |

DTC control register 4 setting

- DTC control register 4 (DTCCR4)

Set to 8 bits (data size), chain transfer enabled, and normal mode (transfer mode).

Symbol: DTCCR4

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| 0 | SZ | RPTINT | CHNE | DAMOD | SAMOD | RPTSEL | MODE |
| **-** | **1** | **0** | **1** | **0** | **0** | **0** | **0** |

Bit 6

| SZ | Data size selection |
|---|---|
| 0 | 8 bits |
| **1** | **16 bits** |

Bit 5

| RPTINT | Enabling/disabling repeat mode interrupts |
|---|---|
| 0 | Interrupt generation disabled |
| 1 | Interrupt generation enabled |
| **The setting of the RPTINT bit is invalid when the MODE bit is 0 (normal mode).** | |

Bit 4

| CHNE | Enabling/disabling chain transfers |
|---|---|
| 0 | Chain transfers disabled |
| **1** | **Chain transfers enabled** |
| Set the CHNE bit in the DTCCR23 register to 0 (chain transfers disabled). | |

Bit 3

| DAMOD | Transfer destination address control |
|---|---|
| **0** | **Fixed** |
| 1 | Incremented |
| The setting of the DAMOD bit is invalid when the MODE bit is 1 (repeat mode) and the RPTSEL bit is 0 (transfer destination is the repeat area). | |

Bit 2

| SAMOD | Transfer source address control |
|---|---|
| **0** | **Fixed** |
| 1 | Incremented |
| The setting of the SAMOD bit is invalid when the MODE bit is 1 (repeat mode) and the RPTSEL bit is 1 (transfer source is the repeat area). | |

Bit 1

| RPTSEL | Repeat area selection |
|---|---|
| 0 | Transfer destination is the repeat area. |
| 1 | Transfer source is the repeat area. |
| **The setting of the RPTSEL bit is invalid when the MODE bit is 0 (normal mode).** | |

Bit 0

| MODE | Transfer mode selection |
|---|---|
| **0** | **Normal mode** |
| 1 | Repeat mode |

DTC control register 5 setting

- DTC control register 5 (DTCCR5)

Set to 8 bits (data size), chain transfers enabled, and normal mode (transfer mode).

Symbol: DTCCR5

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| 0 | SZ | RPTINT | CHNE | DAMOD | SAMOD | RPTSEL | MODE |
| **-** | **1** | **0** | **1** | **0** | **0** | **0** | **0** |

Bit 6

| SZ | Data size selection |
|---|---|
| 0 | 8 bits |
| **1** | **16 bits** |

Bit 5

| RPTINT | Enabling/disabling repeat mode interrupts |
|---|---|
| 0 | Interrupt generation disabled |
| 1 | Interrupt generation enabled |
| **The setting of the RPTINT bit is invalid when the MODE bit is 0 (normal mode).** | |

Bit 4

| CHNE | Enabling/disabling chain transfers |
|---|---|
| 0 | Chain transfers disabled |
| **1** | **Chain transfers enabled** |
| Set the CHNE bit in the DTCCR23 register to 0 (chain transfers disabled). | |

Bit 3

| DAMOD | Transfer destination address control |
|---|---|
| **0** | **Fixed** |
| 1 | Incremented |
| The setting of the DAMOD bit is invalid when the MODE bit is 1 (repeat mode) and the RPTSEL bit is 0 (transfer destination is the repeat area). | |

Bit 2

| SAMOD | Transfer source address control |
|---|---|
| **0** | **Fixed** |
| 1 | Incremented |
| The setting of the SAMOD bit is invalid when the MODE bit is 1 (repeat mode) and the RPTSEL bit is 1 (transfer source is the repeat area). | |

Bit 1

| RPTSEL | Repeat area selection |
|---|---|
| 0 | Transfer destination is the repeat area. |
| 1 | Transfer source is the repeat area. |
| **The setting of the RPTSEL bit is invalid when the MODE bit is 0 (normal mode).** | |

Bit 0

| MODE | Transfer mode selection |
|---|---|
| **0** | **Normal mode** |
| 1 | Repeat mode |

DTC control register 6 setting

- DTC control register 6 (DTCCR6)

Set to 8 bits (data size), chain transfers enabled, and normal mode (transfer mode).

Symbol: DTCCR6

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| 0 | SZ | RPTINT | CHNE | DAMOD | SAMOD | RPTSEL | MODE |
| **-** | **1** | **0** | **1** | **0** | **0** | **0** | **0** |

Bit 6

| SZ | Data size selection |
|---|---|
| 0 | 8 bits |
| **1** | **16 bits** |

Bit 5

| RPTINT | Enabling/disabling repeat mode interrupts |
|---|---|
| 0 | Interrupt generation disabled |
| 1 | Interrupt generation enabled |
| **The setting of the RPTINT bit is invalid when the MODE bit is 0 (normal mode).** | |

Bit 4

| CHNE | Enabling/disabling chain transfers |
|---|---|
| 0 | Chain transfers disabled |
| **1** | **Chain transfers enabled** |
| Set the CHNE bit in the DTCCR23 register to 0 (chain transfers disabled). | |

Bit 3

| DAMOD | Transfer destination address control |
|---|---|
| **0** | **Fixed** |
| 1 | Incremented |
| The setting of the DAMOD bit is invalid when the MODE bit is 1 (repeat mode) and the RPTSEL bit is 0 (transfer destination is the repeat area). | |

Bit 2

| SAMOD | Transfer source address control |
|---|---|
| **0** | **Fixed** |
| 1 | Incremented |
| The setting of the SAMOD bit is invalid when the MODE bit is 1 (repeat mode) and the RPTSEL bit is 1 (transfer source is the repeat area). | |

Bit 1

| RPTSEL | Repeat area selection |
|---|---|
| 0 | Transfer destination is the repeat area. |
| 1 | Transfer source is the repeat area. |
| **The setting of the RPTSEL bit is invalid when the MODE bit is 0 (normal mode).** | |

Bit 0

| MODE | Transfer mode selection |
|---|---|
| **0** | **Normal mode** |
| 1 | Repeat mode |

### DTC control register 7 setting

- DTC control register 7 (DTCCR7)

Set to 8 bits (data size), chain transfers enabled, and normal mode (transfer mode).

Symbol: DTCCR7

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| 0 | SZ | RPTINT | CHNE | DAMOD | SAMOD | RPTSEL | MODE |
| **-** | **0** | **0** | **1** | **0** | **0** | **0** | **0** |

Bit 6

| SZ | Data size selection |
|---|---|
| **0** | **8 bits** |
| 1 | 16 bits |

Bit 5

| RPTINT | Enabling/disabling repeat mode interrupts |
|---|---|
| 0 | Interrupt generation disabled |
| 1 | Interrupt generation enabled |
| **The setting of the RPTINT bit is invalid when the MODE bit is 0 (normal mode).** | |

Bit 4

| CHNE | Enabling/disabling chain transfers |
|---|---|
| 0 | Chain transfers disabled |
| **1** | **Chain transfers enabled** |
| Set the CHNE bit in the DTCCR23 register to 0 (chain transfers disabled). | |

Bit 3

| DAMOD | Transfer destination address control |
|---|---|
| **0** | **Fixed** |
| 1 | Incremented |
| The setting of the DAMOD bit is invalid when the MODE bit is 1 (repeat mode) and the RPTSEL bit is 0 (transfer destination is the repeat area). | |

Bit 2

| SAMOD | Transfer source address control |
|---|---|
| **0** | **Fixed** |
| 1 | Incremented |
| The setting of the SAMOD bit is invalid when the MODE bit is 1 (repeat mode) and the RPTSEL bit is 1 (transfer source is the repeat area). | |

Bit 1

| RPTSEL | Repeat area selection |
|---|---|
| 0 | Transfer destination is the repeat area. |
| 1 | Transfer source is the repeat area. |
| **The setting of the RPTSEL bit is invalid when the MODE bit is 0 (normal mode).** | |

Bit 0

| MODE | Transfer mode selection |
|---|---|
| **0** | **Normal mode** |
| 1 | Repeat mode |

### DTC control register 8 setting

- DTC control register 8 (DTCCR8)

Set to 8 bits (data size), chain transfers disabled, and normal mode (transfer mode).

Symbol: DTCCR8

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| 0 | SZ | RPTINT | CHNE | DAMOD | SAMOD | RPTSEL | MODE |
| **-** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |

Bit 6

| SZ | Data size selection |
|---|---|
| **0** | **8 bits** |
| 1 | 16 bits |

Bit 5

| RPTINT | Enabling/disabling repeat mode interrupts |
|---|---|
| 0 | Interrupt generation disabled |
| 1 | Interrupt generation enabled |
| **The setting of the RPTINT bit is invalid when the MODE bit is 0 (normal mode).** | |

Bit 4

| CHNE | Enabling/disabling chain transfers |
|---|---|
| **0** | **Chain transfers disabled** |
| 1 | Chain transfers enabled |
| Set the CHNE bit in the DTCCR23 register to 0 (chain transfers disabled). | |

Bit 3

| DAMOD | Transfer destination address control |
|---|---|
| **0** | **Fixed** |
| 1 | Incremented |
| The setting of the DAMOD bit is invalid when the MODE bit is 1 (repeat mode) and the RPTSEL bit is 0 (transfer destination is the repeat area). | |

Bit 2

| SAMOD | Transfer source address control |
|---|---|
| **0** | **Fixed** |
| 1 | Incremented |
| The setting of the SAMOD bit is invalid when the MODE bit is 1 (repeat mode) and the RPTSEL bit is 1 (transfer source is the repeat area). | |

Bit 1

| RPTSEL | Repeat area selection |
|---|---|
| 0 | Transfer destination is the repeat area. |
| 1 | Transfer source is the repeat area. |
| **The setting of the RPTSEL bit is invalid when the MODE bit is 0 (normal mode).** | |

Bit 0

| MODE | Transfer mode selection |
|---|---|
| **0** | **Normal mode** |
| 1 | Repeat mode |

DTC block size register 0 setting

-DTC block size register 0 (DTBLS0)

Set the block size to 1 byte.

Symbol: DTBLS0

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| DTBLS07 | DTBLS06 | DTBLS05 | DTBLS04 | DTBLS03 | DTBLS02 | DTBLS01 | DTBLS00 |
| **0** | **0** | **0** | **0** | **0** | **0** | **0** | **1** |

| DTBLS0 | Transfer block size | |
|---|---|---|
| | | |
| 00H | 256 bytes | 512 bytes |
| **01H** | **1 byte** | 2 bytes |
| 02H | 2 bytes | 4 bytes |
| • | • | • |
| • | • | • |
| • | • | • |
| FEH | 254 bytes | 508 bytes |
| FFH | 255 bytes | 510 bytes |

DTC block size register 1 setting

-DTC block size register 1 (DTBLS1)

Set the block size to 2 bytes.

Symbol: DTBLS1

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| DTBLS17 | DTBLS16 | DTBLS15 | DTBLS14 | DTBLS13 | DTBLS12 | DTBLS11 | DTBLS10 |
| **0** | **0** | **0** | **0** | **0** | **0** | **0** | **1** |

| DTBLS1 | Transfer block size | |
|---|---|---|
| | | |
| 00H | 256 bytes | 512 bytes |
| **01H** | 1 byte | **2 bytes** |
| 02H | 2 bytes | 4 bytes |
| • | • | • |
| • | • | • |
| • | • | • |
| FEH | 254 bytes | 508 bytes |
| FFH | 255 bytes | 510 bytes |

DTC block size register 2 setting

-DTC block size register 2 (DTBLS2)

Set the block size to 2 bytes.

Symbol: DTBLS2

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| DTBLS27 | DTBLS26 | DTBLS25 | DTBLS24 | DTBLS23 | DTBLS22 | DTBLS21 | DTBLS20 |
| **0** | **0** | **0** | **0** | **0** | **0** | **0** | **1** |

| DTBLS2 | Transfer block size | |
|---|---|---|
| 00H | 256 bytes | 512 bytes |
| **01H** | 1 byte | **2 bytes** |
| 02H | 2 bytes | 4 bytes |
| • • • | • • • | • • • |
| FEH | 254 bytes | 508 bytes |
| FFH | 255 bytes | 510 bytes |

DTC block size register 3 setting

-DTC block size register 3 (DTBLS3)

Set the block size to 1 byte.

Symbol: DTBLS3

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| DTBLS37 | DTBLS36 | DTBLS35 | DTBLS34 | DTBLS33 | DTBLS32 | DTBLS31 | DTBLS30 |
| **0** | **0** | **0** | **0** | **0** | **0** | **0** | **1** |

| DTBLS3 | Transfer block size | |
|---|---|---|
| 00H | 256 bytes | 512 bytes |
| **01H** | **1 byte** | 2 bytes |
| 02H | 2 bytes | 4 bytes |
| • • • | • • • | • • • |
| FEH | 254 bytes | 508 bytes |
| FFH | 255 bytes | 510 bytes |

DTC block size register 4 setting

-DTC block size register 4 (DTBLS4)

Set the block size to 2 bytes.

Symbol: DTBLS4

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| DTBLS47 | DTBLS46 | DTBLS45 | DTBLS44 | DTBLS43 | DTBLS42 | DTBLS41 | DTBLS40 |
| **0** | **0** | **0** | **0** | **0** | **0** | **0** | **1** |

| DTBLS4 | Transfer block size | |
|---|---|---|
| 00H | 256 bytes | 512 bytes |
| **01H** | 1 byte | **2 bytes** |
| 02H | 2 bytes | 4 bytes |
| • • • | • • • | • • • |
| FEH | 254 bytes | 508 bytes |
| FFH | 255 bytes | 510 bytes |

DTC block size register 5 setting

-DTC block size register 5 (DTBLS5)

Set the block size to 2 bytes.

Symbol: DTBLS5

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| DTBLS57 | DTBLS56 | DTBLS55 | DTBLS54 | DTBLS53 | DTBLS52 | DTBLS51 | DTBLS50 |
| **0** | **0** | **0** | **0** | **0** | **0** | **0** | **1** |

| DTBLS5 | Transfer block size | |
|---|---|---|
| 00H | 256 bytes | 512 bytes |
| **01H** | 1 byte | **2 bytes** |
| 02H | 2 bytes | 4 bytes |
| • • • | • • • | • • • |
| FEH | 254 bytes | 508 bytes |
| FFH | 255 bytes | 510 bytes |

DTC block size register 6 setting

-DTC block size register 6 (DTBLS6)

Set the block size to 2 bytes.

Symbol: DTBLS6

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| DTBLS67 | DTBLS66 | DTBLS65 | DTBLS64 | DTBLS63 | DTBLS62 | DTBLS61 | DTBLS60 |
| **0** | **0** | **0** | **0** | **0** | **0** | **0** | **1** |

| DTBLS6 | Transfer block size | |
|---|---|---|
| 00H | 256 bytes | 512 bytes |
| **01H** | 1 byte | **2 bytes** |
| 02H | 2 bytes | 4 bytes |
| • • • | • • • | • • • |
| FEH | 254 bytes | 508 bytes |
| FFH | 255 bytes | 510 bytes |

DTC block size register 7 setting

-DTC block size register 7 (DTBLS7)

Set the block size to 1 byte.

Symbol: DTBLS7

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| DTBLS77 | DTBLS76 | DTBLS75 | DTBLS74 | DTBLS73 | DTBLS72 | DTBLS71 | DTBLS70 |
| **0** | **0** | **0** | **0** | **0** | **0** | **0** | **1** |

| DTBLS7 | Transfer block size | |
|---|---|---|
| 00H | 256 bytes | 512 bytes |
| **01H** | **1 byte** | 2 bytes |
| 02H | 2 bytes | 4 bytes |
| • • • | • • • | • • • |
| FEH | 254 bytes | 508 bytes |
| FFH | 255 bytes | 510 bytes |

DTC block size register 8 setting

-DTC block size register 8 (DTBLS8)

Set the block size to 1 byte.

Symbol: DTBLS8

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| DTBLS87 | DTBLS86 | DTBLS85 | DTBLS84 | DTBLS83 | DTBLS82 | DTBLS81 | DTBLS80 |
| **0** | **0** | **0** | **0** | **0** | **0** | **0** | **1** |

| DTBLS8 | Transfer block size | |
|---|---|---|
| | | |
| 00H | 256 bytes | 512 bytes |
| **01H** | **1 byte** | 2 bytes |
| 02H | 2 bytes | 4 bytes |
| • • • | • • • | • • • |
| FEH | 254 bytes | 508 bytes |
| FFH | 255 bytes | 510 bytes |

### DTC transfer count register 0 setting

- DTC transfer count register 0 (DTCCT0)

Set the number of DTC data transfers to once.

Symbol: DTCCT0

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| DTCCT07 | DTCCT06 | DTCCT05 | DTCCT04 | DTCCT03 | DTCCT02 | DTCCT01 | DTCCT00 |
| **0** | **0** | **0** | **0** | **0** | **0** | **0** | **1** |

| DTCCT0 | Number of transfers |
|---|---|
| 00H | 256 times |
| **01H** | **Once** |
| 02H | 2 times |
| • | • |
| • | • |
| • | • |
| FEH | 254 times |
| FFH | 255 times |

### DTC transfer count register 1 setting

- DTC transfer count register 1 (DTCCT1)

Set the number of DTC data transfers to once.

Symbol: DTCCT1

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| DTCCT17 | DTCCT16 | DTCCT15 | DTCCT14 | DTCCT13 | DTCCT12 | DTCCT11 | DTCCT10 |
| **0** | **0** | **0** | **0** | **0** | **0** | **0** | **1** |

| DTCCT1 | Number of transfers |
|---|---|
| 00H | 256 times |
| **01H** | **Once** |
| 02H | 2 times |
| • | • |
| • | • |
| • | • |
| FEH | 254 times |
| FFH | 255 times |

### DTC transfer count register 2 setting

- DTC transfer count register 2 (DTCCT2)

Set the number of DTC data transfers to 4 times.

Symbol: DTCCT2

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| DTCCT27 | DTCCT26 | DTCCT25 | DTCCT24 | DTCCT23 | DTCCT22 | DTCCT21 | DTCCT20 |
| **0** | **0** | **0** | **0** | **0** | **1** | **0** | **0** |

| DTCCT2 | Number of transfers |
|---|---|
| 00H | 256 times |
| 01H | Once |
| 02H | 2 times |
| • | • |
| • | • |
| • | • |
| **04H** | **4 times** |
| • | • |
| • | • |
| • | • |
| FEH | 254 times |
| FFH | 255 times |

### DTC transfer count register 3 setting

- DTC transfer count register 3 (DTCCT3)

Set the number of DTC data transfers to 4 times.

Symbol: DTCCT3

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| DTCCT37 | DTCCT36 | DTCCT35 | DTCCT34 | DTCCT33 | DTCCT32 | DTCCT31 | DTCCT30 |
| **0** | **0** | **0** | **0** | **0** | **1** | **0** | **0** |

| DTCCT3 | Number of transfers |
|---|---|
| 00H | 256 times |
| 01H | Once |
| 02H | 2 times |
| • | • |
| • | • |
| • | • |
| **04H** | **4 times** |
| • | • |
| • | • |
| • | • |
| FEH | 254 times |
| FFH | 255 times |

### DTC transfer count register 4 setting

- DTC transfer count register 4 (DTCCT4)

Set the number of DTC data transfers to 4 times.

Symbol: DTCCT4

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| DTCCT47 | DTCCT46 | DTCCT45 | DTCCT44 | DTCCT43 | DTCCT42 | DTCCT41 | DTCCT40 |
| **0** | **0** | **0** | **0** | **0** | **1** | **0** | **0** |

| DTCCT4 | Number of transfers |
|---|---|
| 00H | 256 times |
| 01H | Once |
| 02H | 2 times |
| • | • |
| • | • |
| • | • |
| **04H** | **4 times** |
| • | • |
| • | • |
| • | • |
| FEH | 254 times |
| FFH | 255 times |

### DTC transfer count register 5 setting

- DTC transfer count register 5 (DTCCT5)

Set the number of DTC data transfers to 4 times.

Symbol: DTCCT5

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| DTCCT57 | DTCCT56 | DTCCT55 | DTCCT54 | DTCCT53 | DTCCT52 | DTCCT51 | DTCCT50 |
| **0** | **0** | **0** | **0** | **0** | **1** | **0** | **0** |

| DTCCT5 | Number of transfers |
|---|---|
| 00H | 256 times |
| 01H | Once |
| 02H | 2 times |
| • | • |
| • | • |
| • | • |
| **04H** | **4 times** |
| • | • |
| • | • |
| • | • |
| FEH | 254 times |
| FFH | 255 times |

### DTC transfer count register 6 setting

- DTC transfer count register 6 (DTCCT6)

Set the number of DTC data transfers to 4 times.

Symbol: DTCCT6

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| DTCCT67 | DTCCT66 | DTCCT65 | DTCCT64 | DTCCT63 | DTCCT62 | DTCCT61 | DTCCT60 |
| **0** | **0** | **0** | **0** | **0** | **1** | **0** | **0** |

| DTCCT6 | Number of transfers |
|---|---|
| 00H | 256 times |
| 01H | Once |
| 02H | 2 times |
| • | • |
| • | • |
| • | • |
| **04H** | **4 times** |
| • | • |
| • | • |
| • | • |
| FEH | 254 times |
| FFH | 255 times |

### DTC transfer count register 7 setting

- DTC transfer count register 7 (DTCCT7)

Set the number of DTC data transfers to 4 times.

Symbol: DTCCT7

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| DTCCT77 | DTCCT76 | DTCCT75 | DTCCT74 | DTCCT73 | DTCCT72 | DTCCT71 | DTCCT70 |
| **0** | **0** | **0** | **0** | **0** | **1** | **0** | **0** |

| DTCCT7 | Number of transfers |
|---|---|
| 00H | 256 times |
| 01H | Once |
| 02H | 2 times |
| • | • |
| • | • |
| • | • |
| **04H** | **4 times** |
| • | • |
| • | • |
| • | • |
| FEH | 254 times |
| FFH | 255 times |

DTC transfer count register 8 setting

- DTC transfer count register 8 (DTCCT8)

Set the number of DTC data transfers to 4 times.

Symbol: DTCCT8

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| DTCCT87 | DTCCT86 | DTCCT85 | DTCCT84 | DTCCT83 | DTCCT82 | DTCCT81 | DTCCT80 |
| **0** | **0** | **0** | **0** | **0** | **1** | **0** | **0** |

| DTCCT8 | Number of transfers |
|---|---|
| 00H | 256 times |
| 01H | Once |
| 02H | 2 times |
| • | • |
| • | • |
| • | • |
| **04H** | **4 times** |
| • | • |
| • | • |
| • | • |
| FEH | 254 times |
| FFH | 255 times |

### DTC transfer count reload register 0 setting

-DTC transfer count reload register 0 (DTRLD0)
Set the transfer reload count to once.

Symbol: DTRLD0

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| DTRLD07 | DTRLD06 | DTRLD05 | DTRLD04 | DTRLD03 | DTRLD02 | DTRLD01 | DTRLD00 |
| **0** | **0** | **0** | **0** | **0** | **0** | **0** | **1** |

### DTC transfer count reload register 1 setting

-DTC transfer count reload register 1 (DTRLD1)
Set the transfer reload count to zero.

Symbol: DTRLD1

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| DTRLD17 | DTRLD16 | DTRLD15 | DTRLD14 | DTRLD13 | DTRLD12 | DTRLD11 | DTRLD10 |
| **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |

### DTC transfer count reload register 2 setting

-DTC transfer count reload register 2 (DTRLD2)
Set the transfer reload count to 4 times.

Symbol: DTRLD2

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| DTRLD27 | DTRLD26 | DTRLD25 | DTRLD24 | DTRLD23 | DTRLD22 | DTRLD21 | DTRLD20 |
| **0** | **0** | **0** | **0** | **0** | **1** | **0** | **0** |

### DTC transfer count reload register 3 setting

-DTC transfer count reload register 3 (DTRLD3)
Set the transfer reload count to zero.

Symbol: DTRLD3

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| DTRLD37 | DTRLD36 | DTRLD35 | DTRLD34 | DTRLD33 | DTRLD32 | DTRLD31 | DTRLD30 |
| **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |

### DTC transfer count reload register 4 setting

-DTC transfer count reload register 4 (DTRLD4)
Set the transfer reload count to zero.

Symbol: DTRLD4

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| DTRLD47 | DTRLD46 | DTRLD45 | DTRLD44 | DTRLD43 | DTRLD42 | DTRLD41 | DTRLD40 |
| **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |

### DTC transfer count reload register 5 setting

-DTC transfer count reload register 5 (DTRLD5)
Set the transfer reload count to zero.

Symbol: DTRLD5

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| DTRLD57 | DTRLD56 | DTRLD55 | DTRLD54 | DTRLD53 | DTRLD52 | DTRLD51 | DTRLD50 |
| **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |

### DTC transfer count reload register 6 setting

-DTC transfer count reload register 6 (DTRLD6)
Set the transfer reload count to zero.

Symbol: DTRLD6

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| DTRLD67 | DTRLD66 | DTRLD65 | DTRLD64 | DTRLD63 | DTRLD62 | DTRLD61 | DTRLD60 |
| **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |

### DTC transfer count reload register 7 setting

- DTC transfer count reload register 7 (DTRLD7)
Set the transfer reload count to zero.

Symbol: DTRLD7

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| DTRLD77 | DTRLD76 | DTRLD75 | DTRLD74 | DTRLD73 | DTRLD72 | DTRLD71 | DTRLD70 |
| **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |

DTC transfer count reload register 8 setting

-DTC transfer count reload register 8 (DTRLD8)
Set the transfer reload count to zero.

Symbol: DTRLD8

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| DTRLD87 | DTRLD86 | DTRLD85 | DTRLD84 | DTRLD83 | DTRLD82 | DTRLD81 | DTRLD80 |
| **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |

### DTC source address register 0 setting

- DTC source address register 0 (DTSAR0).
  Set the transfer destination address to “FD00H”.

Symbol: DTSAR0

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| DTSAR0 15 | DTSAR0 14 | DTSAR0 13 | DTSAR0 12 | DTSAR0 11 | DTSAR0 10 | DTSAR0 9 | DTSAR0 8 | DTSAR0 7 | DTSAR0 6 | DTSAR0 5 | DTSAR0 4 | DTSAR0 3 | DTSAR0 2 | DTSAR0 1 | DTSAR0 0 |
| **1** | **1** | **1** | **1** | **1** | **1** | **0** | **1** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |

### DTC source address register 1 setting

- DTC source address register 1 (DTSAR1)
  Set the transfer destination address to “FD04H”.

Symbol: DTSAR1

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| DTSAR1 15 | DTSAR1 14 | DTSAR1 13 | DTSAR1 12 | DTSAR1 11 | DTSAR1 10 | DTSAR1 9 | DTSAR1 8 | DTSAR1 7 | DTSAR1 6 | DTSAR1 5 | DTSAR1 4 | DTSAR1 3 | DTSAR1 2 | DTSAR1 1 | DTSAR1 0 |
| **1** | **1** | **1** | **1** | **1** | **1** | **0** | **1** | **0** | **0** | **0** | **0** | **0** | **1** | **0** | **0** |

### DTC source address register 2 setting

- DTC source address register 2 (DTSAR2)
  Set the transfer destination address to “FF1EH”.

Symbol: DTSAR2

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| DTSAR2 15 | DTSAR2 14 | DTSAR2 13 | DTSAR2 12 | DTSAR2 11 | DTSAR2 10 | DTSAR2 9 | DTSAR2 8 | DTSAR2 7 | DTSAR2 6 | DTSAR2 5 | DTSAR2 4 | DTSAR2 3 | DTSAR2 2 | DTSAR2 1 | DTSAR2 0 |
| **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **0** | **0** | **0** | **1** | **1** | **1** | **1** | **0** |

### DTC source address register 3 setting

- DTC source address register 3 (DTSAR3)
  Set the transfer destination address to “FD02H”.

Symbol: DTSAR3

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| DTSAR3 15 | DTSAR3 14 | DTSAR3 13 | DTSAR3 12 | DTSAR3 11 | DTSAR3 10 | DTSAR3 9 | DTSAR3 8 | DTSAR3 7 | DTSAR3 6 | DTSAR3 5 | DTSAR3 4 | DTSAR3 3 | DTSAR3 2 | DTSAR3 1 | DTSAR3 0 |
| **1** | **1** | **1** | **1** | **1** | **1** | **0** | **1** | **0** | **0** | **0** | **0** | **0** | **0** | **1** | **0** |

### DTC source address register 4 setting

- DTC source address register 4 (DTSAR4)
  Set the transfer destination address to “FD06H”.

Symbol: DTSAR4

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| DTSAR4 15 | DTSAR4 14 | DTSAR4 13 | DTSAR4 12 | DTSAR4 11 | DTSAR4 10 | DTSAR4 9 | DTSAR4 8 | DTSAR4 7 | DTSAR4 6 | DTSAR4 5 | DTSAR4 4 | DTSAR4 3 | DTSAR4 2 | DTSAR4 1 | DTSAR4 0 |
| **1** | **1** | **1** | **1** | **1** | **1** | **0** | **1** | **0** | **0** | **0** | **0** | **0** | **1** | **1** | **0** |

### DTC source address register 5 setting

- DTC source address register 5 (DTSAR5)
  Set the transfer destination address to “FF1EH”.

Symbol: DTSAR5

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| DTSAR5 15 | DTSAR5 14 | DTSAR5 13 | DTSAR5 12 | DTSAR5 11 | DTSAR5 10 | DTSAR5 9 | DTSAR5 8 | DTSAR5 7 | DTSAR5 6 | DTSAR5 5 | DTSAR5 4 | DTSAR5 3 | DTSAR5 2 | DTSAR5 1 | DTSAR5 0 |
| **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **0** | **0** | **0** | **1** | **1** | **1** | **1** | **0** |

### DTC source address register 6 setting

- DTC source address register 6 (DTSAR6)
  Set the transfer destination address to “FD0CH”.

Symbol: DTSAR6

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| DTSAR6 15 | DTSAR6 14 | DTSAR6 13 | DTSAR6 12 | DTSAR6 11 | DTSAR6 10 | DTSAR6 9 | DTSAR6 8 | DTSAR6 7 | DTSAR6 6 | DTSAR6 5 | DTSAR6 4 | DTSAR6 3 | DTSAR6 2 | DTSAR6 1 | DTSAR6 0 |
| **1** | **1** | **1** | **1** | **1** | **1** | **0** | **1** | **0** | **0** | **0** | **0** | **1** | **1** | **0** | **0** |

### DTC source address register 7 setting

- DTC source address register 7 (DTSAR7)
  Set the transfer destination address to “FD08H”.

Symbol: DTSAR7

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| DTSAR7 15 | DTSAR7 14 | DTSAR7 13 | DTSAR7 12 | DTSAR7 11 | DTSAR7 10 | DTSAR7 9 | DTSAR7 8 | DTSAR7 7 | DTSAR7 6 | DTSAR7 5 | DTSAR7 4 | DTSAR7 3 | DTSAR7 2 | DTSAR7 1 | DTSAR7 0 |
| **1** | **1** | **1** | **1** | **1** | **1** | **0** | **1** | **0** | **0** | **0** | **0** | **1** | **0** | **0** | **0** |

DTC source address register 8 setting

- DTC source address register 8 (DTSAR8)
  Set the transfer destination address to “FD0AH”.

Symbol: DTSAR8

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| DTSAR8 15 | DTSAR8 14 | DTSAR8 13 | DTSAR8 12 | DTSAR8 11 | DTSAR8 10 | DTSAR8 9 | DTSAR8 8 | DTSAR8 7 | DTSAR8 6 | DTSAR8 5 | DTSAR8 4 | DTSAR8 3 | DTSAR8 2 | DTSAR8 1 | DTSAR8 0 |
| **1** | **1** | **1** | **1** | **1** | **1** | **0** | **1** | **0** | **0** | **0** | **0** | **1** | **0** | **1** | **0** |

### DTC destination address register 0 setting

- DTC destination address register 0 (DTDAR0)
  Set the transfer source address to “FF05H”.

Symbol: DTDAR0

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| DTDAR015 | DTDAR014 | DTDAR013 | DTDAR012 | DTDAR011 | DTDAR010 | DTDAR09 | DTDAR08 | DTDAR07 | DTDAR06 | DTDAR05 | DTDAR04 | DTDAR03 | DTDAR02 | DTDAR01 | DTDAR00 |
| **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **0** | **0** | **0** | **0** | **0** | **1** | **0** | **1** |

### DTC destination address register 1 setting

- DTC destination address register 1 (DTDAR1)
  Set the transfer source address to “FF90H”.

Symbol: DTDAR1

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| DTDAR115 | DTDAR114 | DTDAR113 | DTDAR112 | DTDAR111 | DTDAR110 | DTDAR19 | DTDAR18 | DTDAR17 | DTDAR16 | DTDAR15 | DTDAR14 | DTDAR13 | DTDAR12 | DTDAR11 | DTDAR10 |
| **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **0** | **0** | **1** | **0** | **0** | **0** | **0** |

### DTC destination address register 2 setting

- DTC destination address register 2 (DTDAR2)
  Set the transfer source address to “FC04H”.

Symbol: DTDAR2

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| DTDAR215 | DTDAR214 | DTDAR213 | DTDAR212 | DTDAR211 | DTDAR210 | DTDAR29 | DTDAR28 | DTDAR27 | DTDAR26 | DTDAR25 | DTDAR24 | DTDAR23 | DTDAR22 | DTDAR21 | DTDAR20 |
| **1** | **1** | **1** | **1** | **1** | **1** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **1** | **0** | **0** |

### DTC destination address register 3 setting

- DTC destination address register 3 (DTDAR3)
  Set the transfer source address to “FF05H”.

Symbol: DTDAR3

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| DTDAR315 | DTDAR314 | DTDAR313 | DTDAR312 | DTDAR311 | DTDAR310 | DTDAR39 | DTDAR38 | DTDAR37 | DTDAR36 | DTDAR35 | DTDAR34 | DTDAR33 | DTDAR32 | DTDAR31 | DTDAR30 |
| **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **0** | **0** | **0** | **0** | **0** | **1** | **0** | **1** |

### DTC destination address register 4 setting

- DTC destination address register 4 (DTDAR4)
  Set the transfer source address to “FF90H”.

Symbol: DTDAR4

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| DTDAR4 15 | DTDAR4 14 | DTDAR4 13 | DTDAR4 12 | DTDAR4 11 | DTDAR4 10 | DTDAR4 9 | DTDAR4 8 | DTDAR4 7 | DTDAR4 6 | DTDAR4 5 | DTDAR4 4 | DTDAR4 3 | DTDAR4 2 | DTDAR4 1 | DTDAR4 0 |
| **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **0** | **0** | **1** | **0** | **0** | **0** | **0** |

### DTC destination address register 5 setting

- DTC destination address register 5 (DTDAR5)
  Set the transfer source address to “0512H”.

Symbol: DTDAR5

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| DTDAR5 15 | DTDAR5 14 | DTDAR5 13 | DTDAR5 12 | DTDAR5 11 | DTDAR5 10 | DTDAR5 9 | DTDAR5 8 | DTDAR5 7 | DTDAR5 6 | DTDAR5 5 | DTDAR5 4 | DTDAR5 3 | DTDAR5 2 | DTDAR5 1 | DTDAR5 0 |
| **0** | **0** | **0** | **0** | **0** | **1** | **0** | **1** | **0** | **0** | **0** | **1** | **0** | **0** | **1** | **0** |

### DTC destination address register 6 setting

- DTC destination address register 6 (DTDAR6)
  Set the transfer source address to “0514H”.

Symbol: DTDAR6

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| DTDAR6 15 | DTDAR6 14 | DTDAR6 13 | DTDAR6 12 | DTDAR6 11 | DTDAR6 10 | DTDAR6 9 | DTDAR6 8 | DTDAR6 7 | DTDAR6 6 | DTDAR6 5 | DTDAR6 4 | DTDAR6 3 | DTDAR6 2 | DTDAR6 1 | DTDAR6 0 |
| **0** | **0** | **0** | **0** | **0** | **1** | **0** | **1** | **0** | **0** | **0** | **1** | **0** | **1** | **0** | **0** |

### DTC destination address register 7 setting

- DTC destination address register 7 (DTDAR7)
  Set the transfer source address to “0010H”.

Symbol: DTDAR7

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| DTDAR7 15 | DTDAR7 14 | DTDAR7 13 | DTDAR7 12 | DTDAR7 11 | DTDAR7 10 | DTDAR7 9 | DTDAR7 8 | DTDAR7 7 | DTDAR7 6 | DTDAR7 5 | DTDAR7 4 | DTDAR7 3 | DTDAR7 2 | DTDAR7 1 | DTDAR7 0 |
| **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **1** | **0** | **0** | **0** | **0** |

### DTC destination address register 8 setting

- DTC destination address register 8 (DTDAR8)
  Set the transfer source address to “0010H”.

Symbol: DTDAR8

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| DTDAR8 15 | DTDAR8 14 | DTDAR8 13 | DTDAR8 12 | DTDAR8 11 | DTDAR8 10 | DTDAR8 9 | DTDAR8 8 | DTDAR8 7 | DTDAR8 6 | DTDAR8 5 | DTDAR8 4 | DTDAR8 3 | DTDAR8 2 | DTDAR8 1 | DTDAR8 0 |
| **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **1** | **0** | **0** | **0** | **0** |

### 5.7.10 ELC Initialization

Figure 5.13 is a flowchart for initial setting of the ELC.

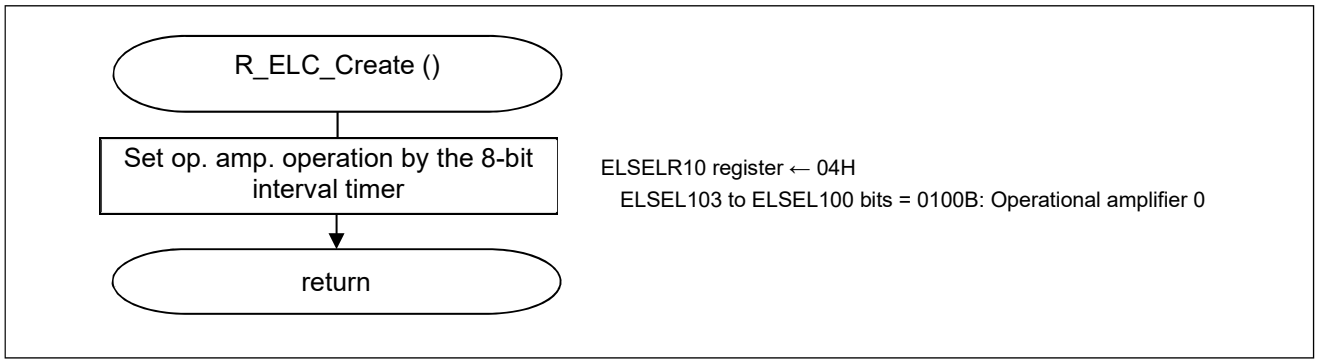


**Figure 5.13 Initial Setting of the ELC**

Operational amplifier operation setting by the 8-bit interval timer

- Event output destination select register 10 (ELSELR10)

Set operation start of the operational amplifiers by compare match of the 8-bit interval timer.

Symbol: ELSELR10

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | ELSEL103 | ELSEL102 | ELSEL101 | ELSEL100 |
| x | x | x | x | **0** | **1** | **0** | **0** |

Bits 3 to 0

| Bit 3 | Bit 2 | Bit 1 | Bit 0 | Event link selection of 8-bit interval timer 0 selection |
|---|---|---|---|---|
| 0 | 0 | 0 | 0 | Event link disabled |
| 0 | 0 | 0 | 1 | Select operation of peripheral function 1 to link |
| 0 | 0 | 1 | 0 | Select operation of peripheral function 2 to link |
| 0 | 0 | 1 | 1 | Select operation of peripheral function 3 to link |
| **0** | **1** | **0** | **0** | **Peripheral function to link: operational amplifier 0 Operation at event acceptance: Operation start** |
| 0 | 1 | 0 | 1 | Select operation of peripheral function 5 to link |
| 0 | 1 | 1 | 0 | Select operation of peripheral function 6 to link |
| 0 | 1 | 1 | 1 | Select operation of peripheral function 7 to link |
| **Other than above** | | | | Setting prohibited |

### 5.7.11 DOC Initialization

Figure 5.14 is a flowchart for initial setting of DOC.

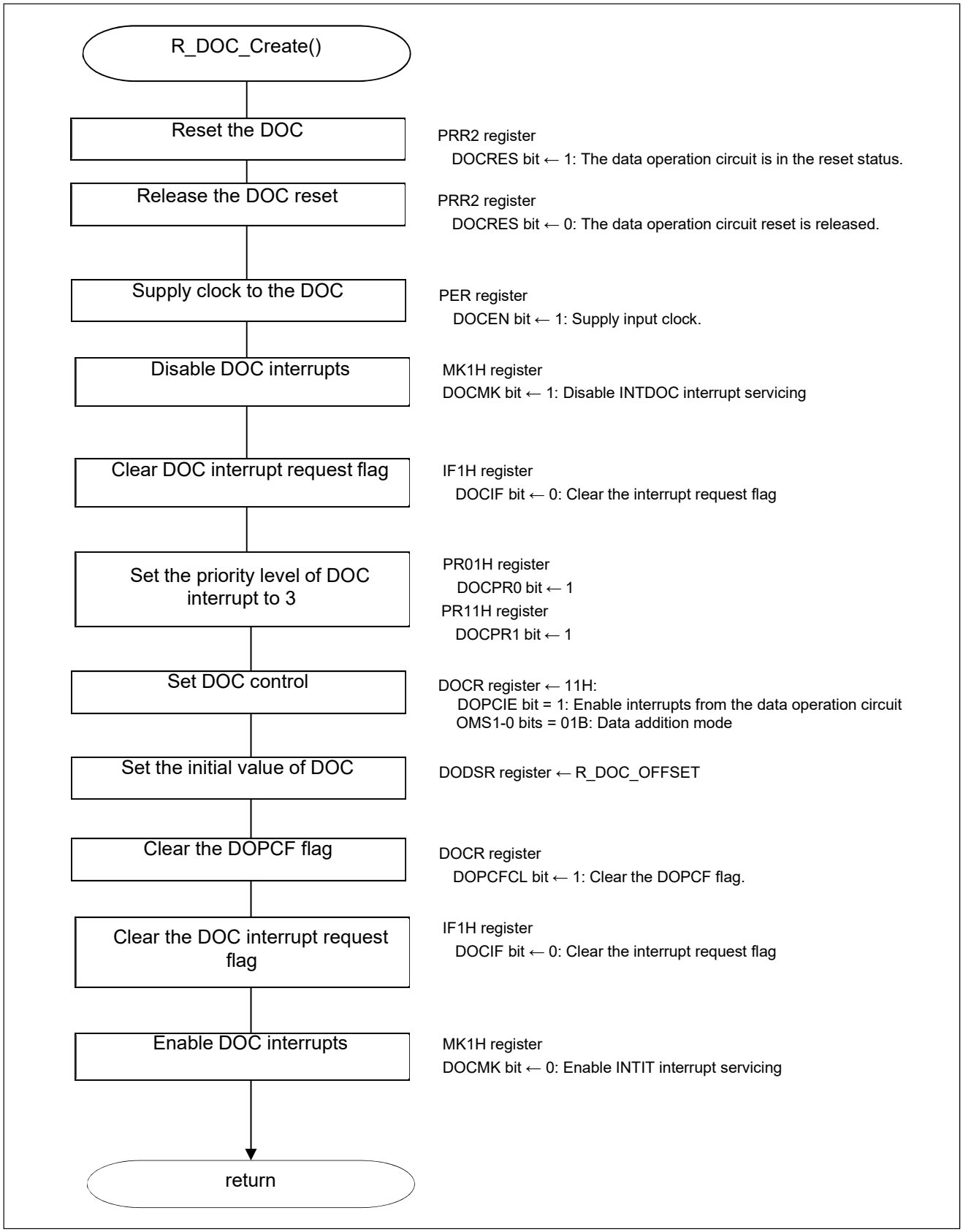


**Figure 5.14 Initial Setting of the DOC**

DOC reset

- Peripheral reset control register 2 (PRR2)
  Reset DOC.

Symbol: PRR2

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| TMKARES | 0 | DOCRES | 0 | 0 | 0 | 0 | 0 |
| x | x | **1** | x | x | x | x | x |

Bit 5

| DOCRES | Reset control of data operation circuit |
|---|---|
| 0 | The data operation circuit reset is released. |
| **1** | **The data operation circuit is in the reset status.** |

DOC reset release

- Peripheral reset control register 2 (PRR2)
  Release the DOC reset status.

Symbol: PRR2

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| TMKARES | 0 | DOCRES | 0 | 0 | 0 | 0 | 0 |
| x | x | **0** | x | x | x | x | x |

Bit 5

| DOCRES | Reset control of data operation circuit |
|---|---|
| **0** | **The data operation circuit reset is released.** |
| 1 | The data operation circuit is in the reset status. |

DOC clock supply start

- Peripheral enable register 2 (PER2)

Start DOC clock supply.

Symbol: PER2

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| TMKAEN | FMCEN | DOCEN | 0 | 0 | 0 | 0 | 0 |
| x | x | **1** | x | x | x | x | x |

Bit 5

| DOCEN | Control of data operation circuit input clock supply |
|---|---|
| 0 | Stops input clock supply. |
| **1** | **Supplies input clock.** |

DOC interrupt setting

-Interrupt mask flag register (MK1H)

Disable interrupt servicing.

-Interrupt request flag register (IF1H)

Clear the interrupt request flag.

Symbol: MK1H

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| 0 | DOCMK | CMPMK1 | CMPMK0 | KRMK | TMKAMK | RTCMK | ADMK |
| x | **1** | x | x | x | x | x | x |

Bit 6

| DOCMK | Interrupt servicing control |
|---|---|
| 0 | Interrupt servicing enabled |
| **1** | **Interrupt servicing disabled** |

Symbol: IF1H

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| 0 | DOCIF | CMPIF1 | CMPIF0 | KRIF | TMKAIFI | RTCIF | ADIF |
| x | **0** | x | x | x | x | x | x |

Bit 6

| DOCIF | Interrupt request flag |
|---|---|
| **0** | **No interrupt request signal is generated.** |
| 1 | Interrupt request is generated, interrupt request status |

Data operation circuit interrupt priority level setting

- Priority specification flag register (PR11H, PR01H)
  Specify level 3 (low priority level).

Symbol: PR11H

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| 0 | DOCPR1 | CMPPR11 | CMPPR10 | KRPR1 | TMKAPR1 | RTCPR1 | ADPR1 |
| x | **1** | x | x | x | x | x | x |

Symbol: : PR01H

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| 0 | DOCPR0 | CMPPR01 | CMPPR00 | KRPR0 | TMKAPR0 | RTCPR0 | ADPR0 |
| x | **1** | x | x | x | x | x | x |

Bit 6

| DOCPR1 | DOCPR0 | Priority level selection |
|---|---|---|
| 0 | 0 | Specify level 0 (high priority level) |
| 0 | 1 | Specify level 1. |
| 1 | 0 | Specify level 2. |
| **1** | **1** | **Specify level 3 (low priority level)** |

Data operation circuit control setting

- DOC control register (DOCR)

Select the data addition mode and enable interrupts form the data operation circuit.

Symbol: DOCR

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| 0 | DOPCFCL | DOPCF | DOPCIE | 0 | DCSEL | OMS1 | OMS0 |
| x | x | x | **1** | x | x | **0** | **1** |

Bit 4

| DOPCIE | Data operation circuit interrupt enabling |
|---|---|
| 0 | Disables interrupts from the data operation circuit. |
| **1** | **Enables interrupts from the data operation circuit.** |

Bits 1 to 0

| OMS1 | OMS0 | Operating mode selection |
|---|---|---|
| 0 | 0 | Data comparison mode |
| **0** | **1** | **Data addition mode** |
| 1 | 0 | Data subtraction mode |
| 1 | 1 | Setting prohibited |

Data operation circuit initial value setting

- DOC data setting register (DODSR)

Set an initial value of the data operation circuit.

Symbol: DODSR

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| **1** | **1** | **1** | **1** | **0** | **1** | **0** | **0** | **1** | **0** | **0** | **0** | **0** | **0** | **1** | **0** |

Bit 15 to bit 0

| Function |
|---|
| **In data addition mode and data subtraction mode, the operation result is stored.** |

### DOPCF flag clear

- DOC control register (DOCR)
  Clear the DOPCF flag.

Symbol: DOCR

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| 0 | DOPCFCL | DOPCF | DOPCIE | 0 | DCSEL | OMS1 | OMS0 |
| x | **1** | x | x | x | x | x | x |

Bit 6

| DOPCFCL | DOPCF clear |
|---|---|
| 0 | Maintains the DOPCF flag state. |
| **1** | **Clears the DOPCF flag.** |

### DOC interrupt setting

- Interrupt request flag register (IF1H)
  Clear the interrupt request flag.
- Interrupt mask flag register (MK1H)
  Enable interrupt servicing.

Symbol: IF1H

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| 0 | DOCIF | CMPIF1 | CMPIF0 | KRIF | TMKAIFI | RTCIF | ADIF |
| x | **0** | x | x | x | x | x | x |

Bit 6

| DOCIF | Interrupt request flag |
|---|---|
| **0** | **No interrupt request signal is generated.** |
| 1 | Interrupt request is generated, interrupt request status |

Symbol: MK1H

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| 0 | DOCMK | CMPMK1 | CMPMK0 | KRMK | TMKAMK | RTCMK | ADMK |
| x | **0** | x | x | x | x | x | x |

Bit 6

| DOCMK | Interrupt servicing control |
|---|---|
| **0** | **Interrupt servicing enabled** |
| 1 | Interrupt servicing disabled |

### 5.7.12 Main Processing

Figure 5.15 is a flowchart of main processing.

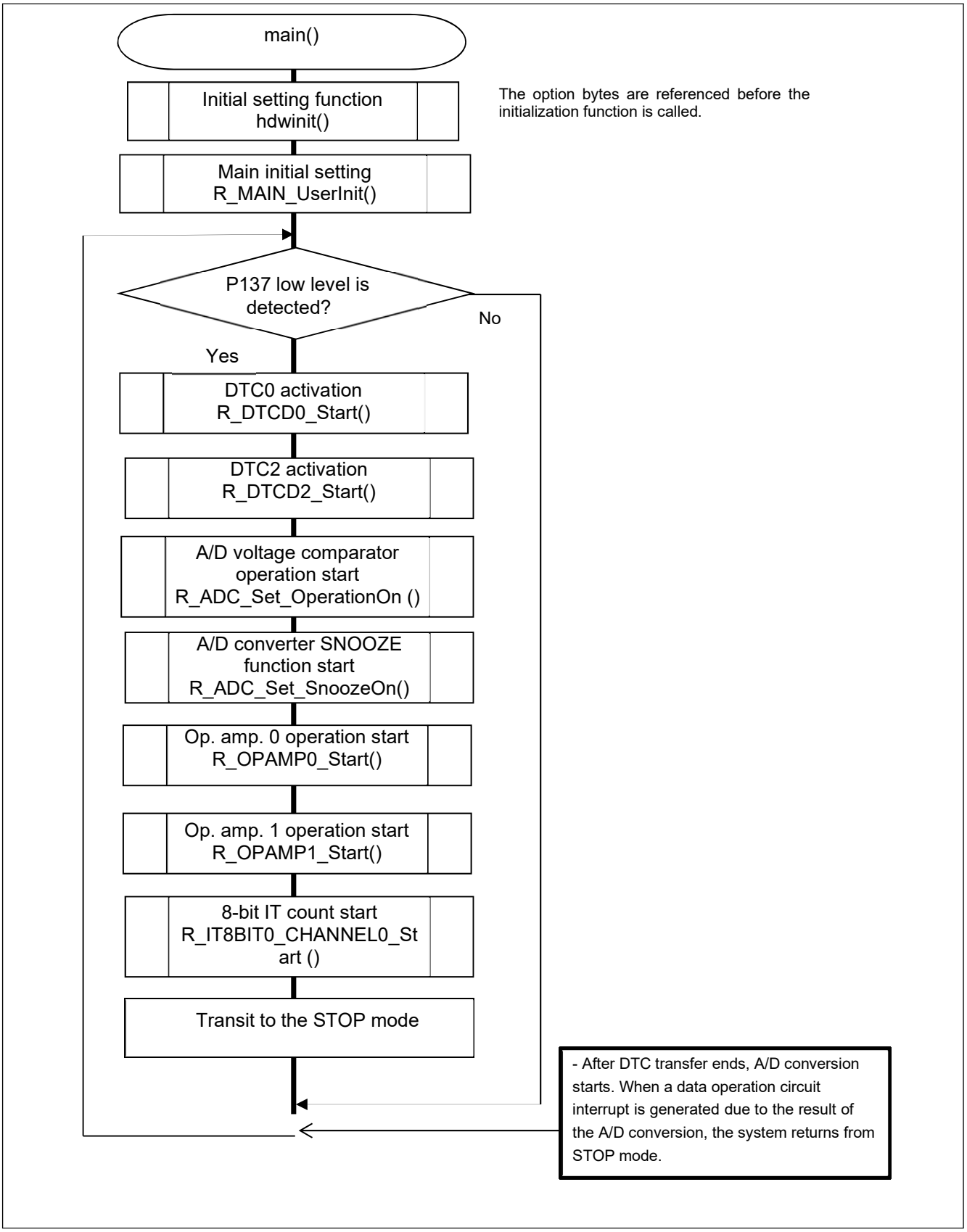


**Figure 5.15 Main Processing**

### 5.7.13 Main Initialization

Figure 5.16 shows a flowchart for main initial setting.

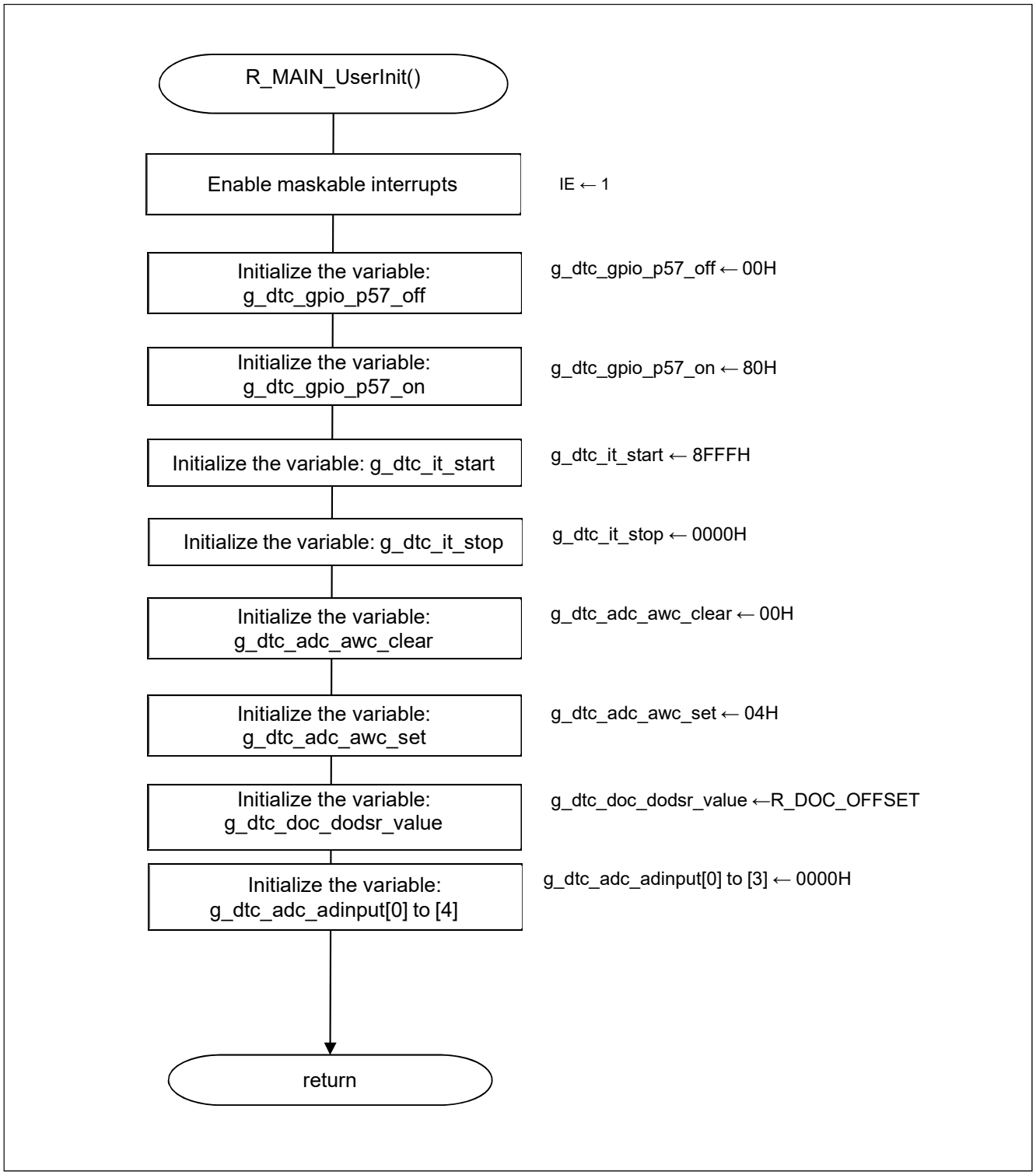


**Figure 5.16 Main Initial Setting**

### 5.7.14 DTC0 Activation

Figure 5.17 is a flowchart for DTC0 activation.

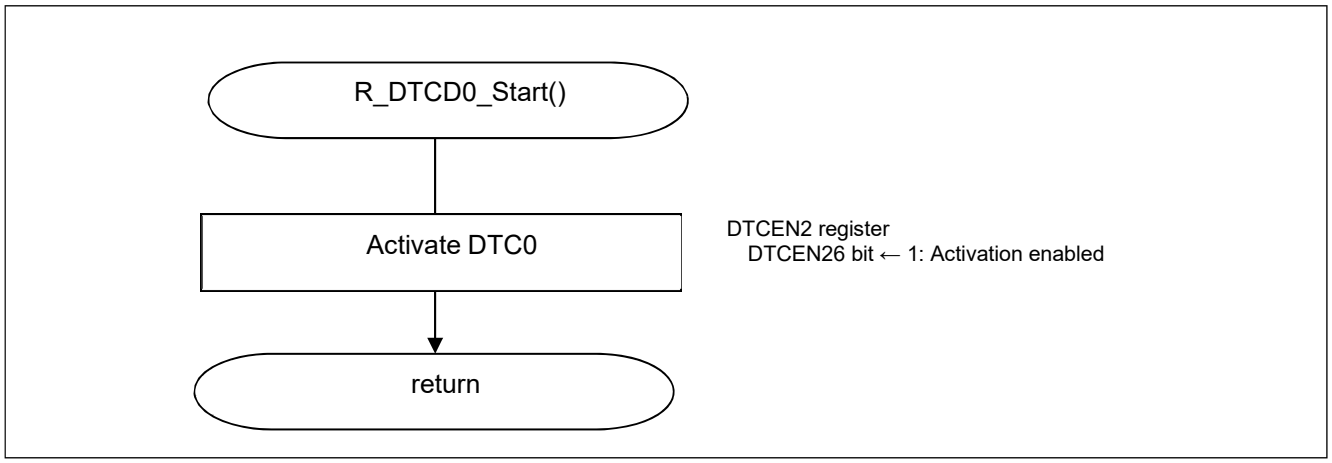


**Figure 5.17 DTC0 Activation**

DTC0 activation

- DTC activation enable register (DTCEN2)
  Enable DTC activation by 8-bit IT.

Symbol: DTCEN2

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| DTCEN27 | DTCEN26 | DTCEN25 | DTCEN24 | DTCEN23 | DTCEN22 | DTCEN21 | DTCEN20 |
| x | **1** | x | x | x | x | x | x |

Bit 6

| DTCEN26 | DTC activation enable 26 |
|---|---|
| 0 | Activation disabled |
| **1** | **Activation enabled** |

Note

1. For details on register settings, refer to RL78/I1D User's Manual: Hardware.

### 5.7.15 DTC2 Activation

Figure 5.18 is a flowchart for DTC2 activation.

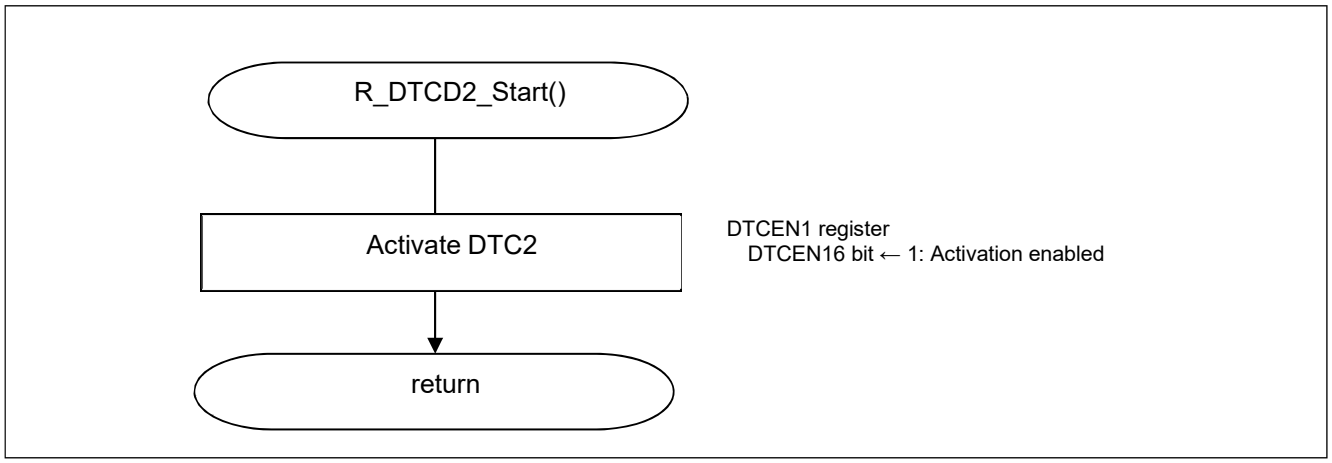


**Figure 5.18 DTC2 Activation**

DTC2 activation

- DTC activation enable register (DTCEN1)
  Enable DTC activation by A/D conversion end.

Symbol: DTCEN1

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| DTCEN17 | DTCEN16 | DTCEN15 | DTCEN14 | DTCEN13 | DTCEN12 | DTCEN11 | DTCEN10 |
| x | **1** | x | x | x | x | x | x |

Bit 6

| DTCEN16 | DTC activation enable 16 |
|---|---|
| 0 | Activation disabled |
| **1** | **Activation enabled** |

Note
1. For details on register settings, refer to RL78/I1D User's Manual: Hardware.

### 5.7.16 A/D Voltage Comparator Operation Start

Figure 5.19 shows a flowchart to start A/D voltage comparator operation.

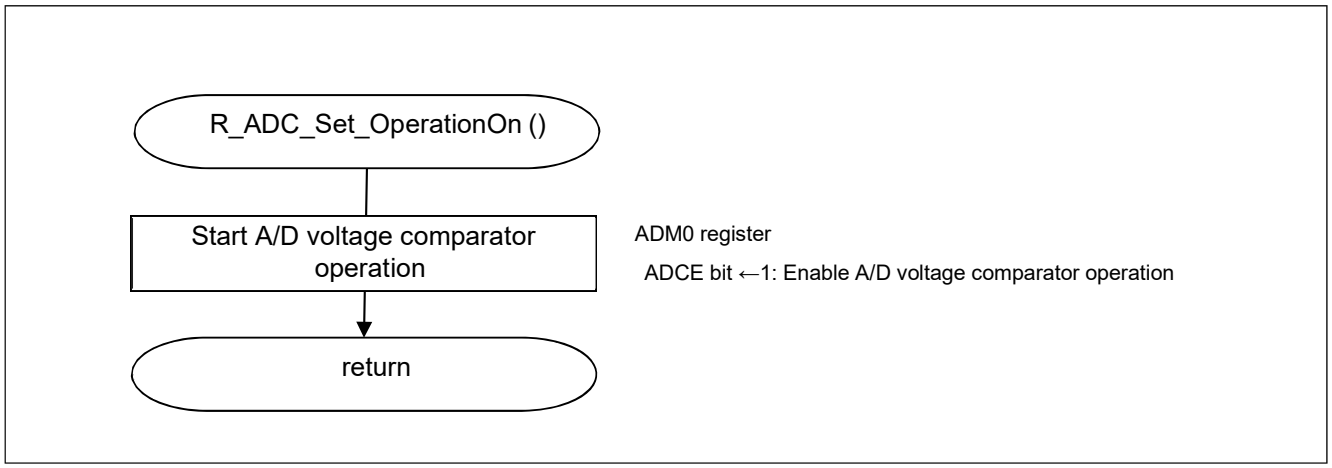


**Figure 5.19 A/D Voltage Comparator Operation Start**

A/D voltage comparator operation start

- A/D converter mode register 0 (ADM0)
  Control A/D voltage comparator operation.

Symbol: ADM0

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| ADCS | ADMD | FR2 | FR1 | FR0 | LV1 | LV0 | ADCE |
| x | x | x | x | x | x | x | **1** |

Bit 0

| ADCE | A/D voltage comparator operation control |
|---|---|
| 0 | Stops A/D voltage comparator operation |
| **1** | **Enables A/D voltage comparator operation** |

Note
1. For details on register settings, refer to RL78/I1D User's Manual: Hardware.

### 5.7.17 A/D Converter SNOOZE Function Start

Figure 5.20 is a flowchart to start the SNOOZE function of the A/D converter.

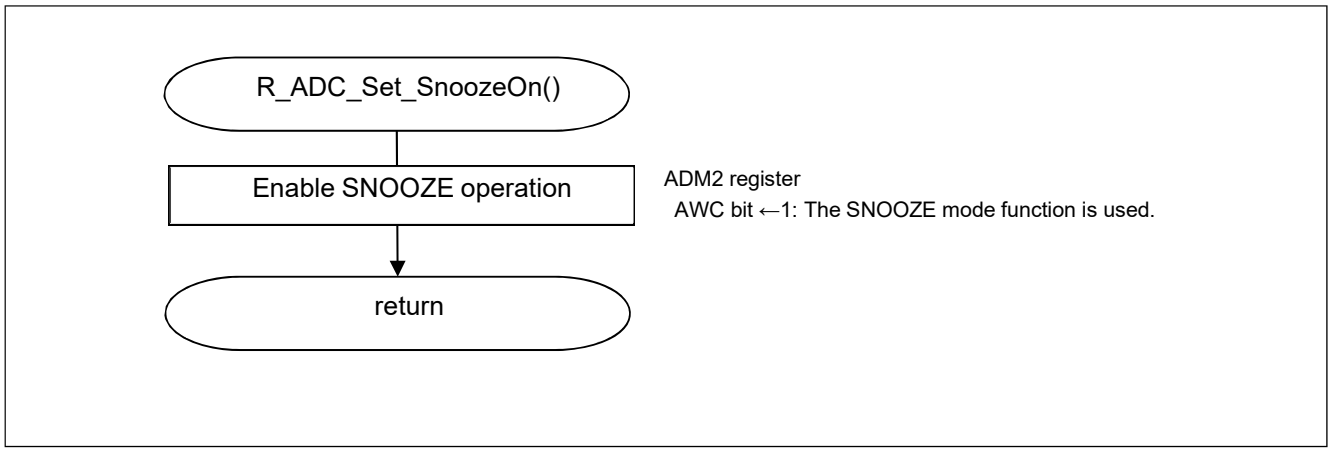


**Figure 5.20 A/D Converter's SNOOZE Function Start**

SNOOZE mode operation start

- A/D converter mode register 2 (ADM2)
Start SNOOZE mode operation.

Symbol: ADM2

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| ADREFP1 | ADREFP0 | ADREFM | 0 | ADRCK | AWC | 0 | ADYTP |
| x | x | x | x | x | **1** | x | x |

Bit 2

| AWC | Specification of the SNOOZE mode |
|---|---|
| 0 | The SNOOZE mode function is not used. |
| **1** | **The SNOOZE mode function is used.** |

### 5.7.18 Operational Amplifier 0 Operation Start

Figure 5.21 is a flowchart to start operation of the operational amplifier 0.

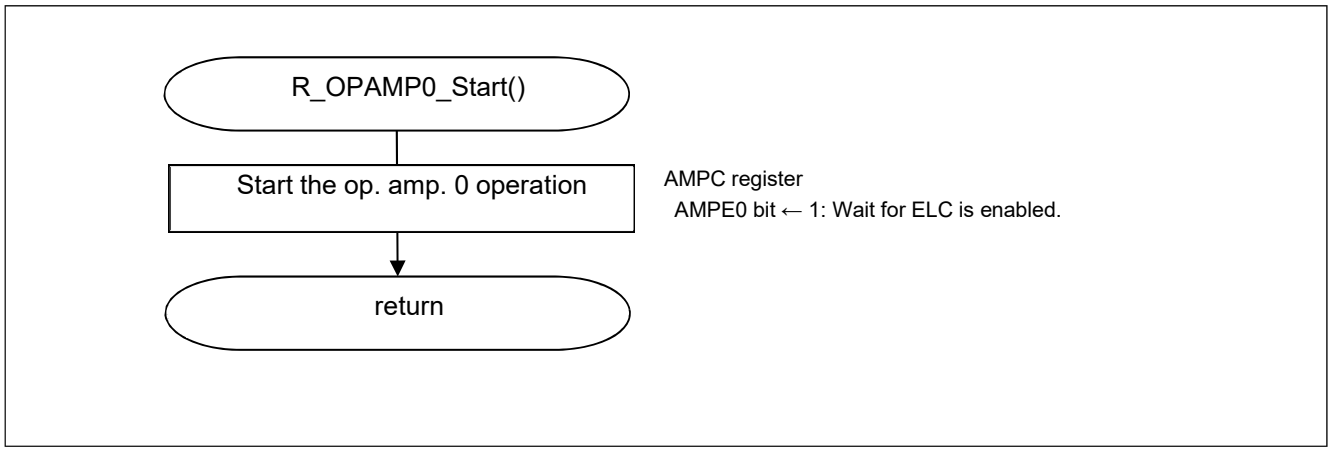


**Figure 5.21 Operational Amplifier 0 Operation Start**

Operational amplifier 0 operation start

- Operational amplifier control register (AMPC)
  Start operation of the operational amplifier 0.

Symbol: AMPC

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| IREFE | 0 | 0 | 0 | AMPE3 | AMPE2 | AMPE1 | AMPE0 |
| x | x | x | x | x | x | x | **1** |

Bit 0

| AMPE0 | Operation control of operational amplifier |
|---|---|
| 0 | Operation amplifier is stopped. |
| **1** | **Software trigger mode: Operation of operational amplifier is enabled.**<br>**ELC trigger mode or ELC and A/D trigger mode: Wait for ELC is enabled.** |

### 5.7.19 Operational Amplifier 1 Operation Start

Figure 5.22 is a flowchart to start operation of the operational amplifier 1.

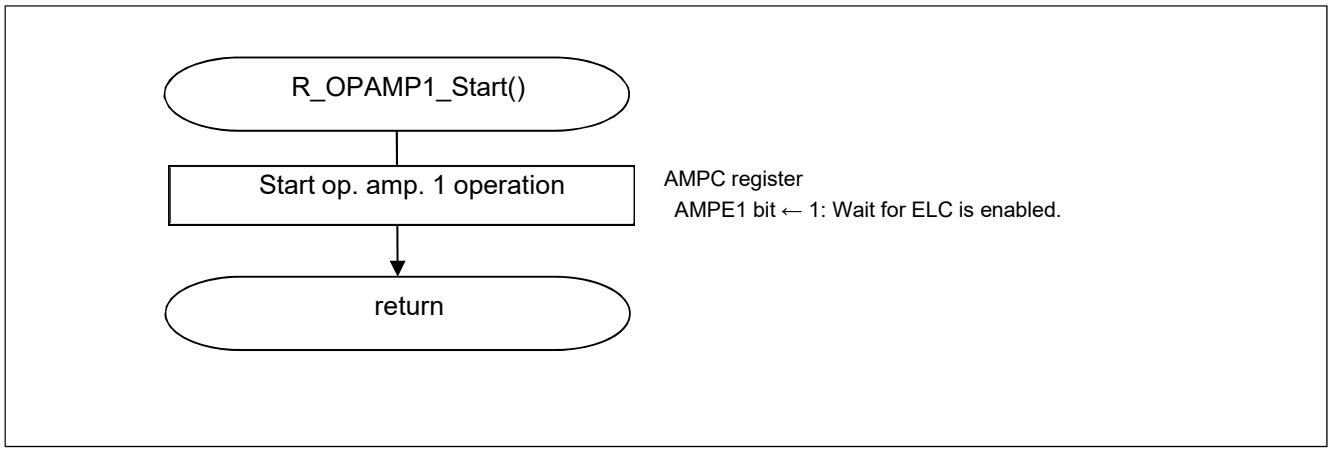


**Figure 5.22 Operational Amplifier 1 Operation Start**

Operational amplifier 1 operation start

- Operational amplifier control register (AMPC)
  Start operation of the operational amplifier 1.

Symbol: AMPC

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| IREFE | 0 | 0 | 0 | AMPE3 | AMPE2 | AMPE1 | AMPE0 |
| x | x | x | x | x | x | **1** | x |

Bit 1

| AMPE1 | Operation control of operational amplifier |
|---|---|
| 0 | Operation amplifier is stopped. |
| **1** | **Software trigger mode: Operation of operational amplifier is enabled.**<br>**ELC trigger mode or ELC and A/D trigger mode: Wait for ELC is enabled.** |

### 5.7.20 8-bit Interval Timer Count Start

Figure 5.23 is a flowchart to start count by the 8-bit interval timer.

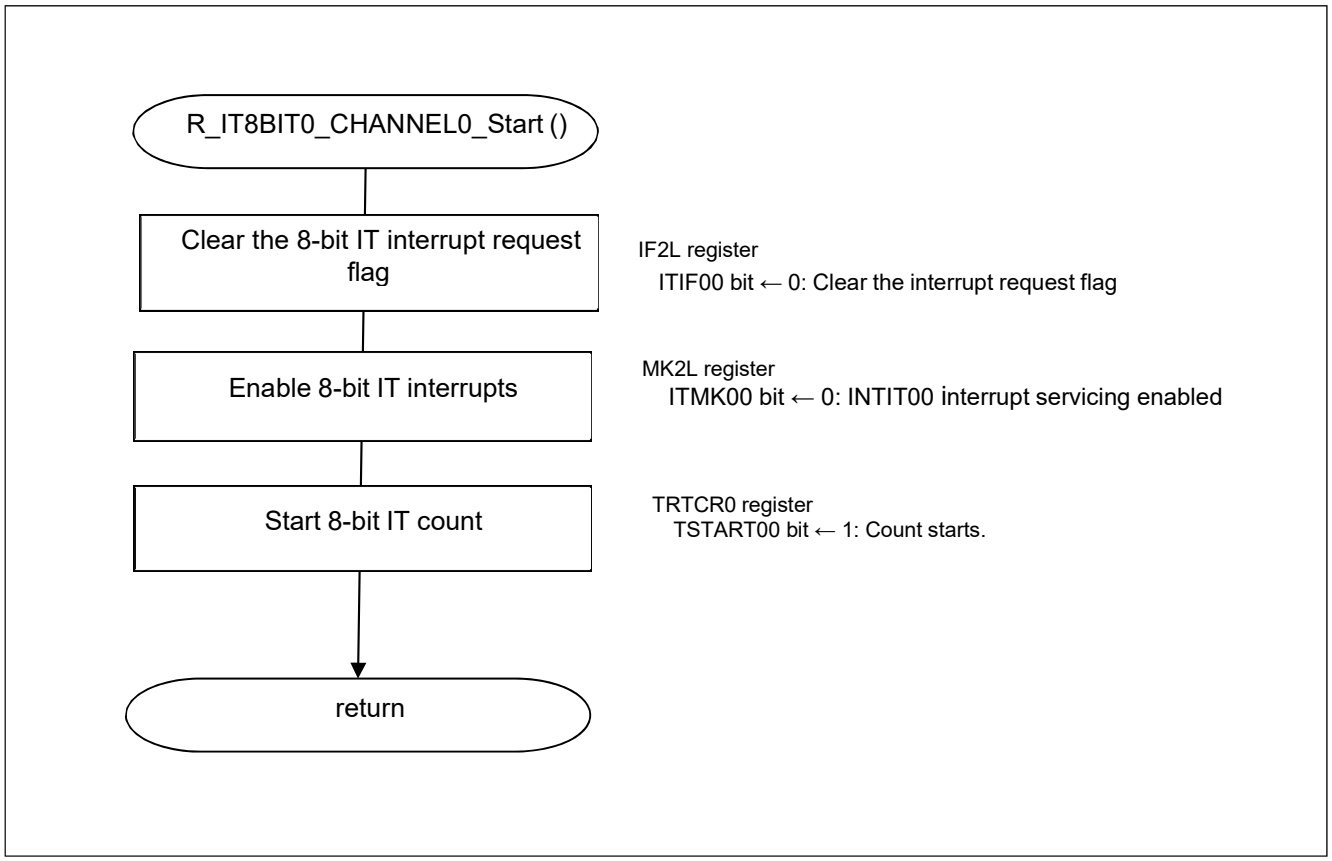


**Figure 5.23 8-bit Interval Timer Count Start**

8-bit interval timer interrupt setting

- Interrupt request flag register (IF2L)
  Clear the interrupt request flag.
- Interrupt request flag register (MK2L)
  Enable interrupt servicing.

Symbol: IF2L

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| FLIF | 0 | 0 | 0 | ITIF11 | ITIF10 | ITIF01 | ITIF00 |
| x | x | x | x | x | x | x | **0** |

Bit 0

| ITIF00 | Interrupt request flag |
|---|---|
| **0** | **No interrupt request signal is generated.** |
| 1 | Interrupt request is generated, interrupt request status |

Symbol: MK2L

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| FLMK | 0 | 0 | 0 | ITMK11 | ITMK10 | ITMK01 | ITMK00 |
| x | x | x | x | x | x | x | **0** |

Bit 0

| ITMK00 | Interrupt servicing control |
|---|---|
| **0** | **Interrupt servicing enabled** |
| 1 | Interrupt servicing disabled |

Note
1. For details on register settings, refer to RL78/I1D User's Manual: Hardware.

8-bit interval timer count start setting

- 8-bit interval timer control register 0 (TRTCR0)
  Start counting by the 8-bit interval timer.

Symbol: TRTCR0

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| TCSMD0 | 0 | 0 | TCLKEN0 | 0 | TSTART01 | 0 | TSTART00 |
| x | x | x | x | x | x | x | **1** |

Bit 0

| TSTART00 | 8-bit interval timer 0 count start |
|---|---|
| 0 | Count stops. |
| **1** | Count starts. |

Note
1. For details on register settings, refer to RL78/I1D User's Manual: Hardware.

### 5.7.21 Data Operation Circuit Interrupt Servicing

Figure 5.24 is a flowchart of main processing.

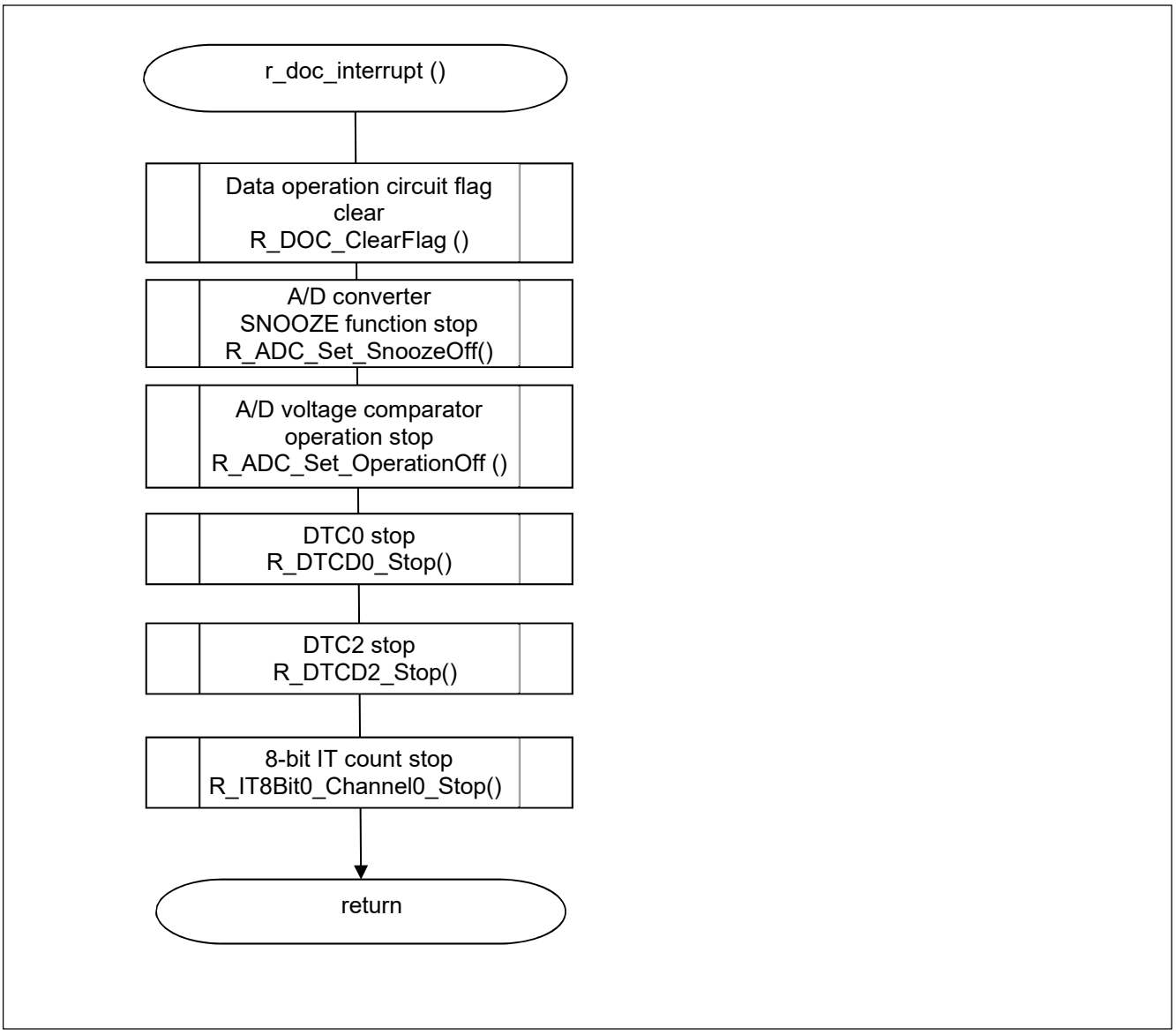


**Figure 5.24 Data Operation Circuit Interrupt Servicing**

### 5.7.22 Data Operation Circuit Flag Clear

Figure 5.25 shows a flowchart to clear the data operation circuit flag.

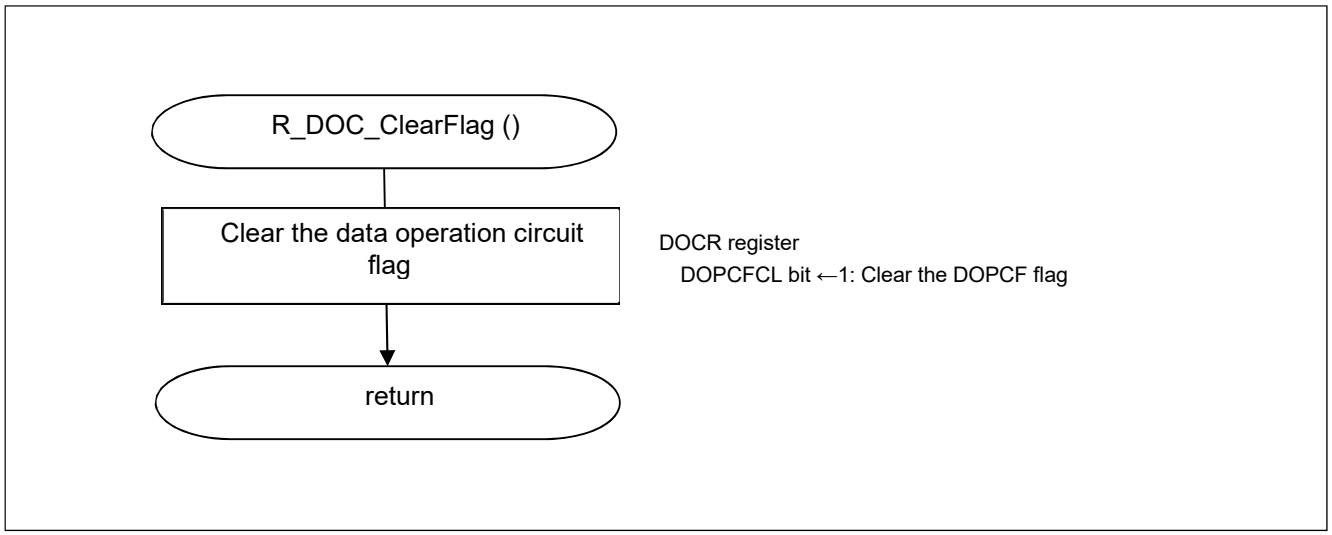


**Figure 5.25 Data Operation Circuit Flag Clear**

Data operation circuit flag clear

- DOC control register (DOCR)
  Set the SNOOZE mode.

  Symbol: DOCR

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| 0 | DOPCFCL | DOPCF | DOPCIE | 0 | DCSEL | OMS1 | OMS0 |
| x | **1** | x | x | x | x | x | x |

Bit 2

| DOPCFCL | DOPCF clear |
|---|---|
| 0 | Maintains the DOPCF flag state. |
| **1** | **Clears the DOPCF flag.** |

### 5.7.23 A/D Converter SNOOZE Function Stop

Figure 5.26 shows a flowchart to stop the SNOOZE function of the A/D converter.

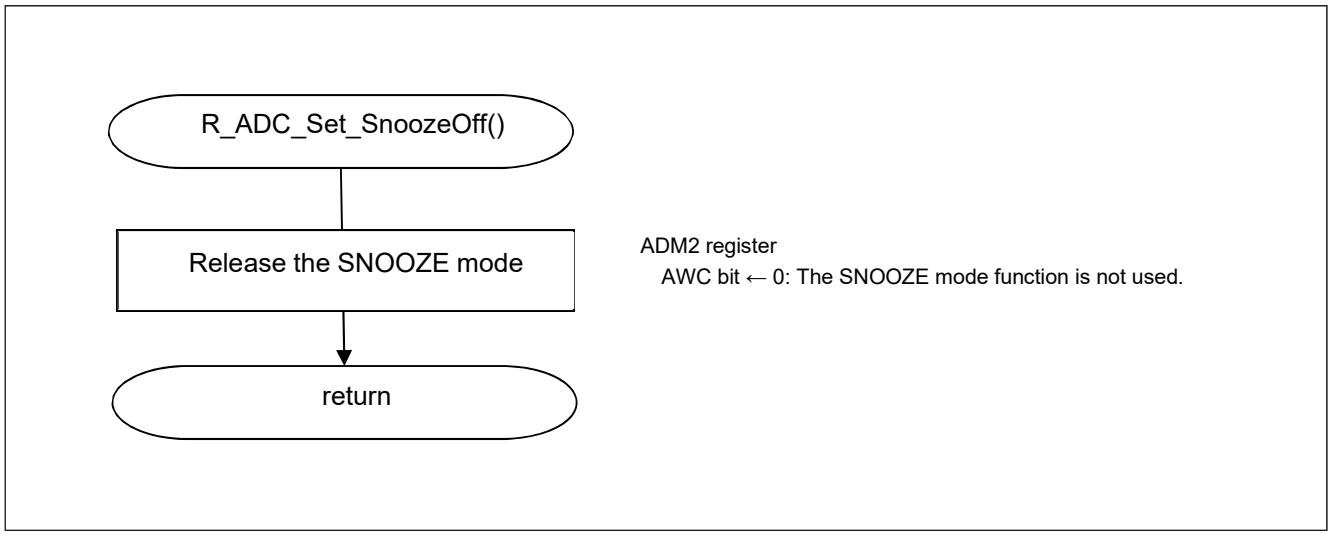


**Figure 5.26 A/D Converter's SNOOZE Function Stop**

SNOOZE mode setting

- A/D converter mode register 2 (ADM2)
  Specify the SNOOZE mode function.
  Symbol: ADM2

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| ADREFP1 | ADREFP0 | ADREFM | 0 | ADRCK | AWC | 0 | ADYTP |
| x | x | x | x | x | **0** | X | X |

Bits 2

| AWC | Specification of the SNOOZE mode |
|---|---|
| **0** | **The SNOOZE mode function is not used.** |
| 1 | The SNOOZE mode function is used. |

### 5.7.24 A/D Voltage Comparator Operation Stop

Figure 5.27 shows a flowchart to stop operation of the A/D voltage comparator.

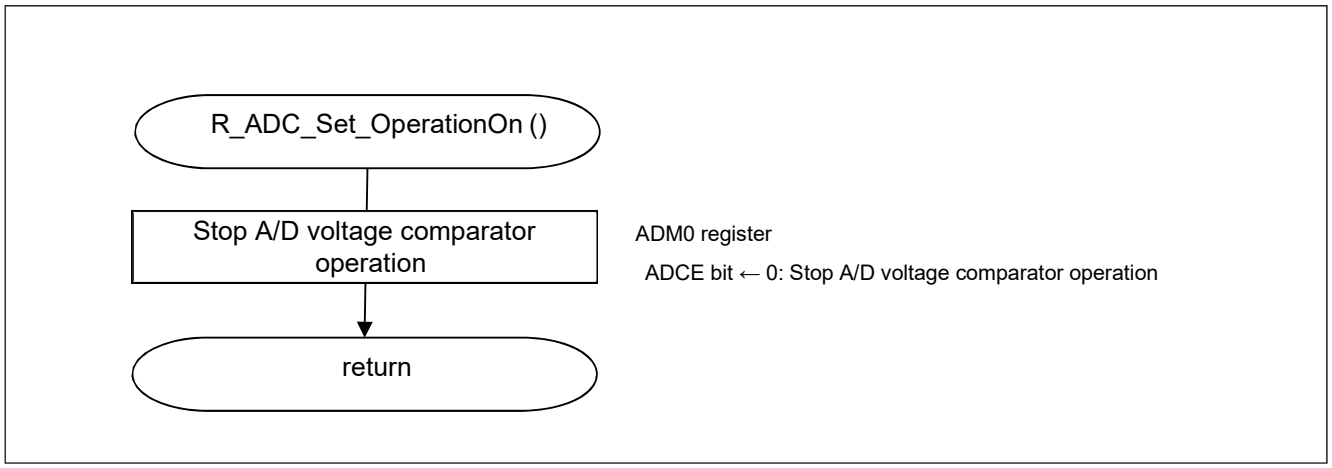


**Figure 5.27 A/D Voltage Comparator Operation Stop**

A/D voltage comparator operation start

- A/D converter mode register 0 (ADM0)
Control A/D voltage comparator operation.

Symbol: ADM0

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| ADCS | ADMD | FR2 | FR1 | FR0 | LV1 | LV0 | ADCE |
| x | x | x | x | x | x | x | **0** |

Bit 0

| ADCE | A/D voltage comparator operation control |
|---|---|
| **0** | **Stops A/D voltage comparator operation** |
| 1 | Enables A/D voltage comparator operation |

Note
1. For details on register settings, refer to RL78/I1D User's Manual: Hardware.

### 5.7.25 DTC0 Stop

Figure 5.28 is a flowchart to stop the DTC0.

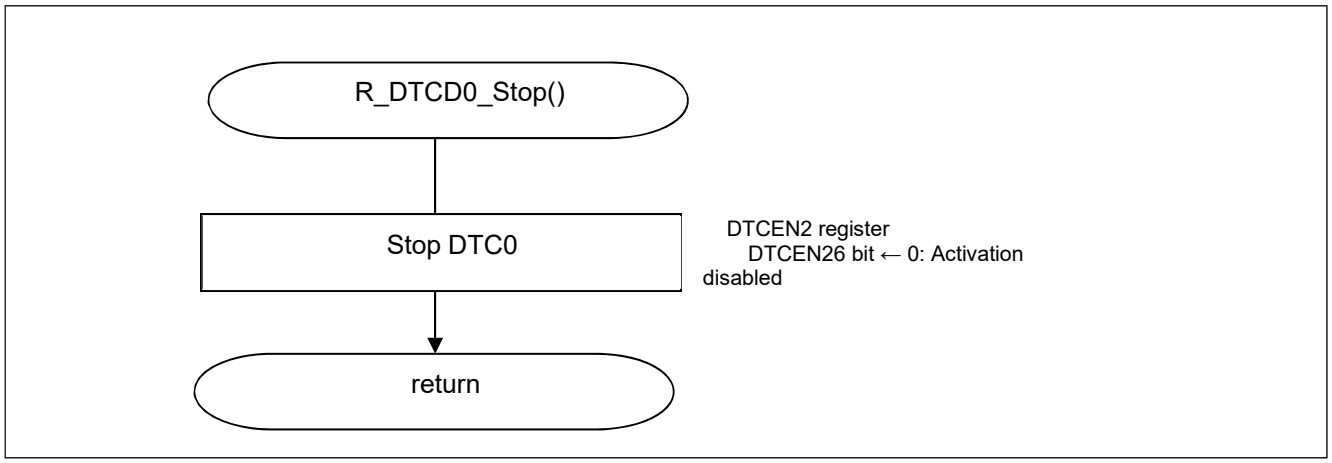


**Figure 5.28 DTC0 Stop**

DTC0 stop

- DTC activation enable register (DTCEN2)
  Disable DTC activation by 8-bit IT.

Symbol: DTCEN2

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| DTCEN27 | DTCEN26 | DTCEN25 | DTCEN24 | DTCEN23 | DTCEN22 | DTCEN21 | DTCEN20 |
| x | **0** | x | x | x | x | x | x |

Bit 6

| DTCEN26 | DTC activation enable 26 |
|---|---|
| **0** | **Activation disabled** |
| 1 | Activation enabled |

Note

1. For details on register settings, refer to RL78/I1D User's Manual: Hardware.

### 5.7.26 DTC2 Stop

Figure 5.29 is a flowchart to stop the DTC2.

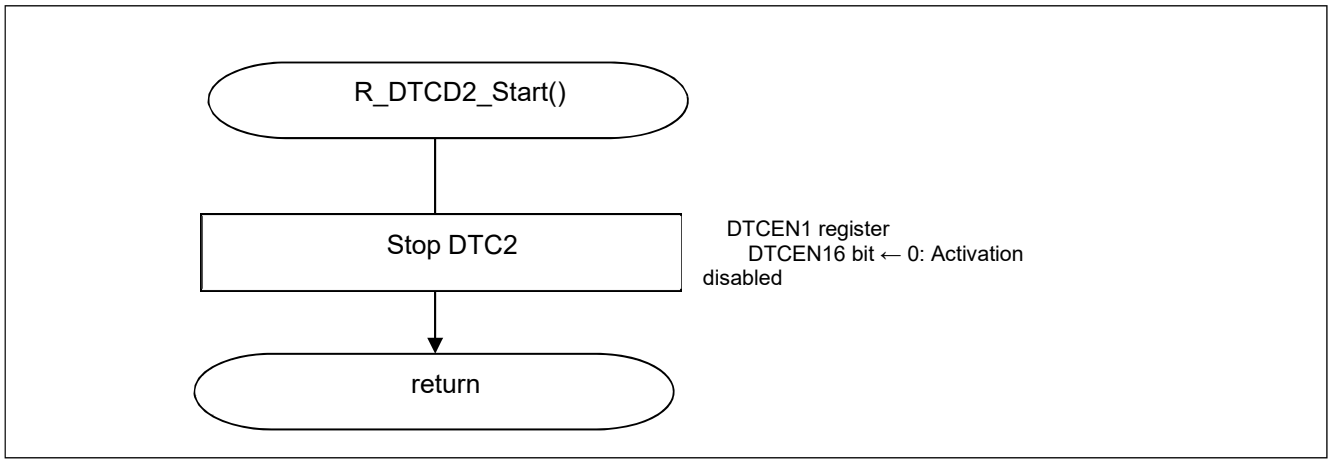


**Figure 5.29 DTC2 Stop**

DTC2 stop

- DTC activation enable register (DTCEN1)
  Disable DTC activation by A/D conversion end.

Symbol: DTCEN1

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| DTCEN17 | DTCEN16 | DTCEN15 | DTCEN14 | DTCEN13 | DTCEN12 | DTCEN11 | DTCEN10 |
| x | **0** | x | x | x | x | x | x |

Bit 6

| DTCEN16 | DTC activation enable 16 |
|---|---|
| **0** | **Activation disabled** |
| 1 | **Activation enabled** |

Note
1. For details on register settings, refer to RL78/I1D User's Manual: Hardware.

### 5.7.27 8-bit Interval Timer Count Stop

Figure 5.30 shows a flowchart to start counting by the 8-bit interval timer.

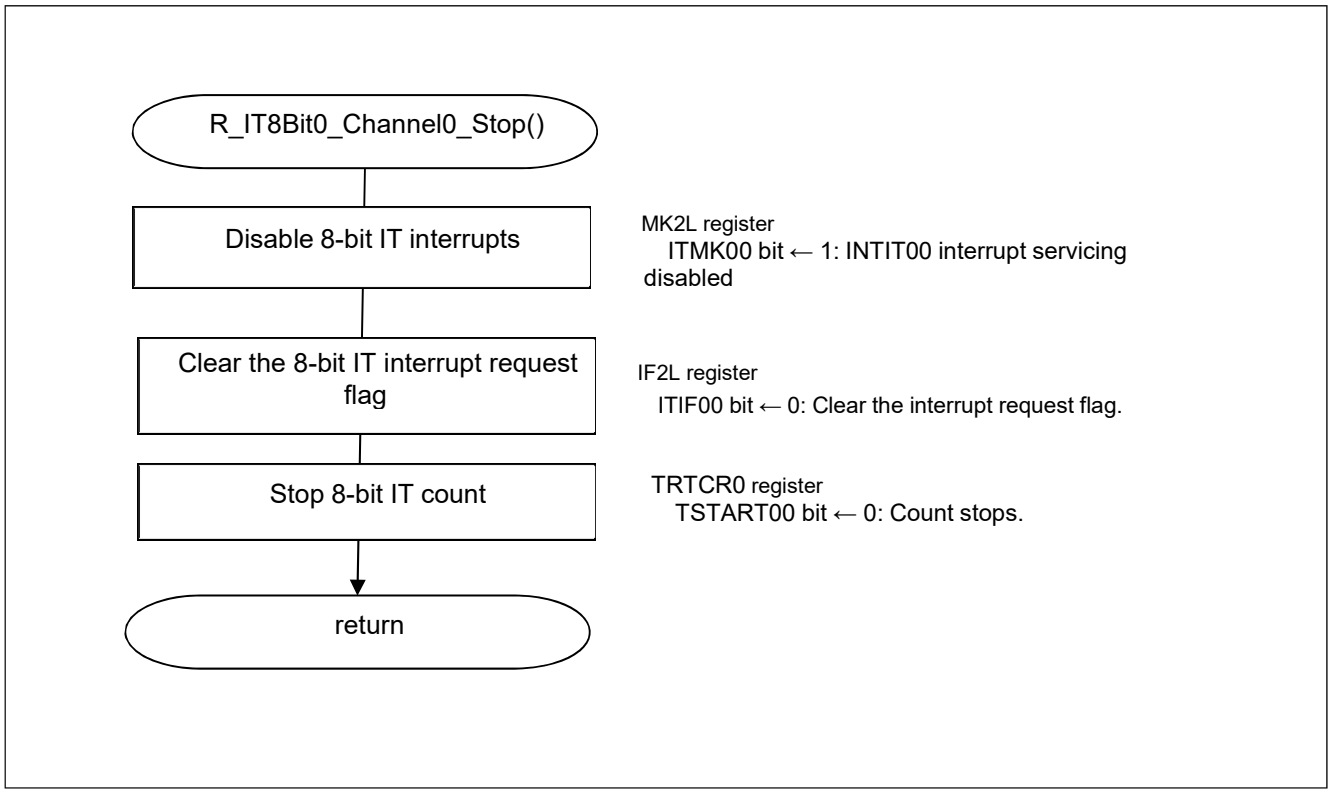


**Figure 5.30 8-bit Interval Timer Count Stop**

8-bit interval timer interrupt setting

- Interrupt request flag register (MK2L)
  Disable interrupt servicing.
- Interrupt request flag register (IF2L)
  Clear the interrupt request flag.

Symbol: MK2L

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| FLMK | 0 | 0 | 0 | ITMK11 | ITMK10 | ITMK01 | ITMK00 |
| x | x | x | x | x | x | x | **1** |

Bit 0

| ITMK00 | Interrupt servicing control |
|---|---|
| 0 | Interrupt servicing enabled |
| **1** | **Interrupt servicing disabled** |

Symbol: IF2L

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| FLIF | 0 | 0 | 0 | ITIF11 | ITIF10 | ITIF01 | ITIF00 |
| x | x | x | x | x | x | x | **0** |

Bit 0

| ITIF00 | Interrupt request flag |
|---|---|
| **0** | **No interrupt request signal is generated.** |
| 1 | Interrupt request is generated, interrupt request status |

Note
1. For details on register settings, refer to RL78/I1D User's Manual: Hardware.

8-bit interval timer count stop setting

- 8-bit interval timer control register 0 (TRTCR0)
  Start counting by the 8-bit interval timer.

Symbol: TRTCR0

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| TCSMD0 | 0 | 0 | TCLKEN0 | 0 | TSTART01 | 0 | TSTART00 |
| x | x | x | x | x | x | x | **0** |

Bit 0

| TSTART00 | 8-bit interval timer 0 count start |
|---|---|
| **0** | **Count stops.** |
| 1 | Count starts. |

Note
1. For details on register settings, refer to RL78/I1D User's Manual: Hardware.

## 6. Sample Code

Sample code can be downloaded from the Renesas Electronics website.

## 7. Reference Documents

RL78/I1D User's Manual: Hardware (R01UH0474E)

RL78 Family User's Manual: Software (R01US0015EJ)

The latest versions can be downloaded from the Renesas Electronics website.

Technical Update/Technical News

The latest information can be downloaded from the Renesas Electronics website.

## Revision History

| Rev. | Date | Description | |
|---|---|---|---|
| | | Page | Summary |
| 1.00 | Feb.03.2017 | - | First edition issued |
| 1.10 | June.24.2022 | 8 | Update Operation Confirmation Conditions |
| | | | |

# General Precautions in the Handling of Microprocessing Unit and Microcontroller Unit Products

The following usage notes are applicable to all Microprocessing unit and Microcontroller unit products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Precaution against Electrostatic Discharge (ESD)
   A strong electrical field, when exposed to a CMOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop the generation of static electricity as much as possible, and quickly dissipate it when it occurs. Environmental control must be adequate. When it is dry, a humidifier should be used. This is recommended to avoid using insulators that can easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors must be grounded. The operator must also be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions must be taken for printed circuit boards with mounted semiconductor devices.
2. Processing at power-on
   The state of the product is undefined at the time when power is supplied. The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the time when power is supplied. In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the time when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the time when power is supplied until the power reaches the level at which resetting is specified.
3. Input of signal during power-off state
   Do not input signals or an I/O pull-up power supply while the device is powered off. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Follow the guideline for input signal during power-off state as described in your product documentation.
4. Handling of unused pins
   Handle unused pins in accordance with the directions given under handling of unused pins in the manual. The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of the LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible.
5. Clock signals
   After applying a reset, only release the reset line after the operating clock signal becomes stable. When switching the clock signal during program execution, wait until the target clock signal is stabilized. When the clock signal is generated with an external resonator or from an external oscillator during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Additionally, when switching to a clock signal produced with an external resonator or by an external oscillator while program execution is in progress, wait until the target clock signal is stable.
6. Voltage application waveform at input pin
   Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between $V_{IL}$ (Max.) and $V_{IH}$ (Min.) due to noise, for example, the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between $V_{IL}$ (Max.) and $V_{IH}$ (Min.).
7. Prohibition of access to reserved addresses
   Access to reserved addresses is prohibited. The reserved addresses are provided for possible future expansion of functions. Do not access these addresses as the correct operation of the LSI is not guaranteed.
8. Differences between products
   Before changing from one product to another, for example to a product with a different part number, confirm that the change will not lead to problems. The characteristics of a microprocessing unit or microcontroller unit products in the same group but having a different part number might differ in terms of internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

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