RX23E-A Group, RX21A Group

Differences Between the RX23E-A Group and the RX21A Group

Summary

This application note is intended as a reference to points of difference between the peripheral functions, I/O registers, and pin functions of the RX23E-A Group and RX21A Group, as well as a guide to key points to consider when migrating between the two groups.

Unless specifically otherwise noted, the information in this application note applies to the 48-pin package version of the RX23E-A Group and the 100-pin package version of the RX21A Group. To confirm details of differences in the specifications of the electrical characteristics, usage notes, and setting procedures, refer to the User's Manual: Hardware of the products in question.

Target Devices

RX23E-A Group and RX21A Group

Contents

1. Comparison of Built-In Functions of RX23E-A Group and RX21A Group

A comparison of the built-in functions of the RX23E-A Group and RX21A Group is provided below. For details of the functions, see section 2, Comparative Overview of Specifications and section 5, Reference Documents.

Table 1.1 is a comparison of built-in functions of RX23E-A Group and RX21A Group.

Table 1.1 Comparison of Built-In Functions of RX23E-A Group and RX21A Group

Function	RX21A	RX23E-A
CPU	●	
Operating modes	▲/■	
Address space	▲	
Resets	■	
Option-setting memory (OFSM)	▲/■	
Voltage detection circuit (LVDAa): RX21A, (LVDAb): RX23E-A	●/■	
Clock generation circuit	●/■	
Clock frequency accuracy measurement circuit (CAC)	●/■	
Low power consumption	●/■	
Register write protection function	●/▲	
Exception handling	●	
Interrupt controller (ICUb)	●/■	
Buses	●	
Memory-protection unit (MPU)	●/■	
DMA controller (DMACA)	○	
Data transfer controller (DTCa)	○	
Event link controller (ELC)	■	
I/O ports	■	
Multi-function pin controller (MPC)	▲	
Multi-function timer pulse unit 2 (MTU2a)	○	
Port output enable 2 (POE2a)	○	
8-bit timer (TMR)	○	
Compare match timer (CMT)	■	
Realtime clock (RTCc)	○	×
Low-power timer (LPT)	×	○
Watchdog timer (WDTA)	○	×
Independent watchdog timer (IWDTa)	▲	
Serial communications interface (SCIc): RX21A, (SCIg, SCIh): RX23E-A	●	
IrDA interface	○	×
I^2C bus interface (RIIC): RX21A, (RIICa): RX23E-A	■	
CAN module (RSCAN)	×	○
Serial peripheral interface (RSPI): RX21A, (RSPIb): RX23E-A	●/■	
CRC calculator (CRC)	○	
Analog frontend (AFE)	×	○
24-bit ΔΣ A/D converter (DSAD): RX21A, (DSADA): RX23E-A	●/■	
10-bit A/D converter (AD): RX21A 12-bit A/D converter (S12ADE): RX23E-A	●/■	
D/A converter (DA)	○	×
Temperature sensor (TEMPSa)	○	▲*1
Comparator A (CMPA)	○	×
Comparator B (CMPB)	○	×
Data operation circuit (DOC)	●	

Function	RX21A	RX23E-A
RAM	●	■
Flash memory (FLASH)	●	■
Packages	●	■

○: Available, ×: Unavailable, ●: Differs due to added functionality,
▲: Differs due to change in functionality, ■: Differs due to removed functionality.

Note: 1. The analog frontend section of the RX23E-A Group user's manual describes functionality equivalent to that described in section 37, Temperature Sensor (TEMPSa), in RX21A Group User's Manual: Hardware.

2. Comparative Overview of Specifications

This section presents a comparative overview of specifications, including registers.

In the comparative overview, red text indicates functions which are included only in one of the MCU groups and also functions for which the specifications differ between the two groups.

In the register comparison, red text indicates differences in specifications for registers that are included in both groups and **black text** indicates registers which are included only in one of the MCU groups. Differences in register specifications are not listed.

2.1 CPU

Table 2.1 is a comparative overview of CPUs, and Table 2.2 is a comparison of CPU registers.

Table 2.1 Comparative Overview of CPUs

Item	RX21A	RX23E-A
CPU	• Maximum operating frequency: 50 MHz • 32-bit RX CPU • Minimum instruction execution time: One instruction per clock cycle • Address space: 4 GB, linear • Register set of the CPU — General purpose: Sixteen 32-bit registers — Control: Eight 32-bit registers — Accumulator: One 64-bit register • Basic instructions: 73 • DSP instructions: 9 • Addressing modes: 10 • Data arrangement — Instructions: Little endian — Data: Selectable between little endian or big endian • On-chip 32-bit multiplier: 32 × 32 → 64 bits • On-chip divider: 32 / 32 → 32 bits • Barrel shifter: 32 bits • Memory-protection unit (MPU)	• Maximum operating frequency: 32 MHz • 32-bit RX CPU (RXv2) • Minimum instruction execution time: One instruction per clock cycle • Address space: 4 GB, linear • Register set of the CPU — General purpose: Sixteen 32-bit registers — Control: Ten 32-bit registers — Accumulator: Two 72-bit registers • Basic instructions: 75, variable-length instruction format • Floating point instructions: 11 • DSP instructions: 23 • Addressing modes: 10 • Data arrangement — Instructions: Little endian — Data: Selectable between little endian or big endian • On-chip 32-bit multiplier: 32 × 32 → 64 bits • On-chip divider: 32 / 32 → 32 bits • Barrel shifter: 32 bits • Memory-protection unit (MPU)
FPU	—	• Single-precision floating-point (32 bits) • Data types and floating-point exceptions conform to IEEE 754 standard

Table 2.2 Comparison of CPU Registers

Register	Bit	RX21A	RX23E-A
FPSW	—	—	Floating point status word
EXTB	—	—	Exception table register
ACC (RX21A) ACC0, ACC1 (RX23E-A)	—	Accumulator	Accumulator 0, accumulator 1

2.2 Operating Modes

Table 2.3 is a comparative overview of operating modes, and Table 2.4 is a comparison of operating mode registers.

Table 2.3 Comparative Overview of Operating Modes

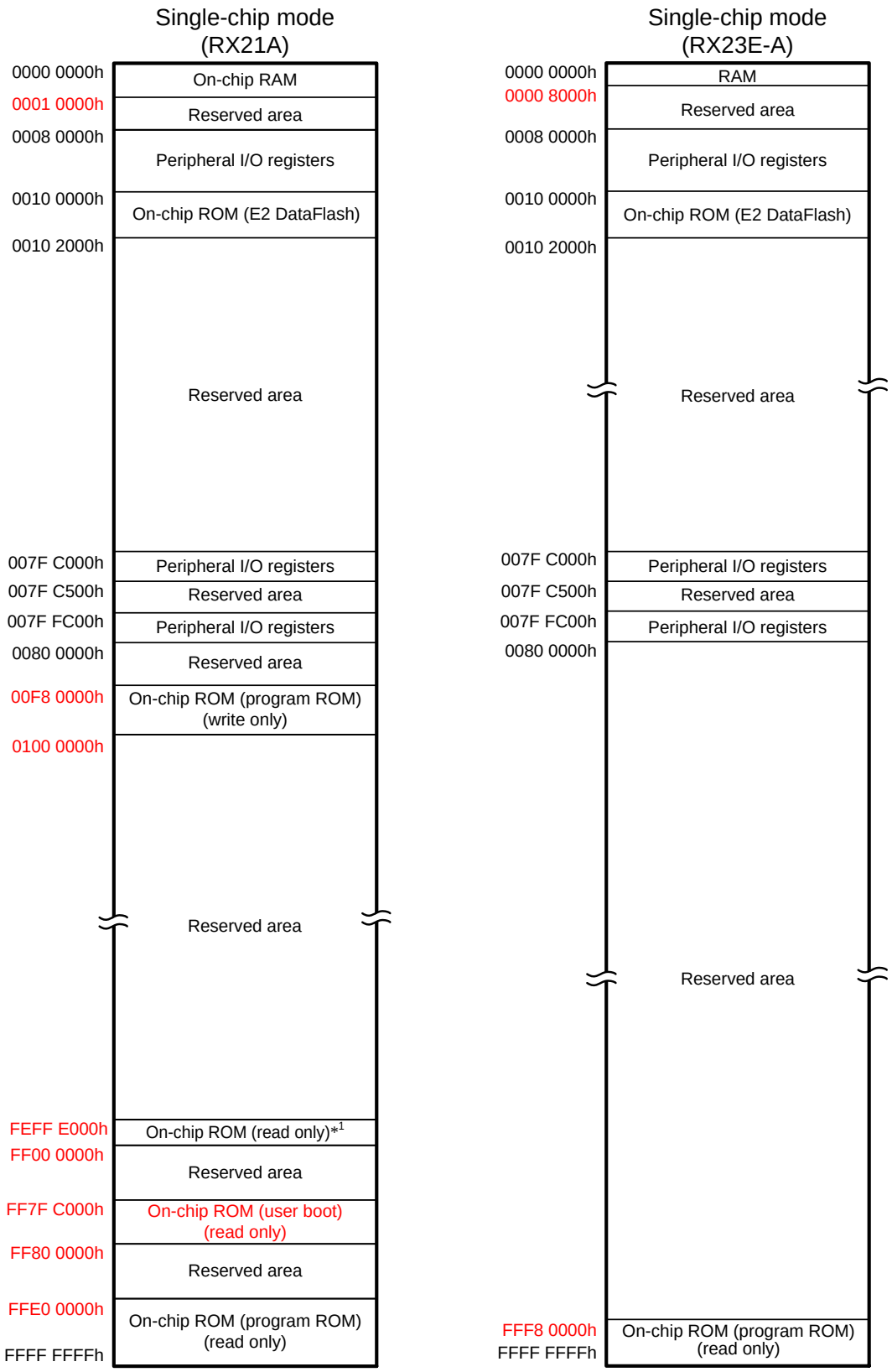
Item	RX21A	RX23E-A
Operating modes specified by mode setting pins	Single-chip mode	Single-chip mode
	Boot mode	Boot mode (SCI interface)
	User boot mode	—
Selection of endian order	MDEB register (user boot mode) MDES register (single-chip mode)	MDE register

Table 2.4 Comparison of Operating Mode Registers

Register	Bit	RX21A	RX23E-A
MDSR	—	Mode status register	—

2.3 Address space

Figure 2.1 is a comparative memory map of single-chip mode.



Note: 1. Only data at some specific addresses is usable. For details, refer to RX21A Group User's Manual: Hardware, referred to in 5, Reference Documents.

Figure 2.1 Comparative Memory Map of Single-Chip Mode

2.4 Resets

Table 2.5 is a comparative overview of resets, and Table 2.6 is a comparison of reset registers.

Table 2.5 Comparative Overview of Resets

Item	RX21A	RX23E-A
RES# pin reset	RES# pin input voltage low	RES# pin input voltage low
Power-on reset	VCC rise (voltage monitored: VPOR)	VCC rise (voltage monitored: VPOR)
Voltage monitoring 0 reset	VCC fall (voltage monitored: Vdet0)	VCC fall (voltage monitored: Vdet0)
Voltage monitoring 1 reset	VCC fall (voltage monitored: Vdet1)	VCC fall (voltage monitored: Vdet1)
Voltage monitoring 2 reset	VCC fall (voltage monitored: Vdet2)	VCC fall (voltage monitored: Vdet2)
Deep software standby reset	Deep software standby mode is canceled by an interrupt.	—
Independent watchdog timer reset	Independent watchdog timer underflow, or refresh error	Independent watchdog timer underflow, or refresh error
Watchdog timer reset	Watchdog timer underflow, or refresh error	—
Software reset	Register setting	Register setting

Table 2.6 Comparison of Reset Registers

Register	Bit	RX21A	RX23E-A
RSTSR0	DPSRSTF	Deep software standby reset detect flag	—
RSTSR2	WDTRF	Watchdog timer reset detect flag	—

2.5 Option-Setting Memory

Figure 2.2 is a comparison of option-setting memory areas, and Table 2.7 is a comparison of option-setting memory registers.

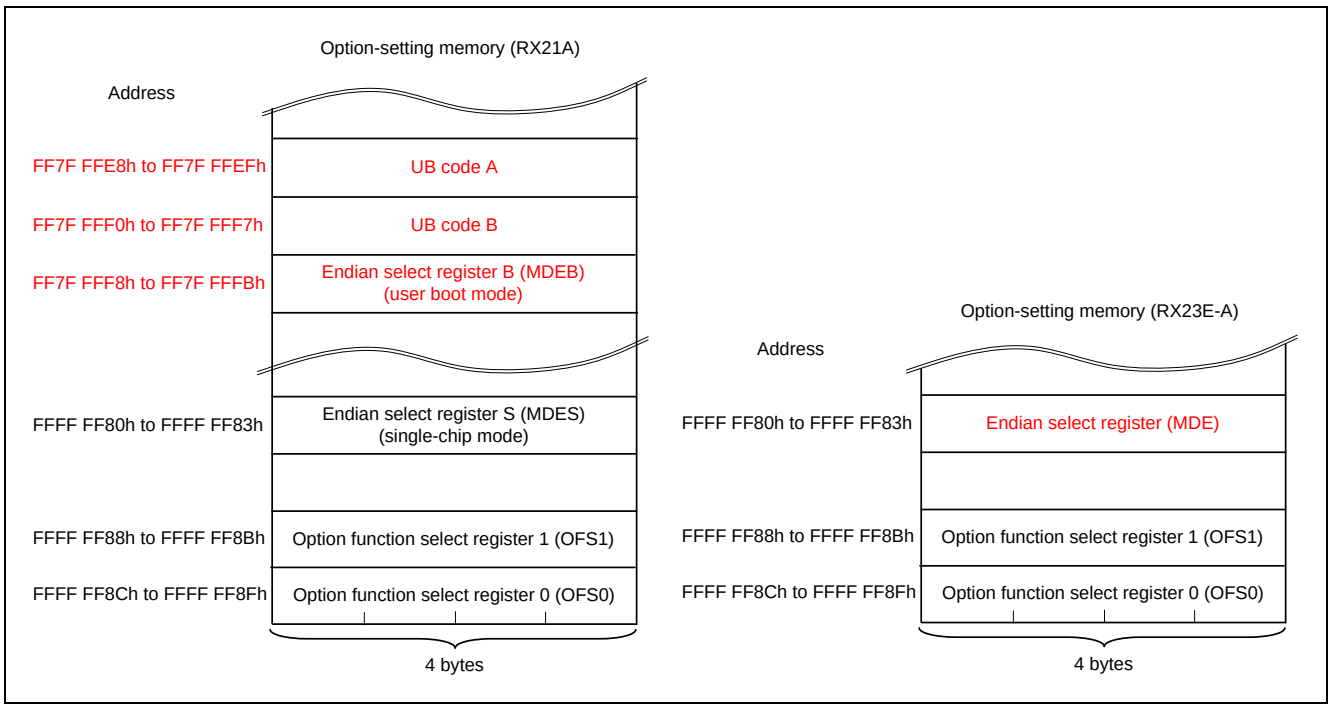


Figure 2.2 Comparison of Option-Setting Memory Areas

Table 2.7 Comparison of Option-Setting Memory Registers

Register	Bit	RX21A	RX23E-A (OFSM)
OFS0	IWDTTOPS [1:0]	IWDT timeout period select bits b3 b2 0 0: 1,024 cycles (03FFh) 0 1: 4,096 cycles (0FFFh) 1 0: 8,192 cycles (1FFFh) 1 1: 16,384 cycles (3FFFh)	IWDT timeout period select bits b3 b2 0 0: 128 cycles (007Fh) 0 1: 512 cycles (01FFh) 1 0: 1,024 cycles (03FFh) 1 1: 2,048 cycles (07FFh)
	IWDTSLCSTP	IWDT sleep mode count stop control bit 0: Counting stop is disabled. 1: Counting stop is enabled when entering sleep, software standby, deep software standby, or all-module clock stop mode.	IWDT sleep mode count stop control bit 0: Counting stop is disabled. 1: Counting stop is enabled when entering sleep, software standby, or deep sleep mode.
	WDTSTRT	WDT start mode select bit	—
	WDTTOPS [1:0]	WDT timeout period select bits	—
	WDTCKS [3:0]	WDT clock frequency division ratio select bits	—
	WDTRPES [1:0]	WDT window end position select bits	—
	WDTRPSS [1:0]	WDT window start position select bits	—
	WDTRSTIRQS	WDT reset interrupt request select bit	—
OFS1	VDSEL [1:0]	Voltage detection 0 level select bits b1 b0 0 0: Setting prohibited. 0 1: 2.80 V is selected 1 0: 1.90 V is selected 1 1: Setting prohibited.	Voltage detection 0 level select bits b1 b0 0 0: 3.84 V is selected 0 1: 2.82 V is selected 1 0: 2.51 V is selected 1 1: 1.90 V is selected
	FASTSTUP	—	Power-on fast startup time bit
MDEB, MDES (RX21A) MDE (RX23E-A)	—	Endian select register B, endian select register S	Endian select register

2.6 Voltage Detection Circuit

Table 2.8 is a comparative overview of the voltage detection circuits, and Table 2.9 is a comparison of voltage detection circuit registers.

In addition, Table 2.10 is a comparison of setting procedures for Vdet1 voltage monitoring, Table 2.11 of setting procedures for Vdet2 voltage monitoring, Table 2.12 of operation setting procedures for voltage monitoring 1 interrupt and voltage monitoring 1 reset related bits, and Table 2.13 of operation setting procedures for voltage monitoring 2 interrupt and voltage monitoring 2 reset related bits.

Table 2.8 Comparative Overview of Voltage Detection Circuits

Item		RX21A (LVDAa)			RX23E-A (LVDAb)		
		Voltage Monitoring 0	**Voltage Monitoring 1**	**Voltage Monitoring 2**	**Voltage Monitoring 0**	**Voltage Monitoring 1**	**Voltage Monitoring 2**
VCC monitoring	Monitored voltage	Vdet0	Vdet1	Vdet2	Vdet0	Vdet1	Vdet2
	Detection target	Voltage drops past Vdet0	When voltage rises above or drops below Vdet1	When voltage rises above or drops below Vdet2 Input voltages to VCC and the CMPA2 pin can be switched using the LVCMPCR.EXVCCINP2 bit	Voltage drops past Vdet0	Voltage rises or drops past Vdet1	Voltage rises or drops past Vdet2
	Detection voltage	Voltage selectable from two levels using OFS1 register	Voltage selectable from nine levels using the LVDLVLR.LVD1LVL[3:0] bits	Varies according to whether VCC or the CMPA2 pin input is selected. Voltage selectable from nine levels using the LVDLVLR.LVD2LVL[3:0] bits	Voltage selectable from four levels using OFS1 register	Voltage selectable from 14 levels using the LVDLVLR.LVD1LVL[3:0] bits	Voltage selectable from four levels using the LVDLVLR.LVD2LVL[1:0] bits
	Monitor flag	—	LVD1SR.LVD1MON flag: Monitors whether voltage is higher or lower than Vdet1	LVD2SR.LVD2MON flag: Monitors whether voltage is higher or lower than Vdet2	—	LVD1SR.LVD1MON flag: Monitors whether voltage is higher or lower than Vdet1	LVD2SR.LVD2MON flag: Monitors whether voltage is higher or lower than Vdet2
			LVD1SR.LVD1DET flag: Vdet1 passage detection	LVD2SR.LVD2DET flag: Vdet2 passage detection		LVD1SR.LVD1DET flag: Vdet1 passage detection	LVD2SR.LVD2DET flag: Vdet2 passage detection
Voltage detection processing	Reset	Voltage monitoring 0 reset	Voltage monitoring 1 reset	Voltage monitoring 2 reset	Voltage monitoring 0 reset	Voltage monitoring 1 reset	Voltage monitoring 2 reset
		Reset when Vdet0 > VCC CPU restart after specified time with VCC > Vdet0	Reset when Vdet1 > VCC CPU restart timing selectable: after specified time with VCC > Vdet1 or Vdet1 > VCC	Reset when Vdet2 > VCC CPU restart timing selectable: after specified time with VCC > Vdet2 or after specified time with Vdet2 > VCC	Reset when Vdet0 > VCC CPU restart after specified time with VCC > Vdet0	Reset when Vdet1 > VCC CPU restart timing selectable: after specified time with VCC > Vdet1 or Vdet1 > VCC	Reset when Vdet2 > VCC CPU restart timing selectable: after specified time with VCC > Vdet2 or Vdet2 > VCC

Item		RX21A (LVDAa)			RX23E-A (LVDAb)		
		Voltage Monitoring 0	**Voltage Monitoring 1**	**Voltage Monitoring 2**	**Voltage Monitoring 0**	**Voltage Monitoring 1**	**Voltage Monitoring 2**
Voltage detection processing	Interrupt	—	Voltage monitoring 1 interrupt	Voltage monitoring 2 interrupt	—	Voltage monitoring 1 interrupt	Voltage monitoring 2 interrupt
			Non-maskable or maskable is selectable	Non-maskable or maskable is selectable		Non-maskable or maskable selectable	Non-maskable or maskable selectable
			Interrupt request issued when Vdet1 > VCC and VCC > Vdet1 or either	Interrupt request issued when Vdet2 > VCC and VCC > Vdet2 or either		Interrupt request issued when Vdet1 > VCC and VCC > Vdet1 or either	Interrupt request issued when Vdet2 > VCC and VCC > Vdet2 or either
Digital filter	Enabled/ disabled switching	No digital filter function	Available	Available	No digital filter function		
	Sampling time	—	1/n LOCO frequency × 2 (n: 1, 2, 4, 8)	1/n LOCO frequency × 2 (n: 1, 2, 4, 8)	—		
Event link function		—	Available Vdet1 passage detection event output	Available Vdet2 passage detection event output	—	Available Vdet1 passage detection event output	Available Vdet2 passage detection event output

Table 2.9 Comparison of Voltage Detection Circuit Registers

Register	Bit	RX21A (LVDAa)	RX23E-A (LVDAb)
LVCMPCR	EXVREFINP1	Comparator A1 reference voltage external input select bit	—
	EXVCCINP1	Comparator A1 comparison voltage external input select bit	—
	EXVREFINP2	Comparator A2 reference voltage external input select bit	—
	EXVCCINP2	Comparator A2 comparison voltage external input select bit	—
LVDLVLR	LVD1LVL[3:0]	Voltage detection 1 level select bits (Standard voltage during drop in voltage) b3 b0 0 1 1 1: 3.10 V 1 0 0 0: 2.95 V 1 0 0 1: 2.80 V 1 0 1 0: 2.65 V 1 0 1 1: 2.50 V 1 1 0 0: 2.35 V 1 1 0 1: 2.20 V 1 1 1 0: 2.05 V 1 1 1 1: 1.90 V Settings other than the above are prohibited.	Voltage detection 1 level select bits (Standard voltage during drop in voltage) b3 b0 0 0 0 0: 4.29 V 0 0 0 1: 4.14 V 0 0 1 0: 4.02 V 0 0 1 1: 3.84 V 0 1 0 0: 3.10 V 0 1 0 1: 3.00 V 0 1 1 0: 2.90 V 0 1 1 1: 2.79 V 1 0 0 0: 2.68 V 1 0 0 1: 2.58 V 1 0 1 0: 2.48 V 1 0 1 1: 2.20 V 1 1 0 0: 1.96 V 1 1 0 1: 1.86 V Settings other than the above are prohibited.

Register	Bit	RX21A (LVDAa)	RX23E-A (LVDAb)
LVDLVLR	LVD2LVL[3:0] (RX21A) LVD2LVL[1:0] (RX23E-A)	Voltage detection 2 level select bits (Standard voltage during drop in voltage) (b7 to b4) (When LVCMPCR.EXVCCINP2 = 0 (VCC selected)) b7 b4 0 1 1 1: 3.10 V 1 0 0 0: 2.95 V 1 0 0 1: 2.80 V 1 0 1 0: 2.65 V 1 0 1 1: 2.50 V 1 1 0 0: 2.35 V 1 1 0 1: 2.20 V 1 1 1 0: 2.05 V 1 1 1 1: 1.90 V (When LVCMPCR.EXVCCINP2 = 1 (CMPA2 selected)) b7 b4 0 0 0 1: 1.33 V Settings other than the above are prohibited.	Voltage detection 2 level select bits (Standard voltage during drop in voltage) (b5, b4) b5 b4 0 0: 4.29 V 0 1: 4.14 V 1 0: 4.02 V 1 1: 3.84 V
LVD1CR0	LVD1DFDIS	Voltage monitoring 1/comparator A1 digital filter disable mode select bit	—
	LVD1FSAMP [1:0]	Sampling clock select bits	—
LVD2CR0	LVD2DFDIS	Voltage monitoring 2/comparator A2 digital filter disable mode select bit	—
	LVD2FSAMP [1:0]	Sampling clock select bits	—

Table 2.10 Comparison of Setting Procedures for Vdet1 Voltage Monitoring

Item		RX21A (LVDAa)	RX23E-A (LVDAb)
Vdet1 voltage monitoring setting procedure	1	Set the LVDLVLR.LVD1LVL[3:0] bits (voltage detection 1 detection voltage).	Set the LVDLVLR.LVD1LVL[3:0] bits (voltage detection 1 detection voltage).
	2	Clear the LVCMPCR.EXVREFINP1 bit to 0 (internal reference voltage). Clear the LVCMPCR.EXVCCINP1 bit to 0 (VCC voltage).	—
	3	• Digital filter in use Select the sampling clock for the digital filter by setting the LVD1CR0.LVD1FSAMP[1:0] bits. • Digital filter not in use Set the LVD1CR0.LVD1DFDIS bit to 1 (digital filter disabled).	—
	4	Set the LVCMPCR.LVD1E bit to 1 (voltage detection 1 circuit enabled).	Set the LVCMPCR.LVD1E bit to 1 (voltage detection 1 circuit enabled).
	5	Wait for at least td(E-A).	Wait for at least td(E-A).
	6	Set the LVD1CR0.LVD1CMPE bit to 1 (voltage monitoring 1 circuit comparison result output enabled).	Set the LVD1CR0.LVD1CMPE bit to 1 (voltage monitoring 1 circuit comparison result output enabled).
	7	• Digital filter in use Wait for at least 1 cycle of LOCO. • Digital filter not in use — (No action required.)	—
	8	• Digital filter in use Clear the LVD1CR0.LVD1DFDIS bit to 0 (digital filter enabled). • Digital filter not in use — (No action required.)	—
	9	• Digital filter in use Wait for at least 2n + 3 cycles of LOCO (n = 1, 2, 4, or 8; digital filter sampling clock = LOCO divided by n). • Digital filter not in use — (No waiting required.)	—

Table 2.11 Comparison of Setting Procedures for Vdet2 Voltage Monitoring

Item		RX21A (LVDAa)	RX23E-A (LVDAb)
Vdet2 voltage monitoring setting procedure	1	Set the LVDLVLR.LVD2LVL[3:0] bits (voltage detection 2 detection voltage).	Set the LVDLVLR.LVD2LVL[1:0] bits (voltage detection 2 detection voltage).
	2	Clear the LVCMPCR.EXVREFINP2 bit to 0 (internal reference voltage). Set the LVCMPCR.EXVCCINP2 bit to 0 (VCC voltage) or 1 (voltage input on CMPA2 pin).	—
	3	• Digital filter in use Select the sampling clock for the digital filter by setting the LVD2CR0.LVD2FSAMP[1:0] bits. • Digital filter not in use Set the LVD2CR0.LVD2DFDIS bit to 1 (digital filter disabled).	—
	4	Set the LVCMPCR.LVD2E bit to 1 (voltage detection 2 circuit enabled).	Set the LVCMPCR.LVD2E bit to 1 (voltage detection 2 circuit enabled).
	5	Wait for at least td(E-A).	Wait for at least td(E-A).
	6	Set the LVD2CR0.LVD2CMPE bit to 1 (voltage monitoring 2 circuit comparison result output enabled).	Set the LVD2CR0.LVD2CMPE bit to 1 (voltage monitoring 2 circuit comparison result output enabled).
	7	• Digital filter in use Wait for at least 1 cycle of LOCO. • Digital filter not in use — (No action required.)	—
	8	• Digital filter in use Clear the LVD2CR0.LVD2DFDIS bit to 0 (digital filter enabled). • Digital filter not in use — (No action required.)	—
	9	• Digital filter in use Wait for at least 2n + 3 cycles of LOCO (n = 1, 2, 4, or 8; digital filter sampling clock = LOCO divided by n). • Digital filter not in use — (No waiting required.)	—

Table 2.12 Comparison of Operation Setting Procedures for Voltage Monitoring 1 Interrupt and Voltage Monitoring 1 Reset Related Bits

Item		RX21A (LVDAa)	RX23E-A (LVDAb)
Voltage monitoring 1 interrupt, voltage monitoring 1 ELC event output	1	Select the detection voltage by setting the LVDLVLR.LVD1LVL[3:0] bits.	Select the detection voltage by setting the LVDLVLR.LVD1LVL[3:0] bits.
	2	Clear the LVCMPCR.EXVREFINP1 bit to 0 (internal reference voltage). Clear the LVCMPCR.EXVCCINP1 bit to 0 (VCC voltage).	—
	3	• Digital filter in use Select the sampling clock for the digital filter by setting the LVD1CR0.LVD1FSAMP[1:0] bits. • Digital filter not in use Set the LVD1CR0.LVD1DFDIS bit to 1 (digital filter disabled).	—
	4	Clear the LVD1CR0.LVD1RI bit to 0 (voltage monitoring 1 interrupt).	Clear the LVD1CR0.LVD1RI bit to 0 (voltage monitoring 1 interrupt).
	5	Select the timing of interrupt requests by setting the LVD1CR1.LVD1IDTSEL[1:0] bits. Select the type of interrupt by setting the LVD1CR1.LVD1IRQSEL bit.	Select the timing of interrupt requests by setting the LVD1CR1.LVD1IDTSEL[1:0] bits. Select the type of interrupt by setting the LVD1CR1.LVD1IRQSEL bit.
	6	Set the LVCMPCR.LVD1E bit to 1 (voltage detection 1 circuit enabled).	Set the LVCMPCR.LVD1E bit to 1 (voltage detection 1 circuit enabled).
	7	Wait for at least td(E-A).	Wait for at least td(E-A).
	8	Set the LVD1CR0.LVD1CMPE bit to 1 (voltage monitoring 1 circuit comparison result output enabled).	Set the LVD1CR0.LVD1CMPE bit to 1 (voltage monitoring 1 circuit comparison result output enabled).
	9	—	Wait for at least 2 µs.
	10	• Digital filter in use Wait for at least 1 cycle of LOCO. • Digital filter not in use — (No action required.)	—
	11	• Digital filter in use Clear the LVD1CR0.LVD1DFDIS bit to 0 (digital filter enabled). • Digital filter not in use — (No action required.)	—
	12	• Digital filter in use Wait for at least 2n + 3 cycles of LOCO (n = 1, 2, 4, or 8; digital filter sampling clock = LOCO divided by n). • Digital filter not in use — (No waiting required.)	—
	13	Clear the LVD1SR.LVD1DET bit to 0.	Clear the LVD1SR.LVD1DET bit to 0.
	14	Set the LVD1CR0.LVD1RIE bit to 1 (voltage monitoring 1 interrupt/reset enabled).	Set the LVD1CR0.LVD1RIE bit to 1 (voltage monitoring 1 interrupt/reset enabled).

Item		RX21A (LVDAa)	RX23E-A (LVDAb)
Voltage monitoring 1 reset	1	Select the detection voltage by setting the LVDLVLR.LVD1LVL[3:0] bits.	Select the detection voltage by setting the LVDLVLR.LVD1LVL[3:0] bits.
	2	Clear the LVCMPCR.EXVREFINP1 bit to 0 (internal reference voltage). Clear the LVCMPCR.EXVCCINP1 bit to 0 (VCC voltage).	—
	3	• Digital filter in use Select the sampling clock for the digital filter by setting the LVD1CR0.LVD1FSAMP[1:0] bits. • Digital filter not in use Set the LVD1CR0.LVD1DFDIS bit to 1 (digital filter disabled).	—
	4	Set the LVD1CR0.LVD1RI bit to 1 (voltage monitoring 1 reset). Select the reset negation type by setting the LVD1CR0.LVD1RN bit.	Set the LVD1CR0.LVD1RI bit to 1 (voltage monitoring 1 reset). Select the reset negation type by setting the LVD1CR0.LVD1RN bit.
	5	Set the LVD1CR0.LVD1RIE bit to 1 (voltage monitoring 1 interrupt/reset enabled).	Set the LVD1CR0.LVD1RIE bit to 1 (voltage monitoring 1 interrupt/reset enabled).
	6	Set the LVCMPCR.LVD1E bit to 1 (voltage detection 1 circuit enabled).	Set the LVCMPCR.LVD1E bit to 1 (voltage detection 1 circuit enabled).
	7	Wait for at least td(E-A).	Wait for at least td(E-A).
	8	Set the LVD1CR0.LVD1CMPE bit to 1 (voltage monitoring 1 circuit comparison result output enabled).	Set the LVD1CR0.LVD1CMPE bit to 1 (voltage monitoring 1 circuit comparison result output enabled).
	9	—	Wait for at least 2 µs.
	10	• Digital filter in use Wait for at least 1 cycle of LOCO. • Digital filter not in use — (No action required.)	—
	11	• Digital filter in use Clear the LVD1CR0.LVD1DFDIS bit to 0 (digital filter enabled). • Digital filter not in use — (No action required.)	—
	12	• Digital filter in use Wait for at least 2n + 3 cycles of LOCO (n = 1, 2, 4, or 8; digital filter sampling clock = LOCO divided by n). • Digital filter not in use — (No waiting required.)	—

Table 2.13 Comparison of Operation Setting Procedures for Voltage Monitoring 2 Interrupt and Voltage Monitoring 2 Reset Related Bits

Item		RX21A (LVDAa)	RX23E-A (LVDAb)
Voltage monitoring 2 interrupt, voltage monitoring 2 ELC event output	1	Select the detection voltage by setting the LVDLVLR.LVD2LVL[3:0] bits.	Select the detection voltage by setting the LVDLVLR.LVD2LVL[1:0] bits.
	2	Clear the LVCMPCR.EXVREFINP2 bit to 0 (internal reference voltage). Set the LVCMPCR.EXVCCINP2 bit to 0 (VCC voltage) or 1 (voltage input on CMPA2 pin).	—
	3	• Digital filter in use Select the sampling clock for the digital filter by setting the LVD2CR0.LVD2FSAMP[1:0] bits. • Digital filter not in use Set the LVD2CR0.LVD2DFDIS bit to 1 (digital filter disabled).	—
	4	Clear the LVD2CR0.LVD2RI bit to 0 (voltage monitoring 2 interrupt).	Clear the LVD2CR0.LVD2RI bit to 0 (voltage monitoring 2 interrupt).
	5	Select the timing of interrupt requests by setting the LVD2CR1.LVD2IDTSEL[1:0] bits. Select the type of interrupt by setting the LVD2CR1.LVD2IRQSEL bit.	Select the timing of interrupt requests by setting the LVD2CR1.LVD2IDTSEL[1:0] bits. Select the type of interrupt by setting the LVD2CR1.LVD2IRQSEL bit.
	6	Set the LVCMPCR.LVD2E bit to 1 (voltage detection 2 circuit enabled).	Set the LVCMPCR.LVD2E bit to 1 (voltage detection 2 circuit enabled).
	7	Wait for at least td(E-A).	Wait for at least td(E-A).
	8	Set the LVD2CR0.LVD2CMPE bit to 1 (voltage monitoring 2 circuit comparison result output enabled).	Set the LVD2CR0.LVD2CMPE bit to 1 (voltage monitoring 2 circuit comparison result output enabled).
	9	—	Wait for at least 2 µs.
	10	• Digital filter in use Wait for at least 1 cycle of LOCO. • Digital filter not in use — (No action required.)	—
	11	• Digital filter in use Clear the LVD2CR0.LVD2DFDIS bit to 0 (digital filter enabled). • Digital filter not in use — (No action required.)	—
	12	• Digital filter in use Wait for at least 2n + 3 cycles of LOCO (n = 1, 2, 4, or 8; digital filter sampling clock = LOCO divided by n). • Digital filter not in use — (No waiting required.)	—
	13	Clear the LVD2SR.LVD2DET bit to 0.	Clear the LVD2SR.LVD2DET bit to 0.
	14	Set the LVD2CR0.LVD2RIE bit to 1 (voltage monitoring 2 interrupt/reset enabled).	Set the LVD2CR0.LVD2RIE bit to 1 (voltage monitoring 2 interrupt/reset enabled).

Item		RX21A (LVDAa)	RX23E-A (LVDAb)
Voltage monitoring 2 reset	1	Select the detection voltage by setting the LVDLVLR.LVD2LVL[3:0] bits.	Select the detection voltage by setting the LVDLVLR.LVD2LVL[1:0] bits.
	2	Clear the LVCMPCR.EXVREFINP2 bit to 0 (internal reference voltage). Set the LVCMPCR.EXVCCINP2 bit to 0 (VCC voltage) or 1 (voltage input on CMPA2 pin).	—
	3	• Digital filter in use Select the sampling clock for the digital filter by setting the LVD2CR0.LVD2FSAMP[1:0] bits. • Digital filter not in use Set the LVD2CR0.LVD2DFDIS bit to 1 (digital filter disabled).	—
	4	Set the LVD2CR0.LVD2RI bit to 1 (voltage monitoring 2 reset). Select the reset negation type by setting the LVD2CR0.LVD2RN bit.	Set the LVD2CR0.LVD2RI bit to 1 (voltage monitoring 2 reset). Select the reset negation type by setting the LVD2CR0.LVD2RN bit.
	5	Set the LVD2CR0.LVD2RIE bit to 1 (voltage monitoring 2 interrupt/reset enabled).	Set the LVD2CR0.LVD2RIE bit to 1 (voltage monitoring 2 interrupt/reset enabled).
	6	Set the LVCMPCR.LVD2E bit to 1 (voltage detection 2 circuit enabled).	Set the LVCMPCR.LVD2E bit to 1 (voltage detection 2 circuit enabled).
	7	Wait for at least td(E-A).	Wait for at least td(E-A).
	8	Set the LVD2CR0.LVD2CMPE bit to 1 (voltage monitoring 2 circuit comparison result output enabled).	Set the LVD2CR0.LVD2CMPE bit to 1 (voltage monitoring 2 circuit comparison result output enabled).
	9	—	Wait for at least 2 µs.
	10	• Digital filter in use Wait for at least 1 cycle of LOCO. • Digital filter not in use — (No action required.)	—
	11	• Digital filter in use Clear the LVD2CR0.LVD2DFDIS bit to 0 (digital filter enabled). • Digital filter not in use — (No action required.)	—
	12	• Digital filter in use Wait for at least 2n + 3 cycles of LOCO (n = 1, 2, 4, or 8; digital filter sampling clock = LOCO divided by n). • Digital filter not in use — (No waiting required.)	—

2.7 Clock Generation Circuit

Table 2.14 is a comparative overview of the clock generation circuits, and Table 2.15 is a comparison of clock generation circuit registers.

Table 2.14 Comparative Overview of Clock Generation Circuits

Item	RX21A	RX23E-A
Use	• Generates the system clock (ICLK) to be supplied to the CPU, DMAC, DTC, ROM, and RAM. • Of the peripheral module clocks (PCLKA, PCLKB, PCLKC, and PCLKD) supplied to the peripheral modules, PCLKA is the operating clock for the DEU, PCLKD is the operating clock for the AD, PCLKC is the operating clock for the DSAD, and PCLKB is the operating clock for modules other than DEU, DSAD, and AD. • Generates the FlashIF clock (FCLK) to be supplied to the FlashIF. • Generates the CAC clock (CACCLK) to be supplied to the CAC. • Generates the RTC-dedicated sub-clock (RTCSCLK) to be supplied to the RTC. • Generates the IWDT-dedicated clock (IWDTCLK) to be supplied to the IWDT.	• Generates the system clock (ICLK) to be supplied to the CPU, DMAC, DTC, ROM, and RAM. • Of the peripheral module clocks (PCLKA, PCLKB, and PCLKD) supplied to the peripheral modules, PCLKA is the operating clock for the MTU2, PCLKD is the operating clock for the S12AD, and PCLKB is the operating clock for modules other than MTU2 and S12AD. • Generates the FlashIF clock (FCLK) to be supplied to the FlashIF. • Generates the CAC clock (CACCLK) to be supplied to the CAC. • Generates the IWDT-dedicated clock (IWDTCLK) to be supplied to the IWDT. • Generates the CAN clock (CANMCLK) to be supplied to the CAN. • Generates the LPT clock (LPTCLK) to be supplied to the LPT.
Operating frequency	• ICLK: 50 MHz (max.) • PCLKA: 50 MHz (max.) • PCLKB: 25 MHz (max.) • PCLKC: 25 MHz (max.) • PCLKD: 25 MHz (max.) • FCLK: — 4 MHz to 25 MHz (for programming and erasing the ROM and E2 DataFlash) — 25 MHz (max.) (for reading from the E2 DataFlash) • CACCLK: Same as clock from respective oscillators • RTCSCLK: 32.768 kHz • IWDTCLK: 125 kHz	• ICLK: 32 MHz (max.) • PCLKA: 32 MHz (max.) • PCLKB: 32 MHz (max.) • PCLKD: 32 MHz (max.) • FCLK: — 1 MHz to 32 MHz (for programming and erasing the ROM and E2 DataFlash) — 32 MHz (max.) (for reading from the E2 DataFlash) • CACCLK: Same as clock from respective oscillators • IWDTCLK: 15 kHz • CANMCLK: 20 MHz (max.) • LPTCLK: Same frequency as that of the selected oscillator

Item	RX21A	RX23E-A
Main clock oscillator	• Resonator frequency: 1 to 20 MHz • External clock input frequency: 20 MHz (max.) • Connectable resonator or additional circuit: ceramic resonator, crystal • Connection pins: EXTAL, XTAL • Oscillation stop detection function: When a main clock oscillation stop is detected, the system clock source is switched to LOCO and MTU pin can be forcedly driven to high-impedance. • Drive capacity switching function	• Resonator frequency: 1 to 20 MHz (VCC ≥ 2.4 V), 1 to 8 MHz (VCC < 2.4 V) • External clock input frequency: 20 MHz (max.) • Connectable resonator or additional circuit: ceramic resonator, crystal • Connection pins: EXTAL, XTAL • Oscillation stop detection function: When a main clock oscillation stop is detected, the system clock source is switched to LOCO and MTU pin can be forcedly driven to high-impedance. • Drive capacity switching function
Sub-clock oscillator	• Resonator frequency: 32.768 kHz • Connectable resonator or additional circuit: crystal • Connection pin: XCIN, XCOUT	—
PLL circuit	• Input clock source: Main clock • Input pulse frequency division ratio: Selectable from 1, 2, and 4 • Input frequency: 4 MHz to 12.5 MHz • Frequency multiplication ratio: Selectable from 8, 10, 12, 16, 20, 24, 25 • VCO oscillation frequency: 50 MHz to 100 MHz	• Input clock source: Main clock • Input pulse frequency division ratio: Selectable from 1, 2, and 4 • Input frequency: 4 MHz to 8 MHz • Frequency multiplication ratio: Selectable from 4 to 8 (increments of 0.5) • Oscillation frequency: 24 MHz to 32 MHz (VCC ≥ 2.4 V)
High-speed on-chip oscillator (HOCO)	• Oscillation frequency: 32 MHz, 36.864 MHz, 40 MHz, and 50 MHz • HOCO power supply control	Oscillation frequency: 32 MHz
Low-speed on-chip oscillator (LOCO)	Oscillation frequency: 125 kHz	Oscillation frequency: 4 MHz
IWDT-dedicated on-chip oscillator	Oscillation frequency: 125 kHz	Oscillation frequency: 15 kHz

Table 2.15 Comparison of Clock Generation Circuit Registers

Register	Bit	RX21A	RX23E-A
SCKCR	—	System clock control register	System clock control register
		The value after a reset differs.	
	PCKC[3:0]	Peripheral module clock C (PCLKC) select bits	—
	BCK[3:0]	External bus clock (BCLK) select bits	—

Register	Bit	RX21A	RX23E-A
SCKCR3	CKSEL[2:0]	Clock source select bits b10 b8 0 0 0: LOCO 0 0 1: HOCO 0 1 0: Main clock oscillator 0 1 1: Sub-clock oscillator 1 0 0: PLL circuit Settings other than the above are prohibited.	Clock source select bits b10 b8 0 0 0: LOCO 0 0 1: HOCO 0 1 0: Main clock oscillator 1 0 0: PLL circuit Settings other than above are prohibited.
PLLCR	STC[4:0] (RX21A) STC[5:0] (RX23E-A)	Frequency multiplication factor select bits (b12 to b8) b12 b8 0 0 1 1 1: ×8 0 1 0 0 1: ×10 0 1 0 1 1: ×12 0 1 1 1 1: ×16 1 0 0 1 1: ×20 1 0 1 1 1: ×24 1 1 0 0 0: ×25 Settings other than the above are prohibited.	Frequency multiplication factor select bits (b13 to b8) b13 b8 0 0 0 1 1 1: ×4 0 0 1 0 0 0: ×4.5 0 0 1 0 0 1: ×5 0 0 1 0 1 0: ×5.5 0 0 1 0 1 1: ×6 0 0 1 1 0 0: ×6.5 0 0 1 1 0 1: ×7 0 0 1 1 1 0: ×7.5 0 0 1 1 1 1: ×8 Settings other than the above are prohibited.
		The value after a reset differs.	
SOSCCR	—	Sub-clock oscillator control register	—
HOCOCR2	—	High-speed on-chip oscillator control register 2	—
OSCOVFSR	—	—	Oscillation stabilization flag register
MOSCWTCR	—	—*1	Main clock oscillator control register
CKOCR	—	—	CLKOUT output control register
MOFCR	—	Main clock oscillator forced oscillation control register	Main clock oscillator forced oscillation control register
		The value after a reset differs.	
	MODRV[2:0]	Main clock oscillator drive capability switch bits	—
	MODRV2[1:0] (RX21A) MODRV21 (RX23E-A)	Main clock oscillator drive capability switch 2 (b5, b4) b5 b4 0 1: 1 MHz to 8 MHz 1 0: 8.1 MHz to 15.9 MHz 1 1: 16 MHz to 20 MHz Settings other than the above are prohibited.	Main clock oscillator drive capability switch (b5) VCC ≥ 2.4 V 0: 1 MHz to less than 10 MHz 1: 10 MHz to 20 MHz VCC < 2.4 V 0: 1 MHz to 8 MHz 1: Setting prohibited.

Register	Bit	RX21A	RX23E-A
LOCOTRR	—	—	Low-speed on-chip oscillator trimming register
ILOCOTRR	—	—	IWDT dedicated on-chip oscillator trimming register
HOCOTRR0	—	—	High-speed on-chip oscillator trimming register 0
HOCOPCR	—	High-speed on-chip oscillator power supply control register	—
PLLPCR	—	PLL power control register	—

Note: 1. A description of the MOSCWTCR register appears in section 11, Low Power Consumption in RX21A Group User's Manual: Hardware

2.8 Clock Frequency Accuracy Measurement Circuit

Table 2.16 is a comparative overview of clock frequency accuracy measurement circuits, and Table 2.17 is a comparison of clock frequency accuracy measurement circuit registers.

Table 2.16 Comparative Overview of Clock Frequency Accuracy Measurement Circuits

Item	RX21A (CAC)	RX23E-A (CAC)
Measurement target clocks	The frequencies of the following clocks can be measured: • Clock output from main clock oscillator (main clock) • Clock output from sub-clock oscillator (sub-clock) • Clock output from high-speed on-chip oscillator (HOCO clock) • Clock output from low-speed on-chip oscillator (LOCO clock) • Clock output from IWDT-dedicated on-chip oscillator (IWDTCLK clock)	The frequencies of the following clocks can be measured: • Main clock • HOCO clock • LOCO clock • IWDT-dedicated clock (IWDTCLK) • Peripheral module clock B (PCLKB)
Measurement reference clocks	• External clock input on CACREF pin • Clock output from main clock oscillator (main clock) • Clock output from sub-clock oscillator (sub-clock) • Clock output from high-speed on-chip oscillator (HOCO clock) • Clock output from low-speed on-chip oscillator (LOCO clock) • Clock output from IWDT-dedicated on-chip oscillator (IWDTCLK clock)	• External clock input on CACREF pin • Main clock • HOCO clock • LOCO clock • IWDT-dedicated clock (IWDTCLK) • Peripheral module clock B (PCLKB)
Selectable function	Digital filter function	Digital filter function
Interrupt sources	• Measurement end interrupt • Frequency error interrupt • Overflow interrupt	• Measurement end interrupt • Frequency error interrupt • Overflow interrupt
Low power consumption function	Ability to specify module stop state	Ability to transition to module stop state

Table 2.17 Comparison of Clock Frequency Accuracy Measurement Circuit Registers

Register	Bit	RX21A (CAC)	RX23E-A (CAC)
CACR1	FMCS[2:0]	Frequency measurement clock select bits b3 b1 0 0 0: Output clock of main clock oscillator 0 0 1: Output clock of sub-clock oscillator 0 1 0: Output clock of high-speed on-chip oscillator 0 1 1: Output clock of low-speed on-chip oscillator 1 0 0: Output clock of IWDT-dedicated on-chip oscillator Settings other than the above are prohibited.	Measurement target clock select bits b3 b1 0 0 0: Main clock 0 1 0: HOCO clock 0 1 1: LOCO clock 1 0 0: IWDT-dedicated clock (IWDTCLK) 1 0 1: Peripheral module clock B (PCLKB) Settings other than the above are prohibited.
CACR2	RSCS[2:0]	Reference signal generation clock select bits b3 b1 0 0 0: Output clock of main clock oscillator 0 0 1: Output clock of sub-clock oscillator 0 1 0: Output clock of high-speed on-chip oscillator 0 1 1: Output clock of low-speed on-chip oscillator 1 0 0: Output clock of IWDT-dedicated on-chip oscillator Settings other than the above are prohibited.	Measurement reference clock select bits b3 b1 0 0 0: Main clock 0 1 0: HOCO clock 0 1 1: LOCO clock 1 0 0: IWDT-dedicated clock (IWDTCLK) 1 0 1: Peripheral module clock B (PCLKB) Settings other than the above are prohibited.

2.9 Low Power Consumption

Table 2.18 is a comparative overview of the low power consumption functions, Table 2.19 is a comparison of procedures for entering and exiting low power consumption modes and operating states in each mode, and Table 2.20 is a comparison of low power consumption registers.

Table 2.18 Comparative Overview of Low Power Consumption Functions

Item	RX21A	RX23E-A
Reducing power consumption by switching clock signals	The frequency division ratio can be set independently for the system clock (ICLK), DEU clock (PCLKA), peripheral module clock (PCLKB), DSAD clock (PCLKC), AD clock (PCLKD), and FlashIF clock (FCLK).	The frequency division ratio can be set independently for the system clock (ICLK), high speed peripheral module clock (PCLKA), peripheral module clock (PCLKB), S12AD clock (PCLKD), and FlashIF clock (FCLK).
Module stop function	Each peripheral module can be stopped independently by the module stop control register.	Each peripheral module can be stopped independently by the module stop control register.
Function for transition to low power consumption mode	Transition to a low power consumption mode in which the CPU, peripheral modules, or oscillators are stopped is enabled.	Transition to a low power consumption mode in which the CPU, peripheral modules, or oscillators are stopped is enabled.
Low power consumption modes	• Sleep mode • All-module clock stop mode • Software standby mode • Deep software standby mode	• Sleep mode • Deep sleep mode • Software standby mode
Function for lower operating power consumption	• Power consumption can be reduced in normal operation, sleep mode, and all-module clock stop mode by selecting an appropriate operating power control mode according to the operating frequency and operating voltage. • Seven operating power control modes are available — High-speed operating mode — Middle-speed operating mode 1A — Middle-speed operating mode 1B — Middle-speed operating mode 2A — Middle-speed operating mode 2B — Low-speed operating mode 1 — Low-speed operating mode 2	• Power consumption can be reduced in normal operation, sleep mode, and deep sleep mode by selecting an appropriate operating power control mode according to the operating frequency and operating voltage. • Two operating power control modes are available — High-speed operating mode — Middle-speed operating mode

Table 2.19 Comparison of Procedures for Entering and Exiting Low Power Consumption Modes and Operating States in Each Mode

Mode	Entering and Exiting Low Power Consumption Modes and Operating States	RX21A	RX23E-A
Sleep mode	Transition method	Control register + instruction	Control register + instruction
	Method of cancellation other than reset	Interrupt	Interrupt
	State after cancellation	Program execution state (interrupt processing)	Program execution state (interrupt processing)
	Main clock oscillator	Operation possible	Operation possible
	Sub-clock oscillator	Operation possible	—
	High-speed on-chip oscillator	Operation possible	Operation possible
	Low-speed on-chip oscillator	Operation possible	Operation possible
	IWDT-dedicated on-chip oscillator	Operation possible	Operation possible
	PLL	Operation possible	Operation possible
	CPU	Stopped (retained)	Stopped (retained)
	RAM (0000 0000h to 0000 FFFFh)	Operation possible (retained)	Operation possible (retained)
	DMAC	Operation possible	Operation possible
	DTC	Operation possible	Operation possible
	Flash memory	Operation	Operation
	Watchdog timer	Stopped (retained)	—
	Independent watchdog timer (IWDT)	Operation possible	Operation possible
	Realtime clock (RTC)	Operation possible	—
	Low-power timer (LPT)	—	Operation possible
	8-bit timer (unit 0, unit 1) (TMR)	Operation possible	Operation possible
	Voltage detection circuit (LVD)	Operation possible	Operation possible
	Power-on reset circuit	Operation	Operation
	Peripheral modules	Operation possible	Operation possible
	I/O ports	Operation	Operation
	CLKOUT output	—	Operation possible
Software standby mode	Transition method	Control register + instruction	Control register + instruction
	Method of cancellation other than reset	Interrupt	Interrupt
	State after cancellation	Program execution state (interrupt processing)	Program execution state (interrupt processing)
	Main clock oscillator	Stopped	Stopped
	Sub-clock oscillator	Operation possible	—
	High-speed on-chip oscillator	Stopped	Stopped
	Low-speed on-chip oscillator	Stopped	Stopped
	IWDT-dedicated on-chip oscillator	Operation possible	Operation possible
	PLL	Stopped	Stopped
	CPU	Stopped (retained)	Stopped (retained)
	RAM (0000 0000h to 0000 FFFFh)	Stopped (retained)	Stopped (retained)
	DMAC	Stopped (retained)	Stopped (retained)
	DTC	Stopped (retained)	Stopped (retained)
	Flash memory	Stopped (retained)	Stopped (retained)
	Watchdog timer	Stopped (retained)	—
	Independent watchdog timer (IWDT)	Operation possible	Operation possible

Mode	Entering and Exiting Low Power Consumption Modes and Operating States	RX21A	RX23E-A
Software standby mode	Realtime clock (RTC)	Operation possible	—
	Low-power timer (LPT)	—	Operation possible
	8-bit timer (unit 0, unit 1) (TMR)	Stopped (retained)	Stopped (retained)
	Voltage detection circuit (LVD)	Operation possible	Operation possible
	Power-on reset circuit	Operation	Operation
	Peripheral modules	Stopped (retained)	Stopped (retained)
	I/O ports	Retained	Retained
	CLKOUT output	—	Stopped

Note: "Operation possible" means that whether the state is operating or stopped is controlled by the control register setting.
"Stopped (retained)" means that internal register values are retained and internal operations are suspended.
"Stopped (undefined)" means that internal register values are undefined and power is not supplied to the internal circuit.

Table 2.20 Comparison of Low Power Consumption Registers

Register	Bit	RX21A	RX23E-A
SBYCR	SSBY	Software standby bit 0: Transition to sleep mode or all-module clock stop mode after the WAIT instruction is executed. 1: Transition to software standby mode after the WAIT instruction is executed.	Software standby bit 0: Transition to sleep mode or deep sleep mode after the WAIT instruction is executed. 1: Transition to software standby mode after the WAIT instruction is executed.
MSTPCRA	—	Module stop control register A	Module stop control register A
		The value after a reset differs.	
	MSTPA14	Compare match timer (unit 1) module stop bit	—
	MSTPA16	—	AFE module stop setting bit
	MSTPA17	—	12-bit A/D converter module stop bit
	MSTPA19	D/A converter module stop bit	—
	MSTPA23	10-bit A/D converter module stop bit	—
	MSTPA24	Module stop A24 bit	—
	MSTPA25	24-bit ΔΣ A/D converter module stop bit Target module: DSAD	DSAD0 module stop bit Target module: DSAD0
	MSTPA26	—	DSAD1 module stop bit
	MSTPA27	Module stop A27 bit	—
	MSTPA29	Module stop A29 bit	—
	ACSE	All-module clock stop mode enable bit	—
MSTPCRB	MSTPB0	—	RSCAN0 module stop bit
	MSTPB4	—	Serial communication interface SCIh module stop bit
	MSTPB8	Temperature sensor module stop bit	—
	MSTPB10	Comparator B module stop bit	—
	MSTPB16	Serial peripheral interface 1 module stop bit	—
	MSTPB20	I^2C bus interface 1 module stop bit	—

Register	Bit	RX21A	RX23E-A
MSTPCRC	MSTPC20	IrDA module stop bit	—
	MSTPC26	Serial communication interface 9 module stop bit	—
	MSTPC27	Serial communication interface 8 module stop bit	—
	DSLPE	—	Deep sleep mode enable bit
MSTPCRD	—	Module stop control register D	—
OPCCR	OPCM[2:0]	Operating power control mode select bits b2 b0 0 0 0: High-speed operating mode 0 1 0: Middle-speed operating mode 1A 0 1 1: Middle-speed operating mode 1B 1 0 0: Middle-speed operating mode 2A 1 0 1: Middle-speed operating mode 2B 1 1 0: Low-speed operating mode 1 1 1 1: Low-speed operating mode 2 Settings other than the above are prohibited.	Operating power control mode select bits b2 b0 0 0 0: High-speed operating mode 0 1 0: Middle-speed operating mode Settings other than the above are prohibited.
	OPCMTSF	Operating power control mode transition status flag • Read 0: Transition completed 1: Transition in progress • Write The write value should be 0.	Operating power control mode transition status flag 0: Transition completed 1: Transition in progress
RSTCKCR	—	Sleep mode return clock source switching register	—
MOSCWTCR	—	Main clock oscillator wait control register	—*1
SOSCWTCR	—	Sub-clock oscillator wait control register	—
PLLWTCR	—	PLL wait control register	—
HOCOWTCR2	—	HOCO wait control register 2	—
DPSBYCR	—	Deep standby control register	—
DPSIER0	—	Deep standby interrupt enable register 0	—
DPSIER2	—	Deep standby interrupt enable register 2	—
DPSIFR0	—	Deep standby interrupt flag register 0	—
DPSIFR2	—	Deep standby interrupt flag register 2	—
DPSIEGR0	—	Deep standby interrupt edge register 0	—
DPSIEGR2	—	Deep standby interrupt edge register 2	—

Register	Bit	RX21A	RX23E-A
FHSSBYCR	—	Flash HOCO software standby control register	—
DPSBKRy	—	Deep standby backup register y (y = 0 to 31)	—

Note: 1. A description of the MOSCWTCR register appears in the clock generation circuit section of the RX23E-A Group User's Manual: Hardware.

2.10 Register Write Protection Function

Table 2.21 is a comparative overview of the register write protection functions, and Table 2.22 is a comparison of register write protection function registers.

Table 2.21 Comparative Overview of Register Write Protection Functions

Item	RX21A	RX23E-A
PRC0 bit	Registers related to the clock generation circuit: SCKCR, SCKCR3, PLLCR, PLLCR2, MOSCCR, SOSCCR, LOCOCR, ILOCOCR, HOCOCR, OSTDCR, OSTDSR, HOCOCR2	Registers related to the clock generation circuit: SCKCR, SCKCR3, PLLCR, PLLCR2, MOSCCR, LOCOCR, ILOCOCR, HOCOCR, OSTDCR, OSTDSR, CKOCR, LOCOTRR, ILOCOTRR, HOCOTRR0
PRC1 bit	• Register related to the operating modes: SYSCR1 • Registers related to the low power consumption functions: SBYCR, MSTPCRA, MSTPCRB, MSTPCRC, MSTPCRD, OPCCR, RSTCKCR, MOSCWTCR*1, SOSCWTCR, PLLWTCR, DPSBYCR, DPSIER0, DPSIER2, DPSIFR0, DPSIFR2, DPSIEGR0, DPSIEGR2, FHSSBYCR, HOCOWTCR2 • Registers related to the clock generation circuit: MOFCR, HOCOPCR, PLLPCR • Software reset register: SWRR	• Register related to the operating modes: SYSCR1 • Registers related to the low power consumption functions: SBYCR, MSTPCRA, MSTPCRB, MSTPCRC, OPCCR • Registers related to clock generation circuit: MOFCR, MOSCWTCR*1 • Software reset register: SWRR
PRC2 bit	—	Registers related to the low power timer: LPTCR1, LPTCR2, LPTCR3, LPTPRD, LPCMR0, LPWUCR
PRC3 bit	Registers related to LVD: LVCMPCR, LVDLVLR, LVD1CR0, LVD1CR1, LVD1SR, LVD2CR0, LVD2CR1, LVD2SR	Registers related to LVD: LVCMPCR, LVDLVLR, LVD1CR0, LVD1CR1, LVD1SR, LVD2CR0, LVD2CR1, LVD2SR

Note: 1. A description of the MOSCWTCR register appears in section 11, Low Power Consumption in RX21A Group User's Manual: Hardware and in the clock generation circuit section of the RX23E-A Group User's Manual: Hardware.

Table 2.22 Comparison of Register Write Protection Function Registers

Register	Bit	RX21A	RX23E-A
PRCR	PRC2	—	Enables writing to the registers related to low-power timer.

2.11 Exception Handling

Table 2.23 is a comparative overview of exception handling, Table 2.24 is a comparative listing of vectors, and Table 2.25 is a comparison of instructions for returning from exception handling routines.

Table 2.23 Comparative Overview of Exception Handling

Item	RX21A	RX23E-A
Exception events	• Undefined instruction exception • Privileged instruction exception • Access exception • Reset • Non-maskable interrupt • Interrupt • Unconditional trap	• Undefined instruction exception • Privileged instruction exception • Access exception • Floating-point exception • Reset • Non-maskable interrupt • Interrupt • Unconditional trap

Table 2.24 Comparison of Vectors

Item		RX21A	RX23E-A
Undefined instruction exception		Fixed vector table	Exception vector table (EXTB)
Privileged instruction exception		Fixed vector table	Exception vector table (EXTB)
Access exception		Fixed vector table	Exception vector table (EXTB)
Floating-point exception		—	Exception vector table (EXTB)
Reset		Fixed vector table	Exception vector table (EXTB)
Non-maskable interrupt		Fixed vector table	Exception vector table (EXTB)
Interrupt	Fast interrupt	FINTV	FINTV
	Other than fast interrupt	Relocatable vector table (INTB)	Interrupt vector table (INTB)
Unconditional trap		Relocatable vector table (INTB)	Interrupt vector table (INTB)

Table 2.25 Comparison of Instructions for Returning from Exception Handling Routines

Item		RX21A	RX23E-A
Undefined instruction exception		RTE	RTE
Privileged instruction exception		RTE	RTE
Access exception		RTE	RTE
Floating-point exception		—	RTE
Reset		Return not possible	Return not possible
Non-maskable interrupt		Return not possible	Prohibited
Interrupt	Fast interrupt	RTFI	RTFI
	Other than fast interrupt	RTE	RTE
Unconditional trap		RTE	RTE

2.12 Interrupt Controller

Table 2.26 is a comparative overview of the interrupt controllers, and Table 2.27 is a comparison of interrupt controller registers.

Table 2.26 Comparative Overview of Interrupt Controllers

Item		RX21A (ICUb)	RX23E-A (ICUb)
Interrupts	Peripheral function interrupts	• Interrupts from peripheral modules • Interrupt detection: Edge detection/level detection Edge detection or level detection is fixed for each source of connected peripheral modules	• Interrupts from peripheral modules • Interrupt detection: Edge detection/level detection Edge detection or level detection is fixed for each source of connected peripheral modules
	External pin interrupts	• Interrupts from pins IRQ0 to IRQ7 • Number of sources: 8 • Interrupt detection: Low level/falling edge/rising edge/rising and falling edges. One of these detection methods can be set for each source. • Digital filter function: Supported	• Interrupts from pins IRQ0 to IRQ7 • Number of sources: 8 • Interrupt detection: Low level/falling edge/rising edge/rising and falling edges. One of these detection methods can be set for each source. • Digital filter function: Supported
	Software interrupt	• Interrupt generated by writing to a register. • One interrupt source	• Interrupt generated by writing to a register. • One interrupt source
	Event link interrupt	The ELSR18I or ELSR19I interrupt is generated by an ELC event	The ELSR8I, ELSR18I, or ELSR19I interrupt is generated by an ELC event
	Interrupt priority level	Priority levels are specified by registers.	Priority levels are specified by registers.
	Fast interrupt function	Faster interrupt processing of the CPU can be set only for a single interrupt source.	Faster interrupt processing of the CPU can be set only for a single interrupt source.
	DTC and DMAC control	The DTC and DMAC can be activated by interrupt sources.	The DTC and DMAC can be activated by interrupt sources.
Non-maskable interrupts	NMI pin interrupt	• Interrupt from the NMI pin • Interrupt detection: Falling edge/rising edge • Digital filter function: Supported	• Interrupt from the NMI pin • Interrupt detection: Falling edge/rising edge • Digital filter function: Supported
	Oscillation stop detection interrupt	Interrupt on detection of oscillation having stopped	Interrupt on detection of oscillation having stopped
	WDT underflow/ refresh error	Interrupt on an underflow of the down counter or occurrence of a refresh error	—
	IWDT underflow/ refresh error	Interrupt on an underflow of the down counter or occurrence of a refresh error	Interrupt on an underflow of the down counter or occurrence of a refresh error
	Voltage monitoring 1 interrupt	Voltage monitoring interrupt of voltage monitoring circuit 1 (LVD1)	Interrupt from voltage monitoring circuit 1 (LVD1)

Item		RX21A (ICUb)	RX23E-A (ICUb)
Non-maskable interrupts	Voltage monitoring 2 interrupt	Voltage monitoring interrupt of voltage monitoring circuit 2 (LVD2)	Voltage monitoring interrupt of voltage monitoring circuit 2 (LVD2)
Return from low power consumption modes	Sleep mode	Return is initiated by a non-maskable interrupt or any other interrupt source.	Return is initiated by a non-maskable interrupt or any other interrupt source.
	Deep sleep mode	—	Return is initiated by a non-maskable interrupt or any other interrupt source.
	All-module clock stop mode	Return is initiated by a non-maskable interrupt, IRQ0 to IRQ7 interrupt, TMR interrupt, or an RTC alarm/periodic interrupt.	—
	Software standby mode	Return is initiated by a non-maskable interrupt, IRQ0 to IRQ7 interrupt, or an RTC alarm/periodic interrupt.	Return is initiated by a non-maskable interrupt or IRQ0 to IRQ7 interrupt.

Table 2.27 Comparison of Interrupt Controller Registers

Register	Bit	RX21A (ICUb)	RX23E-A (ICUb)
IRn*1	—	Interrupt request register n (n = 016 to 253)	Interrupt request register n (n = 016 to 255)
IPRn*1	—	Interrupt source priority register n (n = 000 to 253)	Interrupt source priority register n (n = 000 to 255)
DTCERn*1	—	DTC activation enable register n (n = 027 to 252)	Transfer request enable register n (n = 027 to 255)
NMISR	WDTST	WDT underflow/refresh error status flag	—
NMIER	WDTEN	WDT underflow/refresh error enable bit	—
NMICLR	WDTCLR	IWDT clear bit	—

Note: 1. On the RX21A Group n = 254 and 255, and on the RX23E-A Group n = 250 to 255, are reserved areas.

2.13 Buses

Table 2.28 is a comparative overview of the buses, and Table 2.29 is a comparison of bus registers.

Table 2.28 Comparative Overview of Buses

Item		RX21A	RX23E-A
CPU buses	Instruction bus	• Connected to the CPU (for instructions) • Connected to on-chip memory (RAM, ROM) • Operates in synchronization with the system clock (ICLK)	• Connected to the CPU (for instructions) • Connected to on-chip memory (RAM, ROM) • Operates in synchronization with the system clock (ICLK)
	Operand bus	• Connected to the CPU (for operands) • Connected to on-chip memory (RAM, ROM) • Operates in synchronization with the system clock (ICLK)	• Connected to the CPU (for operands) • Connected to on-chip memory (RAM, ROM) • Operates in synchronization with the system clock (ICLK)
Memory buses	Memory bus 1	Connected to RAM	Connected to RAM
	Memory bus 2	Connected to ROM	Connected to ROM
Internal main buses	Internal main bus 1	• Connected to the CPU • Operates in synchronization with the system clock (ICLK)	• Connected to the CPU • Operates in synchronization with the system clock (ICLK)
	Internal main bus 2	• Connected to the DMAC and DTC • Connected to on-chip memory (RAM, ROM) • Operates in synchronization with the system clock (ICLK)	• Connected to the DMAC and DTC • Connected to on-chip memory (RAM, ROM) • Operates in synchronization with the system clock (ICLK)
Internal peripheral buses	Internal peripheral bus 1	• Connected to peripheral modules (DTC, DMAC, interrupt controller, and bus error monitoring section) • Operates in synchronization with the system clock (ICLK)	• Connected to peripheral modules (DTC, DMAC, interrupt controller, and bus error monitoring section) • Operates in synchronization with the system clock (ICLK)
	Internal peripheral bus 2	• Connected to peripheral modules (modules other than those connected to internal peripheral bus 1) • Operates in synchronization with the peripheral-module clock (PCLKB, PCLKC, PCLKD)	• Connected to peripheral modules (modules other than those connected to internal peripheral buses 1, 3, and 4) • Operates in synchronization with the peripheral-module clock (PCLKB)
	Internal peripheral bus 3	—	• Connected to peripheral modules (RSCAN, DSAD0, DSAD1, and AFE) • Operates in synchronization with the peripheral-module clock (PCLKB)
	Internal peripheral bus 4	• Connected to peripheral modules (DEU) • Operates in synchronization with the peripheral-module clock (PCLKA)	• Connected to peripheral modules (MTU2) • Operates in synchronization with the peripheral-module clock (PCLKA)

Item		RX21A	RX23E-A
Internal peripheral buses	Internal peripheral bus 6	• Connected to the ROM (during programming and erasing) and E2 DataFlash memory • Operates in synchronization with the FlashIF clock (FCLK)	• Connected to the flash control module and E2 DataFlash memory • Operates in synchronization with the FlashIF clock (FCLK)

Table 2.29 Comparison of Bus Registers

Register	Bit	RX21A	RX23E-A
BEREN	TOEN	—	Timeout detection enable bit*1*2
BERSR1	TO	—	Timeout bit
BUSPRI	BPGB[1:0]	Internal peripheral bus 2 priority control bits	Internal peripheral bus 2 and 3 priority control bits

Notes: 1. If bus access is attempted when detection is disabled (TOEN bit = 0), the bus may freeze.
2. Do not clear the TOEN bit to 0 (detection disabled) when timeout error detection is enabled.

2.14 Memory-Protection Unit

Table 2.30 is a comparison of memory-protection unit registers.

Table 2.30 Comparison of Memory-Protection Unit Registers

Register	Bit	RX21A (MPU)	RX23E-A (MPU)
MPESTS	IA (RX21A) IMPER (RX23E-A)	Instruction memory-protection error generated bit	Instruction memory-protection error generated bit
	DA (RX21A) DMPER (RX23E-A)	Data memory-protection error generation bit	Data memory-protection error generation bit

2.15 Event Link Controller

Table 2.31 is a comparative overview of the event link controllers, Table 2.32 is a comparison of event link controller registers, Table 2.33 lists correspondences between ELSRn registers and peripheral modules, and Table 2.34 shows correspondences between values set in ELSRn.ELS[7:0] and event signal names and numbers.

Table 2.31 Comparative Overview of Event Link Controllers

Item	RX21A (ELC)	RX23E-A (ELC)
Event link function	• 69 event signals can be directly connected to modules. • Operation of timer modules while inputting an event signal can be selected. • Event linkage operation is possible on ports B and E. — Single port*1: Event link operation can be enabled on a single port corresponding to the specified bit. — Port group*1: Among the eight I/O ports, event link operation can be enabled for a group of ports corresponding to multiple specified bits.	• 56 event signals can be directly interconnected to modules. • Operation of timer modules while inputting an event signal can be selected. • Event linkage operation is possible on port B. — Single port*1: Event link operation can be specified on a single port corresponding to the specified bit.
Low power consumption function	Ability to specify module stop state	Ability to transition to module stop state

Note: 1. An event is generated when the corresponding input signal on a single port or port group set to input changes.

Table 2.32 Comparison of Event Link Controller Registers

Register	Bit	RX21A (ELC)	RX23E-A (ELC)
ELSRn	—	Event link setting register n (n = 0 to 5, 7, 10, 12, 14, 16, 18 to 36)	Event link setting register n (n = 1 to 4, 7, 8, 10, 12, 15, 18, 19, 24, 25, 28, 29, 46, 47)
	ELS[7:0]	Event link select bits 00000000: Event link function is disabled. 00000001 to 01101001: Specifies the number of the event signal to be linked. Settings other than the above are prohibited.	Event link select bits 00h: Event signal output to the corresponding peripheral module is disabled. 08h to 6Ah: Specifies the number of the event signal to be linked. Settings other than the above are prohibited.
ELOPA	MTU0MD [1:0]	MTU0 operation select bits	—
ELOPB	MTU5MD [1:0]	MTU5 operation select bits	—
ELOPC	LPTMD[1:0]	—	LPT operation select bits
PGRn	—	Port group setting register n (n = 1 and 2)	—

Register	Bit	RX21A (ELC)	RX23E-A (ELC)
PGCn	—	Port Group Control Register n (n = 1 and 2)	—
PDBFn	—	Port buffer register n (n = 1 and 2)	—
PELn	—	Event link port setting register n (n = 0 to 3)	Event link port setting register n (n = 0 and 1)
PELn	PSP[1:0]	Port number specification bits b4 b3 0 0: Setting is invalid. 0 1: Port B (corresponding to PGR1) 1 0: Port E (corresponding to PGR2) 1 1: Do not set this value.	Port number specification bits b4 b3 0 0: Setting is invalid. 0 1: Port B (corresponding to PGR1) 1 0: Setting prohibited. 1 1: Setting prohibited.

Table 2.33 Correspondence between ELSRn Registers and Peripheral Modules

Register	RX21A (ELC)	RX23E-A (ELC)
ELSR0	MTU0	—
ELSR1	MTU1	MTU1
ELSR2	MTU2	MTU2
ELSR3	MTU3	MTU3
ELSR4	MTU4	MTU4
ELSR5	MTU5	—
ELSR7	CMT1	CMT1
ELSR8	—	ICU (dedicated LPT interrupt)*1
ELSR10	TMR0	TMR0
ELSR12	TMR2	TMR2
ELSR14	10-bit A/D converter	—
ELSR15	—	S12AD
ELSR16	DA0	—
ELSR18	Interrupt 1*2	ICU (Interrupt 1)*2
ELSR19	Interrupt 2*2	ICU (Interrupt 2)*2
ELSR20	Output port group 1	—
ELSR21	Output port group 2	—
ELSR22	Input port group 1	—
ELSR23	Input port group 2	—
ELSR24	Single port 0	Single port 0*3
ELSR25	Single port 1	Single port 1*3
ELSR26	Single port 2	—
ELSR27	Single port 3	—
ELSR28	Clock source switching to LOCO	Clock source switching to LOCO
ELSR29	POE	POE
ELSR30	24-bit ΔΣA/D converter channel 0	—
ELSR31	24-bit ΔΣA/D converter channel 1	—
ELSR32	24-bit ΔΣA/D converter channel 2	—
ELSR33	24-bit ΔΣA/D converter channel 3	—
ELSR34	24-bit ΔΣA/D converter channel 4	—
ELSR35	24-bit ΔΣA/D converter channel 5	—
ELSR36	24-bit ΔΣA/D converter channel 6	—
ELSR46	—	DSAD0
ELSR47	—	DSAD1

Notes: 1. Specify 32h (LPT compare match) as the event signal.
2. On the RX21A Group specify an event signal value between 63h and 69h, and on the RX23E-A Group specify an event signal value between 65h to 6Ah. Do not specify a value other than the above.
3. Do not specify data operation circuit (DOC) condition satisfied signal (6Ah) in the ELSR24 or ELSR25 register.

Table 2.34 Correspondence between Values Set in ELSRn.ELS[7:0] Bits and Event Signal Names and Numbers

Value of ELS[7:0] Bits	Peripheral Module	RX21A (ELC)	RX23E-A (ELC)
01h	Multi-function timer pulse unit 2	MTU0 compare match 0A signal	—
02h		MTU0 compare match 0B signal	—
03h		MTU0 compare match 0C signal	—
04h		MTU0 compare match 0D signal	—
05h		MTU0 compare match 0E signal	—
06h		MTU0 compare match 0F signal	—
07h		MTU0 overflow signal	—
08h		MTU1 compare match 1A signal	MTU1 compare match 1A
09h		MTU1 compare match 1B signal	MTU1 compare match 1B
0Ah		MTU1 overflow signal	MTU1 overflow
0Bh		MTU1 underflow signal	MTU1 underflow
0Ch		MTU2 compare match 2A signal	MTU2 compare match 2A
0Dh		MTU2 compare match 2B signal	MTU2 compare match 2B
0Eh		MTU2 overflow signal	MTU2 overflow
0Fh		MTU2 underflow signal	MTU2 underflow
10h		MTU3 compare match 3A signal	MTU3 compare match 3A
11h		MTU3 compare match 3B signal	MTU3 compare match 3B
12h		MTU3 compare match 3C signal	MTU3 compare match 3C
13h		MTU3 compare match 3D signal	MTU3 compare match 3D
14h		MTU3 overflow signal	MTU3 overflow
15h		MTU4 compare match 4A signal	MTU4 compare match 4A
16h		MTU4 compare match 4B signal	MTU4 compare match 4B
17h		MTU4 compare match 4C signal	MTU4 compare match 4C
18h		MTU4 compare match 4D signal	MTU4 compare match 4D
19h		MTU4 overflow signal	MTU4 overflow
1Ah		MTU4 underflow signal	MTU4 underflow
1Bh		MTU5 compare match 5U signal	—
1Ch		MTU5 compare match 5V signal	—
1Dh		MTU5 compare match 5W signal	—
1Fh	Compare match timer	CMT1 compare match 1 signal	CMT1 compare match 1
22h	8-bit timer	TMR0 compare match A0 signal	TMR0 compare match A0
23h		TMR0 compare match B0 signal	TMR0 compare match B0
24h		TMR0 overflow signal	TMR0 overflow
28h		TMR2 compare match A2 signal	TMR2 compare match A2
29h		TMR2 compare match B2 signal	TMR2 compare match B2
2Ah		TMR2 overflow signal	TMR2 overflow
2Eh	Realtime clock	RTC cycle signal	—
31h	Independent watchdog timer	IWDT underflow or refresh error signal	IWDT underflow or refresh error
32h	Low-power timer	—	LPT compare match

Value of ELS[7:0] Bits	Peripheral Module	RX21A (ELC)	RX23E-A (ELC)
34h	12-bit A/D converter	—	S12AD compare condition satisfied
35h		—	S12AD compare condition not satisfied
3Ah	Serial communications interface	SCI5 error (receive error or error signal detection) signal	SCI5 error (receive error or error signal detection)
3Bh		SCI5 receive data full signal	SCI5 receive data full
3Ch		SCI5 transmit data empty signal	SCI5 transmit data empty
3Dh		SCI5 transmit end signal	SCI5 transmit end
4Eh	I^2C bus interface	RIIC0 communication error or event generation signal	RIIC0 communication error or event generation
4Fh		RIIC0 receive data full signal	RIIC0 receive data full
50h		RIIC0 transmit data empty signal	RIIC0 transmit data empty
51h		RIIC0 transmit end signal	RIIC0 transmit end
52h	Serial peripheral interface	RSPI0 error (mode fault, overrun, or parity error) signal	RSPI0 error (mode fault, overrun, or parity error)
53h		RSPI0 idle signal	RSPI0 idle
54h		RSPI0 receive data full signal	RSPI0 receive data full
55h		RSPI0 transmit data empty signal	RSPI0 transmit data empty
56h		RSPI0 transmit end signal (except during clock synchronous operation in slave mode)	RSPI0 transmit end
57h	10-bit A/D converter	A/D conversion end signal of 10-bit A/D converter	—
58h	12-bit A/D converter	—	S12AD A/D conversion end
59h	Comparator B0	Comparator B0 comparison result change signal	—
5Ah	Comparator B0 and B1	Comparator B0 and B1 common comparison result change signal	—
5Bh	Voltage detection circuit	LVD1 voltage detection signal	LVD1 voltage detection
5Ch		LVD2 voltage detection signal	LVD2 voltage detection
5Dh	DMA controller	DMAC0 transfer end signal	DMAC0 transfer end
5Eh		DMAC1 transfer end signal	DMAC1 transfer end
5Fh		DMAC2 transfer end signal	DMAC2 transfer end
60h		DMAC3 transfer end signal	DMAC3 transfer end
61h	Data transfer controller	DTC transfer end signal	DTC transfer end
62h	Clock generation circuit	Oscillation stop detection signal of clock generation circuit	Oscillation stop detection of clock generation circuit
63h	I/O ports	Input edge detection signal of input port group 1	—
64h		Input edge detection signal of input port group 2	—
65h		Input edge detection signal of single input port 0	Input edge detection of single input port 0
66h		Input edge detection signal of single input port 1	Input edge detection of single input port 1
67h		Input edge detection signal of single input port 2	—
68h		Input edge detection signal of single input port 3	—

Value of ELS[7:0] Bits	Peripheral Module	RX21A (ELC)	RX23E-A (ELC)
69h	Event link controller	Software event signal	Software event
6Ah	Data operation circuit	—	DOC data operation condition met
Settings other than the above are prohibited.			

2.16 I/O Ports

Table 2.35 is a comparative overview of the I/O ports of 64-pin (RX21A) and 48-pin (RX23E-A) and 40-pin (RX23E-A) products, Table 2.36 is a comparison of I/O port functions, and Table 2.37 is a comparison of I/O port registers.

Table 2.35 Comparative Overview of I/O Ports of 64-Pin (RX21A) and 48-Pin (RX23E-A) and 40-pin (RX23E-A) Products

Port Symbol	RX21A (64-Pin)	RX23E-A (48-Pin)	RX23E-A (40-Pin)
PORT0	P03, P05	—	—
PORT1	P14 to P17	P14 to P17	P14 to P17
PORT2	P26, P27	P26, P27	P26, P27
PORT3	P30 to P32, P35 to P37	P30, P31, P35 to P37	P30, P31, P35 to P37
PORT4	P40, P41	—	—
PORT5	P54, P55	—	—
PORTA	PA0, PA1, PA3, PA4, PA6	—	—
PORTB	PB0, PB1, PB3, PB5 to PB7	PB0, PB1	PB0, PB1
PORTC	PC2 to PC7	PC4 to PC7	PC4, PC5
PORTH	PH0 to PH3	PH0 to PH3	PH0, PH1

Table 2.36 Comparison of I/O Port Functions

Item	Port Symbol	RX21A	RX23E-A
Input pull-up function	PORT0	P03, P05, P07	—
	PORT1	P12 to P17	P14 to P17
	PORT2	P20 to P27	P26, P27
	PORT3	P30 to P34, P36, P37	P30, P31, P36, P37
	PORT4	P40 to P43	—
	PORT5	P50 to P55	—
	PORTA	PA0 to PA7	—
	PORTB	PB0 to PB7	PB0, PB1
	PORTC	PC0 to PC7	PC4 to PC7
	PORTE	PE6, PE7	—
	PORTH	PH0 to PH3	PH0 to PH3
	PORTJ	PJ1, PJ3	—
Open-drain output function	PORT1	P12 to P17	P14 to P17
	PORT2	P20 to P27	P26, P27
	PORT3	P30 to P34, P36, P37	P30, P31, P36, P37
	PORTA	PA0 to PA7	—
	PORTB	PB0 to PB7	PB0, PB1
	PORTC	PC0 to PC7	PC4 to PC7
	PORTE	PE6, PE7	—
	PORTH	—	PH0 to PH3
Drive capacity switching function	PORT0	P03, P05, P07	—
	PORT1	P12 to P17	P14 to P17
	PORT2	P20 to P27	P26, P27
	PORT3	P30 to P34, P36, P37	P30, P31, P36, P37
	PORT4	P40 to P43	—
	PORT5	P50 to P55	—
	PORTA	PA0 to PA7	—
	PORTB	PB0 to PB7	PB0, PB1
	PORTC	PC0 to PC7	PC4 to PC7
	PORTE	PE6, PE7	—

Item	Port Symbol	RX21A	RX23E-A
Drive capacity switching function	PORTH	PH0 to PH3	PH0 to PH3
	PORTJ	PJ1, PJ3	—
5 V tolerant	PORT1	P12, P13, P16, P17	P16, P17
	PORT2	P20, P21	—

Table 2.37 Comparison of I/O Port Registers

Register	Bit	RX21A	RX23E-A
PDR	B0 to B7	Pm0 to Pm7 I/O select bits (m = 0 to 5, A to C, E, H, J)	Pm0 to Pm7 I/O select bits (m = 1 to 3, B, C, H)
PODR	B0 to B7	Pm0 to Pm7 output data store bits (m = 0 to 5, A to C, E, H, J)	Pm0 to Pm7 output data store bits (m = 1 to 3, B, C, H)
PIDR	B0 to B7	Pm0 to Pm7 bits (m = 0 to 5, A to C, E, H, J)	Pm0 to Pm7 bits (m = 1 to 3, B, C, H)
PMR	B0 to B7	Pm0 pin mode control bits (m = 0 to 5, A to C, E, H, J)	Pm0 to Pm7 pin mode control bits (m = 1 to 3, B, C, H)
ODR0	B0	Pm0 output type select bit (m = 1 to 3, A to C)	Pm0 output type select bit (m = 3, B, H)
	B2, B3	Pm1 output type select bits (m = 1 to 3, A to C) • P21, P31, PA1, PB1, PC1 b2 0: CMOS output 1: N-channel open-drain b3 This bit is read as 0. The write value should be 0.	Pm0 output type select bits (m = 3, B, H) • P31, PH1 b2 0: CMOS output 1: N-channel open-drain b3 This bit is read as 0. The write value should be 0. • PB1 b3 b2 0 0: CMOS output 0 1: N-channel open-drain 1 0: P-channel open-drain 1 1: Setting prohibited.
	B4	Pm2 output type select bit (m = 1 to 3, A to C)	Pm2 output type select bits (m = 3, B, H)
	B6	Pm3 output type select bit (m = 1 to 3, A to C)	Pm3 output type select bit (m = 3, B, H)
ODR1	B0	Pm4 output type select bit (m = 1 to 3, A to C, E)	Pm4 output type select bit (m = 1 to 3, C)
	B2	Pm5 output type select bit (m = 1 to 3, A to C, E)	Pm5 output type select bit (m = 1 to 3, C)
	B4	Pm6 output type select bit (m = 1 to 3, A to C, E)	Pm6 output type select bit (m = 1 to 3, C)
	B6	Pm7 output type select bit (m = 1 to 3, A to C, E)	Pm7 output type select bit (m = 1 to 3, C)
PCR	B0 to B7	Pm0 to Pm7 input pull-up resistor control bits (m = 0 to 5, A to C, E, H, J)	Pm0 to Pm7 input pull-up resistor control bits (m = 1 to 3, B, C, H)
DSCR	B0 to B7	Pm0 to Pm7 drive capacity control bits (m = 1 to 3, 5, A to C, E, H, J)	Pm0 to Pm7 drive capacity control bits (m = 1 to 3, B, C, H)
PSRA	—	—	Port switching register A

2.17 Multi-Function Pin Controller

Table 2.38 is a comparison of the assignments of multiplexed pins, and Table 2.39 to Table 2.50 are comparisons of multi-function pin controller registers.

In the following comparison of the assignments of multiplexed pins, **light blue text** designates pins that exist on the RX23E-A Group only and **orange text** pins that exist on the RX21A Group only. A circle (○) indicates that a function is assigned, a cross (×) that the pin does not exist or that no function is assigned, and grayed out items mean that the function is not implemented.

Table 2.38 Comparison of Multiplexed Pin Assignments

Module/Function	Pin Function	Port Allocation	RX21A	RX23E-A	
			64-Pin	48-Pin	40-Pin
Interrupt	NMI (input)	P35	○	○	○
	IRQ0-DS (input)	P30	○		
	IRQ0 (input)	PH1	○	○	○
		P30	×	○	○
	IRQ1-DS (input)	P31	○		
	IRQ1 (input)	PH2	○	○	×
		P31	×	○	○
	IRQ2-DS (input)	P32	○		
	IRQ2 (input)	P26	×	○	○
	IRQ3 (input)	P27	×	○	○
	IRQ4-DS (input)	PB1	○		
	IRQ4 (input)	P14	○	○	○
		PB0	×	○	○
	IRQ5-DS (input)	PA4	○		
	IRQ5 (input)	P15	○	○	○
	IRQ6-DS (input)	PA3	○		
	IRQ6 (input)	P16	○	○	○
	IRQ7 (input)	P17	○	○	○
Multi-function timer unit 2	MTIOC0A (input/output)	PB3	○	×	×
		P30	×	○	○
	MTIOC0B (input/output)	P15	○	○	○
		PA1	○	×	×
	MTIOC0C (input/output)	P32	○	×	×
		PB1	○	×	×
		PB0	×	○	○
	MTIOC0D (input/output)	PA3	○	×	×
		PH0	×	○	○
	MTIOC1A (input/output)	P31	×	○	○
	MTIOC1B (input/output)	PB5	○	×	×
		PB1	×	○	○
	MTIOC2A (input/output)	P26	○	○	○
		PB5	○	×	×
		PB1	×	○	○
	MTIOC2B (input/output)	P27	○	○	○
	MTIOC3A (input/output)	P14	○	○	○
		P17	○	○	○
		PC7	○	○	×

Module/Function	Pin Function	Port Allocation	RX21A	RX23E-A	
			64-Pin	48-Pin	40-Pin
Multi-function timer unit 2	MTIOC3B (input/output)	P17	○	○	○
		PB7	○	×	×
		PC5	○	○	○
	MTIOC3C (input/output)	P16	○	○	○
		PC6	○	○	×
	MTIOC3D (input/output)	P16	○	○	○
		PB6	○	×	×
		PC4	○	○	○
	MTIOC4A (input/output)	PA0	○	×	×
		PB3	○	×	×
		P27	×	○	○
	MTIOC4B (input/output)	P30	○	○	○
		P54	○	×	×
		PC2	○	×	×
	MTIOC4C (input/output)	PB1	○	×	×
		P26	×	○	○
	MTIOC4D (input/output)	P31	○	○	○
		P55	○	×	×
		PC3	○	×	×
	MTIC5U (input)	PA4	○	×	×
		PH1	×	○	×
	MTIC5V (input)	PA6	○	×	×
		PH2	×	○	×
	MTIC5W (input)	PB0	○	×	×
		PH3	×	○	×
	MTCLKA (input)	P14	○	○	○
		PA4	○	×	×
		PC6	○	○	×
		PH2	×	○	×
	MTCLKB (input)	P15	○	○	○
		PA6	○	×	×
		PC7	○	○	×
		PH3	×	○	×
	MTCLKC (input)	PA1	○	×	×
		PC4	○	○	○
		PH0	×	○	○
	MTCLKD (input)	PA3	○	×	×
		PC5	○	○	○
		PH1	×	○	○
Port output enable 2	POE0# (input)	PC4	○	○	○
	POE1# (input)	PB5	○	×	×
		PB1	×	○	○
	POE2# (input)	PA6	○	×	×
		PH1	×	○	○
		PH3	×	○	×
	POE3# (input)	PB3	○	×	×
		PB0	×	○	○
	POE8# (input)	P17	○	○	○
		P30	○	○	○

Module/Function	Pin Function	Port Allocation	RX21A 64-Pin	RX23E-A 48-Pin	RX23E-A 40-Pin
8-bit timer	TMO0 (output)	PB3	○	×	×
		PH1	○	○	○
		P26	×	○	○
	TMCI0 (input)	PB1	○	×	×
		PH3	○	○	×
		PB0	×	○	○
	TMRI0 (input)	PA4	○	×	×
		PH2	○	○	×
		PH0	×	○	○
	TMO1 (output)	P17	○	○	○
		P26	○	×	×
	TMCI1 (input)	P54	○	×	×
		PC4	○	○	○
	TMRI1 (input)	PB5	○	×	×
		PB1	×	○	○
	TMO2 (output)	P16	○	○	○
		PC7	○	○	×
	TMCI2 (input)	P15	○	○	○
		P31	○	×	×
		PC6	○	○	×
	TMRI2 (input)	P14	○	○	○
		PC5	○	○	○
	TMO3 (output)	P32	○	×	×
		P55	○	×	×
		P31	×	○	○
	TMCI3 (input)	P27	○	×	×
		PA6	○	×	×
		P30	×	○	○
	TMRI3 (input)	P30	○	×	×
		P27	×	○	○
Serial communications interface	RXD1 (input) / SMISO1 (input/output) / SSCL1 (input/output)	P15	○	○	○
		P30	○	○	○
	TXD1 (output) / SMOSI1 (input/output) / SSDA1 (input/output)	P16	○	○	○
		P26	○	○	○
	SCK1 (input/output)	P17	○	○	○
		P27	○	○	○
	CTS1# (input) / RTS1# (output) / SS1# (input)	P14	○	○	○
		P31	○	○	○
	RXD5 (input) / SMISO5 (input/output) / SSCL5 (input/output) / IRRXD5 (input)	PA3	○		
		PC2	○		

Module/Function	Pin Function	Port Allocation	RX21A	RX23E-A	
			64-Pin	48-Pin	40-Pin
Serial communications interface	RXD5 (input) / SMISO5 (input/output) / SSCL5 (input/output)	PH0		○	○
	TXD5 (output) / SMOSI5 (input/output) / SSDA5 (input/output) / IRTXD5 (output)	PA4	○		
		PC3	○		
	TXD5 (output) / SMOSI5 (input/output) / SSDA5 (input/output)	PH1		○	○
	SCK5 (input/output)	PA1	○	×	×
		PC4	○	×	×
		PH2	×	○	×
		PC5	×	○	○
	CTS5# (input) / RTS5# (output) / SS5# (input)	PA6	○	×	×
		PC4	×	○	○
	RXD6 (input) / SMISO6 (input/output) / SSCL6 (input/output)	PB0	○	×	×
		PC6	×	○	×
	TXD6 (output) / SMOSI6 (input/output) / SSDA6 (input/output)	P32	○	×	×
		PB1	○	×	×
		PC7	×	○	×
	SCK6 (input/output)	PB3	○	×	×
		PC5	×	○	×
	CTS6# (input) / RTS6# (output) / SS6# (input)	PH3	×	○	×
	RXD8 (input) / SMISO8 (input/output) / SSCL8 (input/output)	PC6	○		
	TXD8 (output) / SMOSI8 (input/output) / SSDA8 (input/output)	PC7	○		
	SCK8 (input/output)	PC5	○		
	CTS8# (input) / RTS8# (output) / SS8# (input)	PC4	○		
	RXD9 (input) / SMISO9 (input/output) / SSCL9 (input/output)	PB6	○		

Module/Function	Pin Function	Port Allocation	RX21A	RX23E-A	
			64-Pin	48-Pin	40-Pin
Serial communications interface	TXD9 (output) / SMOSI9 (input/output) / SSDA9 (input/output)	PB7	○		
	SCK9 (input/output)	PB5	○		
	RXD12 (input) / SMISO12 (input/output) / SSCL12 (input/output) / RXDX12 (input)	PB0		○	○
	TXD12 (output) / SMOSI12 (input/output) / SSDA12 (input/output) / TXDX12 (output) / SIOX12 (input/output)	PB1		○	○
	SCK12 (input/output)	PC5		○	○
	CTS12# (input) / RTS12# (output) / SS12# (input)	PC4		○	○
I²C bus interface	SCL0-DS (input/output) / SCL (input/output)	P16	○		
	SDA0-DS (input/output) / SDA (input/output)	P17	○		
Serial peripheral interface	RSPCKA (input/output)	PB0	○	×	×
		PC5	○	○	○
		PH3	×	○	×
	MOSIA (input/output)	P16	○	○	○
		PA6	○	×	×
		PC6	○	○	×
		PH2	×	○	×
	MISOA (input/output)	P17	○	○	○
		PC7	○	○	×
	SSLA0 (input/output)	PA4	○	×	×
		PC4	○	○	○
		PH1	×	○	○
	SSLA1 (output)	PA0	○	×	×
		P15	×	○	○
	SSLA2 (output)	PA1	○	×	×
		PH0	×	○	○
	SSLA3 (output)	PC2	○	×	×
		P14	×	○	○
	RSPCKB (input/output)	P27	○		
	MOSIB (input/output)	P26	○		
	MISOB (input/output)	P30	○		
	SSLB0 (input/output)	P31	○		

Module/Function	Pin Function	Port Allocation	RX21A	RX23E-A	
			64-Pin	48-Pin	40-Pin
Realtime clock	RTCOUT (output)	P16	○		
		P32	○		
	RTCIC0 (input)	P30	○		
	RTCIC1 (input)	P31	○		
	RTCIC2 (input)	P32	○		
10-bit A/D converter/ 12-bit A/D converter	AN0 (input)	P40	○		
	AN1 (input)	P41	○		
	AN4 (input)	P03	○		
	AN5 (input)	P05	○		
	ADTRG0# (input)	P16	○	○	○
Clock frequency accuracy measurement circuit	CACREF (input)	PA0	○	×	×
		PC7	○	○	×
		PH0	○	○	○
Comparator A	CMPA1 (input)	PA0	○		
	CVREFA (input)	PA1	○		
Comparator B	CMPB0 (input)	PB0	○		
	CVREFB0 (input)	PA6	○		
	CMPB1 (input)	PA3	○		
	CVREFB1 (input)	PA4	○		
Clock generation circuit	CLKOUT (output)	PH1		○	○
RSCAN	CTXD0 (output)	P14		○	○
	CRXD0 (input)	P15		○	○

Table 2.39 Comparison of P0n Pin Function Control Register (P0nPFS)

Register	Bit	RX21A	RX23E-A
P0nPFS	—	P0n pin function control register (n = 3, 5, 7)	—

Table 2.40 Comparison of P1n Pin Function Control Register (P1nPFS)

Register	Bit	RX21A (n = 2 to 7)	RX23E-A (n = 4 to 7)
P12PFS	—	P12 pin function control register	—
P13PFS	—	P13 pin function control register	—
P14PFS	PSEL[3:0] (RX21A) PSEL[4:0] (RX23E-A)	Pin function select bits (b3 to b0) b3 b0 0000b: Hi-Z 0001b: MTIOC3A 0010b: MTCLKA 0101b: TMRI2 1011b: CTS1#/RTS1#/SS1#	Pin function select bits (b4 to b0) b4 b0 00000b: Hi-Z 00001b: MTIOC3A 00010b: MTCLKA 00101b: TMRI2 01011b: CTS1#/RTS1#/SS1# 01101b: SSLA3 10000b: CTXD0
P15PFS	PSEL[3:0] (RX21A) PSEL[4:0] (RX23E-A)	Pin function select bits (b3 to b0) b3 b0 0000b: Hi-Z 0001b: MTIOC0B 0010b: MTCLKB 0101b: TMCI2 1010b: RXD1/SMISO1/SSCL1	Pin function select bits (b4 to b0) b4 b0 00000b: Hi-Z 00001b: MTIOC0B 00010b: MTCLKB 00101b: TMCI2 01010b: RXD1/SMISO1/SSCL1 01101b: SSLA1 10000b: CRXD0
P16PFS	PSEL[3:0] (RX21A) PSEL[4:0] (RX23E-A)	Pin function select bits (b3 to b0) b3 b0 0000b: Hi-Z 0001b: MTIOC3C 0010b: MTIOC3D 0101b: TMO2 0111b: RTCOUT 1001b: ADTRG0# 1010b: TXD1/SMOSI1/SSDA1 1101b: MOSIA 1111b: SCL0-DS	Pin function select bits (b4 to b0) b4 b0 00000b: Hi-Z 00001b: MTIOC3C 00010b: MTIOC3D 00101b: TMO2 01001b: ADTRG0# 01010b: TXD1/SMOSI1/SSDA1 01101b: MOSIA 01111b: SCL
P17PFS	PSEL[3:0] (RX21A) PSEL[4:0] (RX23E-A)	Pin function select bits (b3 to b0) b3 b0 0000b: Hi-Z 0001b: MTIOC3A 0010b: MTIOC3B 0101b: TMO1 0111b: POE8# 1010b: SCK1 1101b: MISOA 1111b: SDA0-DS	Pin function select bits (b4 to b0) b4 b0 00000b: Hi-Z 00001b: MTIOC3A 00010b: MTIOC3B 00101b: TMO1 00111b: POE8# 01010b: SCK1 01101b: MISOA 01111b: SDA

Register	Bit	RX21A (n = 2 to 7)	RX23E-A (n = 4 to 7)
P1nPFS	ISEL	Interrupt input function select bit 0: Not used as IRQn input pin 1: Used as IRQn input pin P12: IRQ2 (100/80-pin) P13: IRQ3 (100/80-pin) P14: IRQ4 (100/80/64-pin) P15: IRQ5 (100/80/64-pin) P16: IRQ6 (100/80/64-pin) P17: IRQ7 (100/80/64-pin)	Interrupt input function select bit 0: Not used as IRQn input pin 1: Used as IRQn input pin P14: IRQ4 P15: IRQ5 P16: IRQ6 P17: IRQ7

Table 2.41 Comparison of P2n Pin Function Control Register (P2nPFS)

Register	Bit	RX21A (n = 0 to 7)	RX23E-A (n = 6, 7)
P20PFS	—	P20 pin function control register	—
P21PFS	—	P21 pin function control register	—
P22PFS	—	P22 pin function control register	—
P23PFS	—	P23 pin function control register	—
P24PFS	—	P24 pin function control register	—
P25PFS	—	P25 pin function control register	—
P26PFS	PSEL[3:0] (RX21A) PSEL[4:0] (RX23E-A)	Pin function select bits (b3 to b0) b3 b0 0000b: Hi-Z 0001b: MTIOC2A 0101b: TMO1 1010b: TXD1/SMOSI1/SSDA1 1101b: MOSIB	Pin function select bits (b4 to b0) b4 b0 00000b: Hi-Z 00001b: MTIOC2A 00010b: MTIOC4C 00101b: TMO0 01010b: TXD1/SMOSI1/SSDA1
P27PFS	PSEL[3:0] (RX21A) PSEL[4:0] (RX23E-A)	Pin function select bits (b3 to b0) b3 b0 0000b: Hi-Z 0001b: MTIOC2B 0101b: TMCI3 1010b: SCK1 1101b: RSPCKB	Pin function select bits (b4 to b0) b4 b0 00000b: Hi-Z 00001b: MTIOC2B 00010b: MTIOC4A 00101b: TMRI3 01010b: SCK1
P2nPFS	ISEL	—	Interrupt input function select bit

Table 2.42 Comparison of P3n Pin Function Control Register (P3nPFS)

Register	Bit	RX21A (n = 0 to 4)	RX23E-A (n = 0, 1)
P30PFS	PSEL[3:0] (RX21A) PSEL[4:0] (RX23E-A)	Pin function select bits (b3 to b0) b3 b0 0000b: Hi-Z 0001b: MTIOC4B 0101b: TMRI3 0111b: POE8# 1010b: RXD1/SMISO1/SSCL1 1101b: MISOB	Pin function select bits (b4 to b0) b4 b0 00000b: Hi-Z 00001b: MTIOC4B 00010b: MTIOC0A 00101b: TMCI3 00111b: POE8# 01010b: RXD1/SMISO1/SSCL1
P31PFS	PSEL[3:0] (RX21A) PSEL[4:0] (RX23E-A)	Pin function select bits (b3 to b0) b3 b0 0000b: Hi-Z 0001b: MTIOC4D 0101b: TMCI2 1011b: CTS1#/RTS1#/SS1# 1101b: SSLB0	Pin function select bits (b4 to b0) b4 b0 00000b: Hi-Z 00001b: MTIOC4D 00010b: MTIOC1A 00101b: TMO3 01011b: CTS1#/RTS1#/SS1#
P32PFS	—	P32 pin function control register	—
P33PFS	—	P33 pin function control register	—
P34PFS	—	P34 pin function control register	—
P3nPFS	ISEL	Interrupt input function select bit 0: Not used as IRQn input pin 1: Used as IRQn input pin P30: IRQ0-DS (100/80/64-pin) P31: IRQ1-DS (100/80/64-pin) P32: IRQ2-DS (100/80/64-pin) P33: IRQ3-DS (100-pin P34: IRQ4 (100/80-pin)	Interrupt input function select bit 0: Not used as IRQn input pin 1: Used as IRQn input pin P30: IRQ0 P31: IRQ1

Table 2.43 Comparison of P4n Pin Function Control Register (P4nPFS)

Register	Bit	RX21A	RX23E-A
P4nPFS	—	P4n pin function control register (n = 0 to 3)	—

Table 2.44 Comparison of P5n Pin Function Control Register (P5nPFS)

Register	Bit	RX21A	RX23E-A
P5nPFS	—	P5n pin function control register (n = 0 to 2, 4, 5)	—

Table 2.45 Comparison of PAn Pin Function Control Register (PAnPFS)

Register	Bit	RX21A	RX23E-A
PAnPFS	—	PAn pin function control register (n = 0 to 7)	—

Table 2.46 Comparison of PBn Pin Function Control Register (PBnPFS)

Register	Bit	RX21A (n = 0 to 7)	RX23E-A (n = 0, 1)
PB0PFS	PSEL[3:0] (RX21A) PSEL[4:0] (RX23E-A)	Pin function select bits (b3 to b0) b3 b0 0000b: Hi-Z 0001b: MTIC5W 1011b: RXD6/SMISO6/SSCL6 1101b: RSPCKA	Pin function select bits (b4 to b0) b4 b0 00000b: Hi-Z 00001b: MTIOC0C 00101b: TMCI0 00111b: POE3# 01100b: RXD12/RXDX12/ SMISO12/SSCL12
PB1PFS	PSEL[3:0] (RX21A) PSEL[4:0] (RX23E-A)	Pin function select bits (b3 to b0) b3 b0 0000b: Hi-Z 0001b: MTIOC0C 0010b: MTIOC4C 0101b: TMCI0 1011b: TXD6/SMOSI6/SSDA6	Pin function select bits (b4 to b0) b4 b0 00000b: Hi-Z 00001b: MTIOC2A 00010b: MTIOC1B 00101b: TMRI1 00111b: POE1# 01100b: TXD12/TXDX12/SIOX12/ SMOSI12/SSDA12
PB2PFS	—	PB2 pin function control register	—
PB3PFS	—	PB3 pin function control register	—
PB4PFS	—	PB4 pin function control register	—
PB5PFS	—	PB5 pin function control register	—
PB6PFS	—	PB6 pin function control register	—
PB7PFS	—	PB7 pin function control register	—
PBnPFS	ISEL	Interrupt input function select bit 0: Not used as IRQn input pin 1: Used as IRQn input pin PB1: IRQ4-DS (100/80/64-pin)	Interrupt input function select bit 0: Not used as IRQn input pin 1: Used as IRQn input pin PB0: IRQ4
	ASEL	Analog function select bit	—

Table 2.47 Comparison of PCn Pin Function Control Register (PCnPFS)

Register	Bit	RX21A (n = 0 to 7)	RX23E-A (n = 4 to 7)
PC0PFS	—	PC0 pin function control register	—
PC1PFS	—	PC1 pin function control register	—
PC2PFS	—	PC2 pin function control register	—
PC3PFS	—	PC3 pin function control register	—
PC4PFS	PSEL[3:0] (RX21A) PSEL[4:0] (RX23E-A)	Pin function select bits (b3 to b0) b3 b0 0000b: Hi-Z 0001b: MTIOC3D 0010b: MTCLKC 0101b: TMCI1 0111b: POE0# 1010b: SCK5 1011b: CTS8#/RTS8#/SS8# 1101b: SSLA0	Pin function select bits (b4 to b0) b4 b0 00000b: Hi-Z 00001b: MTIOC3D 00010b: MTCLKC 00101b: TMCI1 00111b: POE0# 01011b: CTS5#/RTS5#/SS5# 01100b: CTS12#/RTS12#/SS12# 01101b: SSLA0
PC5PFS	PSEL[3:0] (RX21A) PSEL[4:0] (RX23E-A)	Pin function select bits (b3 to b0) b3 b0 0000b: Hi-Z 0001b: MTIOC3B 0010b: MTCLKD 0101b: TMRI2 1010b: SCK8 1101b: RSPCKA	Pin function select bits (b4 to b0) b4 b0 00000b: Hi-Z 00001b: MTIOC3B 00010b: MTCLKD 00101b: TMRI2 01010b: SCK5 01011b: SCK6 01100b: SCK12 01101b: RSPCKA
PC6PFS	PSEL[3:0] (RX21A) PSEL[4:0] (RX23E-A)	Pin function select bits (b3 to b0) b3 b0 0000b: Hi-Z 0001b: MTIOC3C 0010b: MTCLKA 0101b: TMCI2 1010b: RXD8/SMISO8/SSCL8 1101b: MOSIA	Pin function select bits (b4 to b0) b4 b0 00000b: Hi-Z 00001b: MTIOC3C 00010b: MTCLKA 00101b: TMCI2 01011b: RXD6/SMISO6/SSCL6 01101b: MOSIA
PC7PFS	P)SEL[3:0] (RX21A) PSEL[4:0] (RX23E-A)	Pin function select bits (b3 to b0) b3 b0 0000b: Hi-Z 0001b: MTIOC3A 0010b: MTCLKB 0101b: TMO2 0111b: CACREF 1010b: TXD8/SMOSI8/SSDA8 1101b: MISOA	Pin function select bits (b4 to b0) b4 b0 00000b: Hi-Z 00001b: MTIOC3A 00010b: MTCLKB 00101b: TMO2 00111b: CACREF 01011b: TXD6/SMOSI6/SSDA6 01101b: MISOA

Table 2.48 Comparison of PEn Pin Function Control Register (PEnPFS)

Register	Bit	RX21A	RX23E-A
PEnPFS	—	PEn pin function control register (n = 6, 7)	—

Table 2.49 Comparison of PHn Pin Function Control Register (PHnPFS)

Register	Bit	RX21A (n = 0 to 3)	RX23E-A (n = 0 to 3)
PH0PFS	PSEL[3:0] (RX21A) PSEL[4:0] (RX23E-A)	Pin function select bits (b3 to b0) b3 b0 0000b: Hi-Z 0111b: CACREF	Pin function select bits (b4 to b0) b4 b0 00000b: Hi-Z 00001b: MTIOC0D 00010b: MTCLKC 00101b: TMRI0 00111b: CACREF 01010b: RXD5/SMISO5/SSCL5 01101b: SSLA2
PH1PFS	PSEL[3:0] (RX21A) PSEL[4:0] (RX23E-A)	Pin function select bits (b3 to b0) b3 b0 0000b: Hi-Z 0101b: TMO0	Pin function select bits (b4 to b0) b4 b0 00000b: Hi-Z 00001b: MTIC5U 00010b: MTCLKD 00101b: TMO0 00111b: POE2# 01001b: CLKOUT 01010b: TXD5/SMOSI5/SSDA5 01101b: SSLA0
PH2PFS	PSEL[3:0] (RX21A) PSEL[4:0] (RX23E-A)	Pin function select bits (b3 to b0) b3 b0 0000b: Hi-Z 0101b: TMRI0	Pin function select bits (b4 to b0) b4 b0 00000b: Hi-Z 00001b: MTIC5V 00010b: MTCLKA 00101b: TMRI0 01010b: SCK5 01101b: MOSIA
PH3PFS	PSEL[3:0] (RX21A) PSEL[4:0] (RX23E-A)	Pin function select bits (b3 to b0) b3 b0 0000b: Hi-Z 0101b: TMCI0	Pin function select bits (b4 to b0) b4 b0 00000b: Hi-Z 00001b: MTIC5W 00010b: MTCLKB 00101b: TMCI0 00111b: POE2# 01011b: CTS6#/RTS6#/SS6# 01101b: RSPCKA

Table 2.50 Comparison of PJn Pin Function Control Register (PJnPFS)

Register	Bit	RX21A	RX23E-A
PJPFS	—	PJn pin function control register (n =1, 3)	—

2.18 Compare Match Timer

Table 2.51 is a comparative overview of compare match timer, and Table 2.52 is a comparison of compare match timer registers.

Table 2.51 Comparative Overview of Compare Match Timer

Item	RX21A (CMT)	RX23E-A (CMT)
Number of channels	4 channels	2 channels
Count clocks	Four frequency-divided clocks: One clock among PCLK/8, PCLK/32, PCLK/128, and PCLK/512 can be selected independently for each channel.	Four frequency-divided clocks: One clock among PCLK/8, PCLK/32, PCLK/128, and PCLK/512 can be selected for each channel.
Interrupts	A compare match interrupt can be requested independently for each channel.	A compare match interrupt can be requested for each channel.
Event link function (output)	An event signal is output at CMT1 compare match.	An event signal is output at CMT1 compare match.
Event link function (input)	• Ability to link to a specified module • Ability to initiate (1) counter start, (2) event counter, or (3) count restart operation by a specified event	• Ability to link to a specified module • Support for CMT1 count start, event counter, or count restart operation
Low power consumption function	Ability to specify module stop state for each unit	Ability to specify to module stop state

Table 2.52 Comparison of Compare Match Timer Registers

Register	Bit	RX21A (CMT)	RX23E-A (CMT)
CMSTR1	—	Compare match timer start register 1	—

2.19 Independent Watchdog Timer

Table 2.53 is a comparative overview of independent watchdog timer, and Table 2.54 is a comparison of independent watchdog timer registers.

Table 2.53 Comparative Overview of Independent Watchdog Timer

Item	RX21A (IWDTa)	RX23E-A (IWDTa)
Count source	IWDT-dedicated clock (IWDTCLK)	IWDT-dedicated clock (IWDTCLK)
Clock division ratio	Division by 1, 16, 32, 64, 128, or 256	Division by 1, 16, 32, 64, 128, or 256
Counter operation	Counting down using a 14-bit down-counter	Counting down using a 14-bit down-counter
Conditions for starting the counter	• Counting starts automatically after a reset (auto-start mode). • Counting is started by a refresh (writing 00h and then FFh to the IWDTRR register) (register start mode).	• Auto-start mode: Counting starts automatically after a reset is canceled. • Register start mode: Counting is started by refresh operation (writing 00h and then FFh to the IWDTRR register).
Conditions for stopping the counter	• A reset occurs. (The down-counter and registers return to their initial values.) • In a low power consumption state (depending on register setting) • A counter underflows or a refresh error is generated (register start mode: by a refresh).	• A reset occurs. (The down-counter and registers return to their initial values.) • In a low power consumption state (depending on register setting) • A counter underflows or a refresh error occurs (register start mode only)
Window function	Window start and end positions can be specified (for periods when refreshed are permitted or prohibited).	Window start and end positions can be specified (for periods when refreshed are permitted or prohibited).
Reset output sources	• Down-counter underflow • Refresh outside the refresh-permitted period (refresh error)	• Down-counter underflow • Refresh outside the refresh-permitted period (refresh error)
Interrupt sources	Interrupt request output sources • When a non-maskable interrupt (WUNI) is generated by an underflow of the down-counter • When a refresh occurs outside the refresh-permitted period (refresh error)	Non-maskable interrupt sources • Down-counter underflow • When a refresh occurs outside the refresh-permitted period (refresh error)
Reading the counter value	The down-counter value can be read from the IWDTSR register.	The down-counter value can be read from the IWDTSR register.
Event link function (output)	• Down-counter underflow • Refreshing outside the refresh-permitted period (refresh error)	• Down-counter underflow event output • Refresh error event output
Output signals (internal signals)	• Reset output • Interrupt request output • Sleep mode count stop control output	• Reset output • Interrupt request output • Sleep mode count stop control output

Item	RX21A (IWDTa)	RX23E-A (IWDTa)
Auto-start mode (controlled by option function select register 0 (OFS0))	• Selection of clock frequency division ratio after a reset (OFS0.IWDTCKS[3:0] bits) • Selection of time-out period of watchdog timer (OFS0.IWDTTOPS[1:0] bits) • Selection of window start position in the watchdog timer (OFS0.IWDTRPSS[1:0] bits) • Selection of window end position in the watchdog timer (OFS0.IWDTRPES[1:0] bits) • Selection of reset output or interrupt request output (OFS0.IWDTRSTIRQS bit) • Selection of down-count stop function at transition to sleep mode, software standby mode, deep software standby mode, or all-module clock stop mode (OFS0.IWDTSLCSTP bit)	• Selection of clock frequency division ratio after a reset (OFS0.IWDTCKS[3:0] bits) • Selection of timeout period of independent watchdog timer (OFS0.IWDTTOPS[1:0] bits) • Selection of window start position in the independent watchdog timer (OFS0.IWDTRPSS[1:0] bits) • Selection of window end position in the independent watchdog timer (OFS0.IWDTRPES[1:0] bits) • Selection of reset output or interrupt request output (OFS0.IWDTRSTIRQS bit) • Selection of down-count stop function at transition to sleep mode, software standby mode, or deep sleep mode (OFS0.IWDTSLCSTP bit)
Register start mode (controlled by IWDT registers)	• Selection of clock frequency division ratio after a refresh (IWDTCR.CKS[3:0] bits) • Selection of time-out period of watchdog timer (IWDTCR.TOPS[1:0] bits) • Selection of window start position in the watchdog timer (IWDTCR.RPSS[1:0] bits) • Selection of window end position in the watchdog timer (IWDTCR.RPES[1:0] bits) • Selection of reset output or interrupt request output (IWDTRCR.RSTIRQS bit) • Selection of down-count stop function at transition to sleep mode, software standby mode, deep software standby mode, or all-module clock stop mode (IWDTCSTPR.SLCSTP bit)	• Selection of clock frequency division ratio after a refresh (IWDTCR.CKS[3:0] bits) • Selection of timeout period of independent watchdog timer (IWDTCR.TOPS[1:0] bits) • Selection of window start position in the independent watchdog timer (IWDTCR.RPSS[1:0] bits) • Selection of window end position in the independent watchdog timer (IWDTCR.RPES[1:0] bits) • Selection of reset output or interrupt request output (IWDTRCR.RSTIRQS bit) • Selection of down-count stop function at transition to sleep mode, software standby mode, or deep sleep mode (IWDTCSTPR.SLCSTP bit)

Table 2.54 Comparison of Independent Watchdog Timer Registers

Register	Bit	RX21A (IWDTa)	RX23E-A (IWDTa)
IWDTRCR	TOPS[1:0]	Time-out period selection bits b1 b0 0 0: 1,024 cycles (03FFh) 0 1: 4,096 cycles (0FFFh) 1 0: 8,192 cycles (1FFFh) 1 1: 16,384 cycles (3FFFh)	Time-out period selection bits b1 b0 0 0: 128 cycles (007Fh) 0 1: 512 cycles (01FFh) 1 0: 1,024 cycles (03FFh) 1 1: 2,048 cycles (07FFh)

2.20 Serial Communications Interface

Table 2.55 is a comparative overview of the serial communications interfaces, and Table 2.56 is a comparison of serial communications interface channel specifications, and Table 2.57 is a comparison of serial communications interface registers.

Table 2.55 Comparative Overview of Serial Communications Interfaces

Item		RX21A (SCIc)	RX23E-A (SCIg, SCIh)
Number of channels		• SCIc: 5 channels	• SCIg: 3 channels • SCIh: 1 channel
Serial communications modes		• Asynchronous • Clock synchronous • Smart card interface • Simple I^2C bus • Simple SPI bus	• Asynchronous • Clock synchronous • Smart card interface • Simple I^2C bus • Simple SPI bus
Transfer speed		Bit rate specifiable by on-chip baud rate generator.	Bit rate specifiable by on-chip baud rate generator.
Full-duplex communication		• Transmitter: Continuous transmission possible using double-buffer structure. • Receiver: Continuous reception possible using double-buffer structure.	• Transmitter: Continuous transmission possible using double-buffer structure. • Receiver: Continuous reception possible using double-buffer structure.
Data transfer		Selectable as LSB first or MSB first transfer.	Selectable as LSB first or MSB first transfer.
Interrupt sources		Transmit end, transmit data empty, receive data full, and receive error, completion of generation of a start condition, restart condition, or stop condition (for simple I^2C mode)	Transmit end, transmit data empty, receive data full, and receive error, completion of generation of a start condition, restart condition, or stop condition (for simple I^2C mode)
Low power consumption function		Module stop state can be set for each channel.	Module stop state can be set for each channel.
Asynchronous mode	Data length	7 or 8 bits	7, 8, or 9 bits
	Transmission stop bits	1 or 2 bits	1 or 2 bits
	Parity	Even parity, odd parity, or no parity	Even parity, odd parity, or no parity
	Receive error detection function	Parity, overrun, and framing errors	Parity, overrun, and framing errors
	Hardware flow control	CTSn# and RTSn# pins can be used in controlling transmission/reception.	CTSn# and RTSn# pins can be used in controlling transmission/reception.
	Start-bit detection	Low level	Low level or falling edge is selectable.
	Break detection	When a framing error occurs, a break can be detected by reading the RXDn pin level directly.	When a framing error occurs, a break can be detected by reading the RXDn pin level directly.

Item		RX21A (SCIc)	RX23E-A (SCIg, SCIh)
Asynchronous mode	Clock source	• An internal or external clock can be selected. • Transfer rate clock input from the TMR can be used (SCI5 and SCI6).	• An internal or external clock can be selected. • Transfer rate clock input from the TMR can be used (SCI5 and SCI6).
	Double-speed mode	—	Baud rate generator double-speed mode is selectable.
	Multi-processor communications function	Serial communication among multiple processors	Serial communication among multiple processors
	Noise cancellation	The signal paths from input on the RXDn pins incorporate digital noise filters.	The signal paths from input on the RXDn pins incorporate digital noise filters.
Clock synchronous mode	Data length	8 bits	8 bits
	Receive error detection	Overrun error	Overrun error
	Hardware flow control	CTSn# and RTSn# pins can be used in controlling transmission/ reception.	CTSn# and RTSn# pins can be used in controlling transmission/ reception.
Smart card interface mode	Error processing	An error signal can be automatically transmitted when detecting a parity error during reception	An error signal can be automatically transmitted when detecting a parity error during reception
		Data can be automatically retransmitted when receiving an error signal during transmission	Data can be automatically retransmitted when receiving an error signal during transmission
	Data type	Both direct convention and inverse convention are supported.	Both direct convention and inverse convention are supported.
Simple I^2C mode	Communication format	I^2C bus format (MSB-first transfer only)	I^2C bus format
	Operating mode	Master (single-master operation only)	Master (single-master operation only)
	Transfer rate	Max. 384 kbps	Fast mode is supported.
	Noise cancellation	The signal paths from input on the SSCLn and SSDAn pins incorporate digital noise filters, and the interval for noise cancellation is adjustable.	The signal paths from input on the SSCLn and SSDAn pins incorporate digital noise filters, and the interval for noise cancellation is adjustable.
Simple SPI mode	Data length	8 bits	8 bits
	Detection of errors	Overrun error	Overrun error
	SS input pin function	Applying the high level to the SSn# pin can cause the output pins to enter the high-impedance state.	Applying the high level to the SSn# pin can cause the output pins to enter the high-impedance state.
	Clock settings	Four kinds of settings for clock phase and clock polarity are selectable.	Four kinds of settings for clock phase and clock polarity are selectable.

Item		RX21A (SCIc)	RX23E-A (SCIg, SCIh)
Extended serial mode (supported by SCI12 only)	Start frame transmission	—	• Break field low width output and generation of interrupt on completion • Detection of bus collision and generation of interrupt on detection
	Start frame reception	—	• Detection of break field low width and generation of interrupt on detection • Data comparison of control fields 0 and 1 and generation of interrupt when they match • Ability to specify two kinds of data for comparison (primary and secondary) in control field 1 • Ability to specify priority interrupt bit in control field 1 • Support for start frames that do not include a break field • Support for start frames that do not include a control field 0 • Function for measuring bit rates
	I/O control function	—	• Ability to select polarity or TXDX12 and RXDX12 signals • Ability to specify digital filtering of RXDX12 signal • Half-duplex operation employing RXDX12 and TXDX12 signals multiplexed on the same pin • Ability to select receive data sampling timing of RXDX12 pin
	Timer function	—	Usable as reloading timer
Bit rate modulation function		—	Correction of outputs from the on-chip baud rate generator can reduce errors.
Event link function (supported by SCI5 only)		• Error (receive error, error signal detection) event output • Receive data full event output • Transmit data empty event output • Transmit end event output	• Error (receive error, error signal detection) event output • Receive data full event output • Transmit data empty event output • Transmit end event output

Table 2.56 Comparison of Serial Communications Interface Channel Specifications

Item	RX21A (SCIc)	RX23E-A (SCIg, SCIh)
Synchronous mode	SCI1, SCI5, SCI6, SCI8, SCI9	SCI1, SCI5, SCI6, SCI12
Clock synchronous mode	SCI1, SCI5, SCI6, SCI8, SCI9	SCI1, SCI5, SCI6, SCI12
Smart card interface mode	SCI1, SCI5, SCI6, SCI8, SCI9	SCI1, SCI5, SCI6, SCI12
Simple I^2C mode	SCI1, SCI5, SCI6, SCI8, SCI9	SCI1, SCI5, SCI6, SCI12
Simple SPI mode	SCI1, SCI5, SCI6, SCI8, SCI9	SCI1, SCI5, SCI6, SCI12
Extended serial mode	—	SCI12
TMR clock input	SCI5, SCI6	SCI5, SCI6, SCI12
Event link function	SCI5	SCI5

Table 2.57 Comparison of Serial Communications Interface Registers

Register	Bit	RX21A (SCIc)	RX23E-A (SCIg, SCIh)
RDRH, RDRL, RDRHL	—	—	Receive data registers H, L, and HL
TDRH, TDRL, TDRHL	—	—	Transmit data registers H, L, and HL
SMR	CHR	Character length bit When SCMR.SMIF bit = 0 (valid in asynchronous mode only) 0: Transmission/reception using 8-bit data length 1: Transmission/reception using 7-bit data length	Character length bits When SCMR.SMIF bit = 0 (valid in asynchronous mode only) Select the setting of these bits in combination with the setting of the SCMR.CHR1 bit. CHR1 CHR 0 0: Transmission/reception using 9-bit data length 0 1: Transmission/reception using 9-bit data length 1 0: Transmission/reception using 8-bit data length 1 1: Transmission/reception using 7-bit data length
SSR	RDRF	—	Receive data full flag
	TDRE	—	Transmit data empty flag
SCMR	CHR1	—	Character length bit 1
MDDR	—	—	Modulation duty register
SEMR	BRME	—	Serial extended mode register
	BGDM	—	Baud rate generator double-speed mode select bit
	RXDESEL	—	Asynchronous start bit edge detection select bit
ESMER	—	—	Extended serial mode enable register
CR0	—	—	Control register 0
CR1	—	—	Control register 1
CR2	—	—	Control register 2
CR3	—	—	Control register 3
PCR	—	—	Port control register
ICR	—	—	Interrupt control register
STR	—	—	Status register
STCR	—	—	Status clear register

Register	Bit	RX21A (SCIc)	RX23E-A (SCIg, SCIh)
CF0DR	—	—	Control Field 0 data register
CF0CR	—	—	Control Field 0 compare enable register
CF0RR	—	—	Control Field 0 receive data register
PCF1DR	—	—	Primary Control Field 1 data register
SCF1DR	—	—	Secondary Control Field 1 data register
CF1CR	—	—	Control Field 1 compare enable register
CF1RR	—	—	Control Field 1 receive data register
TCR	—	—	Timer control register
TMR	—	—	Timer mode register
TPRE	—	—	Timer prescaler register
TCNT	—	—	Timer count register

2.21 I²C Bus Interface

Table 2.58 is a comparative overview of I²C bus interface, and Table 2.59 is a comparison of I²C bus interface registers.

Table 2.58 Comparative Overview of I²C Bus Interface

Item	RX21A (RIIC)	RX23E-A (RIICa)
Number of channels	2 channels	1 channel
Communication format	• I²C bus format or SMBus format • Selectable between master mode and slave mode • Automatic securing of set-up times, hold times, and bus-free times to match the specified transfer speed	• I²C bus format or SMBus format • Selectable between master mode and slave mode • Automatic securing of set-up times, hold times, and bus-free times to match the specified transfer speed
Transfer speed	Up to 400 kbps	Support for fast mode (up to 400 kbps)
SCL clock	Ability to select duty cycle of SCL clock within range of 4% to 96% during master operation	Ability to select duty cycle of SCL clock within range of 4% to 96% during master operation
Issuing and detecting conditions	• Automatic generation of start, restart, and stop conditions • Ability to detect start conditions (including restart conditions) and stop conditions	• Automatic generation of start, restart, and stop conditions • Ability to detect start conditions (including restart conditions) and stop conditions
Slave address	• Ability to set up to three slave addresses • Support for 7- and 10-bit address formats (along with use of both at once) • Ability to detect general call addresses, device ID addresses, and SMBus host addresses	• Ability to set up to three different slave addresses • Support for 7- and 10-bit address formats (along with use of both at once) • Ability to detect general call addresses, device ID addresses, and SMBus host addresses
Acknowledgment	• Automatic loading of acknowledge bit during transmission — Ability to suspend the next data transfer automatically on detection of a not-acknowledge bit • Automatic transmission of acknowledge bit during reception — Support for software control of value of the acknowledge bit according to the received data when a wait between the eighth and ninth clock cycles is selected	• Automatic loading of acknowledge bit during transmission — Ability to suspend the next data transfer automatically on detection of a not-acknowledge bit • Automatic transmission of acknowledge bit during reception — Support for software control of value of the acknowledge bit according to the received data when a wait between the eighth and ninth clock cycles is selected
Wait function	• Ability to implement a wait by holding the SCL clock signal low — Wait between the eighth and ninth clock cycles — Wait between the ninth and first clock cycles (WAIT function)	• Ability to implement a wait by holding the SCL clock signal low — Wait between the eighth and ninth clock cycles — Wait between the ninth and first clock cycles
SDA output delay function	Ability to delay output timing of transmitted data, including the acknowledge bit	Ability to delay output timing of transmitted data, including the acknowledge bit

Item	RX21A (RIIC)	RX23E-A (RIICa)
Arbitration	• Multi-master support — Ability to synchronize operation with the clock of another master in cases of conflict with the SCL clock — Ability to detect loss of arbitration in case of an SDA line signal state mismatch when a start condition issuance conflict occurs — Ability to detect loss of arbitration when a start transmit data mismatch occurs during master operation • Ability to detect loss of arbitration due to start condition issuance when the bus is busy (to prevent issuance of duplicate start conditions) • Ability to detect loss of arbitration in case of an SDA line signal state mismatch when a not-acknowledge bit is sent • Ability to detect loss of arbitration when a data mismatch occurs during slave transmission	• Multi-master support — Ability to synchronize operation with the clock of another master in cases of conflict with the SCL clock — Ability to detect loss of arbitration in case of an SDA line signal state mismatch when a start condition issuance conflict occurs — Ability to detect loss of arbitration when a start transmit data mismatch occurs during master operation • Ability to detect loss of arbitration due to start condition issuance when the bus is busy (to prevent issuance of duplicate start conditions) • Ability to detect loss of arbitration in case of an SDA line signal state mismatch when a not-acknowledge bit is sent • Ability to detect loss of arbitration when a data mismatch occurs during slave transmission
Timeout detection function	Ability to detect extended stopping of the SCL clock using built-in time-out function	Ability to detect extended stopping of the SCL clock using built-in time-out function
Noise cancellation	Built-in digital noise filters for SCL and SDA signals, and ability to adjust the noise cancellation width by software.	Built-in digital noise filters for SCL and SDA signals, and ability to adjust the noise cancellation width by software.
Interrupt sources	Four sources • Communication error/event occurrence (AL detection, NACK detection, timeout detection, start condition (including restart condition) detection, or stop condition detection) • Receive data full (including match with slave address) • Transmit data empty (including match with slave address) • Transmission complete	Four sources • Communication error/event occurrence, arbitration detection, NACK detection, timeout detection, start condition (including restart condition) detection, or stop condition detection • Receive data full (including match with slave address) • Transmit data empty (including match with slave address) • Transmission complete
Low power consumption function	Ability to specify module stop state	Ability to transition to module stop state
RIIC operating modes	Four modes: • Master transmit mode • Master receive mode • Slave transmit mode • Slave receive mode	Four modes: • Master transmit mode • Master receive mode • Slave transmit mode • Slave receive mode

Item	RX21A (RIIC)	RX23E-A (RIICa)
Event link function (output)	Four sources (RIIC0) • Communication error/event occurrence, AL detection, NACK detection, timeout detection, start condition (including restart condition) detection, or stop condition detection • Receive data full (including match with slave address) • Transmit data empty (including match with slave address) • Transmission complete	Four sources (RIIC0) • Communication error/event occurrence, arbitration detection, NACK detection, timeout detection, start condition (including restart condition) detection, or stop condition detection • Receive data full (including match with slave address) • Transmit data empty (including match with slave address) • Transmission complete

Table 2.59 Comparison of I^2C Bus Interface Registers

Register	Bit	RX21A (RIIC)	RX23E-A (RIICa)
ICMR2	TMWE	Timeout internal counter write enable bit	—
TMOCNT	—	Timeout internal counter	—

2.22 Serial Peripheral Interface

Table 2.60 is a comparative overview of the serial peripheral interfaces, and Table 2.61 is a comparison of serial peripheral interface registers.

Table 2.60 Comparative Overview of Serial Peripheral Interfaces

Item	RX21A (RSPI)	RX23E-A (RSPIb)
Number of channels	2 channels	1 channel
RSPI transfer functions	• Use of MOSI (master out/slave in), MISO (master in/slave out), SSL (slave select), and RSPCK (RSPI clock) signals allows serial communications through SPI operation (4-wire method) or clock synchronous operation (3-wire method). • Transmit-only operation is available. • Serial communication is possible in master or slave mode. • The polarity of the serial transfer clock can be changed. • The phase of the serial transfer clock can be changed.	• Use of MOSI (master out/slave in), MISO (master in/slave out), SSL (slave select), and RSPCK (RSPI clock) signals allows serial communications through SPI operation (4-wire method) or clock synchronous operation (3-wire method). • Transmit-only operation is available. • Communication mode: Full-duplex or transmit-only can be selected. • Switching of the polarity of RSPCK • Switching of the phase of RSPCK
Data format	• MSB first/LSB first selectable • Transfer bit length is selectable as 8, 9, 10, 11, 12, 13, 14, 15, 16, 20, 24, or 32 bits. • 128-bit transmit/receive buffers • Up to four frames can be transferred in one round of transmission/reception (each frame consisting of up to 32 bits).	• MSB first/LSB first selectable • Transfer bit length is selectable as 8, 9, 10, 11, 12, 13, 14, 15, 16, 20, 24, or 32 bits. • 128-bit transmit/receive buffers • Up to four frames can be transferred in one round of transmission/reception (each frame consisting of up to 32 bits).
Bit rate	• In master mode, the on-chip baud rate generator generates RSPCK by frequency-dividing PCLK (the maximum division ratio ranges divided by 4,096). • In slave mode the external input clock is used as the serial clock. (The maximum frequency is PCLK divided by 8.) Width at high level: 4 cycles of PCLK; width at low level: 4 cycles of PCLK	• In master mode, the on-chip baud rate generator generates RSPCK by frequency-dividing PCLK (the division ratio ranges from divided by 2 to divided by 4,096). • In slave mode, the minimum PCLK clock divided by 6 can be input as RSPCK (the maximum frequency of RSPCK is that of PCLK divided by 6). Width at high level: 3 cycles of PCLK; width at low level: 3 cycles of PCLK
Buffer configuration	• Double buffer configuration for the transmit/receive buffers	• Double buffer configuration for the transmit/receive buffers • 128 bits for the transmit/receive buffers
Error detection	• Mode fault error detection • Overrun error detection • Parity error detection	• Mode fault error detection • Overrun error detection*1 • Parity error detection • Underrun error detection

Item	RX21A (RSPI)	RX23E-A (RSPIb)
SSL control function	• Four SSL signals (SSLn0 to SSLn3) for each channel • In single-master mode, SSLn0 to SSLn3 signals are output. • In multi-master mode: SSLn0 signal for input, and SSLn1 to SSLn3 signals for either output or unused. • In slave mode: SSLn0 signal for input, and SSLn1 to SSLn3 signals for unused. • Controllable delay from SSL output assertion to RSPCK operation (RSPCK delay) — Setting range: 1 to 8 RSPCK cycles — Setting unit: 1 RSPCK cycle • Controllable delay from RSPCK stop to SSL output negation (SSL negation delay) — Setting range: 1 to 8 RSPCK cycles — Setting unit: 1 RSPCK cycle • Controllable wait for next-access SSL output assertion (next-access delay) — Setting range: 1 to 8 RSPCK cycles — Setting unit: 1 RSPCK cycle • Function for changing SSL polarity	• Four SSL pins (SSLA0 to SSLA3) for each channel • In single-master mode, SSLA0 to SSLA3 pins are output. • In multi-master mode: SSLA0 pin for input, and SSLA1 to SSLA3 pins for either output or unused. • In slave mode: SSLA0 pin for input, and SSLA1 and SSLA3 pins for unused. • Controllable delay from SSL output assertion to RSPCK operation (RSPCK delay) — Setting range: 1 to 8 RSPCK cycles — Setting unit: 1 RSPCK cycle • Controllable delay from RSPCK stop to SSL output negation (SSL negation delay) — Setting range: 1 to 8 RSPCK cycles — Setting unit: 1 RSPCK cycle • Controllable wait for next-access SSL output assertion (next-access delay) — Setting range: 1 to 8 RSPCK cycles — Setting unit: 1 RSPCK cycle • Function for changing SSL polarity
Control in master transfer	• A transfer of up to eight commands can be executed sequentially in looped execution. • For each command, the following can be set: SSL signal value, bit rate, RSPCK polarity/phase, transfer data length, MSB/LSB first, burst, RSPCK delay, SSL negation delay, and next-access delay • A transfer can be initiated by writing to the transmit buffer. • MOSI signal value specifiable in SSL negation	• A transfer of up to eight commands can be executed sequentially in looped execution. • For each command, the following can be set: SSL signal value, bit rate, RSPCK polarity/phase, transfer data length, MSB/LSB first, burst, RSPCK delay, SSL negation delay, and next-access delay • A transfer can be initiated by writing to the transmit buffer. • MOSI signal value specifiable in SSL negation • RSPCK auto-stop function
Interrupt sources	Maskable interrupt sources • RSPI receive interrupt (receive buffer full) • RSPI transmit interrupt (transmit buffer empty) • RSPI error interrupt (mode fault, overrun, or parity error) • RSPI idle interrupt (RSPI idle)	• Receive buffer full interrupt • Transmit buffer empty interrupt • RSPI error interrupt (mode fault, overrun, underrun, or parity error) • RSPI idle interrupt (RSPI idle)

Item	RX21A (RSPI)	RX23E-A (RSPIb)
Event link function (output)	Supported by RSPI0 only • Receive buffer full event output • Transmit buffer empty event output • Mode fault, overrun, or parity error event output • RSPI idle event output • Transmission-completed event output	The following events can be output to the event link controller. (RSPI0) • Receive buffer full event signal • Transmit buffer empty event signal • Mode fault, overrun, underrun, or parity error event signal • RSPI idle event signal • Transmission-completed event signal
Other functions	• Function for switching between CMOS output and open-drain output • Function for initializing the RSPI • Loopback mode	• Function for switching between CMOS output and open-drain output • Function for initializing the RSPI • Loopback mode
Low power consumption function	Ability to specify module stop state	Ability to specify module stop state

Note: 1. In master receive mode with the RSPCK auto-stop function enabled, the transfer clock stops when an overrun error is detected, so no overrun error is generated.

Table 2.61 Comparison of Serial Peripheral Interface Registers

Register	Bit	RX21A (RSPI)	RX23E-A (RSPIb)
SPSR	MODF	Mode fault error flag 0: No mode fault error occurred. 1: A mode fault error occurred.	Mode fault error flag*1 0: No mode fault error or underrun error occurred. 1: A mode fault error or underrun error occurred.
	UDRF	—	Underrun error flag*1
	SPTEF	—	Transmit buffer empty flag
	SPRF	—	Receive buffer full flag
SPCR2	SCKASE	—	RSPCK auto-stop function enable bit

Note: 1. When clearing the UDRF flag to 0, also clear the MODF flag to 0 at the same time.

2.23 24-Bit ΔΣ A/D Converter

Table 2.62 is a comparative overview of the 24-bit ΔΣ A/D converters, and Table 2.63 is a comparison of the 24-bit ΔΣ A/D converter registers.

Table 2.62 Comparative Overview of 24-Bit ΔΣ A/D Converters

Item	RX21A (DSAD)	RX23E-A (DSADA)
Number of units	Max. 7 units	2 units
Input channels	Max. 7 channels	6 channels (12 inputs)
A/D conversion method	Second-order ΔΣ modulation	ΔΣ modulation
Resolution	24 bits	24 bits
Analog input	• Differential input: 4 channels (ANDS0P/ANDS0N, ANDS1P/ANDS1N, ANDS2P/ANDS2N, ANDS3P/ANDS3N) • Single-ended input: 3 channels (ANDS4, ANDS5, ANDS6)	Ability to select input type individually for each channel using analog multiplexer (AMUX) • Differential input • Pseudo-differential input • Single-ended input
Modulator clock frequency (fMOD)	—	• Normal mode: 500 kHz • Low-power mode: 125 kHz
Programmable gain amplifier (PGA)	• ANDS0P to ANDS3P and ANDS0N to ANDS3N: ×1, ×2, ×4, ×8, ×16, ×32, ×64 • ANDS4 to ANDS6: ×1, ×2, ×4	• Ability to set the PGA gain individually for each channel (×1, ×2, ×4, ×8, ×16, ×32, ×64, or ×128) • Ability to bypass the PGA and route input directly to the DSAD • Ability to bypass the PGA and route input to the DSAD via the analog input buffer (BUF)
Data register	• A/D conversion result register for each analog input channel • Expansion of upper bits of conversion result and storage as signed 32-bit data	One A/D conversion result register and one A/D conversion average value register • Ability to check dedicated register for channel number corresponding to A/D conversion result • Overflow flags corresponding to A/D conversion results • Ability to express output code as two's complement or in straight binary format
Operating clock	Ability to set frequency division ratio of peripheral module clock PCLKB and A/D conversion clock DSADCLK as follows: • PCLKB:DSADCLK frequency division ratio = N:1 (N: 1, 2, 4, 8, 16, or 32) • DSADCLK = 25 MHz (fixed)	• Normal mode: 4 MHz • Low power mode: 1 MHz Generation of PCLKB with frequency division ratio of 1, 2, 3, 4, 5, 6, 7.5, or 8

Item	RX21A (DSAD)	RX23E-A (DSADA)
Conversion start conditions	• Occurrence of event set by event link controller (ELC) • Ability to set an event for each channel independently	• Software trigger • Hardware trigger
Start synchronization between units	—	Ability to synchronize the start of unit 0 and unit 1
Operating modes	• One-shot operation	• Continuous scan mode (operation until auto scan is stopped) • Single scan mode (stop after one auto scan cycle) • One-shot operation (stop after A/D conversion completes)
A/D conversion count	• 1 time (stop after A/D conversion completes)	Ability to set for each channel the A/D conversion count per auto scan cycle • Setting range of 1 to 8,032 times or 1 to 255 times depending on register settings • A setting of 0 times results in one-shot operation.
Input selection	• Normal conversion: A/D conversion of signals input on analog input pins • ΔΣ modulator single conversion: A/D conversion of signals input to ΔΣ modulator from on-chip D/A converter	• A/D conversion of signals input on analog input pins
Conversion mode	—	• Normal operation • Single-cycle settling
Oversampling comparison (OSR)	—	• Selectable among 64, 128, 256, 512, 1,024, 2,048, and user-defined value. • User-defined value: 32 to 65,536 (multiples of 16 only) • Can be set individually for each channel.
A/D conversion result averaging	—	• Ability to select type of averaging operation — No averaging — Perform averaging and generate A/D conversion end interrupt for each A/D conversion. — Perform averaging and generate A/D conversion end interrupt when average value is stored. • Ability to specify number of data units to be averaged independently for each channel (8, 16, 32, or 64)

Item	RX21A (DSAD)	RX23E-A (DSADA)
Interrupt sources	• Generation of interrupt request (DSADI0 to DSADI6) at completion of A/D conversion on each channel, and ability to activate the DMA controller (DMAC) or data transfer controller (DTC) can be activated by any interrupt • Generation of data register overwrite interrupt request (DSADORI) when a conversion result overwrites the previous conversion result before the data register is read	• A/D conversion end interrupt (ADI0 and ADI1) • Scan end interrupt (SCANEND0 and SCANEND1)
Scan operation	Operation timing is controlled independently for each channel on which A/D conversion is enabled.	Conversion takes place sequentially, starting from channel 0, on channels on which A/D conversion is enabled.
Digital filter	Decimation filter	4-stage sinc filter
Offset and gain error correction	—	Automatic offset and gain error correction using register settings
Disconnection detection assist	—	Input signal disconnection detection assist function • Ability to set disconnection detection current independently for each channel (0.5 µA, 2 µA, 4 µA, or 20 µA)
Error detection	—	If errors occur in an A/D conversion result, an error is reported together with the A/D conversion result.
Event link function	A/D conversion start at trigger from ELC (hardware trigger)	A/D conversion start at trigger from ELC (hardware trigger)
Low power consumption function	• Ability to specify the module stop state to stop supply of the clock • Ability to independently start or stop the on-chip BGR, individual channels of the PGA, and ΔΣ modulator	Ability to transition to module stop state

Table 2.63 Comparison of 24-Bit ΔΣ A/D Converter Registers

Register	Bit	RX21A (DSAD)	RX23E-A (DSADA)
CCR	—	—	DSAD operating clock control register
MR	—	—	DSAD operating mode register
MRm	—	—	Channel m operation mode register (m = 0 to 5)
CRm	—	—	Channel m control register (m = 0 to 5)
ADST	—	—	A/D conversion start register
ADSTP	—	—	A/D conversion end register
DSADDR0 to DSADDR6: (RX21A) DR: (RX23E-A)	DATA[23:0]	—	Data bits
	OVF	—	Overflow flag
	ERR	—	Error detection flag
	CCH[2:0]	—	Conversion channel indication bits
AVDR	—	—	Average value data register
SR	—	—	Status register
OSRm	—	—	Channel m oversampling comparison setting register (m = 0 to 5)
GCRm	—	—	Channel m gain correction register (m = 0 to 5)
OFCRm	—	—	Channel m offset correction register (m = 0 to 5)
DSADCR0 to DSADCR6	—	ΔΣA/D control registers 0 to 6	—
DSADRSTR	—	ΔΣA/D reset register	—
DSADCSR0 to DSADCSR6	—	ΔΣ A/D control/status registers 0 to 6	—
DSADGSR0 to DSADGSR3	—	ΔΣ A/D gain select registers 0 to 3	—
DSADGSR4 to DSADGSR6	—	ΔΣ A/D gain select registers 4 to 6	—
DSADFR0 to DSADFR6	—	ΔΣ A/D overwrite flag registers 0 to 6	—
DSADRCR	—	ΔΣ A/D reference control register	—
DSADCER	—	ΔΣ A/D control expansion register	—
DSADISR0 to DSADISR6	—	ΔΣ A/D input select registers 0 to 6	—
DSADIIC	—	ΔΣ A/D input impedance calibration data register	—
DSADGmXn	—	ΔΣ A/D gain calibration data registers (m = 0 to 6, n = 1, 2, 4, 8, 16, 32)	—

2.24 10-Bit A/D Converter/12-Bit A/D Converter

Table 2.64 is a comparative overview of the 10-bit and 12-bit A/D converters, Table 2.65 is a comparison of 12-bit A/D converter registers), and Table 2.66 is a comparison of A/D conversion start triggers that can be set in the ADSTRGR register.

Table 2.64 Comparative Overview of 10-Bit and 12-Bit A/D Converters

Item	RX21A (AD)	RX23E-A (S12ADE)
Number of units	1 unit	1 unit
Input channels	7 channels	6 channels
Extended analog function	Temperature sensor output, internal reference voltage	—
A/D conversion method	Successive approximation method	Successive approximation method
Resolution	10 bits	12 bits
Conversion time	2.0 µs per channel (when A/D conversion clock ADCLK = 25 MHz)	1.4 µs per channel (when A/D conversion clock ADCLK = 32 MHz)
A/D conversion clock	Peripheral module clock PCLK and A/D conversion clock ADCLK can be set so that the frequency ratio should be one of the following. PCLK to ADCLK frequency division ratio = 1:1, 1:2, 1:4, 1:8, 2:1, 4:1 ADCLK is set using the clock generation circuit.	Peripheral module clock PCLK and A/D conversion clock ADCLK can be set so that the frequency ratio should be one of the following. PCLK to ADCLK frequency ratio = 1:1, 1:2, 2:1, 4:1, 8:1 ADCLK is set using the clock generation circuit.
Data register	• 7 registers for analog input • One register for temperature sensor • One register for internal reference • The results of A/D conversion are stored in 10-bit A/D data registers. • The value obtained by adding up A/D-converted results is stored as a value in the number of 12 bits in the A/D data registers in A/D-converted value addition mode.	• 6 registers for analog input, 1 for A/D-converted data duplication in double trigger mode. • One register for self-diagnosis • The results of A/D conversion are stored in 12-bit A/D data registers. • 12-bit accuracy output for the results of A/D conversion • The value obtained by adding up A/D-converted results is stored as a value in the number of bit for conversion accuracy + 2 bits/4 bits in the A/D data registers in A/D-converted value addition mode. • Double trigger mode (selectable in single scan and group scan modes): The first piece of A/D-converted analog-input data on one selected channel is stored in the data register for the channel, and the second piece is stored in the duplication register.

Item	RX21A (AD)	RX23E-A (S12ADE)
Operating modes	• Single scan mode: — A/D conversion is performed only once on the analog inputs of up to 7 channels arbitrarily selected. — A/D conversion is performed only once on the temperature sensor output. — A/D conversion is performed only once on the internal reference voltage. • Continuous scan mode: A/D conversion is performed repeatedly on the analog inputs of up to 7 channels arbitrarily selected.	• Single scan mode: — A/D conversion is performed only once on the analog inputs of up to 6 channels arbitrarily selected. • Continuous scan mode: A/D conversion is performed repeatedly on the analog inputs of up to 6 channels arbitrarily selected. • Group scan mode: — Analog inputs of up to 6 channels arbitrarily selected, are divided into group A and group B, and A/D conversion of the analog input selected on a group basis is performed only once. — The conditions for scanning start of group A and group B (synchronous trigger) can be independently selected, thus allowing A/D conversion of group A and group B to be started independently. • Group scan mode (when group A is given priority): — If a group A trigger is input during A/D conversion on group B, the A/D conversion on group B is stopped and A/D conversion is performed on group A. — Restart (rescan) of A/D conversion on group B after completion of A/D conversion on group A can be set.
Conditions for A/D conversion start	• Software trigger • Synchronous trigger Trigger by the MTU, ELC, or temperature sensor. • Asynchronous trigger A/D conversion can be triggered by the ADTRG0# pin.	• Software trigger • Synchronous trigger Trigger by the multi-function timer pulse unit (MTU) or event link controller (ELC). • Asynchronous trigger A/D conversion can be triggered by the external trigger ADTRG0# pin.

Item	RX21A (AD)	RX23E-A (S12ADE)
Functions	• Sample-and hold function • Variable sampling state count • Self-diagnosis of 10-bit A/D converter • A/D-converted value addition mode • Analog input disconnection detection assist function	• Variable sampling state count • Self-diagnosis of 12-bit A/D converter • Selectable A/D-converted value addition mode or average mode • Analog input disconnection detection function (discharge function/precharge function) • Double trigger mode (duplication of A/D conversion data) • Automatic clear function of A/D data registers • Compare function (window A and window B) • 16 ring buffers when the compare function is used
Interrupt sources	• A/D scan end interrupt request (ADI) can be generated on completion of single scan. • The ADI interrupt can activate the DMA controller (DMAC) and the data transfer controller (DTC).	• In the modes except double trigger mode and group scan mode, A/D scan end interrupt request (S12ADI0) can be generated on completion of single scan. • In double trigger mode, A/D scan end interrupt request (S12ADI0) can be generated on completion of double scan. • In group scan mode, an A/D scan end interrupt request (S12ADI0) can be generated on completion of group A scan, whereas an A/D scan end interrupt request (GBADI) for group B can be generated on completion of group B scan. • When double trigger mode is selected in group scan mode, A/D scan end interrupt request (S12ADI0) can be generated on completion of double scan of group A, whereas A/D scan end interrupt request (GBADI) specially for group B can be generated on completion of group B scan. • The S12ADI0 and GBADI interrupts can activate the DMA controller (DMAC) and the data transfer controller (DTC).

Item	RX21A (AD)	RX23E-A (S12ADE)
Event link function	• An ELC event can be generated on completion of scans. • A/D conversion can be started by a trigger output by the ELC.	• An ELC event is generated on completion of scans other than group B scan in group scan mode. • An ELC event is generated on completion of group B scan in group scan mode. • An ELC event is generated on completion of all scans. • Scan can be started by a trigger output by the ELC. • An ELC event is generated according to the event conditions of the window compare function in single scan mode.
Low power consumption function	Ability to specify module stop state	Ability to specify module stop state

Table 2.65 Comparison of 12-Bit A/D Converter Registers

Register	Bit	RX21A (AD)	RX23E-A (S12ADE)
ADDRy	—	A/D data register y (y = 0 to 6)	A/D data register y (y = 0 to 5)
ADDBLDR	—	—	A/D data duplication register
ADTSDR	—	A/D temperature sensor data register	—
ADOCDR	—	A/D internal reference voltage data register	—
ADCSR	DBLANS[4:0]	—	Double trigger channel select bits
	GBADIE	—	Group B scan end interrupt enable bit
	DBLE	—	Double trigger mode select bit
	ADHSC	—	A/D-converted value addition channel select bits
	ADCS (RX21A) ADCS[1:0] (RX23E-A)	Scan mode select bits (b14) 0: Single scan mode 1: Continuous scan mode	Scan mode select bits (b14, b13) b14 b13 0 0: Single scan mode 0 1: Group scan mode 1 0: Continuous scan mode 1 1: Setting prohibited.
ADANSA (RX21A) ADANSA0 (RX23E-A)	ANSA[6:0] (RX21A) ANSA0n (RX23E-A)	A/D converter channel select bits (b6 to b0)	A/D converter channel select bits (n = 00 to 05)
ADANSB0	—	—	A/D channel select register B0
ADADS (RX21A) ADADS0 (RX23E-A)	ADS[6:0] (RX21A) ADS0n (RX23E-A)	A/D-converted value addition channel select bits (b6 to b0)	A/D-converted value addition/average channel select bits (n = 00 to 05)

Register	Bit	RX21A (AD)	RX23E-A (S12ADE)
ADADC	ADC[1:0] (RX21A) ADC[2:0] (RX23E-A)	Addition count select bits (b1, b0) b1 b0 0 0: 1-time conversion (no addition; same as normal conversion) 0 1: 2-time conversion (addition one time) 1 0: 3-time conversion (addition two times) 1 1: 4-time conversion (addition three times)	Addition count select bits (b2 to b0) b2 b0 0 0 0: 1-time conversion (no addition; same as normal conversion) 0 0 1: 2-time conversion (addition one time) 0 1 0: 3-time conversion (addition two times) 0 1 1: 4-time conversion (addition three times) 1 0 1: 16-time conversion (addition 15 times) Settings other than the above are prohibited.
	AVEE	—	Averaging mode enable bit
ADSTRGR	TRSB[5:0]	—	A/D conversion start trigger select for group B bits
	TRSA[4:0] (RX21A) TRSA[5:0] (RX23E-A)	A/D conversion start trigger select bits (b12 to b8)	A/D conversion start trigger select bits (b13 to b8)
ADEXICR	—	A/D conversion extended input control register	—
ADSSTRn	—	A/D sampling state register n (n = 0 to 6, T, O)	A/D sampling state register n (n = 0 to 5)
ADDISCR	ADNDIS[3:0] (RX21A) ADNDIS[4:0] (RX23E-A)	Disconnection detection assist setting bits (b3 to b0)	A/D disconnection detection assist setting bits (b4 to b0)
ADELCCR	—	—	A/D event link control register
ADGSPCR	—	—	A/D group scan priority control register
ADCMPCR	—	—	A/D comparison function control register
ADCMPANSR0	—	—	A/D comparison function window A channel select register 0
ADCMPLR0	—	—	A/D comparison function window A comparison condition setting register 0
ADCMPDR0	—	—	A/D comparison function window A lower level setting register
ADCMPDR1	—	—	A/D comparison function window A upper level setting register
ADCMPSR0	—	—	A/D comparison function window A channel status register 0
ADHVREFCNT	—	—	A/D high-potential/low-potential reference voltage control register
ADWINMON	—	—	A/D comparison function window A/B status monitoring register
ADCMPBNSR	—	—	A/D comparison function window B channel select register

Register	Bit	RX21A (AD)	RX23E-A (S12ADE)
ADWINLLB	—	—	A/D comparison function window B lower level setting register
ADWINULB	—	—	A/D comparison function window B upper level setting register
ADCMPBSR	—	—	A/D comparison function window B channel status register
ADBUFn	—	—	A/D data storage buffer register n (n = 0 to 15)
ADBUFEN	—	—	A/D data storage buffer enable register
ADBUFPTR	—	—	A/D data storage buffer pointer register

Table 2.66 Comparison of A/D Conversion Start Triggers Set in ADSTRGR Register

Bit	RX21A (AD)	RX23E-A (S12ADE)
TRSA[4:0] (RX21A) TRSA[5:0] (RX23E-A)	A/D conversion start trigger select bits (b12 to b8) b12 b8 0 0 0 0 0: ADTRG0# 0 0 0 0 1: TRG0AN 0 0 0 1 0: TRG0BN 0 0 0 1 1: TRGAN 0 0 1 0 0: TRG0EN 0 0 1 0 1: TRG0FN 0 0 1 1 0: TRG4AN 0 0 1 1 1: TRG4BN 0 1 0 0 0: TRG4ABN 0 1 0 0 1: ELC 0 1 0 1 0: Temperature sensor	A/D conversion start trigger select bits (b13 to b8) b13 b8 1 1 1 1 1 1: No trigger source selected state 0 0 0 0 0 0: ADTRG0# 0 0 0 0 0 1: TRG0AN 0 0 0 0 1 0: TRG0BN 0 0 0 0 1 1: TRGAN 0 0 0 1 0 0: TRG0EN 0 0 0 1 0 1: TRG0FN 0 0 0 1 1 0: TRG4AN 0 0 0 1 1 1: TRG4BN 0 0 1 0 0 0: TRG4ABN 0 0 1 0 0 1: ELCTRG0

2.25 Data Operation Circuit

Table 2.67 is a comparative overview of data operation circuit.

Table 2.67 Comparative Overview of Data Operation Circuit

Item	RX21A (DOC)	RX23E-A (DOC)
Data operation functions	16-bit data comparison, addition, and subtraction	16-bit data comparison, addition, and subtraction
Low power consumption function	Ability to specify module stop state	Ability to specify module stop state
Interrupts	• When compared values either match or mismatch • When the result of data addition is greater than FFFFh • When the result of data subtraction is less than 0000h	• When compared values either match or mismatch • When the result of data addition is greater than FFFFh • When the result of data subtraction is less than 0000h
Event link function (output)	—	• When compared values either match or mismatch • When the result of data addition is greater than FFFFh • When the result of data subtraction is less than 0000h

2.26 RAM

Table 2.68 is a comparative overview of RAM.

Table 2.68 Comparative Overview of RAM

Item	RX21A	RX23E-A
Capacity	• 64 KB (0000 0000h to 0000 FFFFh) • 32 KB (0000 0000h to 0000 7FFFh)	• 32 KB (0000 0000h to 0000 7FFFh) • 16 KB (0000 0000h to 0000 3FFFh)
Access	• Single-cycle access is possible for both reading and writing. • On-chip RAM can be enabled or disabled.	• Single-cycle access is possible for both reading and writing. • On-chip RAM can be enabled or disabled.
Low power consumption function	Ability to specify module stop state	Ability to transition to module stop state

2.27 Flash Memory

Table 2.69 is a comparative overview of flash memory, and Table 2.70 is a comparison of flash memory registers.

Table 2.69 Comparative Overview of Flash Memory

Item	RX21A	RX23E-A (FLASH)
Memory capacity	• User area: 512 KB • Data area: 8 KB • User boot area: 16 KB	• User area: Up to 256 KB • Data area: 8 KB • Extra area: Stores the start-up area information, access window information, and unique ID
Addresses	• Products with capacity of 512 KB FFF8 0000h to FFFF FFFFh • Products with capacity of 384 KB FFFA 0000h to FFFF FFFFh • Products with capacity of 256 KB FFFC 0000h to FFFF FFFFh	• Products with capacity of 256 KB FFFC 0000h to FFFF FFFFh • Products with capacity of 128 KB FFFE 0000h to FFFF FFFFh
FCU commands (RX21A)/ Software commands (RX23E-A)	• The following FCU commands are supported: P/E normal mode transition, status read mode transition, lock bit read mode transition (lock bit read 1), peripheral clock notification, programming, block erase, P/E suspend, P/E resume, status register clear, lock bit read 2/blank check, lock bit programming	• The following software commands are implemented: Program, blank check, block erase, and all-block erase • The following commands are implemented for programming the extra area: Start-up area information program and access window information program
Value after erasure	• ROM: FFh • E2 DataFlash: FFh	• ROM: FFh • E2 DataFlash: FFh
Interrupt	Generation of interrupt (FRDYI) at completion of FCU command execution	An interrupt (FRDYI) is generated upon completion of software command processing or forced stop processing.
On-board programming	• Reprogramming in boot mode — The asynchronous serial interface (SCI1) is used. — The communication speed is adjusted automatically. — The user boot area can be programmed.	• Boot mode (SCI interface) — Channel 1 of the serial communications interface (SCI1) is used for asynchronous communication. — The user area and data area can be programmed. • Boot mode (FINE interface) — The FINE interface is used. — The user area and data area can be programmed.

Item		RX21A	RX23E-A (FLASH)
On-board programming		• Reprogramming in user boot mode — A user-specific boot program can be created. • Reprogramming using a ROM reprogramming routine in a user program — The ROM/E2 DataFlash memory can be reprogrammed without resetting the system.	• Self-programming (single-chip mode) — The user area and data area can be programmed using a flash programming routine in a user program.
Off-board programming		The user area and data area can be programmed using a flash programmer compatible with the MCU.	The user area and data area can be programmed using a flash programmer compatible with the MCU.
ID codes protection		• Connection with a serial programmer can be controlled using ID codes in boot mode. • Connection with an on-chip debugging emulator can be controlled using ID codes.	• Connection with a serial programmer can be controlled using ID codes in boot mode. • Connection with an on-chip debugging emulator can be controlled using ID codes.
Protection	Software-controlled protection function	• The FENTRYR.FENTRY0, FWEPROR.FLWE[1:0], and lock bits, and the DFLRE0 and DFLWE0 registers, can be used to prevent unintentional programming. • Protection using the DFLRE0 and DFLWE0 registers is applied in 2 KB units.	• The DFLCTL.DFLEN and FENTRYR.FENTRY0 bits can be used to prevent unintentional programming.
	Command-locked state	When abnormal operations are detected during programming or erasure, this function disables any further programming/erasure.	—
	Boot program protection	Programming and erasure of the user boot area are possible only in boot mode.	—
	Start-up program protection function	—	This function is used to safely program blocks 0 to 7.
	Area protection	—	During self-programming, this function enables programming only of specified blocks in the user area and disables programming of the other blocks.
Background operation (BGO) function		• A program located in the ROM area can run while the E2 DataFlash memory is being programmed or erased. • A program located in other than the ROM/E2 DataFlash memory can run on the CPU while the ROM is being programmed or erased.	Programs in the ROM can run while the E2 DataFlash is being programmed.

Table 2.70 Comparison of Flash Memory Registers

Register	Bit	RX21A	RX23E-A (FLASH)
DFLCTL	—	—	E2 DataFlash control register
FPR	—	—	Protection cancellation register
FPSR	—	—	Protection cancellation status register
FPMCR	—	—	Flash P/E mode control register
FISR	—	—	Flash initial setting register
FRESETR	—	Flash reset register FRESETR is a 16-bit register.	Flash reset register FRESETR is an 8-bit register.
	FRKEY[7:0]	Key code	—
FASR	—	—	Flash area select register
FCR	—	—	Flash control register
FEXCR	—	—	Flash extra area control register
FSARH	—	—	Flash processing start address register H
FSARL	—	—	Flash processing start address register L
FEARH	—	—	Flash processing end address register H
FEARL	—	—	Flash processing end address register L
FWBn	—	—	Flash write buffer n register (n = 0 to 3)
FSTATR0	ERSERR (RX21A) ERERR (RX23E-A)	Erasure error bit (b5)	Erasure error flag (b0)
	PRGERR	Programming error bit (b4)	Programming error flag (b1)
	BCERR	—	Blank check error flag
	ILGLERR	Illegal command error bit (b6)	Illegal command error flag (b4)
	EILGLERR	—	Extra area illegal command error flag
	PRGSPD	Programming suspend status bit	—
	ERSSPD	Erasure suspend status bit	—
	SUSRDY	Suspend ready bit	—
	FRDY	Flash ready bit	—
FSTATR1	FRDY	—	Flash ready flag
	EXRDY	—	Extra area ready flag
	FLOCKST	Lock bit status bit	—
	FCUERR	FCU error bit	—
FEAMH	—	—	Flash error address monitor register H
FEAML	—	—	Flash error address monitor register L
FSCMR	—	—	Flash startup setting monitor register
FAWSMR	—	—	Flash access window start address monitor register
FAWEMR	—	—	Flash access window end address monitor register

Register	Bit	RX21A	RX23E-A (FLASH)
FWEPROR	—	Flash write erase protection register	—
FMODR	—	Flash mode register	—
FASTAT	—	Flash access status register	—
FAEINT	—	Flash access error interrupt enable register	—
FRDYIE	—	Flash ready interrupt enable register	—
FPROTR	—	Flash protection register	—
FCMDR	—	FCU command register	—
FCPSR	—	FCU processing switching register	—
FPESTAT	—	Flash P/E status register	—
PCKAR	—	Peripheral clock notification register	—
DFLRE0	—	E2 DataFlash read enable register 0	—
DFLWE0	—	E2 DataFlash programming/ erasure enable register 0	—
DFLBCCNT	—	E2 DataFlash blank check control register	—
DFLBCSTAT	—	E2 DataFlash blank check status register	—

2.28 Packages

As indicated in Table 2.71, there are discrepancies in the package drawing codes and availability of some package types, and this should be borne in mind at the board design stage.

Table 2.71 Packages

Package Type	Renesas Code	
	RX21A	RX23E-A
100-pin TFLGA	○	×
100-pin LQFP	○	×
80-pin LQFP	○	×
64-pin LQFP	○	×
48-pin LFQFP	×	○
40-pin HWQFN	×	○

○: Package available (Renesas code omitted); ×: Package not available

3. Comparison of Pin Functions

This section presents a comparative description of pin functions as well as a comparison of the pins for the power supply, clocks, and system control. Items that exist only on one group are indicated by blue text. Items that exists on both groups with different specifications are indicated by red text. **Black text** indicates there is no differences in the item's specifications between groups.

The RX21A Group and RX23E-A Group do not include packages with the same pin count, but with some exceptions the pin functions are compatible. The pin design therefore makes migration relatively easy.

3.1 64-Pin Package (RX21A: LQFP)/48-Pin Package (RX23E-A: LQFP)/ 40-Pin Package (RX23E-A: HWQFN)

Table 3.1 is a comparative listing of the pin functions of 64-pin package (RX21A) and 48-pin package (RX23E-A) and 40-pin package (RX23E-A) products.

Table 3.1 Comparative Listing of 64-Pin Package (RX21A) and 48-Pin Package (RX23E-A) and 40-Pin Package (RX23E-A) Pin Functions

64-Pin	48-Pin	40-Pin	RX21A (64-Pin LQFP)	RX23E-A (48-Pin LFQFP)	RX23E-A (40-Pin HWQFN)
1	1	—	P03/AN4	AIN10/AN004/IEXC0/ IEXC1/IEXC2/IEXC3	—
2	10	8	VCL	VCL	VCL
3	11	9	MD/FINED	MD/FINED	MD/FINED
4	—	—	XCIN	—	—
5	—	—	XCOUT	—	—
6	5	3	RES#	RES#	RES#
7	6	4	XTAL/P37	XTAL/P37	XTAL/P37
8	7	5	VSS	VSS	VSS
9	8	6	EXTAL/P36	EXTAL/P36	EXTAL/P36
10	9	7	VCC	VCC	VCC
11	12	10	P35/NMI	P35/NMI	P35/NMI
12	—	—	P32/MTIOC0C/TMO3/ TXD6/SMOSI6/SSDA6/ IRQ2-DS/RTCOUT/ RTCIC2	—	—
13	13	11	P31/MTIOC4D/TMCI2/ CTS1#/RTS1#/SS1#/ SSLB0/IRQ1-DS/RTCIC1	P31/MTIOC1A/MTIOC4D/ TMO3/CTS1#/RTS1#/ SS1#/IRQ1	P31/MTIOC1A/MTIOC4D/ TMO3/CTS1#/RTS1#/ SS1#/IRQ1
14	14	12	P30/MTIOC4B/TMRI3/ POE8#/RXD1/SMISO1/ SSCL1/MISOB/IRQ0-DS/ RTCIC0	P30/MTIOC0A/MTIOC4B/ TMCI3/POE8#/RXD1/ SMISO1/SSCL1/IRQ0	P30/MTIOC0A/MTIOC4B/ TMCI3/POE8#/RXD1/ SMISO1/SSCL1/IRQ0
15	15	13	P27/MTIOC2B/TMCI3/ SCK1/RSPCKB	P27/MTIOC2B/MTIOC4A/ TMRI3/SCK1/IRQ3	P27/MTIOC2B/MTIOC4A/ TMRI3/SCK1/IRQ3
16	16	14	P26/MTIOC2A/TMO1/ TXD1/SMOSI1/SSDA1/ MOSIB	P26/MTIOC2A/MTIOC4C/ TMO0/TXD1/SMOSI1/ SSDA1/IRQ2	P26/MTIOC2A/MTIOC4C/ TMO0/TXD1/SMOSI1/ SSDA1/IRQ2
17	17	15	P17/MTIOC3A/MTIOC3B/ TMO1/POE8#/SCK1/ MISOA/SDA0-DS/IRQ7	P17/MTIOC3A/MTIOC3B/ TMO1/POE8#/SCK1/ MISOA/SDA/IRQ7	P17/MTIOC3A/MTIOC3B/ TMO1/POE8#/SCK1/ MISOA/SDA/IRQ7
18	18	16	P16/MTIOC3C/MTIOC3D/ TMO2/TXD1/SMOSI1/ SSDA1/MOSIA/SCL0-DS/ IRQ6/RTCOUT/ADTRG0#	P16/MTIOC3C/MTIOC3D/ TMO2/TXD1/SMOSI1/ SSDA1/MOSIA/SCL/IRQ6/ ADTRG0#	P16/MTIOC3C/MTIOC3D/ TMO2/TXD1/SMOSI1/ SSDA1/MOSIA/SCL/IRQ6/ ADTRG0#

64-Pin	48-Pin	40-Pin	RX21A (64-Pin LQFP)	RX23E-A (48-Pin LFQFP)	RX23E-A (40-Pin HWQFN)
19	19	17	P15/MTIOC0B/MTCLKB/ TMCI2/RXD1/SMISO1/ SSCL1/IRQ5	P15/MTIOC0B/MTCLKB/ TMCI2/RXD1/SMISO1/ SSCL1/SSLA1/CRXD0/ IRQ5	P15/MTIOC0B/MTCLKB/ TMCI2/RXD1/SMISO1/ SSCL1/SSLA1/CRXD0/ IRQ5
20	20	18	P14/MTIOC3A/MTCLKA/ TMRI2/CTS1#/RTS1#/ SS1#/IRQ4	P14/MTIOC3A/MTCLKA/ TMRI2/CTS1#/RTS1#/ SS1#/SSLA3/CTXD0/ IRQ4	P14/MTIOC3A/MTCLKA/ TMRI2/CTS1#/RTS1#/ SS1#/SSLA3/CTXD0/ IRQ4
21	21	—	PH3/TMCI0	PH3/MTIC5W/MTCLKB/ TMCI0/POE2#/CTS6#/ RTS6#/SS6#/RSPCKA	—
22	22	—	PH2/TMRI0/IRQ1	PH2/MTIC5V/MTCLKA/ TMRI0/SCK5/MOSIA/IRQ1	—
23	23	19	PH1/TMO0/IRQ0	PH1/MTIC5U/MTCLKD/ TMO0/POE2#/TXD5/ SMOSI5/SSDA5/SSLA0/ IRQ0/CLKOUT	PH1/MTCLKD/TMO0/ POE2#/TXD5/SMOSI5/ SSDA5/SSLA0/IRQ0/ CLKOUT
24	24	20	PH0/CACREF	PH0/MTIOC0D/MTCLKC/ TMRI0/CACREF/RXD5/ SMISO5/SSCL5/SSLA2	PH0/MTIOC0D/MTCLKC/ TMRI0/CACREF/RXD5/ SMISO5/SSCL5/SSLA2
25	—	—	P55/MTIOC4D/TMO3	—	—
26	—	—	P54/MTIOC4B/TMCI1	—	—
27	25	—	PC7/MTIOC3A/TMO2/ MTCLKB/TXD8/SMOSI8/ SSDA8/MISOA/CACREF	PC7/MTIOC3A/MTCLKB/ TMO2/CACREF/TXD6/ SMOSI6/SSDA6/MISOA	—
28	26	—	PC6/MTIOC3C/MTCLKA/ TMCI2/RXD8/SMISO8/ SSCL8/MOSIA	PC6/MTIOC3C/MTCLKA/ TMCI2/RXD6/SMISO6/ SSCL6/MOSIA	—
29	27	21	PC5/MTIOC3B/MTCLKD/ TMRI2/SCK8/RSPCKA	PC5/MTIOC3B/MTCLKD/ TMRI2/SCK5/SCK6/ SCK12/RSPCKA	PC5/MTIOC3B/MTCLKD/ TMRI2/SCK5/SCK12/ RSPCKA
30	28	22	PC4/MTIOC3D/MTCLKC/ TMCI1/POE0#/SCK5/ CTS8#/RTS8#/SS8#/ SSLA0	PC4/MTIOC3D/MTCLKC/ TMCI1/POE0#/CTS5#/ RTS5#/SS5#/CTS12#/ RTS12#/SS12#/SSLA0	PC4/MTIOC3D/MTCLKC/ TMCI1/POE0#/CTS5#/ RTS5#/SS5#/CTS12#/ RTS12#/SS12#/SSLA0
31	—	—	PC3/MTIOC4D/TXD5/ SMOSI5/SSDA5/IRTXD5	—	—
32	—	—	PC2/MTIOC4B/RXD5/ SMISO5/SSCL5/IRRXD5/ SSLA3	—	—
33	—	—	PB7/PC1/MTIOC3B/TXD9/ SMOSI9/SSDA9	—	—
34	—	—	PB6/PC0/MTIOC3D/RXD9/ SMISO9/SSCL9	—	—
35	—	—	PB5/MTIOC2A/MTIOC1B/ TMRI1/POE1#/SCK9	—	—
36	—	—	PB3/MTIOC0A/MTIOC4A/ TMO0/POE3#/SCK6	—	—
37	29	23	PB1/MTIOC0C/MTIOC4C/ TMCI0/TXD6/SMOSI6/ SSDA6/IRQ4-DS	PB1/MTIOC1B/MTIOC2A/ TMRI1/POE1#/TXD12/ TXDX12/SIOX12/ SMOSI12/SSDA12	PB1/MTIOC1B/MTIOC2A/ TMRI1/POE1#/TXD12/ TXDX12/SIOX12/ SMOSI12/SSDA12
38	30	24	VCC	VCC	VCC

64-Pin	48-Pin	40-Pin	RX21A (64-Pin LQFP)	RX23E-A (48-Pin LFQFP)	RX23E-A (40-Pin HWQFN)
39	31	25	PB0/MTIC5W/RXD6/ SMISO6/SSCL6/RSPCKA/ CMPB0	PB0/MTIOC0C/TMCI0/ POE3#/RXD12/RXDX12/ SMISO12/SSCL12/IRQ4	PB0/MTIOC0C/TMCI0/ POE3#/RXD12/RXDX12/ SMISO12/SSCL12/IRQ4
40	32	26	VSS	VSS	VSS
41	—	—	PA6/MTIC5V/MTCLKB/ TMCI3/POE2#/CTS5#/ RTS5#/SS5#/MOSIA/ CVREFB0	—	—
42	—	—	PA4/MTIC5U/MTCLKA/ TMRI0/TXD5/SMOSI5/ SSDA5/IRTXD5/SSLA0/ IRQ5-DS/CVREFB1	—	—
43	—	—	PA3/MTIOC0D/MTCLKD/ RXD5/SMISO5/SSCL5/ IRRXD5/IRQ6-DS/CMPB1	—	—
44	—	—	PA1/MTIOC0B/MTCLKC/ SCK5/SSLA2/CVREFA	—	—
45	—	—	PA0/MTIOC4A/SSLA1/ CACREF/CMPA1	—	—
46	—	—	BGR_BO	—	—
47	—	—	ANDS0N	—	—
48	—	—	ANDS0P	—	—
49	—	—	ANDS1N	—	—
50	—	—	ANDS1P	—	—
51	—	—	AVSSA	—	—
52	—	—	AVCCA	—	—
53	—	—	VREFDSL	—	—
54	—	—	VREFDSH	—	—
55	—	—	VCOMDS	—	—
56	—	—	ANDS4	—	—
57	—	—	ANDSSG	—	—
58	46	38	P41/AN1	AIN7/AN001/IEXC0/ IEXC1/IEXC2/IEXC3	AIN7/AN001/IEXC0/ IEXC1/IEXC2/IEXC3
59	47	39	VREFL0	VREFL0/AIN8/AN002/ IEXC0/IEXC1/IEXC2/ IEXC3	VREFL0/AIN8/AN002/ IEXC0/IEXC1/IEXC2/ IEXC3
60	45	37	P40/AN0	AIN6/AN000/IEXC0/ IEXC1/IEXC2/IEXC3	AIN6/AN000/IEXC0/ IEXC1/IEXC2/IEXC3
61	48	40	VREFH0	VREFH0/AIN9/AN003/ IEXC0/IEXC1/IEXC2/ IEXC3	VREFH0/AIN9/AN003/ IEXC0/IEXC1/IEXC2/ IEXC3
62	4	2	AVCC0	AVCC0	AVCC0
63	2	—	P05/AN5	AIN11/AN005/IEXC0/ IEXC1/IEXC2/IEXC3	—
64	3	1	AVSS0	AVSS0	AVSS0
—	33	27	—	AVCC0	AVCC0
—	34	28	—	AVSS0	AVSS0
—	35	29	—	REFOUT	REFOUT
—	36	30	—	LSW	LSW
—	37	31	—	REF0N	REF0N
—	38	32	—	REF0P	REF0P

64-Pin	48-Pin	40-Pin	RX21A (64-Pin LQFP)	RX23E-A (48-Pin LFQFP)	RX23E-A (40-Pin HWQFN)
—	39	33	—	AIN0/IEXC0/IEXC1/IEXC2/IEXC3	AIN0/IEXC0/IEXC1/IEXC2/IEXC3
—	40	34	—	AIN1/IEXC0/IEXC1/IEXC2/IEXC3	AIN1/IEXC0/IEXC1/IEXC2/IEXC3
—	41	—	—	AIN2/IEXC0/IEXC1/IEXC2/IEXC3	—
—	42	—	—	AIN3/IEXC0/IEXC1/IEXC2/IEXC3	—
—	43	35	—	AIN4/IEXC0/IEXC1/IEXC2/IEXC3/REF1N	AIN4/IEXC0/IEXC1/IEXC2/IEXC3/REF1N
—	44	36	—	AIN5/IEXC0/IEXC1/IEXC2/IEXC3/REF1P	AIN5/IEXC0/IEXC1/IEXC2/IEXC3/REF1P

4. Important Information when Migrating Between MCUs

This section presents important information on differences between the RX23E-A Group and the RX21A Group. 4.1, Notes on Pin Design, presents information regarding the hardware, and 4.2, Notes on Functional Design, presents information regarding the software.

4.1 Notes on Pin Design

4.1.1 VCL Pin (External Capacitor)

To stabilize the internal power supply on the RX23E-A Group, connect a 4.7 μF smoothing capacitor to the VCL pin.

4.1.2 Mode Setting Pins

On the RX21A Group the pins for setting the mode on release from the reset state are MD and PC7, but on the RX23E-A Group they are MD only.

4.2 Notes on Functional Design

Some software that runs on the RX21A Group is compatible with the RX23E-A Group. Nevertheless, appropriate caution must be exercised due to differences in aspects such as operation timing and electrical characteristics.

Software-related considerations regarding function settings that differ between the RX21A Group and RX23E-A Group are as follows:

For differences between modules and functions, refer to 2, Comparative Overview of Specifications. For further information, refer to the User's Manual: Hardware of each MCU group, listed in 5, Reference Documents.

4.2.1 MOSCWTCR Register

On the RX21A Group this register counts cycles of the main clock, and on the RX23E-A Group it counts cycles of the LOCO clock.

4.2.2 Limitations Applying to I/O Port Register Settings

On the RX23E-A Group an indefinite value is returned when reading the bits in the PDR, PODR, and PMR registers corresponding to pins P12, P13, P20, P32, P33, and P34. When writing to these bits, write-back the read value.

4.2.3 Exception Vector Table

Addresses allocated in the vector table are fixed on the RX21A Group. On the RX23E-A Group, the vector addresses are relocatable using the value set in the exception table register (EXTB) as the start address.

4.2.4 I^2C Bus Interface Noise Cancellation

On the RX21A Group the SCL and SDA lines have integrated analog noise filters, but on the RX23E-A Group there is no integrated analog noise filter.

4.2.5 24-Bit ΔΣ A/D Converter

The registers of the RX23E-A Group are substantially changed in comparison with the 24-bit ΔΣ A/D converter registers on the RX21A Group. Please note that this significantly reduces software compatibility.

4.2.6 Compare Function Limitations

On the RX23E-A Group the compare function of the 12-bit A/D converter is subject to the following limitations:

1. The self-diagnostic function and double-trigger mode must not be used at the same time. (The ADRD and ADDBLDR registers are not covered by the compare function.)
2. It is necessary to specify single-scan mode when using matched/unmatched event output.
3. Window A and window B must not be set to the same channel.
4. It is necessary to specify single-scan mode when using the buffer function. (The buffer function and double-trigger mode must not be used together.)
5. It is necessary to ensure that the high-side reference value is greater than or equal to the low-side reference value.

4.2.7 User Boot Mode

The RX21A Group has UB code A, UB code B, and user boot mode, but none of these exist on the RX23E-A Group.

When using the startup program protection function on the RX23E-A Group, it is possible to use a user-defined interface to program and erase the user area in the flash memory instead of user boot mode.

For details, refer to the startup program protection function section in RX23E-A Group User's Manual: Hardware, referenced in section 5, Reference Documents.

4.2.8 Using Flash Memory Programming Commands

On the RX21A Group, programming and erasing the flash memory are performed by issuing commands to the FCU. On the RX23E-A Group programming and erasing of the flash memory are performed by issuing software commands after transitioning to a dedicated sequencer mode for programming and erasing the ROM.

Table 4.1 is a comparative listing of FCU and software commands.

Table 4.1 Comparison of FCU and Software Command Specifications

Item	FCU Command (RX21A)	Software Command (RX23E-A)
Command issue area	Programming/erasing address (00F8 0000h to 00FF FFFFh)	—
Available command	• P/E normal mode transition • Status read mode transition • Lock bit read mode transition (lock bit read 1) • Peripheral clock notification • Programming • Block erase • Blank check • P/E suspend • P/E resume • Status register clear • Lock bit read 2 • Lock bit programming	• Programming • Block erase • All-block erase • Blank check • Startup area information programming • Access window information programming

5. Reference Documents

User's Manual: Hardware

RX21A Group User's Manual: Hardware Rev.1.10 (R01UH0251EJ0110)
(The latest version can be downloaded from the Renesas Electronics website.)

RX23E-A Group User's Manual: Hardware Rev.1.00 (R01UH0801EJ0100)
(The latest version can be downloaded from the Renesas Electronics website.)

Technical Update/Technical News

(The latest information can be downloaded from the Renesas Electronics website.)

Related Technical Updates

This module reflects the content of the following technical updates:

TN-RX*-A107A/E

TN-RX*-A118A/E

TN-RX*-A128A/E

TN-RX*-A130B/E

TN-RX*-A138A/E

TN-RX*-A141A/E

TN-RX*-A0147B/E

TN-RX*-A151A/E

TN-RX*-A188A/E

TN-RX*-A0224B/E

TN-RX*-A0225A/E

TN-RX*-A0227A/E

Revision History

Rev.	Date	Description	
		Page	Summary
1.00	Oct. 31, 2019	—	First edition issued
1.10	Dec. 11, 2020	4	1 Table 1.1 Comparison of Built-In Functions of RX23E-A Group and RX21A Group revised
		7	2.2 Table 2.3 Comparative Overview of Operating Modes revised
		9	2.3 Table 2.5 Comparative Memory Map of Single-Chip Mode deleted and Figure 2.1 Comparative Memory Map of Single-Chip Mode added
		10	2.5 Figure 2.2 Comparison of Option-Setting Memory Areas added
		23	2.7 Table 2.15 Comparison of Clock Generation Circuit Registers revised
		34	2.11 Table 2.24 Comparison of Vectors and Table 2.25 Comparison of Instructions for Returning from Exception Handling Routines added
		45	2.16 Table 2.36 Comparison of I/O Port Functions added
		47	2.17 Table 2.38 Comparison of Multiplexed Pin Assignments added
		52 to 58	2.17 Table 2.39 to Table 2.50 added, and Table 2.36 Comparison of Multi-Function Pin Controller Registers deleted
		80	2.24 Table 2.65 Comparison of 12-Bit A/D Converter Registers revised
		82	2.24 Table 2.66 Comparison of A/D Conversion Start Triggers Set in ADSTRGR Register added
		85	2.27 Table 2.69 Comparative Overview of Flash Memory revised
		94	4.2 Explanatory text added
		97	Related Technical Updates revised

General Precautions in the Handling of Microprocessing Unit and Microcontroller Unit Products

The following usage notes are applicable to all Microprocessing unit and Microcontroller unit products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Precaution against Electrostatic Discharge (ESD)

   A strong electrical field, when exposed to a CMOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop the generation of static electricity as much as possible, and quickly dissipate it when it occurs. Environmental control must be adequate. When it is dry, a humidifier should be used. This is recommended to avoid using insulators that can easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors must be grounded. The operator must also be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions must be taken for printed circuit boards with mounted semiconductor devices.
2. Processing at power-on

   The state of the product is undefined at the time when power is supplied. The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the time when power is supplied. In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the time when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the time when power is supplied until the power reaches the level at which resetting is specified.
3. Input of signal during power-off state

   Do not input signals or an I/O pull-up power supply while the device is powered off. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Follow the guideline for input signal during power-off state as described in your product documentation.
4. Handling of unused pins

   Handle unused pins in accordance with the directions given under handling of unused pins in the manual. The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of the LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible.
5. Clock signals

   After applying a reset, only release the reset line after the operating clock signal becomes stable. When switching the clock signal during program execution, wait until the target clock signal is stabilized. When the clock signal is generated with an external resonator or from an external oscillator during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Additionally, when switching to a clock signal produced with an external resonator or by an external oscillator while program execution is in progress, wait until the target clock signal is stable.
6. Voltage application waveform at input pin

   Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between V_{IL} (Max.) and V_{IH} (Min.) due to noise, for example, the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between V_{IL} (Max.) and V_{IH} (Min.).
7. Prohibition of access to reserved addresses

   Access to reserved addresses is prohibited. The reserved addresses are provided for possible future expansion of functions. Do not access these addresses as the correct operation of the LSI is not guaranteed.
8. Differences between products

   Before changing from one product to another, for example to a product with a different part number, confirm that the change will not lead to problems. The characteristics of a microprocessing unit or microcontroller unit products in the same group but having a different part number might differ in terms of internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

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(Rev.4.0-1 November 2017)

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