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Implementing Polyphase Filtering with the HSP50110 (DQT), HSP50210 (DCL) and the HSP43168 (DFF)

Introduction

Polyphase resampling filters are often used for timing adjustments in bit synchronizer loops. They are most commonly used at high baud rates where the sample rate to baud rate ratio (f_S/R_{Baud}) is low. The HSP50110 Digital Quadrature Tuner (DQT) and HSP50210 Digital Costas Loop (DCL) chips support NCO driven polyphase resampling filtering when the HSP43168 Dual FIR Filter (DFF) is inserted between them. This Application Note will address use of the DQT, DFF and DCL in the polyphase filtering configuration.

Polyphase Filtering Overview

In polyphase resamplers, the process ce, followed by a decimation to the desired lower rate. In practice, the process is done in a single step by changing the filter coefficients.

For example, in a 3/5 resampler, the input is interpolated by three using three sets of coefficient phases 0, 1, and 2. The interpolated signal is then decimated by 5, discarding 4/5 of the phases. The two steps are combined by computing three outputs for every five inputs. The resulting phases are:

$IOUT_0 = 0_A$;

$IOUT_1 = 2_B$;

$IOUT_1 = 1_D$;

$IOUT_2 = 0_F$;

$IOUT_3 = 0_F$;

as shown in Table 1. One can see by inspection, that the same result can be accomplished by providing unique sets of coefficients and applying the appropriate filter coefficient set to the input data at the desired output rate. A unique coefficient set is required for every interpolated phase of the data, in this example - 3.

DQT/DCL Resampling Capabilities

The DQT/DCL have four design elements which enable polyphase filtering to be accomplished:

1. A resampling NCO with carry output.
2. A latched resampling NCO phase word: SPH(4:0).
3. A programmable clock counter with carry output.
4. A strobe, SSTRB, latched synchronous to both the Resampler NCO carry and the programmable clock counter carry.

In the DQT/CDL implementation, the resampling ratio is controlled by the resampling NCO. The ratio can be both irrational and variable. The DQT is fixed (controlled by a counter) at an output sample rate faster than the desired rate. The resampling NCO and the DFF are used to choose when to compute the next output and which interpolation phase to use. The DFF can store up to 32 filter phases (coefficient sets). This gives a timing resolution of ~3% of a symbol time.

TABLE 1. INTERPOLATE BY 3 DECIMATE BY 5

INPUT DATA	INTERPOLATE BY 3 DATA	DECIMATE BY 5 DATA
I_A	0_A	$IOUT_0$
	1_A	
	2_A	
I_B	0_B	
	1_B	
	2_B	$IOUT_1$
I_C	0_C	
	1_C	
	2_C	
I_D	0_D	
	1_D	$IOUT_2$
	2_D	
I_E	0_E	
	1_E	
	2_E	
I_F	0_F	$IOUT_3$

The DQT resampling NCO is programmed for the desired output sample rate. When the NCO rolls over, it sets a flag internally so that the NCO's phase, SPH(4:0), is sampled and the SSTRB signal is asserted aligned with the next output sample. The SSTRB signal indicates that a FIR computation is required. The SPH(4:0) signals hold the NCO phase at the output sample time, indicating which filter interpolation coefficient set to use.

Polyphase Filter Design

The coefficients for the interpolation phases are generated by designing the filter at the interpolated rate (32x the input sample rate since there are five bits of phase represented in SPH(4:0)) with desired passband at <1X in input sample rate. With the DFF (without alternating the FWD and RVRS data), the prototype filter would have (32 phases x 8 taps) 256 taps. These taps are divided into the 32 filter phases by taking every 32nd sample and storing the result as coefficient sets 0 through 31. The first coefficient set would be C0, C32, C64, C96, C128, C160, C193, and C224. The last coefficient set would be C31, C63, C95, C127, C159, C192, C223, and C255. Note: Preadders in the DFF cannot be used since interpolation phase coefficients are asymmetric.

Decimation can be used if fewer interpolation phases are used - for example 16 coefficient phases can be realized by decimating by two. Because the resampling filter has only an 8 sample span (4 symbol), the short span yields relatively gradual transition band roll off, making it a poor shaping filter.

Implementing a Resampling Filter Using the DQT, DCL and the DFF

There are several configurations for implementing polyphase filtering using the HSP50110 (DQT) and HSP50210 (DCL) with external FIR Filters. Three distinct operational cases which are related to the selected input mode of the input controller of the DQT are: Normal, Gated, and Interpolated. This Application Note addresses only the Normal Input Mode, which has the $\overline{ENI}$ input to the DQT tied low. Bit position 1 of Control Address = 4 should be set high (1), selecting the gated mode. Hardwiring $\overline{ENI}$ will continuously gate the input.

Consider the implementation shown in Figure 1. The $\overline{SSTRB}$ and the SPH0-4 are used to gate the output of the filter address, the filter and the coefficients respectively. Note that the $\overline{SSTRB}$ must be delayed an amount equivalent to the filter, to properly gate the filter output into the HSP50210 via the $\overline{SYNC}$ input signal. Using the fine phase address bits in SPH0-4, 32 filter phases (coefficient sets) can be realized.

The clocking and control of the FIR using CLK, $\overline{SSTRB}$, $\overline{SYNC}$, DATARDY and SPH0-4 becomes critical. Figure 2 outlines the configuration required. It is very important to understand the relationship between the various DQT clock and control outputs.

CLK, the Programmable Divider, and the Re-Sampler NCO

The Programmable Divider must be configured to have CLK (the DQT input sample clock) as the clock source, rather than the Re-Sampler NCO carry out. To select CLK as the source, BIT-18 of DESTINATION ADDRESS 5 must be set to “1”. The Programmable Divider (Destination Address 5 Bit 6 to 17) is set to a value of 2^n, where n = 0, 1, 2, or 3. This generates a CIC Filter Clock that is CLK, CLK/2, CLK/4 or CLK/8, respectively. This clock will be gated to become the $\overline{DATARDY}$ signal, and will be used to gate the data into the external FIR Filter. This selection of the Programmable Divider determines the SPH_OUT_SEL settings for the shifter or the Re-Sampler Phase output bits. Table 2 details the required settings.

TABLE 2. DIVIDER AND PHASE SHIFT SETTINGS

PROGRAMMABLE DIVIDER	SHIFTER SETTINGS
0H	11
1H	10
3H	01
7H	00

Note that when the CIC Filter is clocked at CLK rate, no shifting occurs. Similarly, when the CIC Filter is clocked at CLK/8 rate, the shifter selects the phase bits fourth from the top as the MSB.

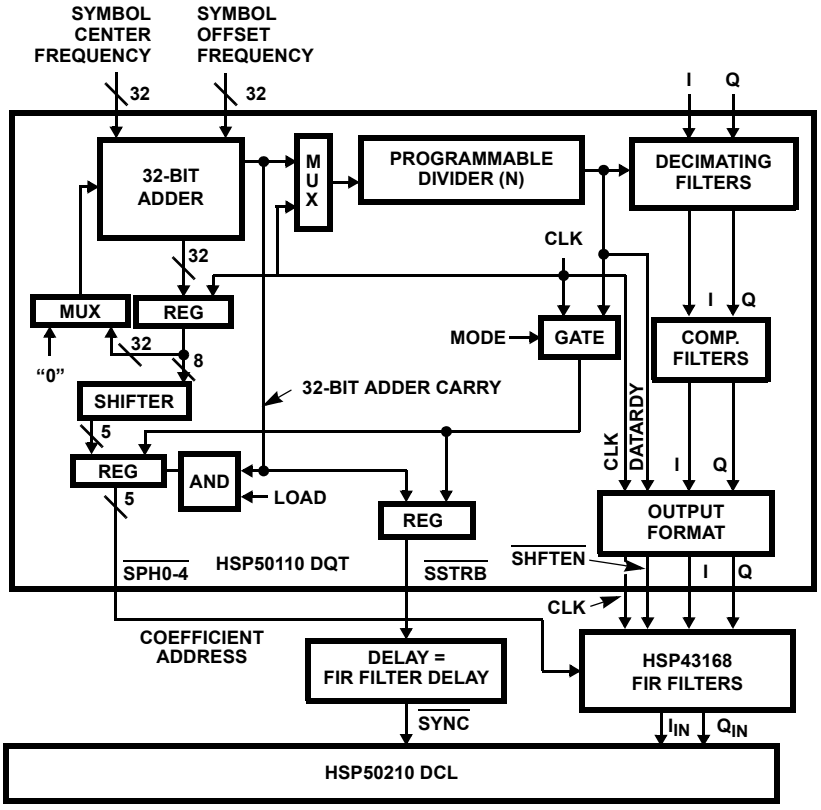

FIGURE 1. SIGNAL GENERATION FOR POLYPHASE FILTERING WITH HSP50110/HSP50210

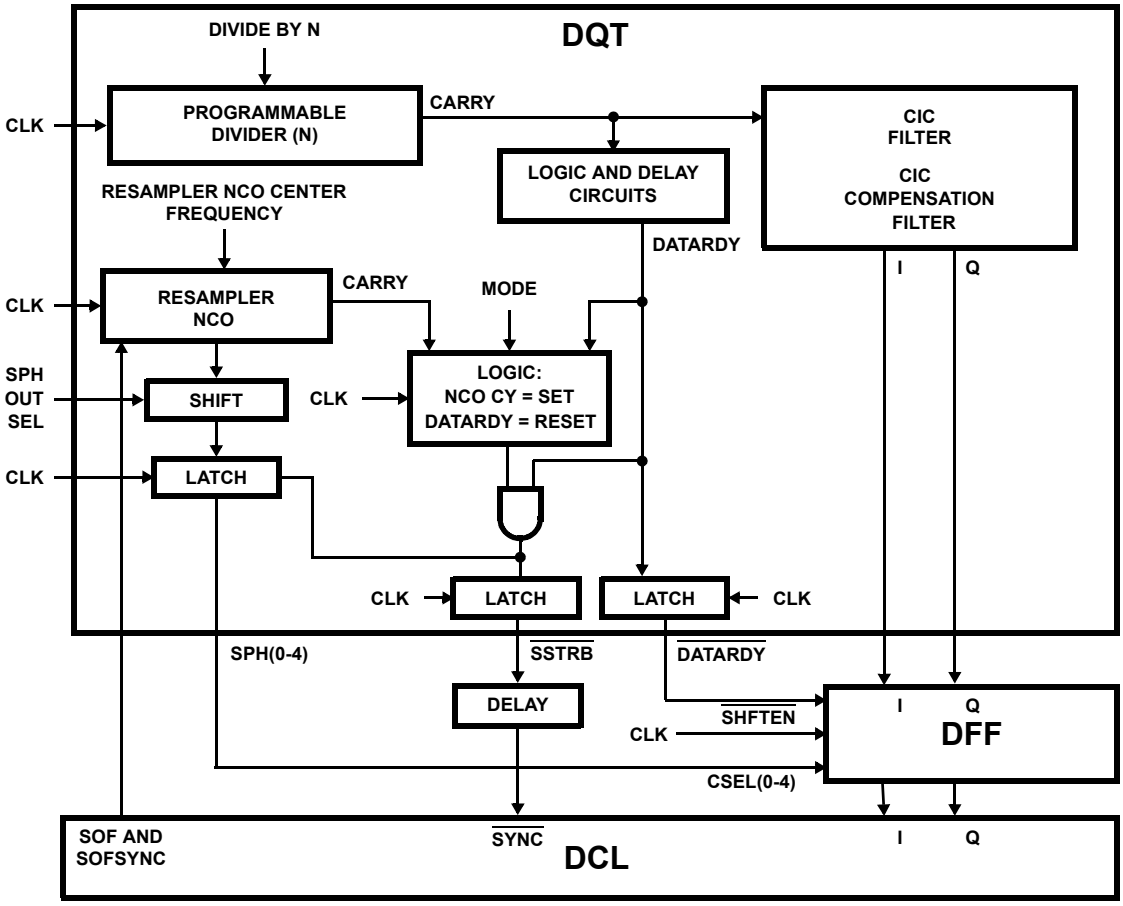

FIGURE 2. CLOCK AND CONTROL CONNECTIONS FOR POLYPHASE FILTERING

We desire finer phase resolution of a single decimated sample time. The Programmable Divider output, which is DQT CIC and DQT CIC compensation filter clock, is one positive (programmable positive or negative) pulse the width of one input sample clock period.

Note that the input sample clock (CLK) is the clock that should be used to clock the FIR Filter input. The $\overline{\text{DATARDY}}$ signal will be used to enable the FIR Filter input data sampling at the decimated rate.

The $\overline{\text{SSTRB}}$ Signal and the Re-Sampler Phase Output

The Re-Sampler NCO is programmed to the desired sample frequency of the DCL input. It is not connected to any clock hardware in the DQT. This NCO provides a carry output, which identifies the zero phase location. Additionally, 5 bits of phase resolution are provided. The $\overline{\text{SSTRB}}$ signal is the gated version of the carry out of the Re-Sampler NCO.

There are two selectable modes of operation for the $\overline{\text{SSTRB}}$ signal. The first mode is an asynchronous continuous mode, where the carry out is passed directly out of the chip without concern for the timing of the programmable counter. The carry out is updated with every CLK rising edge. Do not use the asynchronous continuous mode for this application.

The second mode synchronizes the carry output pulse with the rising clock edge out of the programmable counter. Program BIT POSITION 13 of DESTINATION ADDRESS = 6 to be “0”. This gating will “synchronize” the $\overline{\text{SSTRB}}$ and the 5 bits of sampler phase to the $\overline{\text{DATARDY}}$ signal. The synchronization occurs during gating and the gate will occasionally prevent the $\overline{\text{SSTRB}}$ and phase signals from their expected location, because they did not occur aligned with the $\overline{\text{DATARDY}}$ signal (during that output sample period).

The frequency of the Re-Sampler NCO carry out is equal to the programmed Re-Sampler NCO Center Frequency value multiplied by the frequency of CLK, scaled to 32 bits of resolution. If there is a Symbol Offset Frequency offset term, the sum of the offset and the center frequencies is multiplied by the frequency of CLK, and scaled to 32-bit resolution. This is detailed in Equation 1.

$$FCO = f_S \times (SCF + SOF)/2^{32} \quad \text{(EQ. 1)}$$

where FCO = the frequency of the Re-Sampler NCO carry out; f_S = the DQT input sampling frequency (CLK); SCF = the Sampler Center Frequency; SOF = Sampler Offset Frequency.

NOTES:

1. Because the SCF and SOF are both 32-bit words, the maximum value for the parenthetical expression is (FFFFFFFF + FFFFFFFF)/ 2^{32} = 2, which yields an erroneous value of greater than one for the multiplier of the sampling frequency f_S. This will cause the NCO to "rollover". If the sum of these two values (SCF + SOF) are kept less than 2^{32}, rollover will not be an issue.
2. If the value of SCF is a multiple of 2, then there will be no jitter on the carry out of the NCO (and thus, no jitter on the decimation filter clock or the $\overline{\text{DATARDY}}$ signal) so long as the SOF is zero. But as SOF adjusts the phase of the NCO, jitter on the order of one NCO clock will be introduced due to the non-integer value of the sampling frequency multiplier (SCF + SOF)/ 2^{32}.
3. If the value of SCF is not a multiple of 2, then there will be jitter on carry out of the NCO on the order of one NCO clock due to the non-integer value of the sampling frequency multiplier (SCF)/2^{32}. As the SOF signal adjusts the phase of the NCO, the jitter will remain, except on those rare moments when the sum of SOF and SCF is a multiple of 2.

Figure 3 shows the relationship to the NCO output values and the frequency of the NCO carry out signal. SPH (0-5) are 5 MSB's selected from the top 8 bits of the NCO output word. It is these bits that will be used to provide finer sampler phase resolution to address the coefficient sets in the FIR Filter. A programmable shifter selects which 5 of the 8 MSB's are used as the sampler phase output. Up to thirty two symbol phase values can be achieved with these 5 bits. The shifter scaling retains the 32 state resolution for most NCO frequencies. These 5 bits should be connected to the FIR Filter coefficient address lines.

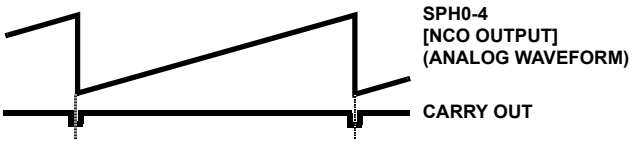

FIGURE 3. THE CARRY OUT SIGNAL RELATIONSHIP TO RESAMPLER PHASE BITS

The External FIR Filter

A FIR Filter is used to provide for the resampling of the DQT output with timing associated with the Re-Sampler NCO frequency. Figure 4 shows a typical filter response for this FIR Filter. The filter is designed as an Interpolate by 32/Decimate by n filter. The Interpolate by 32 is a "virtual" interpolation, since the part is being clocked at CLK rate, but enabled at the $\overline{\text{DATARDY}}$ rate. The FIR decimation rate is with respect to the $\overline{\text{DATARDY}}$ enable rate, which is the rate at which the FIR shifter is enabled. As shown in Figure 5, the filter must be designed to ensure that the RRC filter in the DCL chip is well within the flat passband of the FIR Filter and not corrupted by aliasing. The DFF will aid in, but not be, the primary shaping filter in the receive path.

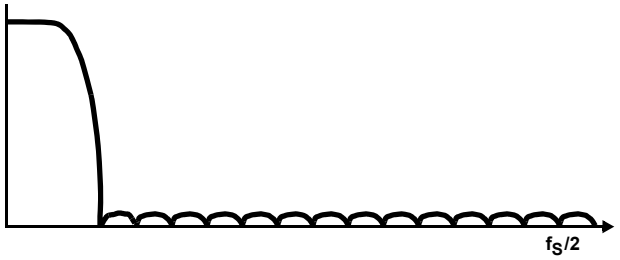

FIGURE 4. A TYPICAL DATA FILTER FOR THE FIR FILTER STRUCTURE

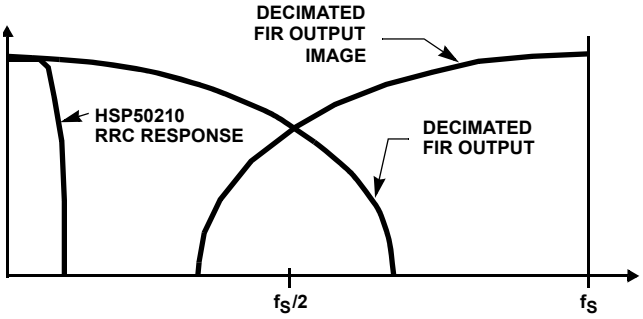

FIGURE 5. KEEPING THE DCL RRC FILTER WELL WITHIN THE FLAT PASSBAND

The HSP43168 dual FIR Filter provides the capability to provide both the I and Q filters in a single chip if a 8 tap symmetric filter meets the customer requirements. Each of the 8 taps is used with 32 coefficient sets to yield a total filter of up to 8 x 32 = 256 taps. Another way to look at this is that this provides 8 filter taps per phase. Each of the 32 filter coefficient sets should be programmed with coefficients for different phases of the response. A typical single phase filter response is shown in Figure 6. This response becomes just one of 32 phase responses that as a composite will represent the filter. The main lobe response of composite filter, with 32 phases, is shown in Figure 7.

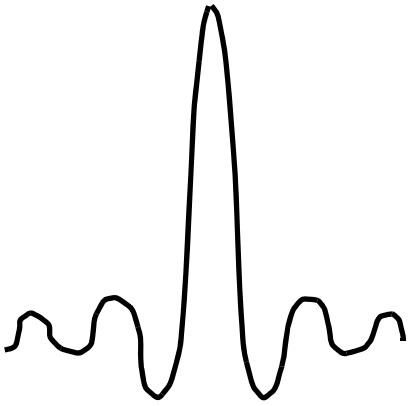

FIGURE 6. A TYPICAL SINGLE PHASE FILTER RESPONSE

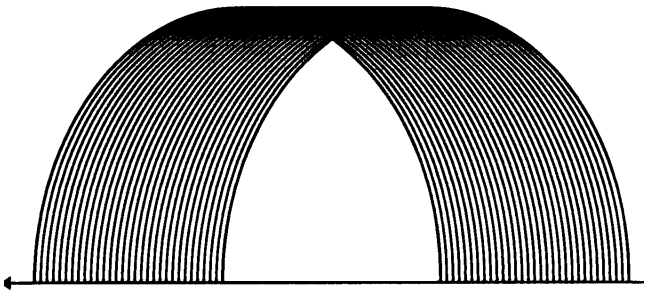

FIGURE 7. THE “MAIN LOBE” COEFFICIENT FILTER RESPONSE FOR A 32 PHASE FILTER

A Typical Single Phase Filter Response

The DCL will accept the output of the FIR Filter at the FIR decimated rate. These inputs will be enabled by the $\overline{\text{SYNC}}$ input, which is the $\overline{\text{SSTRB}}$ signal delayed by exact processing delay of the FIR Filter. Note that the $\overline{\text{SSTRB}}$ represents the “zero or start” phase sample of the 32 phases of the re-sampled rate clock. The designer must provide the input processing clock. This processing clock can be the CLK signal from the DQT, since the DCL inputs are enabled by $\overline{\text{SYNC}}$. Thus the effective sampling rate of the DCL is determined by the $\overline{\text{SSTRB}}$ ($\overline{\text{SYNC}}$) signal. The symbol loop filter output of the DCL, SOF and $\overline{\text{SOFSYNC}}$, should be routed to the DCL Resampler inputs of the same name.

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