System Design Using Digital-DC™ Devices

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Introduction

Using multiple Digital-DC devices in a system enables the use of many of the power management features built in to every ZL device. This application note describes the multi-device operation using several ZL2005 and ZL2105 Digital-DC devices. Refer to the individual product data sheets for details about using each product.

A system using multiple Digital-DC devices is shown in Figure 1. This application has an FPGA, a DSP, various logic, and DDR II memory all requiring separate power rails.

This application note will discuss many features and capabilities of the Digital-DC devices including sequencing, tracking, margining, phase spreading, and fault spreading.

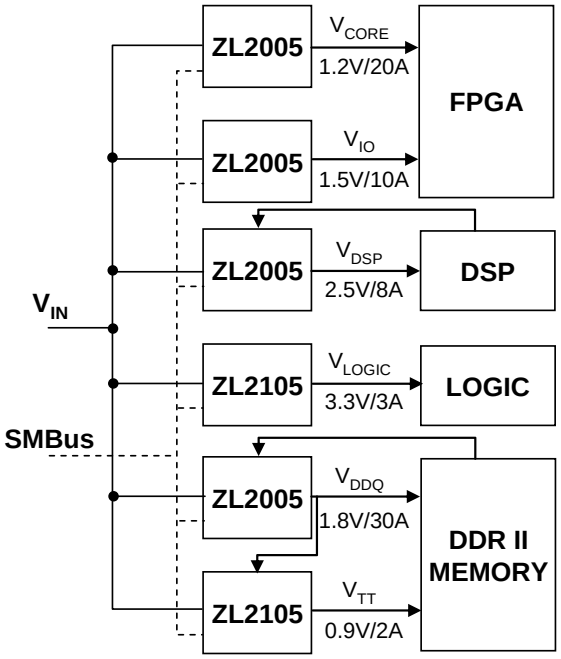

Figure 1. System Using Multiple Digital-DC Devices

Pin-strap and PMBus Operation

All Digital-DC devices are configurable through external pin-strap settings or over the serial interface using the PMBus communications protocol. Configuration settings are stored in internal Flash memory. Regardless of configuration method, the Digital-DC devices can operate with or without a system host processor. Many parameters can be configured using pin-straps. Using the SMBus to configure the device provides more granularity and more options for the device.

SMBus Communication

Digital-DC devices utilize the System Management Bus (SMBus) for device to device communication. The SMBus is a two-wire bus that supports multiple master and slave devices on the same bus. The details of the SMBus are described in the SMBus Specification [1] which is located at smbus.org.

There are inherent timing delays with the SMBus that need to be considered when using multiple Digital-DC devices in a system. The bus delay for commands to propagate over the SMBus is on the order of milliseconds. This delay is dependent on the amount of bus traffic. For example, it may take 3 – 4 milliseconds for a command to travel from a host controller down to a Digital-DC device at the end of the bus.

Selecting the SMBus Address

The SMBus spec has several addresses that are reserved and should not be used as device addresses. The range of addresses between 0x20 and 0x3F provide 32 unique addresses for devices. Digital-DC devices can be assigned addresses in this range. Note that the Zilker Labs POL Evaluation software currently recognizes device addresses in the range of 0x20 to 0x2F.

Certain features use the SMBus address to determine groups. These features include autonomous sequencing, fault spreading, and phase spreading. These features are discussed later in this document.

PMBus Commands

Digital-DC devices support PMBus commands that are used for power supply design. Supported commands are used to configure outputs, fault limits, fault responses, timing, monitoring, status, identification, control, and supervisory functions. Refer to AN2013 *PMBus Command Set* [5] for descriptions of the supported commands.

Sequencing

Power supply sequencing can be configured in several different ways.

Time based sequencing uses the power-up delay for each device to set the sequence order. All devices get their enable at the same time and their individual timers start. Once the delay time has elapsed, the output will ramp. Adjusting the delay and ramps times for each device will determine the sequencing order.

Event based sequencing uses a power good signal from one device to trigger the start of ramp for the next device in a sequence. The power good event must occur before the next device will ramp.

Time Based Sequencing

Time based sequencing allows supply output ramp-up and ramp-down sequencing based on the programmed soft start delay times. The ENABLE pins for all devices are tied together. The start-up and shut-down sequence is determined by the soft start delay settings.

Figure 2 shows four devices with soft start delays set to 10ms, 20ms, 30ms, and 40ms respectively.

Autonomous Sequencing

Digital-DC devices have the capability to sequence power rails simply by pin-strap configuration. In this mode, the SMBus is used as a private bus between devices in the sequencing group. No host controller is needed. Each Digital-DC device is pin-strap configured for its own output voltage, soft start ramp, power-up delay, clock configuration, and bus address as shown in Figure 3**Error! Reference source not found.**.

All devices within the sequencing group must have consecutive bus addresses within a sequencing address group. A sequencing address group consists of all devices whose addresses differ only by the 3 least significant bits of the address. For example, addresses 0x20, 0x25, and 0x27 are all within the same group. Addresses 0x1F, 0x20, and 0x28 are all in different groups.

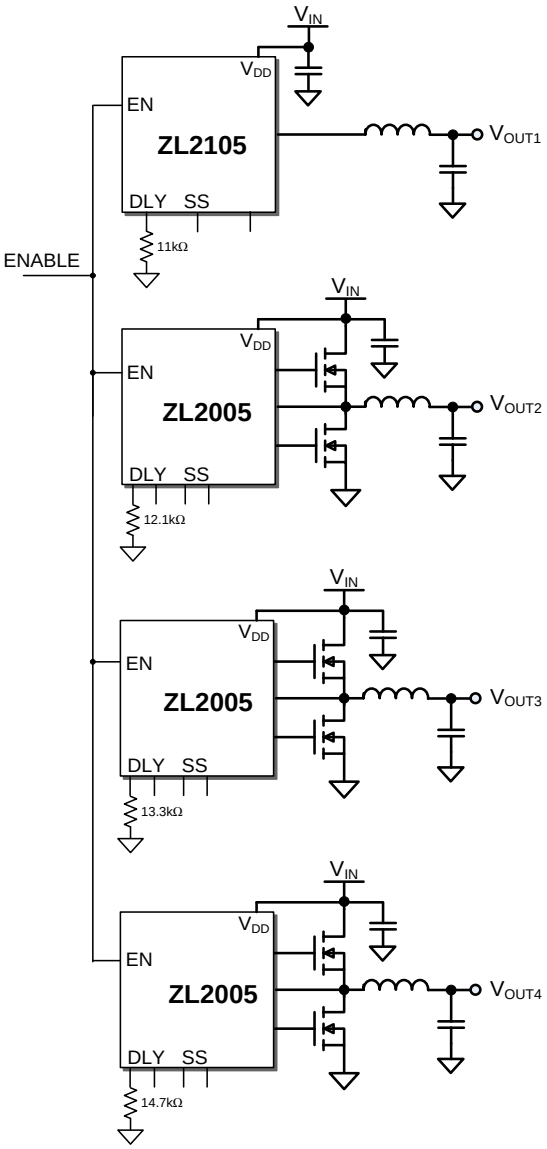

Figure 2. Time Based Sequencing

The sequencing order is determined by the bus address. The CFG pin is used to set the positioning of the device within the group as either the first, last, or middle device. The first Digital-DC device in an autonomous sequencing group is defined by being the lowest address within the group and the setting of the CFG pin. The last device in the sequence group is defined by the highest address in the group and the CFG pin.

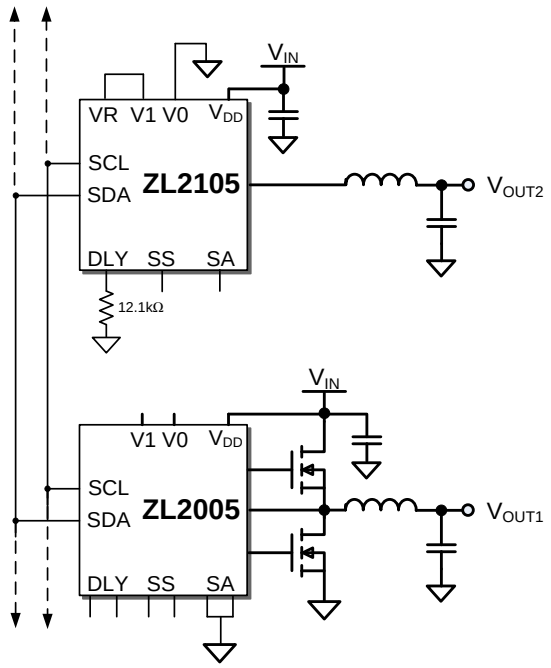

Figure 3. Autonomous Sequencing

All of the device's ENABLE pins are connected together and driven by a single logic source. The first device initiates the power up of the sequencing group following assertion of ENABLE. The last device initiates the power down of the sequencing group following de-assertion of ENABLE. In the event of a fault within the group, shut down will be communicated within the group and an immediate power down of all devices within the group will begin.

To change sequence order, only the device addresses and CFG pin setting need to be modified.

Event Based Sequencing

Event based sequencing of power rails is a method of sequencing where the output of one rail provides the signal to start another rail. This can be achieved in two ways:

1) The power good (PG) signal from one device is tied to the ENABLE of the next device and is repeated throughout the sequence.
2) The PMBus command SEQUENCE is used to configure the order of the devices in the sequence.

Connecting PG to ENABLE, as shown in Figure 4, provides the same order for start-up and shut-down. This method requires a hardware modification if the sequence order is changed.

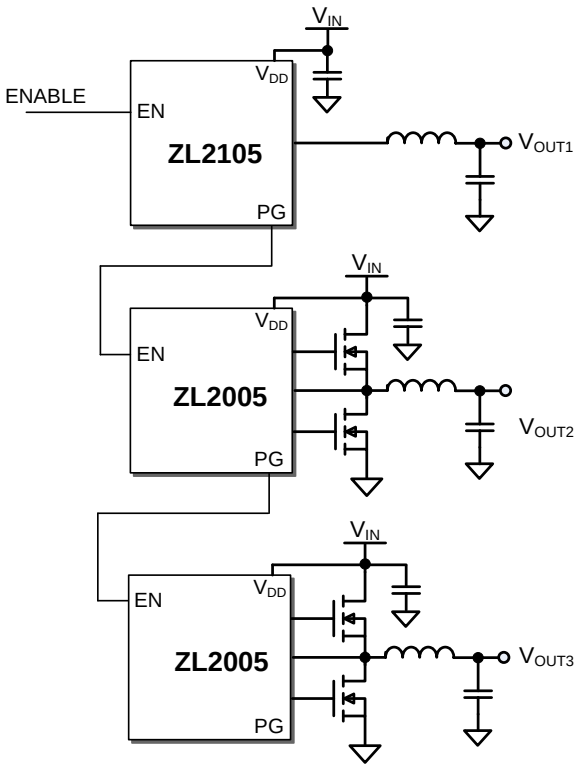

Figure 4. PG to EN Sequencing

Figure 5 illustrates the use of the PMBus to configure sequencing which provides more flexibility in that the sequence order is easily changed by modifying the SEQUENCE command on each device. There are no restrictions on the start-up and shut-down order. The devices communicate over the SMBus. If there is no SMBus controller in the system, this bus acts as a private, self monitoring bus among the Digital-DC devices.

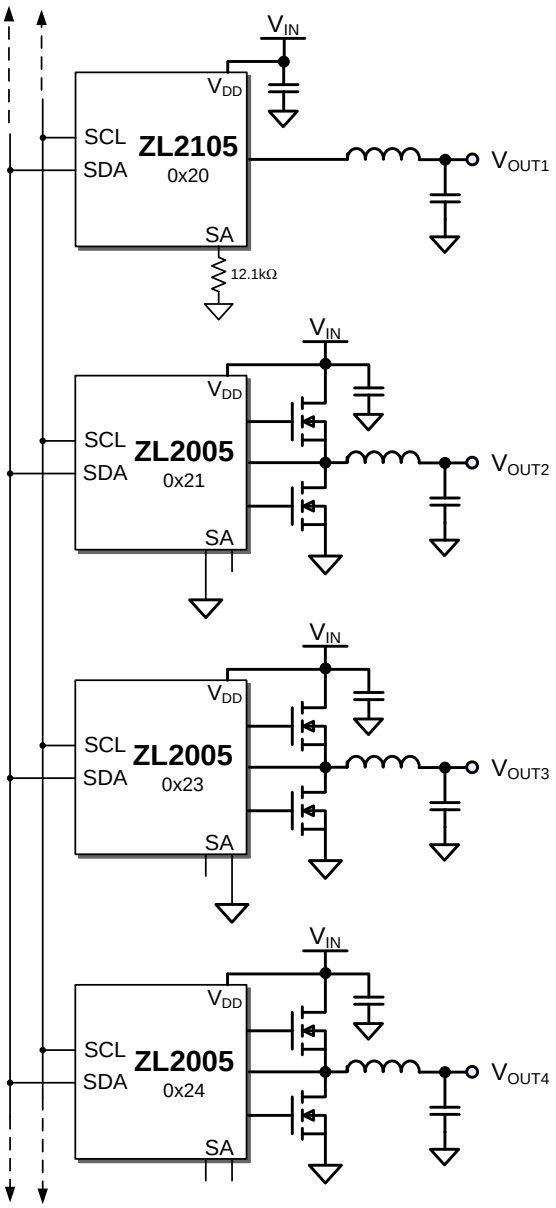

Figure 5. Event Based Sequencing

Configuring the clock and synchronization

The Digital-DC devices incorporate an internal phase locked loop (PLL) to clock the internal circuitry. Refer to the individual Digital-DC device's product data sheet for the specific switching frequency range. The PLL can be driven by an internal oscillator or driven from an external clock source connected to the SYNC pin. When using the internal oscillator, the SYNC pin can be configured as a clock output for use by other devices. The CFG pin is used to select the operating mode of the SYNC pin.

The SYNC pin can also be configured using PMBus commands. The Zilker Labs PoL Eval Software is a user friendly environment for configuring Digital-DC devices. Bits [6:5] of the USER_CONFIG command control the synchronization of the device. Bit 6 switches between auto-configure and setting SYNC to accept and external clock. Bit 5 sets the SYNC pin to an input or an output.

Table 1. USER_CONFIG bits for SYNC Control

Field	Purpose	Value	Description
6	SYNC utilization control	0	Auto-configure using the SYNC pin and FREQUENCY_SWITCH parameter
		1	Switch using the SYNC pin as an input
5	SYNC output control	0	Configure the SYNC pin as an input-only
		1	Drive the switch clock out of the SYNC pin when using the internal oscillator

Voltage Tracking

Voltage tracking allows one or more power rails to track another power rail's voltage.

Digital-DC devices include an analog input pin, VTRK, which is used to track another voltage supply. When the device is configured to the voltage tracking mode as shown in Figure 6, the voltage applied to the VTRK pin acts as the reference for the device's output regulation. Soft start settings are ignored and the output will take on the turn-on/turn-off characteristics of the reference voltage present at the VTRK pin. The delay setting is only used on the turn-off end of the tracking condition. The delay setting sets the timeout for the tracking voltage to turnoff in the event that the tracked voltage does not achieve zero volts. Certain tracking modes are also configurable to set the percentage of tracking and response to the power good signal.

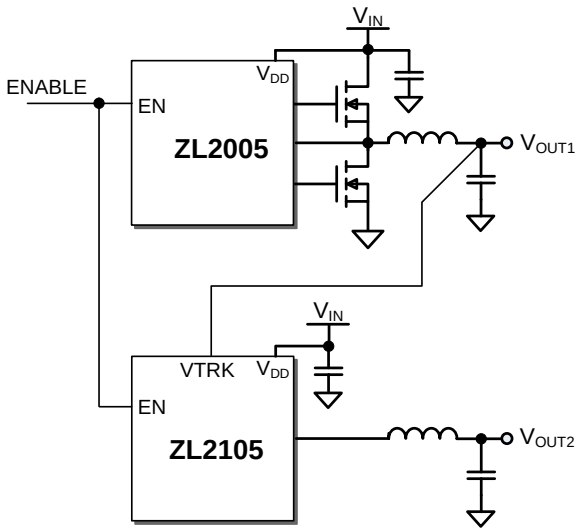

Figure 6. Voltage Tracking Configuration

In a tracking group, the Digital-DC device that is connected to any VTRK pin of another device is defined as the master device. This master device will control the ramp delay and ramp rate of all tracking devices and is not itself placed in the tracking mode. The master device is configured to the highest output voltage for the group since all other device output voltages are meant to track and never exceed the master device output voltage. A delay of at least 10 ms must be configured into the master device to allow the tracking devices to prepare their control loops for tracking following the ENABLE pin assertion. It is assumed for a tracking group, that all of the ENABLE pins are connected together and driven by a single logic source.

Tracking Configured by Pin-strap

The configuration of a master tracking Digital-DC device is set by pin-strap to achieve the desired output voltage with delay and ramp time set accordingly. The master device must have a pin-strap delay setting of at least 10 ms. The master device is not configured to be in the tracking mode.

The tracking devices are configured for tracking mode and will simply track the voltage of the master in the manner defined by the master device and its own configuration. The method for setting tracking mode by pin-strap varies depending on the Digital-DC device. Refer to the individual Digital-DC device data sheet for the tracking mode pin-strap definitions.

Tracking Configured by PMBus

The device address and the output voltage setting are the only two parameters that must be set by pin-strap when configuring a Digital-DC device by PMBus.

The SMBus address is set for each Digital-DC device by pins SA1 and SA0. The address for each device can be selected to fit a system's SMBus addressing scheme. The only restriction on device addressing within a tracking group is the consideration of a device's phase position when placed in a synchronized phase spreading tracking group. Even this restriction is not necessary if the PMBus command, INTERLEAVE, is used. Refer to AN2013, *PMBus Command Set* [5] for description of the INTERLEAVE command.

The PMBus commands for a tracking device are TRACK_CONFIG, TON_DELAY and VOUT_COMMAND.

The TRACK_CONFIG command is used to enable the tracking mode. This command also has bit fields that set options for the tracking mode. The tracking ratio bit sets the tracking percentage to either 50% or 100%. A 50% tracking ratio is typically selected unless the target voltage of the tracking device is set to more than 50% of the target voltage of the master device. In that case, the 100% tracking ratio must be used. The control of ramp-up behavior bit is a third settable option in the TRACK_CONFIG command. This bit sets the behavior of the output voltage during ramp-up in the case that the master voltage does not reach its target voltage and the tracking voltage does not reach the power good threshold. This option allows the tracking device to ramp-down without having to exceed the power good threshold first.

A master device in a tracking group must have its turn-on delay set to a minimum of 10 ms to provide time for initialization of the tracking devices following the enable event. The master tracking device sets the delay for the tracking group. The SS pins or the TON_DELAY command is used to set this delay.

The disable delay time for the tracking device must be set to the sum of the disable delay time and ramp down time for the master device plus 5 ms. This allows the tracking device to disable after tracking the master device to zero volts.

The output voltage of each rail can be set lower than the pin-strap setting by using the PMBus command VOUT_COMMAND. After storing the new output voltage settings using either STORE_USER or STORE_DEFAULT and then restoring the settings by a RESTORE command or power cycled on the Digital-DC device, the VOUT margins and fault thresholds will automatically be recalculated.

Tracking Example

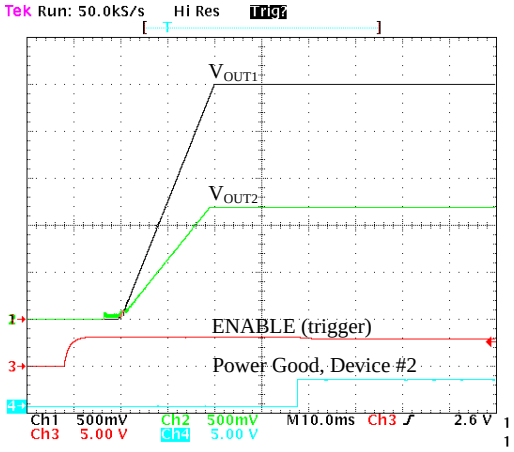

Figure 7. Enable Sequence

Figure 7 shows the scope is set to trigger on the ENABLE event. The ENABLE signal is the first to go high. The next signal to change is the beginning of the V_{OUT1} turn-on ramp since it has been configured to be the master device of the tracking group. It occurs 10 ms after ENABLE (DELAY1 set to 10 ms). The time of the V_{OUT1} ramp is 20 ms (soft start set to 20 ms). V_{OUT2} then begins tracking at 50% of V_{OUT1}. The ramp time for V_{OUT2} is identical to the ramp time of V_{OUT1}. Power Good 2 goes high 10ms after V_{OUT2} is above the power good threshold (by default, power good delay = soft start period = 20 ms).

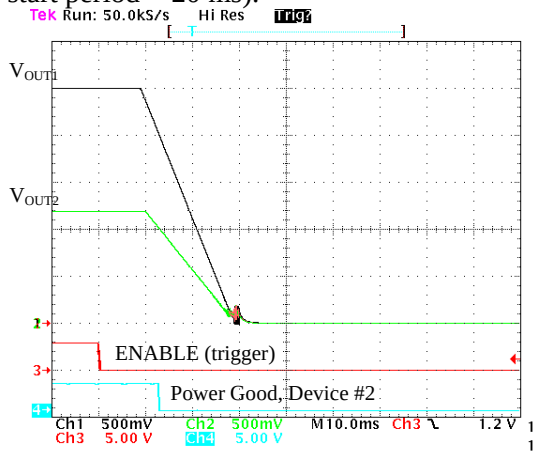

Figure 8. Disable Sequence

Figure 8 shows the scope is set to trigger on the ENABLE event. The ENABLE signal is the first to go low. The delay for V_{OUT1} to begin its turn off is set to 10 ms. The ramp time for V_{OUT1} is 20 ms (soft start set to 20 ms).The next signal to change is the V_{OUT2} turn off ramp since it has been configured to track 50% of V_{OUT1}. The next signal to change is the Power Good 2 which goes low after V_{OUT2} drops below the power good threshold.

Margining

Margining can be implemented by the margin pin or by SMBus. The margin pin is a three-state logic input. When left floating, the output of the device is the nominally set output voltage. Driving the margin pin high will cause the output to margin up and driving the pin low will margin down.

By default, the margin limits are set to ±5% of the set output voltage. These limits can be changed using the standard PMBus commands for margining, VOUT_MARGIN_HIGH and VOUT_MARGIN_LOW. The high margin value can be set at high as VOUT_MAX while the low margin can be set as low as 0 V.

Margining is controlled by the margin pin or through SMBus.

The PMBus command OPERATION is used to control margining. The device must be set up to use PMBus Enable which is configured in the ON_OFF_CONFIG command. Please refer to the PMBus specification for details on specific commands. [4]

Phase spreading

When multiple point of load converters share a common DC input supply, it is desirable to adjust the clock phase offset of each device such that not all devices start to switch simultaneously. Setting each converter to start its switching cycle at a different point in time can dramatically reduce input capacitance requirements and efficiency losses. Since the peak current drawn from the input supply is effectively spread out over a period of time, the peak current drawn at any given moment is reduced and the power losses proportional to the I_{RMS}^2 are reduced dramatically.

In order to enable phase spreading, all converters must be synchronized to the same switching clock. The CFG pin is used to set the configuration of the SYNC pin for each device as described the product data sheets.

Selecting the phase offset for the device is accomplished by selecting a device address according to the following equation:

Phase offset = device address x 45°

For example:

- A device address of 0x00 or 0x20 would configure no phase offset
- A device address of 0x01 or 0x21 would configure 45° of phase offset
- A device address of 0x02 or 0x22 would configure 90° of phase offset

The phase offset of each device may also be set to any value between 0° and 337.5° in 22.5° increments through the SMBus.

Management and Fault Spreading

Digital-DC devices monitor and detect the following fault conditions:

- Output over voltage (OV) and under voltage (UV)
- Input over voltage (OV) and under voltage lockout (UVLO)
- Output over current (OC)
- Over temperature (OT) of internal or external sense diode
- Communication bus

Responses to faults are described in the product data sheets. In general, the Digital-DC devices response to a fault is selectable to one of the following options:

1. Initiate a shutdown and attempt to restart an infinite number of times with a preset delay period between attempts.
2. Initiate a shutdown and attempt to restart a preset number of times with a preset delay period between attempts.
3. Continue operating for a given delay period, followed by shutdown if the fault still exists.
4. Continue operating through the fault (this could result in permanent damage to the power supply).
5. Initiate an immediate shutdown.

When a fault occurs on a given power rail, that rail communicates that a fault occurred to the rest of the Digital-DC devices in the group. The SMBus delay for a fault event to spread to the other group devices is on the order of a millisecond.

The fault broadcast occurs in address groups of up to eight Zilker Labs' Digital-DC devices. An address group consists of all devices whose addresses differ in only the three least significant bits of the address. For example, addresses 0x20, 0x25 and 0x27 are all within the same group. Addresses 0x1F, 0x20 and 0x28 are all in different groups. Devices in the same address group can broadcast fault spreading events with each other. The fault broadcast is not seen by devices in different groups.

A host controller or other Digital-DC devices can monitor for fault conditions by monitoring the SALRT pin, which will be asserted when a fault occurs.

The process between how a PMBus Host should respond to SALRT falling is as follows:

1. Digital-DC device has a fault and pulls SALRT Low
2. The PMBus Host detects that SALRT is now low, performs transmission with Alert Response Address to find which Digital-DC device is pulling SALRT low
3. The PMBus Host talks to the Digital-DC device that has pulled SALRT low. The actions that the host performs are up to the System Designer.

If multiple devices are faulting, SALRT will still be low after doing the above steps and will require transmission with the Alert Response Address repeatedly until all faults are cleared.

Please refer to Application Note 13 *PMBus Command Set* [5] for details on how to monitor specific parameters over the SMBus interface.

Conclusion

The Zilker Labs Digital-DC power conversion and power management devices provide a high level of flexibility and configurability to the design engineer. More information on these specific functions can be accessed in the documents referenced on the following page.

References

[1] *System Management Bus (SMBus) Specification*, Version 2.0, SMBus Org., August 3, 2000

[2] *ZL2005 Data Sheet*, Zilker Labs, Inc., 2007.

[3] *ZL2105 Data Sheet*, Zilker Labs, Inc., 2007.

[4] *PMBus Power System Management Protocol Specification Part II – Command Language*, Rev 1.1, System Management Interface Forum, inc., 2007.

[5] *AN2013 PMBus Command Set*, Zilker Labs, Inc., 2007.

Revision History

Date	Rev. #	
June 2007	1.0	Initial Release
May 4, 2009	AN2014.0	Assigned file number AN2014 to app note as this will be the first release with an Intersil file number. Replaced header and footer with Intersil header and footer. Updated disclaimer information to read “Intersil and it’s subsidiaries including Zilker Labs, Inc.” No changes to app note content.

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