

## RL78/G14, R8C/36M Group

Migration Guide from R8C to RL78:

R01AN3985EC0100

Rev.1.00

Timer RE to Real-Time Clock and Timer Array Unit

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### Introduction

This document describes how to migrate from timer RE in R8C/36M Group to the real-time clock (RTC) and the timer array unit (TAU) in RL78/G14 (This document is described in 64-pin package as an example).

### Target Device

RL78/G14, R8C/36M Group

When using this application note with other Renesas MCUs, careful evaluation is recommended after making modifications to comply with the alternate MCU.

Contents

1. Migration Method from R8C Family to RL78 Family ..... 3

2. Differences between RL78/G14 and R8C/36M Group..... 5

    2.1 Differences in Function Overview ..... 5

    2.2 Differences in Real-Time Clock Mode..... 6

    2.3 Differences in Output Compare Mode ..... 7

    2.4 Assigned I/O Pins..... 8

    2.5 Register Compatibility (Real-Time Clock) ..... 9

    2.6 Register Compatibility (Output Compare Mode)..... 11

3. How to Migrate Timer RE in this Sample Code ..... 12

4. Example of Migration from Real-Time Clock Mode..... 13

    4.1 Specifications ..... 13

    4.2 Operation Check Conditions..... 14

    4.3 Description of Hardware..... 14

        4.3.1 Hardware Configuration Example ..... 14

        4.3.2 List of Pins to be Used ..... 15

    4.4 Description of Software..... 15

        4.4.1 Operation Outline..... 15

        4.4.2 List of Option Byte Setting..... 17

        4.4.3 List of Functions ..... 17

        4.4.4 Function Specification ..... 17

        4.4.5 Flow Chart..... 18

5. Example of Migration from Output Compare Mode ..... 34

    5.1 Specifications ..... 34

    5.2 Operation Check Conditions..... 35

    5.3 Description of Hardware..... 35

        5.3.1 Hardware Configuration Example ..... 35

        5.3.2 List of Pins to be Used ..... 36

    5.4 Description of Software..... 36

        5.4.1 Operation Outline..... 36

        5.4.2 List of Option Byte Setting..... 38

        5.4.3 List of Functions ..... 38

        5.4.4 Function Specification ..... 38

        5.4.5 Flow Chart..... 39

6. Sample Code ..... 55

7. Reference Application Note..... 55

8. Reference Documents..... 55

## 1. Migration Method from R8C Family to RL78 Family

This application note explains how to achieve each mode (real-time clock mode and output compare mode) in timer RE of R8C/36M using RL78/G14.

Table 1.1 shows the mode in timer RE of R8C/36M Group. Table 1.2 shows the mode in Real-Time Clock (RTC) of RL78/G14, and Table 1.3 shows the mode in timer array unit of RL78/G14.

In R8C/36M Group, timer RE has an 8-bit counter with a 4-bit prescaler. Timer RE has two modes: real-time clock mode and output compare mode. In real-time clock mode, timer RE generates 1-second signal from fC4 and counts seconds, minutes, hours, and days of the week. In output compare mode, timer RE counts a count source and detects compare matches.

In RL78/G14, there are real-time clock and timer array unit. Real-time clock has counters of year, month, week, day, hour, minute, and second, and can count up to 99 years. Besides, the timer array unit has four 16-bit timers. Each 16-bit timer is called a channel and can be used as an independent timer. In addition, two or more "channels" can be used to create a high-accuracy timer. A count clock is counted by the TCRmn register. Sets the count value in the TDRmn register.

The same operation as that in real-time clock mode in timer RE of R8C/36M can be realized by using real-time clock of RL78/G14. The real-time clock has counters of year, month, week, day, hour, minute, and second, and can count up to 99 years. And real-time clock has constant-period interrupt function (period: 0.5 seconds, 1 second, 1 minute, 1 hour, 1 day, 1 month), alarm interrupt function (alarm: week, hour, minute) and pin output function of 1 Hz.

The same operation as that in output compare mode in timer RE of R8C/36M can be realized by using square wave output in TAU of RL78/G14. TOmn performs a toggle operation as soon as INTTMmn is generated, and outputs a square wave with a duty factor of 50%.

In this application note, as described in this chapter, explain the migration method for the two modes "real-time clock mode" and "output compare mode".

Remark m: Unit number (m = 0, 1), n: Channel number (n = 0 to 3)

**Table 1.1 Operation Mode of Timer RE in R8C/36M**

Timer RE in R8C/36M	
Mode	Function
Real-Time Clock Mode	Generate 1-second signal from fC4 and count seconds, minutes, hours, and days of the week.
Output Compare Mode	Count a count source and detect compare matches.

**Table 1.2 Corresponding Mode of RTC in RL78/G14**

RTC in RL78/G14	
Peripheral function	Function
Real-Time Clock	<ul style="list-style-type: none"> <li>• Has counters of year, month, week, day, hour, minute, and second, and can count up to 99 years.</li> <li>• Constant-period interrupt function (period: 0.5 seconds, 1 second, 1 minute, 1 hour, 1 day, 1 month)</li> <li>• Alarm interrupt function (alarm: week, hour, minute)</li> <li>• Pin output function of 1 Hz</li> </ul>

Table 1.3 Corresponding Mode of TAU in RL78/G14

TAU in RL78/G14	
Mode	Function
Interval timer	The timer array unit can be used as a reference timer that generates INTTMmn (timer interrupt) at fixed intervals.
<b>Square wave output</b>	<b>TOMn performs a toggle operation as soon as INTTMmn has been generated, and outputs a square wave with a duty factor of 50%.</b>
External event counter	The timer array unit can be used as an external event counter that counts the number of times the valid input edge (external event) is detected in the TImn pin.
Divider	A clock input from a timer input pin (TI00) is divided and output from an output pin (TOM0).
Input pulse interval measurement	The count value can be captured at the TImn valid edge and the interval of the pulse input to TImn can be measured.
Measurement of high-/low-level width of input signal	By starting counting at one edge of the TImn pin input and capturing the number of counts at another edge, the signal width (high-level width/low-level width) of TImn can be measured.
Delay counter	It is possible to start counting down when the valid edge of the TImn pin input is detected (an external event), and then generate INTTMmn (a timer interrupt) after any specified interval.
One-shot pulse output	By using two channels as a set, a one-shot pulse having any delay pulse width can be generated from the signal input to the TImn pin.
PWM output	Two channels can be used as a set to generate a pulse of any period and duty factor.
Multiple PWM output	By extending the PWM function and using multiple slave channels, many PWM waveforms with different duty values can be output.

## 2. Differences between RL78/G14 and R8C/36M Group

### 2.1 Differences in Function Overview

Table 2.1 lists the differences between timer RE in R8C/36M Group and RTC or TAU in RL78/G14.

Table 2.1 Differences

Item	R8C/36M Group Timer RE	RL78/G14 RTC	RL78/G14 TAU
Configuration	8-bit counter with a 4-bit prescaler	16-bit timer	16-bit timer <sup>Note 3</sup>
Count sources	f4, f8, f32, fC4 <sup>Note 1</sup>	fSUB, fIL <sup>Note 2</sup>	fCLK (between fCLK to fCLK/2 <sup>15</sup> )
Counters	<ul style="list-style-type: none"> <li>TRESEC register</li> <li>TREMIN register</li> <li>TREHR register</li> <li>TREWK register</li> </ul>	<ul style="list-style-type: none"> <li>SEC register</li> <li>MIN register</li> <li>HOUR register</li> <li>DAY register</li> <li>WEEK register</li> <li>MONTH register</li> <li>YEAR register</li> </ul>	TCRmn register
Count value setting	<ul style="list-style-type: none"> <li>TRESEC register</li> <li>TREMIN register</li> <li>TREHR register</li> <li>TREWK register</li> </ul>	<ul style="list-style-type: none"> <li>SEC register</li> <li>MIN register</li> <li>HOUR register</li> <li>DAY register</li> <li>WEEK register</li> <li>MONTH register</li> <li>YEAR register</li> </ul>	TDRmn register
Modes	<ul style="list-style-type: none"> <li>Real-time clock mode</li> <li>Output compare mode</li> </ul>	<ul style="list-style-type: none"> <li>Year, month, week, day, hour, minute and second counters</li> <li>Constant-period interrupt function <sup>Note 2</sup></li> </ul>	<ul style="list-style-type: none"> <li>Interval timer</li> <li>Square wave output</li> <li>External event counter</li> <li>Divider (channel 0 in unit 0 only)</li> <li>Input pulse interval measurement</li> <li>Measurement of high-/low-level width of input signal</li> <li>Delay counter</li> <li>One-shot pulse output <sup>Note 4</sup></li> <li>PWM output <sup>Note 4</sup></li> <li>Multiple PWM output <sup>Note 4</sup></li> </ul>
Count operations	Increment	Count up	<ul style="list-style-type: none"> <li>Count up <sup>Note 5</sup></li> <li>Count down <sup>Note 5</sup></li> </ul>
Output pin	TREO pin	RTC1HZ pin	TOMn pin
I/O pin selection (output port)	Yes	No	No
Coordination with event link controller (ELC)	No	Yes	Yes

Notes: 1. Only fC4 can be used in real-time clock mode.

2. The constant-period interrupt function can be used only when fIL is selected as the count source. Years, months, weeks, days, hours, minutes, and seconds can be counted only when fSUB is selected as the count source.

3. Channels 1 and 3 can operate as 8-bit timers.

4. These modes are available by using a master channel to link with slave channels.

5. Count operations depend on modes specified.

## 2.2 Differences in Real-Time Clock Mode

The operation of real-time clock in RL78/G14 corresponds to the real-time clock mode in R8C/36M Group. Table 2.2 lists the differences between real-time clock mode in R8C/36M Group and real-time clock in RL78/G14.

**Table 2.2 Differences between Timer RE (Real-Time Clock Mode) and Real-Time Clock (RTC)**

Item	R8C/36M Group (Timer RE (Real-Time Clock Mode))	RL78/G14 (Real-Time Clock (RTC) when $f_{RTC} = f_{SUB}$ )
Count source	fC4	$f_{SUB}$ <sup>Note 1</sup>
Count operation	Increment	Count up
Count start condition	1 (count starts) is written to TSTART bit in TRECR1 register	1 (starts counter operation) is written to RTCE bit in RTCC0 register
Count stop condition	0 (count stops) is written to TSTART bit in TRECR1 register	0 (stops counter operation) is written to RTCE bit in RTCC0 register
Interrupt request generation timing	<p>Select any one of the following:</p> <ul style="list-style-type: none"> <li>• Update second data</li> <li>• Update minute data</li> <li>• Update hour data</li> <li>• Update day of week data</li> <li>• When day of week data is set to 000b (Sunday)</li> </ul>	<ul style="list-style-type: none"> <li>• Once every 0.5 seconds (synchronized with counting up seconds)</li> <li>• Once per second (same time as counting up seconds)</li> <li>• Once per minute (at 00 seconds every minute)</li> <li>• Once per hour (at 00 minutes and 00 seconds every hour)</li> <li>• Once per day (at 00 hours, 00 minutes, and 00 seconds every day)</li> <li>• Once per month (on the 1st of every month at 00 hours, 00 minutes, and 00 seconds a.m.)</li> </ul>
Pin function	Programmable I/O ports or output of the TREO pin (f2, fC, f4, f8 or, 1Hz)	Programmable I/O ports or output of the RTC1HZ pin (1Hz)
Read from timer	When reading TRESEC, TREMIN, TREHR, or TREWK register, the count value can be read. The values read from registers TRESEC, TREMIN, and TREHR are represented by the BCD code.	Read the counter after setting 1 to RWAIT first. When reading SEC, MIN, HOUR, WEEK, DAY, MONTH or YEAR register, the count value can be read. The values read from registers SEC, MIN, HOUR, WEEK, DAY, MONTH and YEAR are represented by the BCD code.
Write to timer	When bits TSTART and TCSTF in the TRECR1 register are set to 0 (timer stops), the value can be written to registers TRESEC, TREMIN, TREHR, and TREWK. The values written to registers TRESEC, TREMIN, and TREHR are represented by the BCD codes.	Write the counter after setting 1 to RWAIT first. When bit RWAIT in the RTCC1 register is set to 1 (stops SEC to YEAR counters), the value can be written to registers SEC, MIN, HOUR, WEEK, DAY, MONTH and YEAR. The values written to registers SEC, MIN, HOUR, WEEK, DAY, MONTH and YEAR are represented by the BCD code.
Selectable functions	<ul style="list-style-type: none"> <li>• 12-hour mode/24-hour mode switch function</li> <li>• TREO pin select function</li> </ul> P0_4 or P6_0 is selected by the TROSEL0 bit in the TIMSR register.	<ul style="list-style-type: none"> <li>• 12-hour mode/24-hour mode switch function</li> </ul>

Notes: 1. Years, months, weeks, days, hour, minutes, and seconds can be counted only when  $f_{SUB}$  is selected as the count source.

## 2.3 Differences in Output Compare Mode

The operation of square wave output in RL78/G14 corresponds to the output compare mode in R8C/36M Group. Table 2.3 lists the differences between output compare mode in R8C/36M Group and operation as square wave output in RL78/G14.

**Table 2.3 Differences between Output Compare Mode and Operation as Square Wave Output**

Item	R8C/36M Group (Timer RE (Output Compare Mode))	RL78/G14 (TAU (Square Wave Output))
Count sources	f4, f8, f32, fC4	f <sub>TCLK</sub> (between f <sub>CLK</sub> to f <sub>CLK</sub> /2 <sup>15</sup> )
Count operations	<ul style="list-style-type: none"> <li>• Increment</li> <li>• When the 8-bit counter content matches with the TREMIN register content, the value returns to 00H and count continues. The count value is held while count stops.</li> </ul>	<ul style="list-style-type: none"> <li>• Count down</li> <li>• When TCRmn = 0000H, the TCRmn register loads the value of the TDRmn register again. After that, the same operation is repeated.</li> </ul>
Count period	<ul style="list-style-type: none"> <li>• When RCS2 = 0 (4-bit counter is not used) 1/f<sub>i</sub> × 2 × (n+1)</li> <li>• When RCS2 = 1 (4-bit counter is used) 1/f<sub>i</sub> × 32 × (n+1)</li> </ul> f <sub>i</sub> : Frequency of count source n: Setting value of TREMIN register	<ul style="list-style-type: none"> <li>• Period of square wave output from TOMn = Period of count clock × (Set value of TDRmn + 1) × 2</li> <li>• Frequency of square wave output from TOMn = Frequency of count clock / {(Set value of TDRmn + 1) × 2}</li> </ul>
Count start condition	1 (count starts) is written to the TSTART bit in the TRECR1 register	1 is written to the TSmn, TSHm1, or TSHm3 bit in the TSm register
Count stop conditions	0 (count stops) is written to the TSTART bit in the TRECR1 register	1 is written to the TTmn, TTHm1, or TTHm3 bit in the TTm register
Interrupt request generation timing	When the 8-bit counter content matches with the TREMIN register content	When TCRmn = 0000H, INTTMmn is output and TOMn is toggled at the next count clock.
Output pin functions	Select any one of the following: <ul style="list-style-type: none"> <li>• Programmable I/O ports</li> <li>• Output f2, fC, f4, or f8</li> <li>• Compare output</li> </ul>	Select any one of the following: <ul style="list-style-type: none"> <li>• Programmable I/O ports</li> <li>• Square wave output</li> </ul>
Read from timer	When reading the TRESEC register, the 8-bit counter value can be read. When reading the TREMIN register, the compare value can be read.	Read the TCRmn register
Write to timer	Writing to the TRESEC register is disabled. When bits TSTART and TCSTF in the TRECR1 register are set to 0 (timer stops), writing to the TREMIN register is enabled.	Write to the TDRmn register
Selectable functions	<ul style="list-style-type: none"> <li>• Select use of 4-bit counter</li> <li>• Compare output function</li> </ul> Every time the 8-bit counter value matches the TREMIN register value, TREO output polarity is reversed. The TREO pin outputs "L" after reset is deasserted and the timer RE is reset by the TRERST bit in the TRECR1 register. Output level is held by setting the TSTART bit to 0 (count stops). <ul style="list-style-type: none"> <li>• TREO pin select function</li> </ul> P0_4 or P6_0 is selected by the TREOSEL0 bit in the TIMSR register.	<ul style="list-style-type: none"> <li>• Whether the timer interrupt is generated when counting is started</li> <li>• Output pin level when pulse output is started</li> </ul>

Remark m: Unit number (m = 0, 1), n: Channel number (n = 0 ~ 3)

**2.4 Assigned I/O Pins**

Table 2.4 lists the I/O pins assigned for use in R8C/36M Group.

**Table 2.4 R8C/36M Group I/O Pins**

Pin Name	Assigned Pins	I/O
TREO	P0_4, or P6_0	Output

Table 2.5 and Table 2.6 list the I/O pins assigned for use in RL78/G14.

**Table 2.5 RL78/G14 I/O Pins (Real-Time Clock) (64-pin products)**

Pin Name	Assigned Pins	I/O
RTC1HZ	P30	Output

**Table 2.6 RL78/G14 I/O Pins (TAU) (64-pin products)**

Unit Number	Target Channel	Pin Name	Assigned Pins	I/O
Unit 0	Channel 0	TI00	P00	Input
		TO00	P01	Output
	Channel 1	TI01	P16	Input
		TO01	P16	Output
	Channel 2	TI02	P17	Input
		TO02	P17	Output
	Channel 3	TI03	P31	Input
		TO03	P31	Output

## 2.5 Register Compatibility (Real-Time Clock)

Register compatibilities between timer RE in R8C/36M Group and real-time clock in RL78/G14 are listed in Table 2.7 and Table 2.8.

**Table 2.7 Register Compatibility (Real-Time Clock) (1/2)**

Item	R8C/36M Group (Timer RE (Real-Time Clock Mode))	RL78/G14 (Real-Time Clock (RTC) when $f_{RTC} = f_{SUB}$ )
Clock supply to the peripheral hardware	N/A	• PER0 register RTCCEN bit
Second count	• TRESEC register	• SEC register
Count data register	• TRESEC register	N/A
Minute count	• TREMIN register	• MIN register
Compare data register	• TREMIN register	• RTCC0 register Bits CT0 to CT2
Hour count	• TREHR register	• HOUR register
Day of week count	• TREWK register Bits WK0 to WK2	• WEEK register
Busy flag	• BSY bit in the TRESEC register • BSY bit in the TREMIN register • BSY bit in the TREHR register • BSY bit in the TREWK register	N/A
Count status flag	• TRECR1 register TCSTF bit	• RTCC1 register RWST bit
TREO pin output enable	• TRECR1 register TOENA bit	N/A
Interrupt request timing	• TRECR1 register INT bit	N/A
Reset setting	• TRECR1 register TRERST bit	N/A
A.m./p.m. select	• TRECR1 register PM bit	N/A
Operating mode select	• TRECR1 register H12_H24 bit	• RTCC0 register AMPM bit
Count start	• TRECR1 register TSTART bit	• RTCC0 register RTCE bit
Periodic interrupt triggered every second enable/disable	• TRECR2 register SEIE bit	• RTCC0 register Bits CT0 to CT2
Periodic interrupt triggered every minute enable/disable	• TRECR2 register MNIE bit	• RTCC0 register Bits CT0 to CT2
Periodic interrupt triggered every hour enable/disable	• TRECR2 register HRIE bit	• RTCC0 register Bits CT0 to CT2
Periodic interrupt triggered every day enable/disable	• TRECR2 register DYIE bit	• RTCC0 register Bits CT0 to CT2
Periodic interrupt triggered every week enable/disable	• TRECR2 register WKIE bit	N/A

**Table 2.8 Register Compatibility (Real-Time Clock) (2/2)**

Item	R8C/36M Group (Timer RE (Real-Time Clock Mode))	RL78/G14 (Real-Time Clock (RTC) when $f_{RTC} = f_{SUB}$ )
Compare match interrupt enable	• TRECR2 register COMIE bit	N/A
Count source select	• TRECSR register Bits RCS0 and RCS1	• OSMC register WUTMMCK0 bit
Use of 4-bit counter	• TRECSR register RCS2 bit	N/A
Real-time clock mode select	• TRECSR register RCS3 bit	N/A
Clock output select	• TRECSR register Bits RCS4 and RCS5	N/A
TREO pin select	• TIMSR register TREOSEL0 bit	N/A
RTC1HZ output control	N/A	• RTCC0 register RCLOE1 bit
Constant-period (0.5 second) interrupt enable/disable	N/A	• RTCC0 register Bits CT0 to CT2
Constant-period (month) interrupt enable/disable	N/A	• RTCC0 register Bits CT0 to CT2
Alarm control	N/A	• RTCC1 register WALE bit
Alarm interrupt (INTRTC) function control	N/A	• RTCC1 register WALIE bit
Alarm detection status flag	N/A	• RTCC1 register WAFG bit
Constant-period interrupt status flag	N/A	• RTCC1 register RIFG bit
RTC wait control	N/A	• RTCC1 register RWAIT bit
Day count	N/A	• DAY register
Month count	N/A	• MONTH register
Year count	N/A	• YEAR register
Watch error correction timing setting	N/A	• SUBCUD register DEV bit
Watch error correction value setting	N/A	• SUBCUD register F6 bit
Alarm minute setting	N/A	• ALARMWM register
Alarm hour setting	N/A	• ALARMWH register
Alarm day of week setting	N/A	• ALARMWW register

**2.6 Register Compatibility (Output Compare Mode)**

Register compatibilities between timer RE in R8C/36M Group and TAU in RL78/G14 are listed in Table 2.9.

**Table 2.9 Register Compatibility (Output Compare Mode)**

Item	R8C/36M Group (Timer RE (Output Compare Mode))	RL78/G14 (TAU (Square Wave Output))
Clock supply to the peripheral hardware	N/A	• PER0 register Bits TAU0EN and TAU1EN
Count data register	• TRESEC register	• Registers TCRmn, TDRmn (TCRmn: read-only, TDRmn: read/write)
Compare data register	• TREMIN register	• Registers TCRmn, TDRmn (TCRmn: read-only, TDRmn: read/write)
Count status flag	• TRECR1 register TCSTF bit	• TEm register Bits TE mn, TEHm1, TEHm3 <sup>Note 1</sup>
TREO pin output enable	• TRECR1 register TOENA bit	• TOEm register TOEmn bit
Interrupt request timing	• TRECR1 register INT bit	N/A
Reset setting	• TRECR1 register TRERST bit	N/A
Compare match interrupt enable	• TRECR2 register COMIE bit	• Registers MK0H, MK1L, MK1H, MK2L and MK2H Bits TMMKmn or TMMKmnH
Operating mode select	• TRECSR register RCS3 bit	• TMRmn register Bits MDmn1 to MDmn3
Count start	• TRECR1 register TSTART bit	• TSm register Bits TSmn, TSHm1, TSHm3 <sup>Note 2</sup>
Count source select bit	• TRECSR register Bits RCS0 to RCS1	• TPSm register • TMRmn register Bits CKSmn0, CKSmn1, CCSmn
4-bit counter select bit	• TRECSR register RCS2 bit	N/A
Clock output select bit	• TRECSR register Bits RCS4 to RCS6	N/A
TREO pin select pin	• TIMSR register TREOSEL0 bit	• PMCxx register • PMxx register • Pxx register

Notes: 1. When channels 1 and 3 are in 8-bit timer mode, bits TEHm1 and TEHm3 indicate whether the higher 8-bit timer is enabled or stopped.

2. When channels 1 and 3 are in 8-bit timer mode, bits TSHm1 and TSHm3 are triggers to enable operation of (start) the higher 8-bit timer.

### 3. How to Migrate Timer RE in this Sample Code

In this sample program, the operation of timer RE of R8C/36M group is realized with RL78/G14 by the method shown in Table 3.1.

For detailed contents of the sample program, please refer to "4. Example of Migration from Real-Time Clock Mode" ~ "5. Example of Migration from Output Compare Mode".

**Table 3.1 How to migrate from R8C/36M Group to RL78/G14 in this sample program**

<b>Timer RE in R8C/36M</b>	<b>TAU in RL78/G14</b>
<b>Peripheral function</b>	<b>Peripheral function</b>
Timer RE (real-time clock mode)	Real-time clock (RTC)
Timer RE (output compare mode)	TAU (square wave output)

## 4. Example of Migration from Real-Time Clock Mode

### 4.1 Specifications

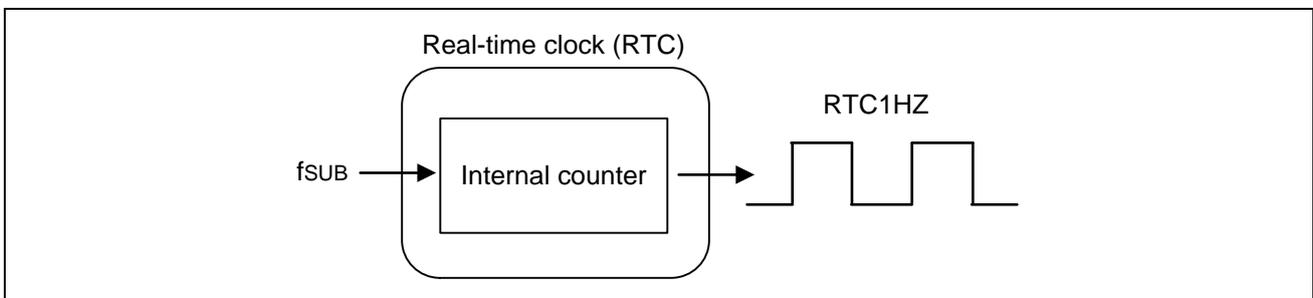
The same operation as that in real-time clock mode in timer RE of R8C/36M can be realized by using real-time clock of RL78/G14. The real-time clock has the following functions.

- Having counters of year, month, week, day, hour, minute, and second, and can count up to 99 years.
- Constant-period interrupt function (period: 0.5 seconds, 1 second, 1 minute, 1 hour, 1 day, 1 month)
- Alarm interrupt function (alarm: week, hour, minute)
- Pin output function of 1 Hz

Table 4.1 lists the peripheral functions to be used and their uses (example of migration from real-time clock mode), and Figure 4.1 shows the operation overview (example of migration from real-time clock mode).

**Table 4.1 Peripheral Functions to be Used and Their Uses**  
(Example of Migration from Real-Time Clock Mode)

Peripheral Function	Use
Real-time clock (RTC)	Use to generate RTC interrupts (INTRTC).



**Figure 4.1 Operation Overview (Example of Migration from Real-Time Clock Mode)**

## 4.2 Operation Check Conditions

The sample code described in this chapter has been checked under the conditions listed in the table below.

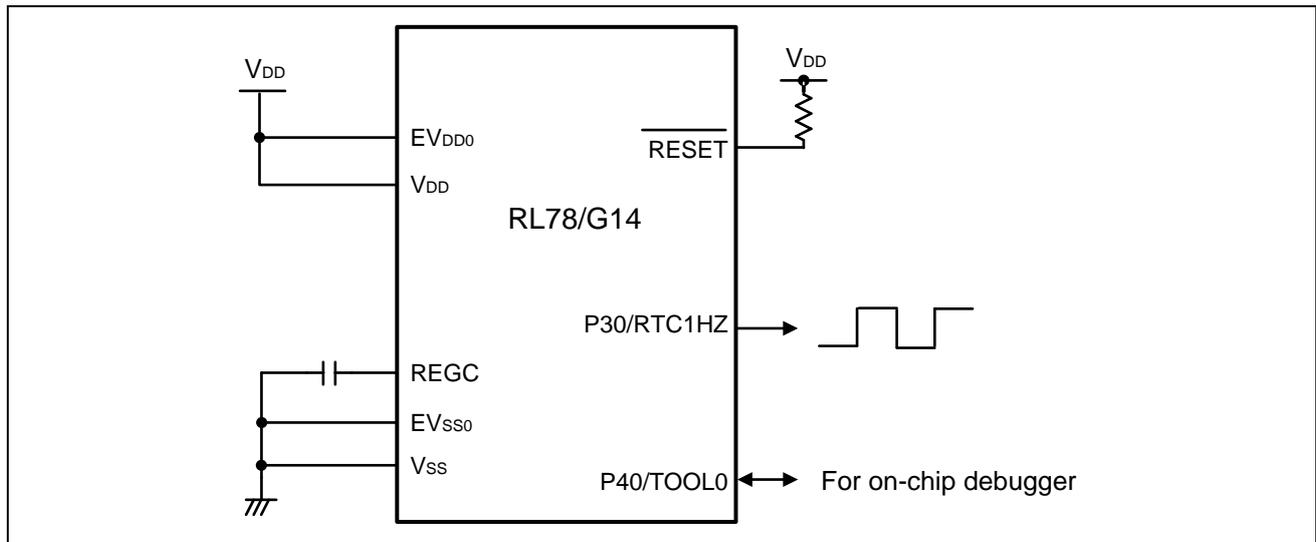
**Table 4.2 Operation Check Conditions**

Item	Description
Microcontroller used	RL78/G14 (R5F104LEAFB)
Operating frequency	High-speed on-chip oscillator (HOCO) clock: 32 MHz CPU/peripheral hardware clock: 32 MHz RTC operation clock (f <sub>SUB</sub> ): 32.768 kHz (typical)
Operating voltage	5.0V (can run on a voltage range of 2.9 V to 5.5 V.) LVD operation (V <sub>LVD</sub> ): Reset mode 2.81 V (2.76 V to 2.87 V)
Integrated development environment (CS+)	CS+ V6.00.00 from Renesas Electronics Corp.
C compiler (CS+)	CC-RL V1.05.00 from Renesas Electronics Corp.
Integrated development environment (e <sup>2</sup> studio)	e <sup>2</sup> studio V6.0.0 from Renesas Electronics Corp.
C compiler (e <sup>2</sup> studio)	CC-RL V1.05.00 from Renesas Electronics Corp.

## 4.3 Description of Hardware

### 4.3.1 Hardware Configuration Example

Figure 4.2 shows an example of hardware configuration that is used for this chapter.



**Figure 4.2 Hardware Configuration**

- Cautions:
1. The purpose of this circuit is only to provide the connection outline and the circuit is simplified accordingly. When designing and implementing an actual circuit, provide proper pin treatment and make sure that the hardware's electrical specifications are met (connect the input-only ports separately to V<sub>DD</sub> or V<sub>SS</sub> via a resistor).
  2. Connect any pins whose name begins with EV<sub>SS</sub> to V<sub>SS</sub> and any pins whose name begins with EV<sub>DD</sub> to V<sub>DD</sub>, respectively.
  3. V<sub>DD</sub> must be held at not lower than the reset release voltage (V<sub>LVD</sub>) that is specified as LVD.

### 4.3.2 List of Pins to be Used

Table 4.3 lists the pins to be used and their functions.

**Table 4.3 Pins to be Used and Their Functions**

Pin Name	I/O	Description
P30/RTC1HZ	Output	Real-time clock correction clock (1 Hz) output.

## 4.4 Description of Software

### 4.4.1 Operation Outline

When a subsystem clock ( $f_{SUB} = 32.768$  kHz) is selected as the operation clock of the real-time clock, the count of year, month, week, day, hour, minutes and second can be performed. And RTC1HZ can output 1 Hz.

Table 4.4 lists the peripheral functions to be used and their uses. Figure 4.3 shows the real-time clock and its interrupt operation.

(1) Initialize the RTC.

<Conditions for setting>

Selects the subsystem clock ( $f_{SUB}$ ) as the RTC operating clock.

Presents the time in 24-hour system.

Sets the selection of fixed-cycle interruption (INTRTC) at a time (simultaneous with second count-up) every second.

Initializes the current date and time to 2017/1/1 (Sunday) 00:00:00.

Sets RTC1HZ pin to output mode.

Enables output of the RTC1HZ pin (1 Hz).

(2) Sets "1" (starts counter operation) to RTCE bit of RTCC0 register to start the count of RTC.

(3) RTC generates a fixed-cycle (1 s) interrupt per second. And 1 Hz is output from the RTC1HZ pin.

Table 4.4 Peripheral Functions to be Used and Their Uses

Peripheral Function	Use
Real-time clock	Perform the count of year, month, week, day, hour, minutes and second

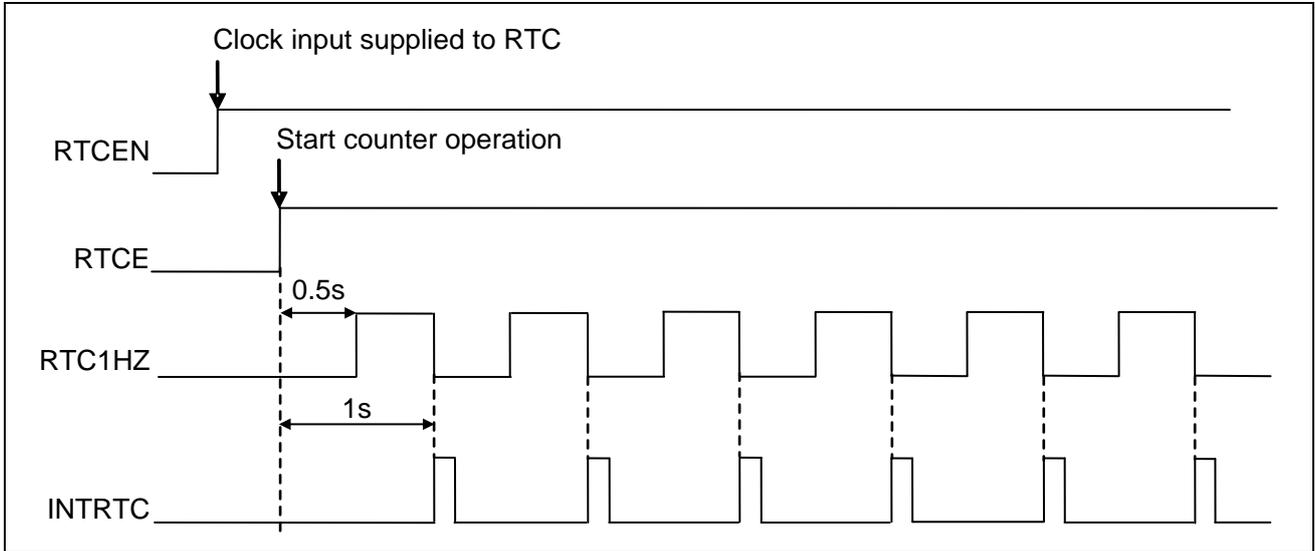


Figure 4.3 Overview of RTC Operation and Interrupts

#### 4.4.2 List of Option Byte Setting

Table 4.5 summarizes the settings of the option bytes.

Table 4.5 Option Byte Settings

Address	Value	Description
000C0H/010C0H	01101110B	Disables the watchdog timer. (Stops counting after the release from the reset state.)
000C1H/010C1H	01111111B	LVD reset mode which uses 2.81 V (2.76 V to 2.87 V)
000C2H/010C2H	11101000B	HS mode, HOCO: 32 MHz
000C3H/010C3H	10000100B	Enables the on-chip debugger.

#### 4.4.3 List of Functions

Table 4.6 lists the functions that are used in this sample program.

Table 4.6 Functions

Function Name	Outline
R_RTC_Create()	Initializes the real-time clock module.
R_RTC_Start()	Enables the real-time clock.

#### 4.4.4 Function Specification

The followings are the functions that are used in this sample program.

[Function Name] R\_RTC\_Create()

---

<b>Synopsis</b>	RTC initialization
<b>Header</b>	r_cg_macrodriver.h r_cg_rtc.h r_cg_userdefine.h
<b>Declaration</b>	void R_RTC_Create(void)
<b>Explanation</b>	This function initializes RTC module and sets RTC1HZ pin.
<b>Arguments</b>	None
<b>Return value</b>	None
<b>Remarks</b>	None

[Function Name] R\_RTC\_Start()

---

<b>Synopsis</b>	RTC operation start
<b>Header</b>	r_cg_macrodriver.h r_cg_rtc.h r_cg_userdefine.h
<b>Declaration</b>	void R_RTC_Start(void)
<b>Explanation</b>	This function enables RTC interrupts and starts count operation.
<b>Arguments</b>	None
<b>Return value</b>	None
<b>Remarks</b>	None

4.4.5 Flow Chart

4.4.5.1 Overall Flow

Figure 4.4 shows the overall flow of the sample program described in this chapter.

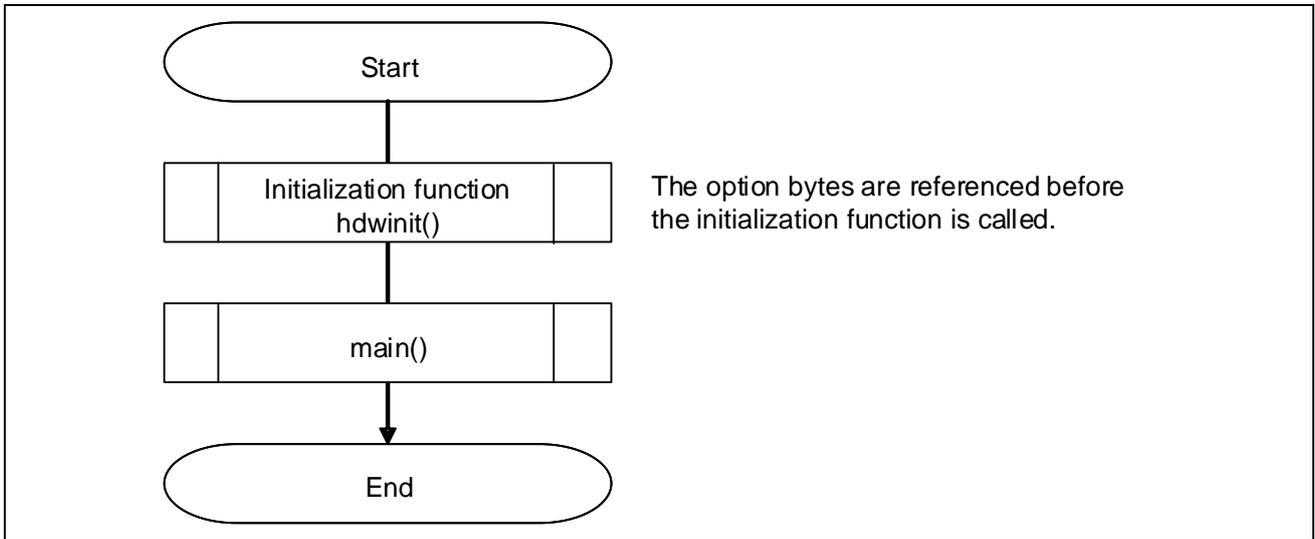


Figure 4.4 Overall Flow

4.4.5.2 Initialization Function

Figure 4.5 shows the flowchart for the initialization function.

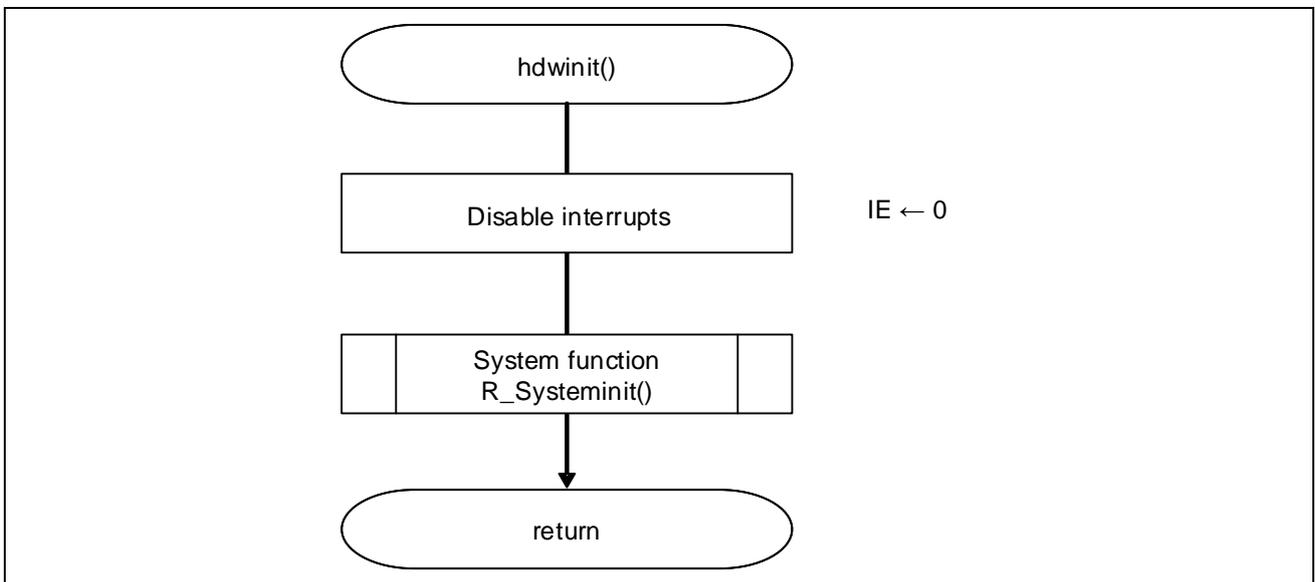


Figure 4.5 Initialization Function

4.4.5.3 System Function

Figure 4.6 shows the flowchart for the system function.

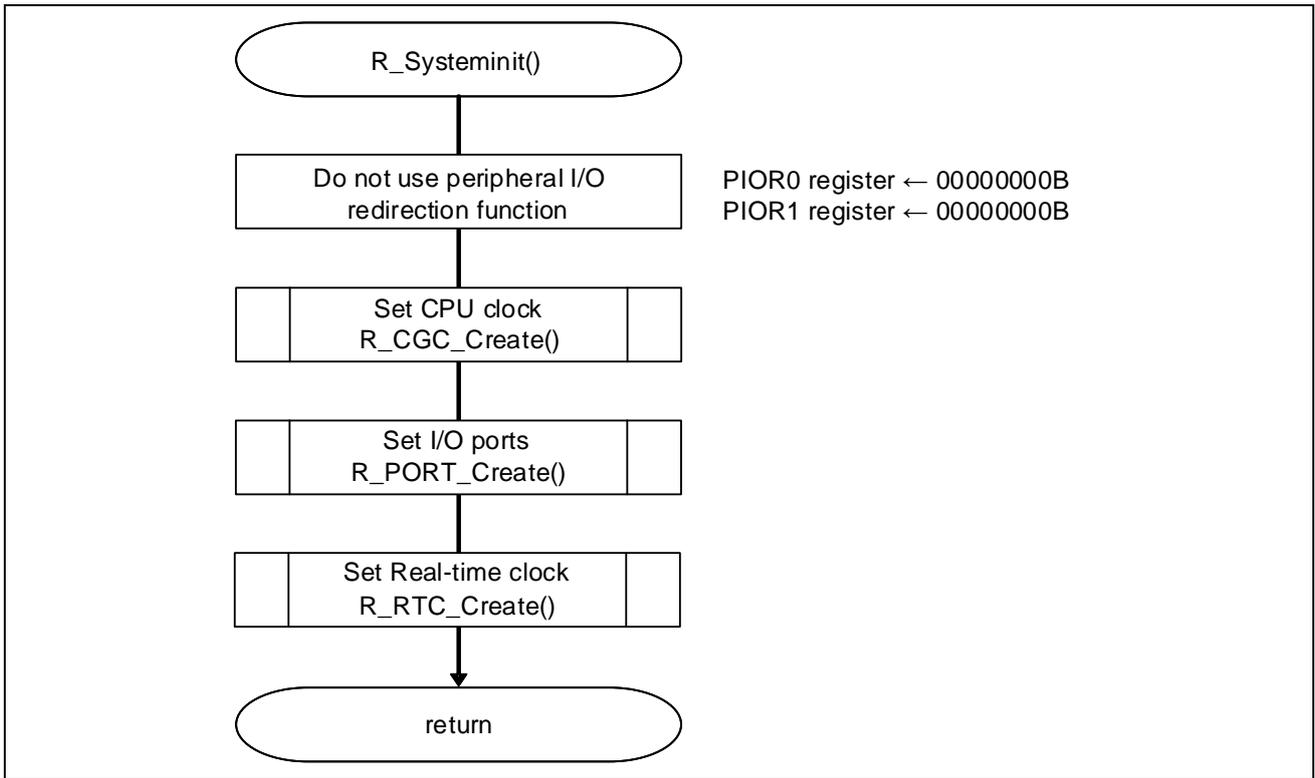


Figure 4.6 System Function

4.4.5.4 CPU Clock Setting

Figure 4.7 shows the flowchart for setting the CPU clock.

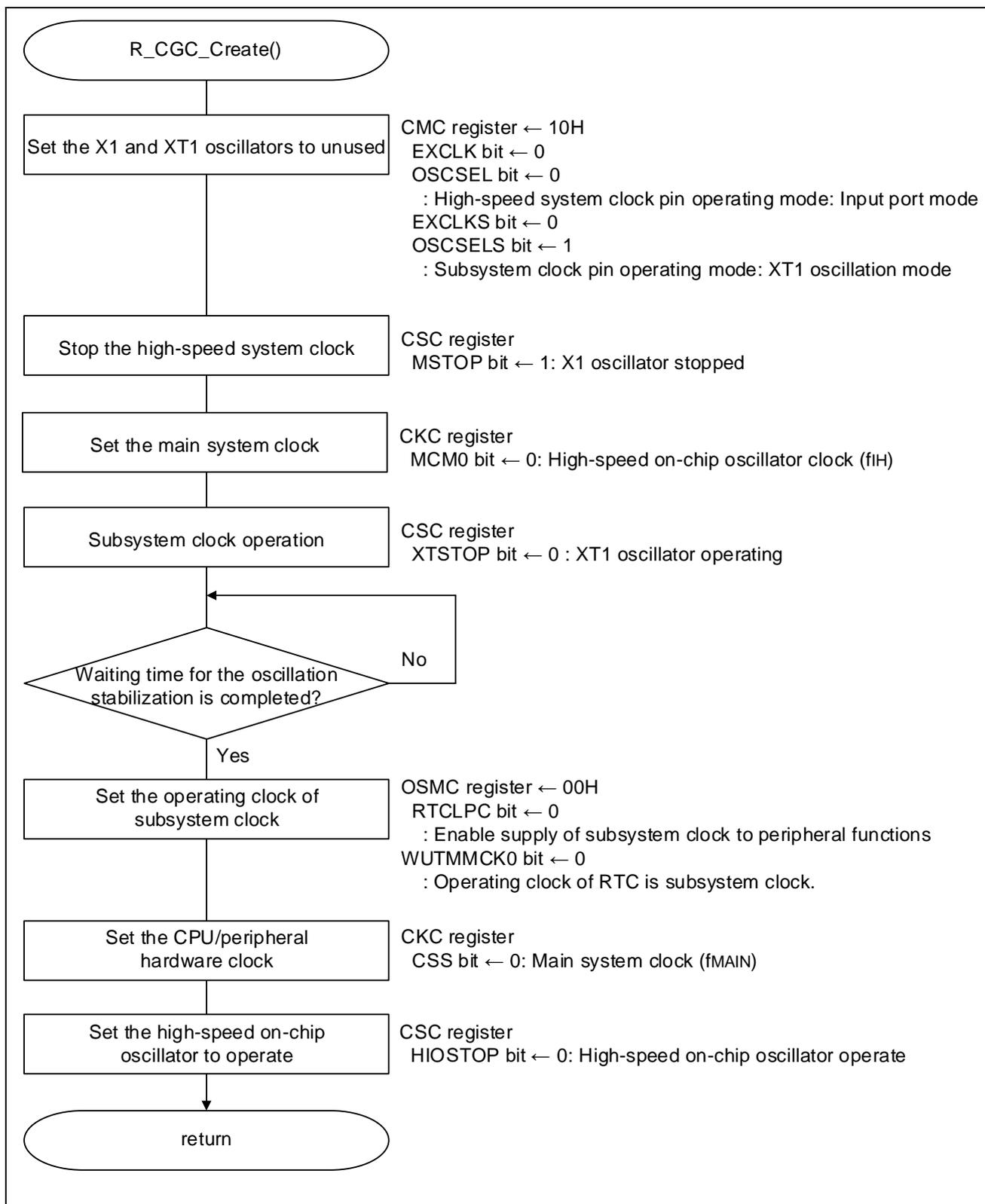
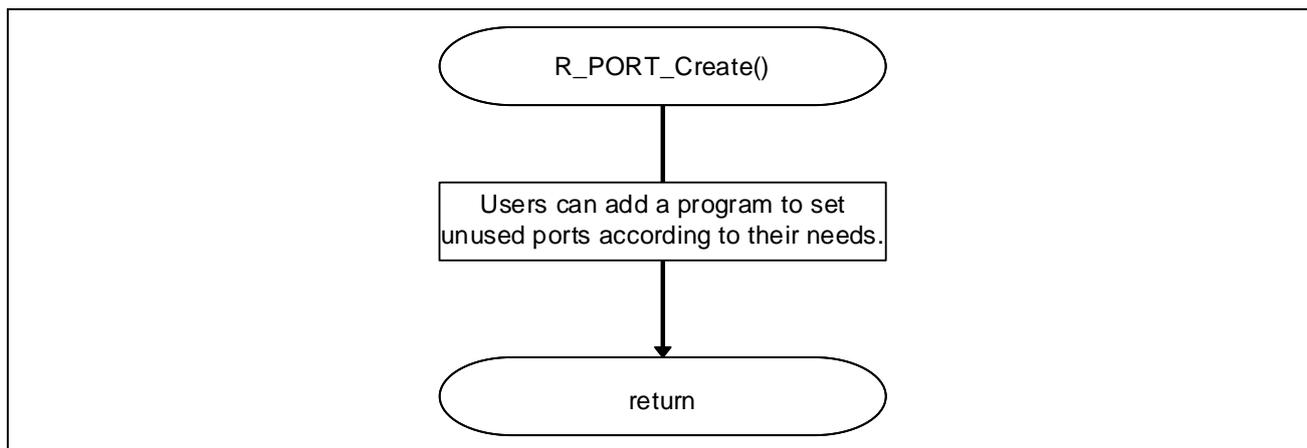


Figure 4.7 CPU Clock Setting

#### 4.4.5.5 I/O Port Setting

Figure 4.8 shows the flowchart for setting the I/O ports.



**Figure 4.8 I/O Port Setting**

Caution: Please provide proper pin treatment and make sure that the electrical specifications are met. Connect each of any unused input-only ports to  $V_{DD}$  or  $V_{SS}$  via a separate resistor.

4.4.5.6 Real-Time Clock Setting

Figure 4.9 shows the flowchart for setting the real-time clock.

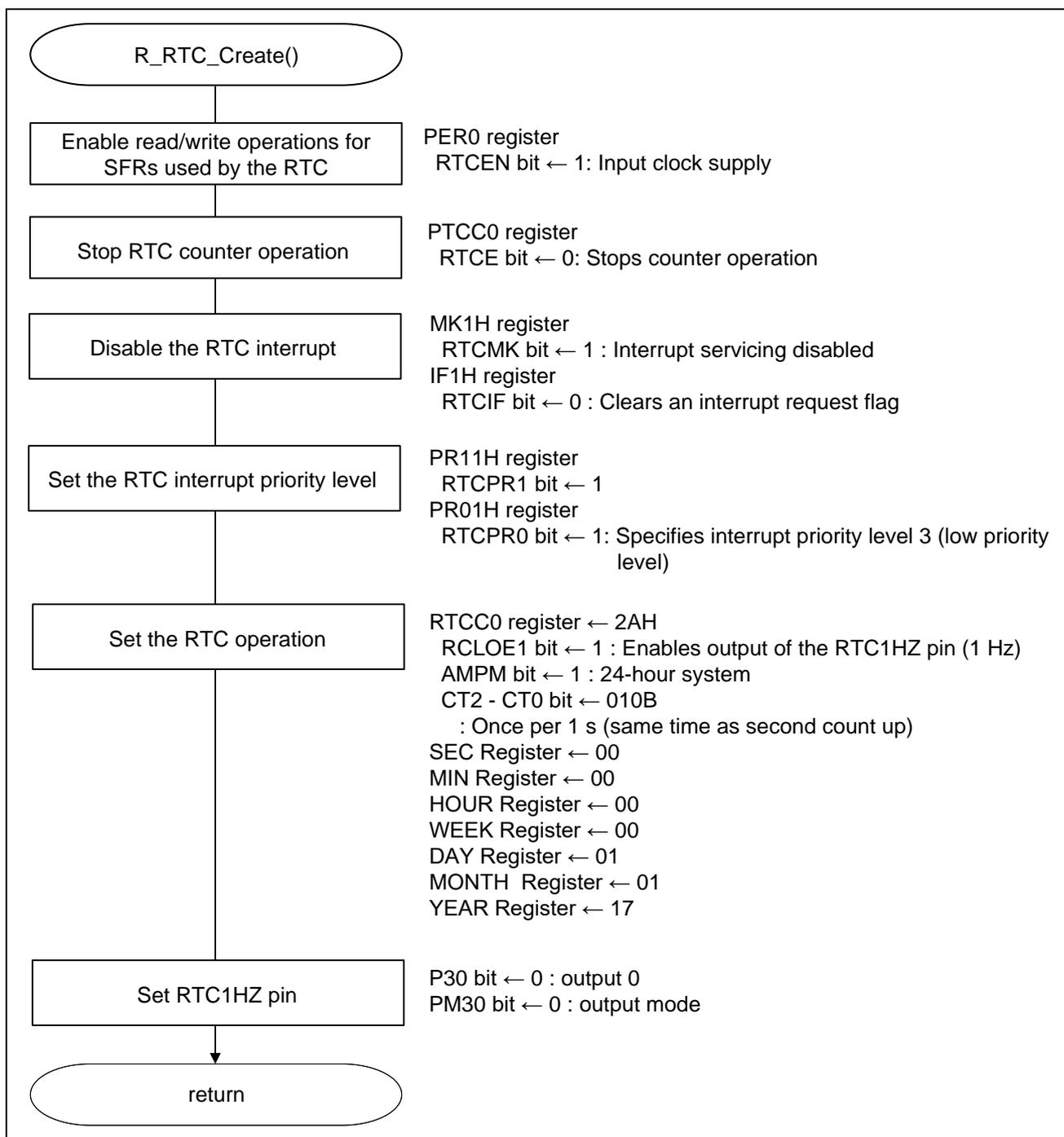


Figure 4.9 Real-Time Clock Setting

Enabling read and write operations for SFRs used by the RTC

- Peripheral enable register 0 (PER0)  
Starts to supply clock to RTC.

Symbol: PER0

7	6	5	4	3	2	1	0
<b>RTCEN</b>	<b>IICA1EN</b>	<b>ADCEN</b>	<b>IICA0EN</b>	<b>SAU1EN</b>	<b>SAU0EN</b>	<b>TAU1EN</b>	<b>TAU0EN</b>
1	x	x	x	x	x	x	x

Bit 7

<b>RTCEN</b>	<b>Control of supplying input clock for real-time clock (RTC) and 12-bit interval timer</b>
0	Stops input clock supply. • SFR used by the real-time clock (RTC) and 12-bit interval timer cannot be written. • The real-time clock (RTC) and 12-bit interval timer are in the reset status.
1	<b>Enables input clock supply.</b> • <b>SFR used by the real-time clock (RTC) and 12-bit interval timer can be read and written.</b>

x: Bits not used in this setting item

Caution: For details on the register setup procedures, refer to RL78/G14 User's Manual: Hardware.

Stopping RTC counter operation

- Real-time clock control register 0 (RTCC0)  
Stops counter operation.

Symbol: RTCC0

7	6	5	4	3	2	1	0
<b>RTCE</b>	<b>0</b>	<b>RCLOE1</b>	<b>0</b>	<b>AMPM</b>	<b>CT2</b>	<b>CT1</b>	<b>CT0</b>
0	0	x	0	x	x	x	x

Bit 7

<b>RTCE</b>	<b>Real-time clock operation control</b>
0	<b>Stops counter operation.</b>
1	Starts counter operation.

Disabling the RTC interrupt

- Interrupt mask flag register (MK1H)  
Disables interrupt processing.
- Interrupt request flag register (IF1H)  
Clears the interrupt request flag.

Symbol: MK1H

7	6	5	4	3	2	1	0
<b>TMMK10</b>	<b>TRJMK0</b>	<b>SRMK3 CSIMK31 IICMK31</b>	<b>STMK3 CSIMK30 IICMK30</b>	<b>KRMK</b>	<b>ITMK</b>	<b>RTCMK</b>	<b>ADMK</b>
x	x	x	x	x	x	1	x

Bit 1

<b>RTCMK</b>	<b>Interrupt servicing control</b>
0	Interrupt servicing enabled
1	<b>Interrupt servicing disabled</b>

Symbol: IF1H

7	6	5	4	3	2	1	0
<b>TMIF10</b>	<b>TRJIF0</b>	<b>SRIF3 CSIIF31 IICIF31</b>	<b>STIF3 CSIIF30 IICIF30</b>	<b>KRIF</b>	<b>ITIF</b>	<b>RTCIF</b>	<b>ADIF</b>
x	x	x	x	x	x	0	x

Bit 1

<b>RTCIF</b>	<b>Interrupt request flag</b>
0	<b>No interrupt request signal is generated.</b>
1	Interrupt request is generated, interrupt request status.

x: Bits not used in this setting item

Caution: For details on the register setup procedures, refer to RL78/G14 User's Manual: Hardware.

## RL78/G14, R8C/36M Group Migration Guide from R8C to RL78: Timer RE to Real-Time Clock and Timer Array Unit

Setting the RTC interrupt priority level

- Priority Specification Flag Register (PR11H, PR01H)  
Specifies level 3 (low priority level).

Symbol: PR11H

7	6	5	4	3	2	1	0
TMPR110	TRJPR10	SRPR13 CSIPR131 IICPR131	STPR13 CSIPR130 IICPR130	KRPR1	ITPR1	RTCPR1	ADPR1
x	x	x	x	x	x	1	x

Symbol: PR01H

7	6	5	4	3	2	1	0
TMPR010	TRJPR00	SRPR03 CSIPR031 IICPR031	STPR03 CSIPR030 IICPR030	KRPR0	ITPR0	RTCPR0	ADPR0
x	x	x	x	x	x	1	x

Bit 1

RTCPR1	RTCPR0	Priority level selection
0	0	Specify level 0 (high priority level)
0	1	Specify level 1
1	0	Specify level 2
1	1	<b>Specify level 3 (low priority level)</b>

x: Bits not used in this setting item

Caution: For details on the register setup procedures, refer to RL78/G14 User's Manual: Hardware.

Setting the RTC operation

- Real-time clock control register 0 (RTCC0)

Outputs signals from the RTC1HZ pin: Stops disabling.

Fixed-cycle interrupt function: 1 time per second (simultaneous with second count-up).

Symbol: RTCC0

7	6	5	4	3	2	1	0
<b>RTCE</b>	<b>0</b>	<b>RCLOE1</b>	<b>0</b>	<b>AMPM</b>	<b>CT2</b>	<b>CT1</b>	<b>CT0</b>
x	0	1	0	1	0	1	0

Bit 5

<b>RCLOE1</b>	<b>RTC1HZ pin output control</b>
0	Disables output of the RTC1HZ pin (1 Hz).
<b>1</b>	<b>Enables output of the RTC1HZ pin (1 Hz).</b>

Bit 3

<b>AMPM</b>	<b>Selection of 12-/24-hour system</b>
0	12-hour system (a.m. and p.m. are displayed.)
<b>1</b>	<b>24-hour system</b>

Bits 2 to 0

<b>CT2</b>	<b>CT1</b>	<b>CT0</b>	<b>Constant-period interrupt (INTRTC) selection</b>
0	0	0	Does not use fixed-cycle interrupt function.
0	0	1	Once per 0.5 s (synchronized with second count up)
<b>0</b>	<b>1</b>	<b>0</b>	<b>Once per 1 s (same time as second count up)</b>
0	1	1	Once per 1 m (second 00 of every minute)
1	0	0	Once per 1 hour (minute 00 and second 00 of every hour)
1	0	1	Once per 1 day (hour 00, minute 00, and second 00 of every day)
1	1	x	Once per 1 month (Day 1, hour 00 a.m., minute 00, and second 00 of every month)

x: Bits not used in this setting item

Caution: For details on the register setup procedures, refer to RL78/G14 User's Manual: Hardware.

## RL78/G14, R8C/36M Group Migration Guide from R8C to RL78: Timer RE to Real-Time Clock and Timer Array Unit

Specifying the date and time in the format of year, month, day, week, hour, minute and second.

- Count registers (YEAR, MONTH, DAY, WEEK, HOUR, MIN and SEC)

Specifies the date and time.

Symbol: YEAR

7	6	5	4	3	2	1	0
YEAR80	YEAR40	YEAR20	YEAR10	YEAR8	YEAR4	YEAR2	YEAR1
17 (BCD code)							

Set a decimal value of 00 to 99 to this register in BCD code.

Symbol: MONTH

7	6	5	4	3	2	1	0
0	0	0	MONTH10	MONTH8	MONTH4	MONTH2	MONTH1
0	0	0	1 (BCD code)				

Set a decimal value of 01 to 12 to this register in BCD code.

Symbol: DAY

7	6	5	4	3	2	1	0
0	0	DAY20	DAY10	DAY8	DAY4	DAY2	DAY1
0	0	1 (BCD code)					

Set a decimal value of 01 to 31 to this register in BCD code.

Symbol: WEEK

7	6	5	4	3	2	1	0
0	0	0	0	0	WEEK4	WEEK2	WEEK1
0	0	0	0	0	0 (BCD code)		

Set a decimal value of 00 to 06 to this register in BCD code.

Bits 2 to 0

Day	WEEK4	WEEK2	WEEK1
Sunday	00 H		
Monday	01 H		
Tuesday	02 H		
Wednesday	03 H		
Thursday	04 H		
Friday	05 H		
Saturday	06 H		

x: Bits not used in this setting item

Caution: For details on the register setup procedures, refer to RL78/G14 User's Manual: Hardware.

Symbol: HOUR

7	6	5	4	3	2	1	0
0	0	HOUR20	HOUR10	HOUR8	HOUR4	HOUR2	HOUR1
0	0	0 (BCD code)					

Specify a decimal value of 00 to 23, 01 to 12, or 21 to 32 by using BCD code according to the time system specified using bit 3 (AMPM) of real-time clock control register 0 (RTCC0).

Bits 5 to 0

24-Hour Display (AMPM = 1)		12-Hour Display (AMPM = 0)	
Time	Bits HOUR1 to HOUR20	Time	Bits HOUR1 to HOUR20
0	00 H	12 a.m.	12 H
1	01 H	1 a.m.	01 H
2	01 H	2 a.m.	02 H
:	:	:	:
:	:	:	:
:	:	:	:
21	21 H	9 p.m.	29 H
22	22 H	10 p.m.	30 H
23	23 H	11 p.m.	31 H

Symbol: MIN

7	6	5	4	3	2	1	0
0	MIN40	MIN20	MIN10	MIN8	MIN4	MIN2	MIN1
0	0 (BCD code)						

Set a decimal value of 00 to 59 to this register in BCD code.

Symbol: SEC

7	6	5	4	3	2	1	0
0	SEC40	SEC20	SEC10	SEC8	SEC4	SEC2	SEC1
0	0 (BCD code)						

Set a decimal value of 00 to 59 to this register in BCD code.

x: Bits not used in this setting item

Caution: For details on the register setup procedures, refer to RL78/G14 User's Manual: Hardware.

Setting the RTC1HZ port

- Port register 3 (P3)  
Sets the output latch value.

Symbol: P3

<b>7</b>	<b>6</b>	<b>5</b>	<b>4</b>	<b>3</b>	<b>2</b>	<b>1</b>	<b>0</b>
<b>0</b>	<b>0</b>	<b>0</b>	<b>0</b>	<b>0</b>	<b>0</b>	<b>P31</b>	<b>P30</b>
0	0	0	0	0	0	x	<b>0</b>

Bit 0

<b>P30</b>	<b>Output data control (in output mode)</b>
<b>0</b>	<b>Output 0</b>
1	Output 1

Symbol: PM3

<b>7</b>	<b>6</b>	<b>5</b>	<b>4</b>	<b>3</b>	<b>2</b>	<b>1</b>	<b>0</b>
<b>1</b>	<b>1</b>	<b>1</b>	<b>1</b>	<b>1</b>	<b>1</b>	<b>PM31</b>	<b>PM30</b>
0	1	1	1	1	1	x	<b>0</b>

Bit 0

<b>PM30</b>	<b>P30 pin I/O mode selection</b>
<b>0</b>	<b>Output mode (the pin functions as an output port (output buffer on))</b>
1	Input mode (the pin functions as an input port (output buffer off))

x: Bits not used in this setting item

Caution: For details on the register setup procedures, refer to RL78/G14 User's Manual: Hardware.

4.4.5.7 Main Processing

Figure 4.10 shows the flowchart for main processing.

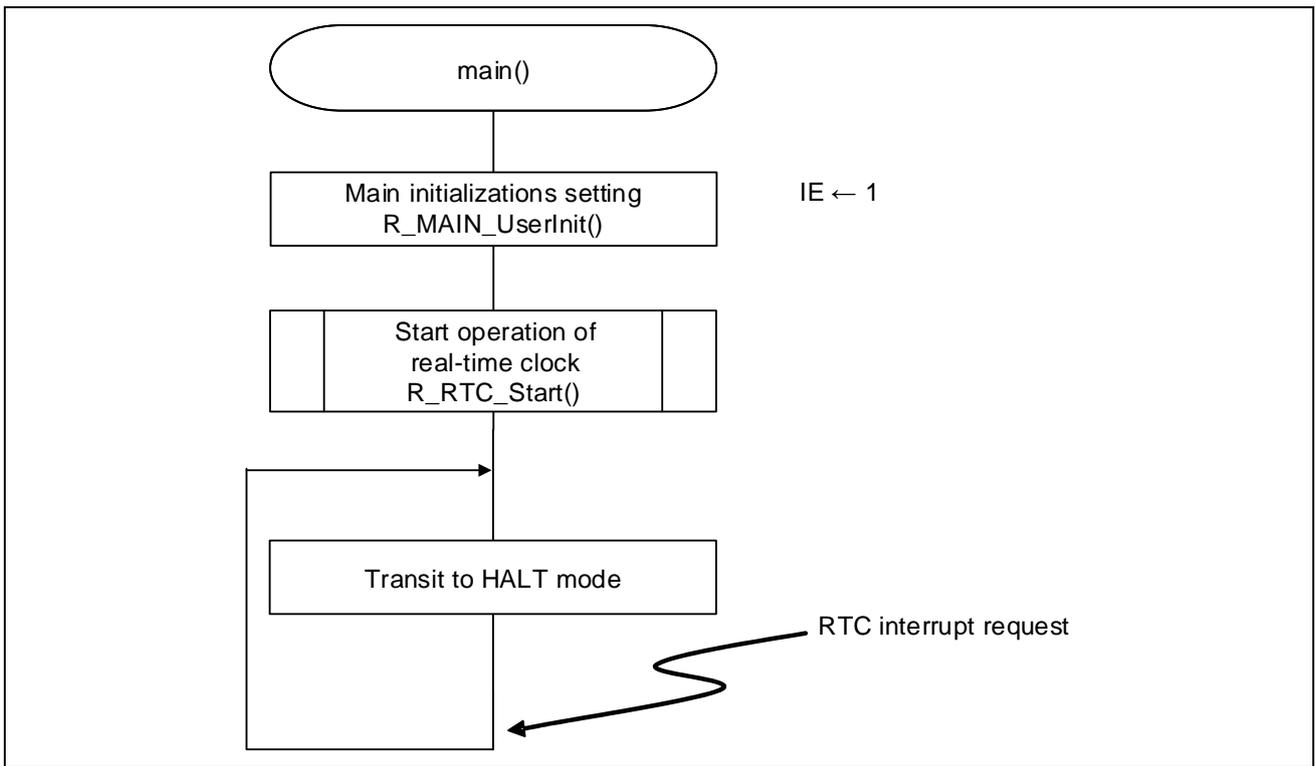


Figure 4.10 Main Processing

#### 4.4.5.8 Real-Time Clock Operation Start

Figure 4.11 shows the flowchart for starting timer array unit operation.

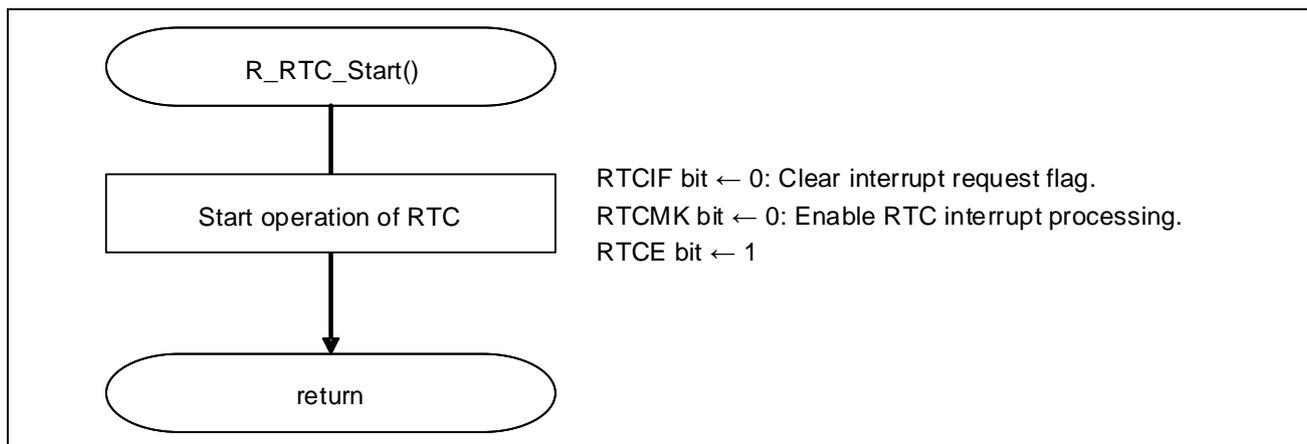


Figure 4.11 Real-Time Clock Operation Start

Configuring the timer interrupt

- Interrupt request flag register (IF1H)  
Clears the interrupt request flag.
- Interrupt mask flag register (MK1H)  
Enables interrupt processing.

Symbol: IF1H

7	6	5	4	3	2	1	0
<b>TMIF10</b>	<b>TRJIF0</b>	<b>SRIF3 CSIIF31 IICIF31</b>	<b>STIF3 CSIIF30 IICIF30</b>	<b>KRIF</b>	<b>ITIF</b>	<b>RTCIF</b>	<b>ADIF</b>
x	x	x	x	x	x	0	x

Bit 1

<b>RTCIF</b>	<b>Interrupt request flag</b>
0	No interrupt request signal is generated
1	Interrupt request is generated, interrupt request status

Symbol: MK1H

7	6	5	4	3	2	1	0
<b>TMMK10</b>	<b>TRJMK0</b>	<b>SRMK3 CSIMK31 IICMK31</b>	<b>STMK3 CSIMK30 IICMK30</b>	<b>KRMK</b>	<b>ITMK</b>	<b>RTCMK</b>	<b>ADMK</b>
x	x	x	x	x	x	0	x

Bit 1

<b>RTCMK</b>	<b>Interrupt processing control</b>
0	Interrupt servicing enabled
1	Interrupt servicing disabled

Starting RTC counter operation

- Real-time clock control register 0 (RTCC0)  
Starts counter operation.

Symbol: RTCC0

7	6	5	4	3	2	1	0
<b>RTCE</b>	<b>0</b>	<b>RCLOE1</b>	<b>0</b>	<b>AMPM</b>	<b>CT2</b>	<b>CT1</b>	<b>CT0</b>
1	0	x	0	x	x	x	x

Bit 7

<b>RTCE</b>	<b>Real-time clock operation control</b>
0	Stops counter operation
1	Starts counter operation

x: Bits not used in this setting item

Caution: For details on the register setup procedures, refer to RL78/G14 User's Manual: Hardware.

4.4.5.9 INTRTC Interrupt Processing

Figure 4.12 shows the flowchart for INTRTC interrupt processing.

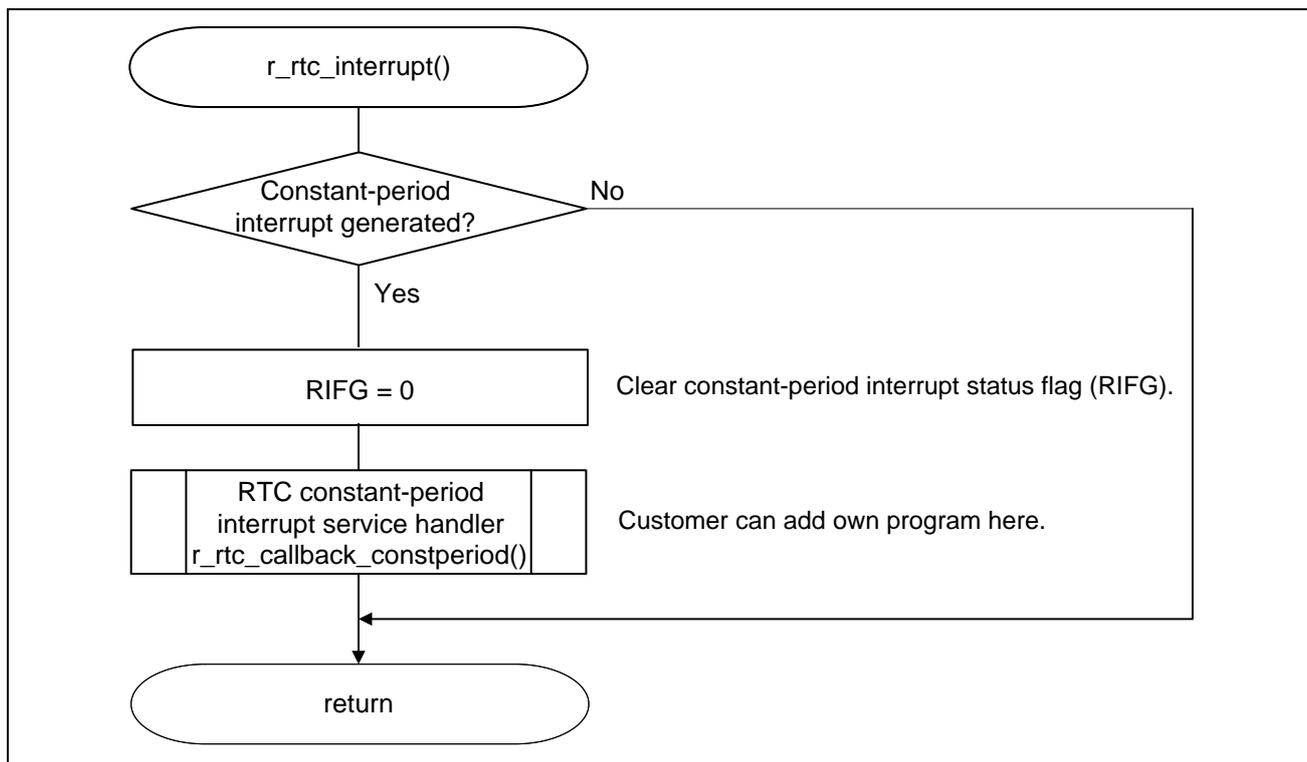


Figure 4.12 INTRTC Interrupt Processing

## 5. Example of Migration from Output Compare Mode

### 5.1 Specifications

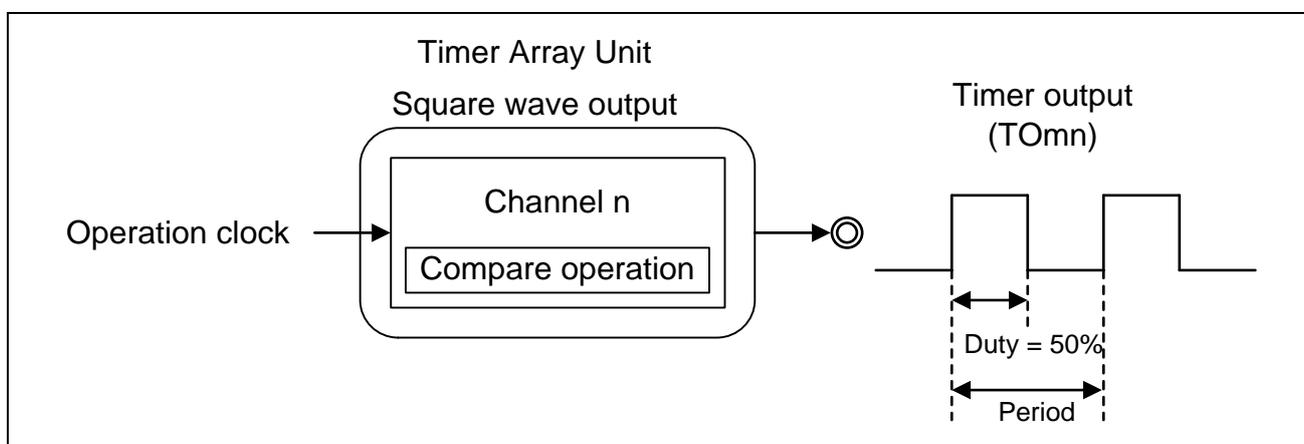
The same operation as that in output compare mode in timer RE of R8C/36M can be realized by using square wave output in TAU of RL78/G14.

TO<sub>m</sub>n performs a toggle operation as soon as INTT<sub>M</sub>m<sub>n</sub> is generated, and outputs a square wave with a duty factor of 50%.

Table 5.1 lists the peripheral functions to be used and their uses (example of migration from output compare mode), and Figure 5.1 shows operation overview (example of migration from output compare mode).

**Table 5.1 Peripheral Functions to be Used and Their Uses**  
(Example of Migration from Output Compare Mode)

Peripheral Function	Use
Timer array unit (square wave output)	TO <sub>m</sub> n outputs a square wave with a duty factor of 50%.



**Figure 5.1 Operation Overview (Example of Migration from Output Compare Mode)**

Remark m: Unit number (m = 0, 1), n: Channel number (n = 0 to 3)

## 5.2 Operation Check Conditions

The sample code described in this chapter has been checked under the conditions listed in the table below.

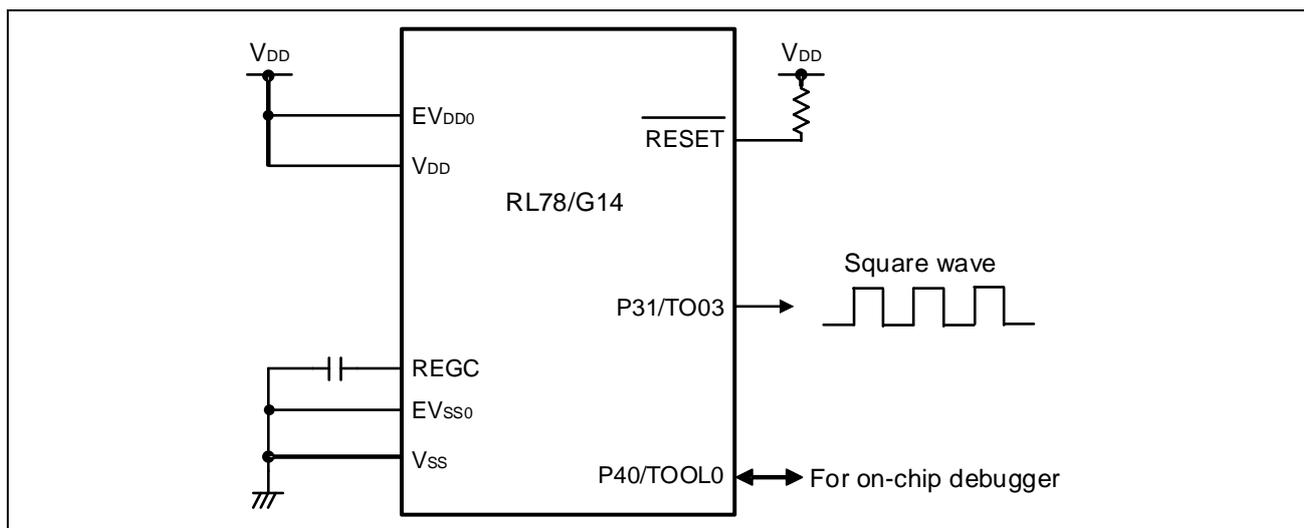
**Table 5.2 Operation Check Conditions**

Item	Description
Microcontroller used	RL78/G14 (R5F104LEAFB)
Operating frequency	High-speed on-chip oscillator (HOCO) clock: 32 MHz CPU/peripheral hardware clock: 32 MHz
Operating voltage	5.0V (can run on a voltage range of 2.9 V to 5.5 V.) LVD operation ( $V_{LVD}$ ): Reset mode 2.81 V (2.76 V to 2.87 V)
Integrated development environment (CS+)	CS+ V6.00.00 from Renesas Electronics Corp.
C compiler (CS+)	CC-RL V1.05.00 from Renesas Electronics Corp.
Integrated development environment (e <sup>2</sup> studio)	e <sup>2</sup> studio V6.0.0 from Renesas Electronics Corp.
C compiler (e <sup>2</sup> studio)	CC-RL V1.05.00 from Renesas Electronics Corp.

## 5.3 Description of Hardware

### 5.3.1 Hardware Configuration Example

Figure 5.2 shows an example of the hardware configuration that is used for this chapter.



**Figure 5.2 Hardware Configuration**

- Cautions:
1. The purpose of this circuit is only to provide the connection outline and the circuit is simplified accordingly. When designing and implementing an actual circuit, provide proper pin treatment and make sure that the hardware's electrical specifications are met (connect the input-only ports separately to  $V_{DD}$  or  $V_{SS}$  via a resistor).
  2. Connect any pins whose name begins with  $EV_{SS}$  to  $V_{SS}$  and any pins whose name begins with  $EV_{DD}$  to  $V_{DD}$ , respectively.
  3.  $V_{DD}$  must be held at not lower than the reset release voltage ( $V_{LVD}$ ) that is specified as LVD.

**5.3.2 List of Pins to be Used**

Table 5.3 lists the pins to be used and their functions.

**Table 5.3 Pins to be Used and Their Functions**

Pin Name	I/O	Description
P31/TO03	Output	Square wave output port

**5.4 Description of Software**

**5.4.1 Operation Outline**

The sample program covered in this chapter implements square wave output from P31/TO03 by operating TAU unit 0 channel 3.

TO03 outputs a square wave with a duty factor of 50%.

Table 5.4 lists the peripheral functions to be used and their uses. Figure 5.3 shows the timer operation and its interrupt generating timing.

(1) Initialize the TAU.

<Conditions for setting>

Uses the square wave output as the timer operation mode.

Initializes timer data register 03 (TDR03) to 100 μs.

Sets the P31/TO03 pin to a square wave output, and the initial output value is 0.

Uses timer interrupts (INTTM03) from timer channel 3.

(2) TAU0's channel 3 starts operation.

(3) A HALT instruction is executed.

(4) When the counter of channel 3 reaches 0000H, the value of the TDR03 register is loaded again to the TCR03 register, and the counter counts down. At the same time, square wave output (TO03) toggles and INTTM03 interrupt occurs.

(5) The operation described in (3) and (4) above are repeated.

Table 5.4 Required Peripheral Functions and Their Uses

Peripheral Function	Use
Timer array unit 0 channel 3	Square wave output control for inversion of TO03 pin output

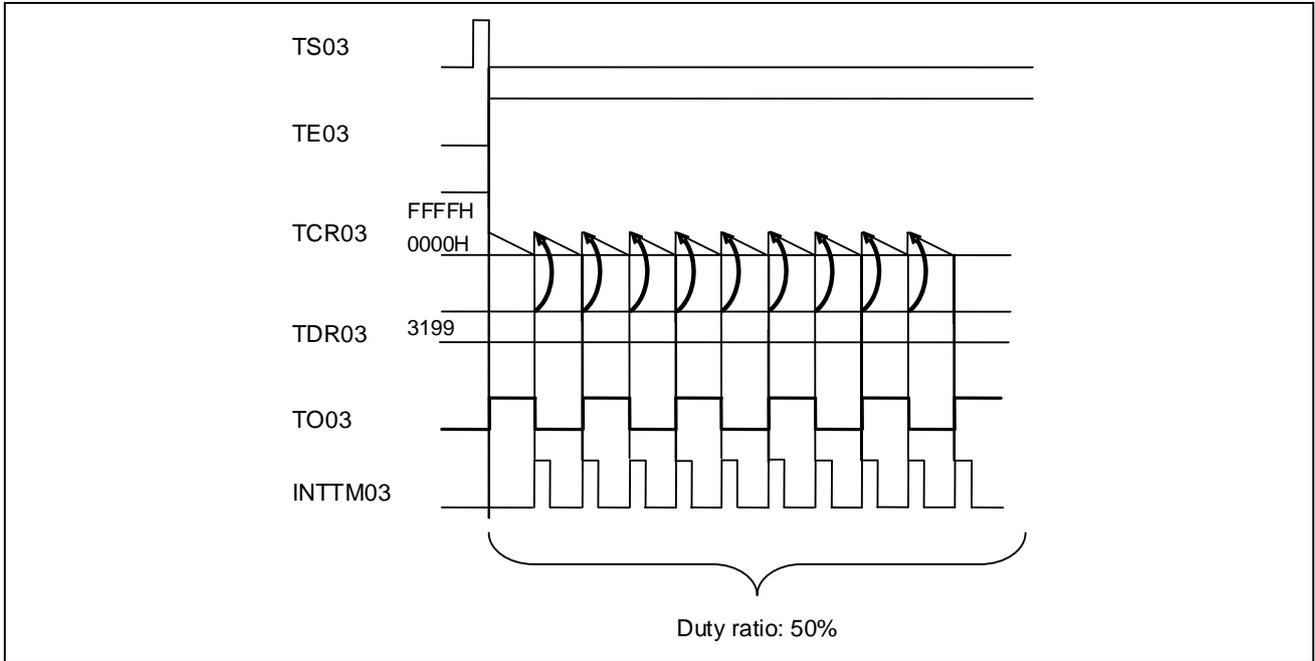


Figure 5.3 Overview of Timer Operation and Interrupts

### 5.4.2 List of Option Byte Setting

Table 5.5 summarizes the settings of the option bytes.

Table 5.5 Option Byte Settings

Address	Value	Description
000C0H/010C0H	01101110B	Disables the watchdog timer. (Stops counting after the release from the reset state.)
000C1H/010C1H	01111111B	LVD reset mode which uses 2.81 V (2.76 V to 2.87 V)
000C2H/010C2H	11101000B	HS mode, HOCO: 32 MHz
000C3H/010C3H	10000100B	Enables the on-chip debugger.

### 5.4.3 List of Functions

Table 5.6 lists the functions that are used in this sample program.

Table 5.6 Functions

Function	Outline
R_TAU0_Create	TAU0 initialization
R_TAU0_Channel3_Start	TAU0 channel 3 start processing

### 5.4.4 Function Specification

The followings are the functions that are used in this sample program.

[Function Name] R\_TAU0\_Create

---

<b>Synopsis</b>	TAU0 initialization
<b>Header</b>	r_cg_macrodriver.h r_cg_timer.h r_cg_userdefine.h
<b>Declaration</b>	void R_TAU0_Create(void)
<b>Explanation</b>	This function initializes TAU0 module.
<b>Arguments</b>	None
<b>Return value</b>	None
<b>Remarks</b>	None

[Function Name] R\_TAU0\_Channel3\_Start

---

<b>Synopsis</b>	TAU0 channel 3 start processing
<b>Header</b>	r_cg_macrodriver.h r_cg_timer.h r_cg_userdefine.h
<b>Declaration</b>	void R_TAU0_Channel3_Start(void)
<b>Explanation</b>	This function starts the count operation of TAU0 channel 3.
<b>Arguments</b>	None
<b>Return value</b>	None
<b>Remarks</b>	None

5.4.5 Flow Chart

5.4.5.1 Overall Flow

Figure 5.4 shows the overall flow of the sample program described in this chapter.

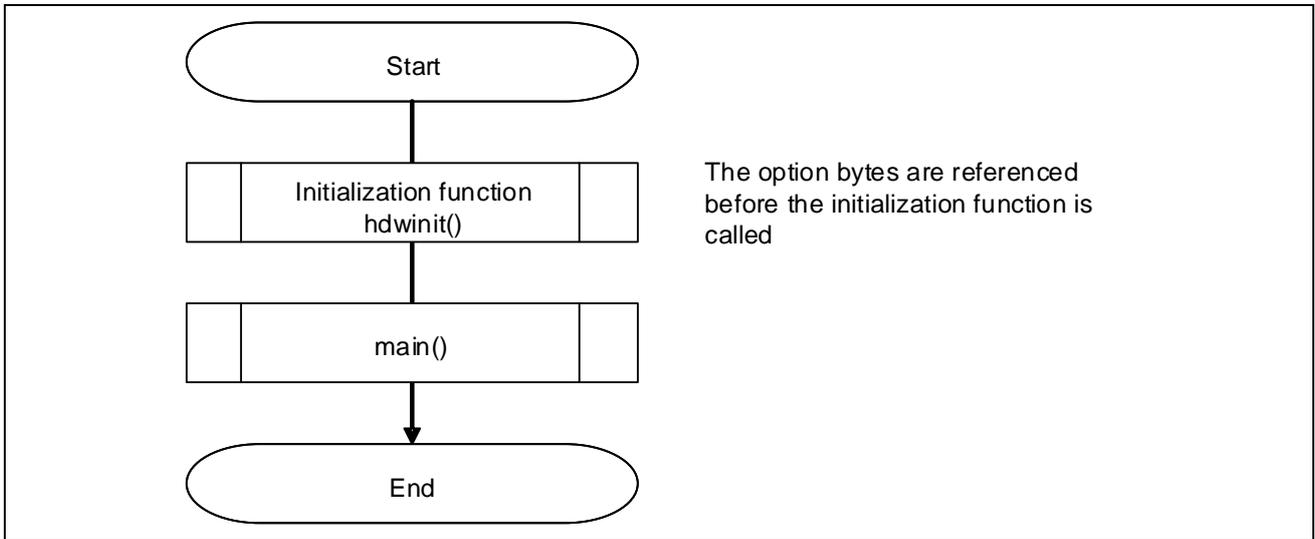


Figure 5.4 Overall Flow

5.4.5.2 Initialization Function

Figure 5.5 shows the flowchart for the initialization function.

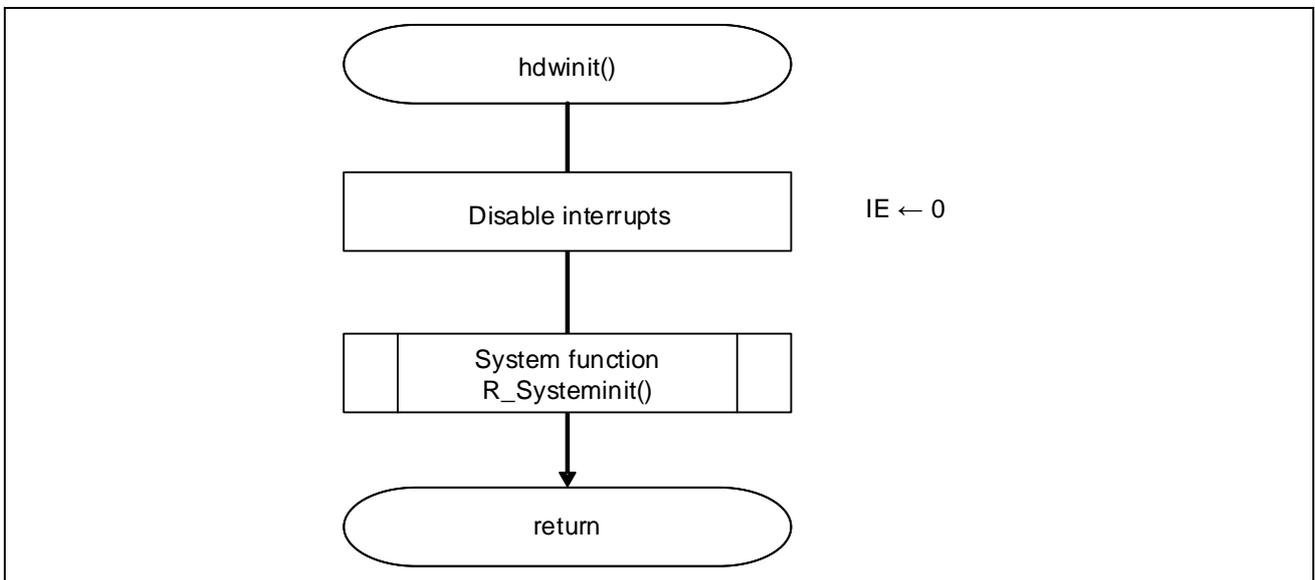


Figure 5.5 Initialization Function

5.4.5.3 System Function

Figure 5.6 shows the flowchart for the system function.

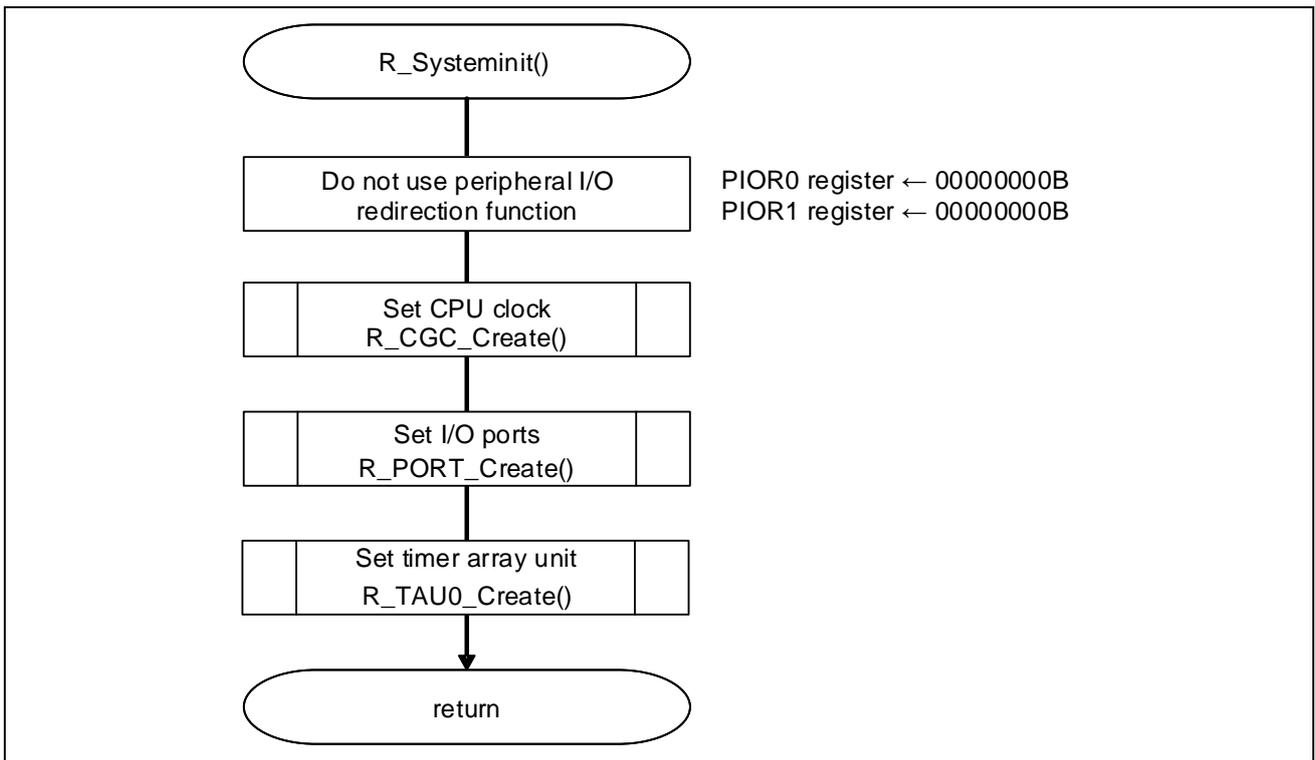


Figure 5.6 System Function

### 5.4.5.4 CPU Clock Setting

Figure 5.7 shows the flowchart for setting the CPU clock.

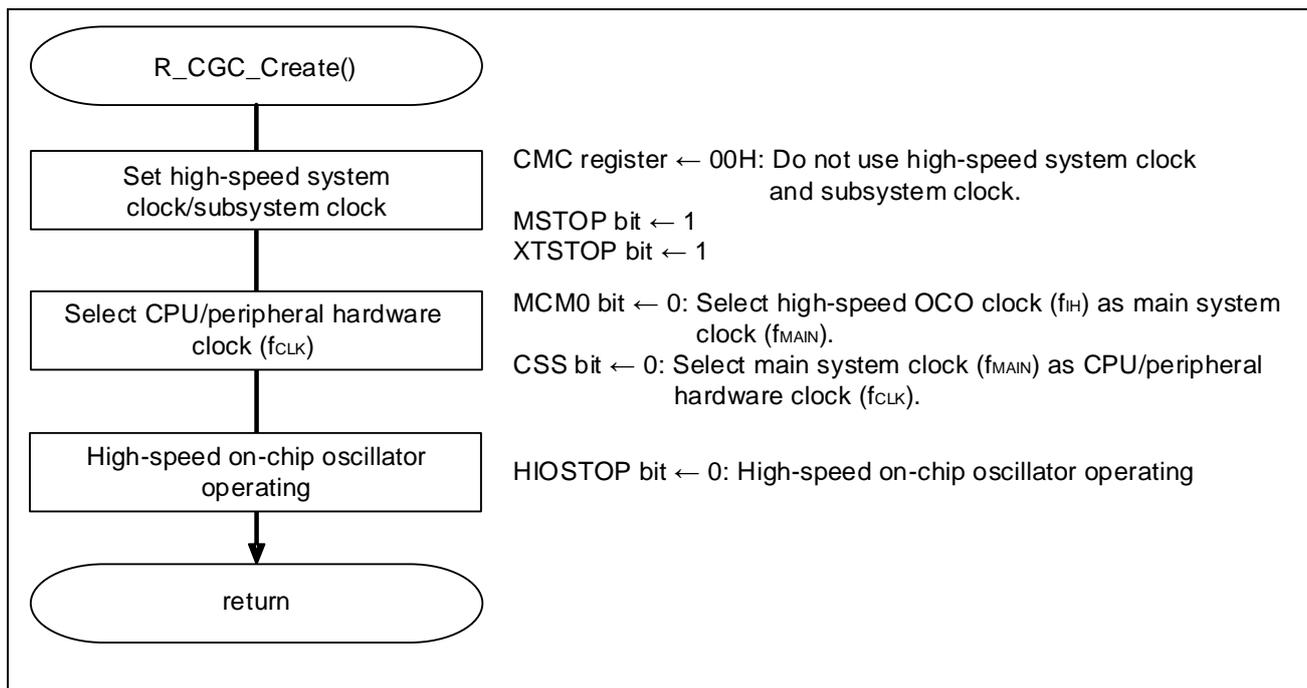


Figure 5.7 CPU Clock Setting

### 5.4.5.5 I/O Port Setting

Figure 5.8 shows the flowchart for setting the I/O ports.

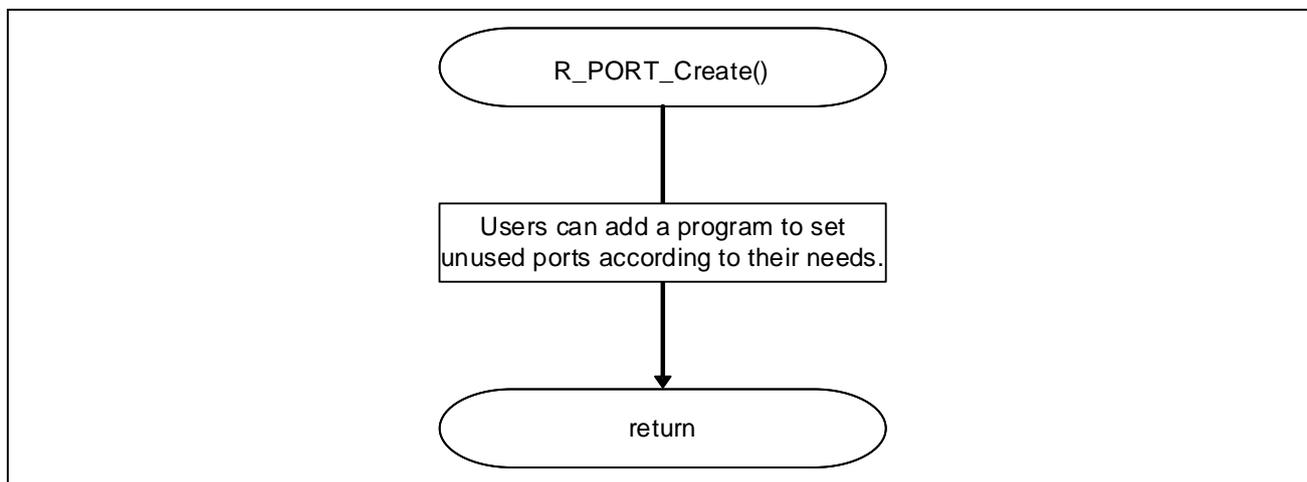


Figure 5.8 I/O Port Setting

Caution: Please provide proper pin treatment and make sure that the electrical specifications are met. Connect each of any unused input-only ports to  $V_{DD}$  or  $V_{SS}$  via a separate resistor.

5.4.5.6 Timer Array Unit Setting

Figures 5.9 shows the flowchart for setting the timer array unit.

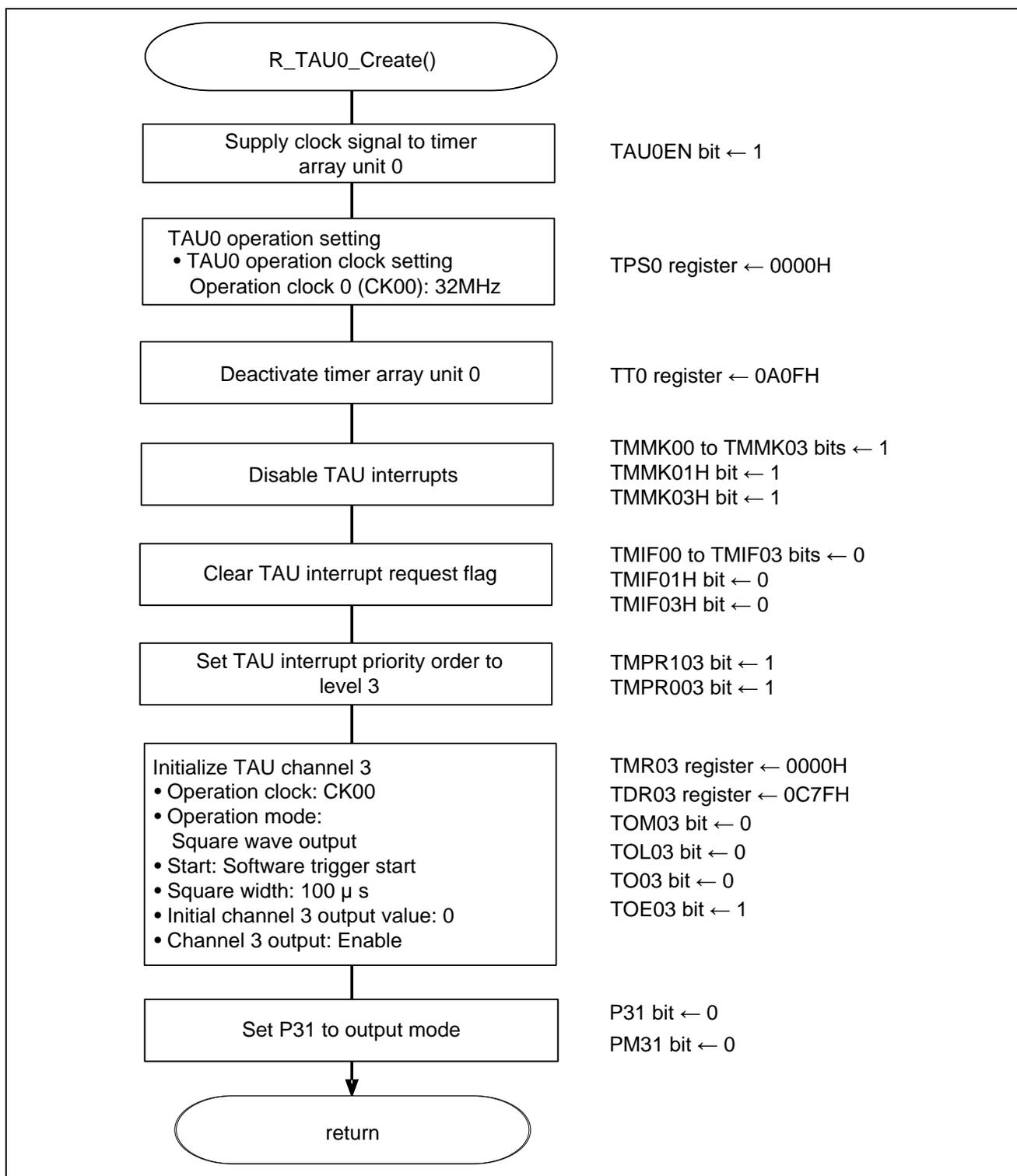


Figure 5.9 Timer Array Unit Setting

Starting clock signal supply to the timer array unit 0

- Peripheral enable register 0 (PER0)  
Starts clock signal supply to the timer array unit 0.

Symbol: PER0

7	6	5	4	3	2	1	0
<b>RTCEN</b>	<b>IICA1EN</b>	<b>ADCEN</b>	<b>IICA0EN</b>	<b>SAU1EN</b>	<b>SAU0EN</b>	<b>TAU1EN</b>	<b>TAU0EN</b>
x	x	x	x	x	x	x	1

Bit 0

<b>TAU0EN</b>	<b>Control of timer array unit 0 input clock supply</b>
0	Stops input clock supply
1	Enables input clock supply

x: Bits not used in this setting item

Caution: For details on the register setup procedures, refer to RL78/G14 User's Manual: Hardware.

Configuring the timer clock frequency

- Timer clock select register 0 (TPS0)  
Selects an operation clock for timer array unit 0.

Symbol: TPS0

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	PRS 031	PRS 030	0	0	PRS 021	PRS 020	PRS 013	PRS 012	PRS 011	PRS 010	PRS 003	PRS 002	PRS 001	PRS 000
0	0	x	x	0	0	x	x	x	x	x	x	0	0	0	0

Bits 3 to 0

PRS 003	PRS 002	PRS 001	PRS 000	Operation clock (CK00) selection					
				f <sub>CLK</sub>	f <sub>CLK</sub> = 2 MHz	f <sub>CLK</sub> = 4 MHz	f <sub>CLK</sub> = 8 MHz	f <sub>CLK</sub> = 20 MHz	f <sub>CLK</sub> = 32 MHz
0	0	0	0	f <sub>CLK</sub>	2 MHz	4 MHz	8 MHz	20 MHz	32 MHz
0	0	0	1	f <sub>CLK</sub> /2	1 MHz	2 MHz	4 MHz	10 MHz	16 MHz
0	0	1	0	f <sub>CLK</sub> /2 <sup>2</sup>	500 kHz	1 MHz	2 MHz	5 MHz	8 MHz
0	0	1	1	f <sub>CLK</sub> /2 <sup>3</sup>	250 kHz	500 kHz	1 MHz	2.5 MHz	4 MHz
0	1	0	0	f <sub>CLK</sub> /2 <sup>4</sup>	125 kHz	250 kHz	500 kHz	1.25 MHz	2 MHz
0	1	0	1	f <sub>CLK</sub> /2 <sup>5</sup>	62.5 kHz	125 kHz	250 kHz	625 kHz	1 MHz
0	1	1	0	f <sub>CLK</sub> /2 <sup>6</sup>	31.3 kHz	62.5 kHz	125 kHz	313 kHz	500 kHz
0	1	1	1	f <sub>CLK</sub> /2 <sup>7</sup>	15.6 kHz	31.3 kHz	62.5 kHz	156 kHz	250 kHz
1	0	0	0	f <sub>CLK</sub> /2 <sup>8</sup>	7.81 kHz	15.6 kHz	31.3 kHz	78.1 kHz	125 kHz
1	0	0	1	f <sub>CLK</sub> /2 <sup>9</sup>	3.91 kHz	7.81 kHz	15.6 kHz	39.1 kHz	62.5 kHz
1	0	1	0	f <sub>CLK</sub> /2 <sup>10</sup>	1.95 kHz	3.91 kHz	7.81 kHz	19.5 kHz	31.25 kHz
1	0	1	1	f <sub>CLK</sub> /2 <sup>11</sup>	977 Hz	1.95 kHz	3.91 kHz	9.77 kHz	15.6 kHz
1	1	0	0	f <sub>CLK</sub> /2 <sup>12</sup>	488 Hz	977 Hz	1.95 kHz	4.88 kHz	7.81 kHz
1	1	0	1	f <sub>CLK</sub> /2 <sup>13</sup>	244 Hz	488 Hz	977 Hz	2.44 kHz	3.91 kHz
1	1	1	0	f <sub>CLK</sub> /2 <sup>14</sup>	122 Hz	244 Hz	488 Hz	1.22 kHz	1.95 kHz
1	1	1	1	f <sub>CLK</sub> /2 <sup>15</sup>	61.0 Hz	122 Hz	244 Hz	610 Hz	977 Hz

x: Bits not used in this setting item

Caution: For details on the register setup procedures, refer to RL78/G14 User's Manual: Hardware.

Setting the channel 3 operation mode

- Timer mode register 03 (TMR03)  
 Selects an operation clock ( $f_{MCK}$ ).  
 Selects a count clock.  
 Selects a start trigger and capture trigger.  
 Sets operation mode.

Symbol: TMR03

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
<b>CKS031</b>	<b>CKS030</b>	<b>0</b>	<b>CCS03</b>	<b>SPLIT03</b>	<b>STS032</b>	<b>STS031</b>	<b>STS030</b>	<b>CIS031</b>	<b>CIS030</b>	<b>0</b>	<b>0</b>	<b>MD033</b>	<b>MD032</b>	<b>MD031</b>	<b>MD030</b>	
0	0	0	0	0	0	0	0	x	x	0	0	0	0	0	0	

Bits 15 and 14

<b>CKS031</b>	<b>CKS030</b>	<b>Selection of operation clock (<math>f_{MCK}</math>) of channel 3</b>
0	0	<b>Operation clock CK00 set by timer clock select register 0 (TPS0)</b>
0	1	Operation clock CK02 set by timer clock select register 0 (TPS0)
1	0	Operation clock CK01 set by timer clock select register 0 (TPS0)
1	1	Operation clock CK03 set by timer clock select register 0 (TPS0)

Bit 12

<b>CCS03</b>	<b>Selection of count clock (<math>f_{TCLK}</math>) of channel 3</b>
0	<b>Operation clock (<math>f_{MCK}</math>) specified by the CKS030 and CKS031 bits</b>
1	Valid edge of input signal input from the TI03 pin

Bits 10 to 8

<b>STS032</b>	<b>STS031</b>	<b>STS030</b>	<b>Setting of start trigger or capture trigger of channel 3</b>
0	0	0	<b>Only software trigger start is valid (other trigger sources are unselected).</b>
0	0	1	Valid edge of the TI03 pin input is used as both the start trigger and capture trigger.
0	1	0	Both the edges of the TI03 pin input are used as a start trigger and a capture trigger.
1	0	0	Interrupt signal of the master channel is used (when the channel is used as a slave channel with the simultaneous channel operation function).
Other than above			Setting prohibited

x: Bits not used in this setting item

Caution: For details on the register setup procedures, refer to RL78/G14 User's Manual: Hardware.

Symbol: TMR03

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CKS 031	CKS 030	0	CCS 03	SPLIT 03	STS 032	STS 031	STS 030	CIS 031	CIS 030	0	0	MD 033	MD 032	MD 031	MD 030
0	0	0	0	0	0	0	0	x	x	0	0	0	0	0	0

Bits 3 to 0

MD033	MD032	MD031	MD030	Operation mode of channel 0	Corresponding function	Count operation of TCR
0	0	0	1/0	Interval timer mode	Interval timer / <b>Square wave output</b> / Divider function / PWM output (master)	<b>Counting down</b>
0	1	0	1/0	Capture mode	Input pulse interval measurement	Counting up
0	1	1	0	Event counter mode	External event counter	Counting down
1	0	0	1/0	One-count mode	Delay counter / One-shot pulse output / PWM output (slave)	Counting down
1	1	0	0	Capture & one-count mode	Measurement of high-/low-level width of input signal	Counting up
Other than above				Setting prohibited		

The operation of each mode varies depending on MD030 bit (see table below).

Operation mode (Value set by the MD033 to MD031 bits (see table above))	MD030	Setting of starting counting and interrupt
<ul style="list-style-type: none"> <li>Interval timer mode (0, 0, 0)</li> <li>Capture mode (0, 1, 0)</li> </ul>	0	<b>Timer interrupt is not generated when counting is started (timer output does not change, either).</b>
	1	Timer interrupt is generated when counting is started (timer output also changes).
<ul style="list-style-type: none"> <li>Event counter mode (0, 1, 1)</li> </ul>	0	Timer interrupt is not generated when counting is started (timer output does not change, either).
<ul style="list-style-type: none"> <li>One-count mode (1, 0, 0)</li> </ul>	0	Start trigger is invalid during counting operation. At that time, interrupt is not generated.
	1	Start trigger is valid during counting operation. At that time, interrupt is not generated.
<ul style="list-style-type: none"> <li>Capture &amp; one-count mode (1, 1, 0)</li> </ul>	0	Timer interrupt is not generated when counting is started (timer output does not change, either). Start trigger is invalid during counting operation. At that time interrupt is not generated.
Other than above		Setting prohibited

x: Bits not used in this setting item

Caution: For details on the register setup procedures, refer to RL78/G14 User's Manual: Hardware.

Setting the square wave width

- Timer data register 03 (TDR03)  
Configures the square wave output width.

Symbol: TDR03

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

$$\text{Square wave width} = (\text{TDR03 setting} + 1) \times \text{Count clock cycle time}$$

$$100 [\mu\text{s}] = (1/32[\text{MHz}]) \times (\text{TDR03 setting} + 1)$$

⇒ TDR03 setting = 3199

Setting the timer output mode

- Timer output mode register 0 (TOM0)  
Sets the timer output mode for each channel.

Symbol: TOM0

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	TOM03	TOM02	TOM01	0
0	0	0	0	0	0	0	0	0	0	0	0	0	x	x	0

Bit 3

TOM03	Control of timer output mode of channel 3
0	Master channel output mode (to produce toggle output by timer interrupt request signal (INTTM03))
1	Slave channel output mode (output is set by the timer interrupt request signal (INTTM00) of the master channel, and reset by the timer interrupt request signal (INTTM03) of the slave channel)

Configuring the output level for the timer output pin

- Timer output level register 0 (TOL0)  
Configures the output level for the timer output pin for each channel.

Symbol: TOL0

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	TOL03	TOL02	TOL01	0
0	0	0	0	0	0	0	0	0	0	0	0	0	x	x	0

Bit 3

TOL03	Control of timer output level of channel 3
0	Positive logic output (active-high)
1	Negative logic output (active-low)

x: Bits not used in this setting item

Caution: For details on the register setup procedures, refer to RL78/G14 User's Manual: Hardware.

## RL78/G14, R8C/36M Group Migration Guide from R8C to RL78: Timer RE to Real-Time Clock and Timer Array Unit

Configuring the output value for the timer output pin

- Timer output register 0 (TO0)

Configures the output value for the timer output pin for channel 3.

Symbol: TO0

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	TO03	TO02	TO01	TO00
0	0	0	0	0	0	0	0	0	0	0	0	0	x	x	x

Bit 3

TO03	Timer output of channel 3
0	Timer output value is "0"
1	Timer output value is "1"

Enabling the timer output

- Timer output enable register 0 (TOE0)

Enables the timer output for channel 3.

Symbol: TOE0

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	TOE03	TOE02	TOE01	TOE00
0	0	0	0	0	0	0	0	0	0	0	0	1	x	x	x

Bit 3

TOE03	Timer output enable/disable of channel 3
0	Timer output is disabled. Timer operation is not applied to the TO03 bit and the output is fixed. Writing to the TO03 bit is enabled and the level set in the TO03 bit is output from the TO03 pin.
1	<b>Timer output is enabled.</b> <b>Timer operation is applied to the TO03 bit and an output waveform is generated.</b> <b>Writing to the TO03 bit is ignored.</b>

x: Bits not used in this setting item

Caution: For details on the register setup procedures, refer to RL78/G14 User's Manual: Hardware.

Setting the PWM output pin

- Port register (P3)  
Sets the output latch.

Symbol: P3

<b>7</b>	<b>6</b>	<b>5</b>	<b>4</b>	<b>3</b>	<b>2</b>	<b>1</b>	<b>0</b>
<b>0</b>	<b>0</b>	<b>0</b>	<b>0</b>	<b>0</b>	<b>0</b>	<b>P31</b>	<b>P30</b>
0	0	0	0	0	0	0	x

Bit 1

<b>P31</b>	<b>Output data control</b>
<b>0</b>	<b>Output 0</b>
1	Output 1

- Port mode register (PM3)  
Selects the P31 I/O mode.

Symbol: PM3

<b>7</b>	<b>6</b>	<b>5</b>	<b>4</b>	<b>3</b>	<b>2</b>	<b>1</b>	<b>0</b>
<b>1</b>	<b>1</b>	<b>1</b>	<b>1</b>	<b>1</b>	<b>1</b>	<b>PM31</b>	<b>PM30</b>
1	1	1	1	1	1	0	x

Bit 1

<b>PM31</b>	<b>P31 pin I/O mode selection</b>
<b>0</b>	<b>Output mode (the pin functions as an output port (output buffer on))</b>
1	Input mode (the pin functions as an input port (output buffer off))

x: Bits not used in this setting item

Caution: For details on the register setup procedures, refer to RL78/G14 User's Manual: Hardware.

### 5.4.5.7 Main Processing

Figure 5.10 shows the flowchart for main processing.

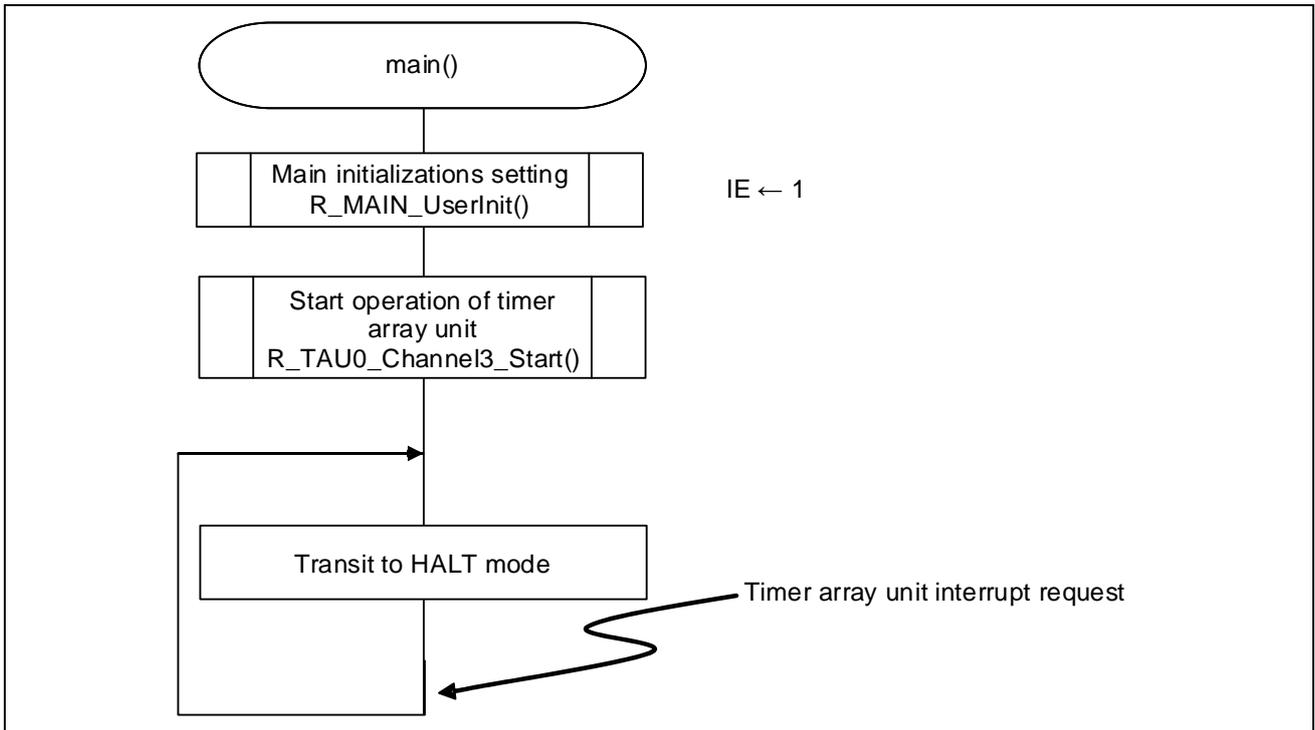


Figure 5.10 Main Processing

### 5.4.5.8 Timer Array Unit Operation Start

Figure 5.11 shows the flowchart for starting timer array unit operation.

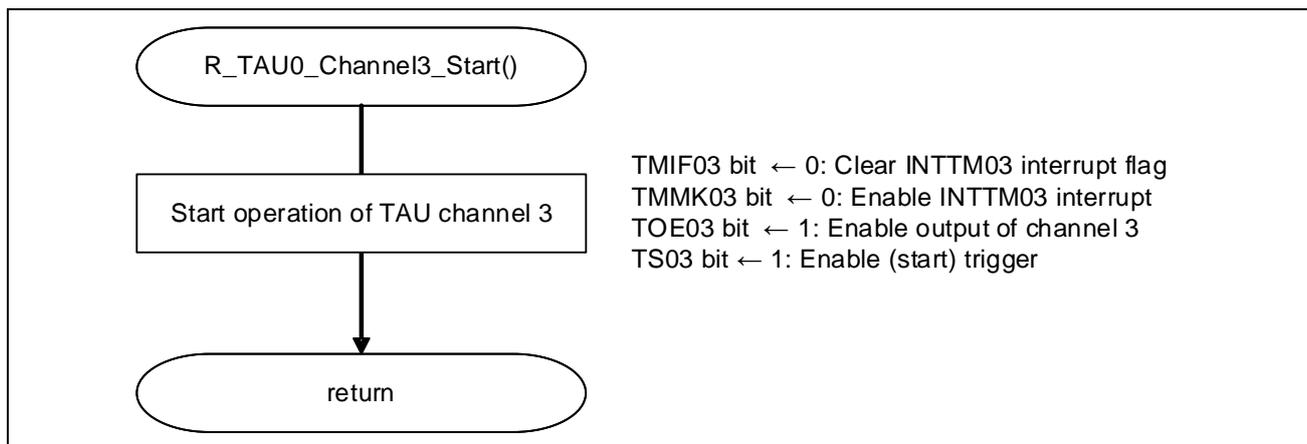


Figure 5.11 Timer Array Unit Operation Start

Configuring the timer interrupt

- Interrupt request flag register (IF1L)  
Clears the interrupt request flag.
- Interrupt mask flag register (MK1L)  
Enables interrupt processing.

Symbol: IF1L

7	6	5	4	3	2	1	0
<b>TMIF03</b>	<b>TMIF02</b>	<b>TMIF01</b>	<b>TMIF00</b>	<b>IICAIF0</b>	<b>SREIF1 TMIF03H</b>	<b>SRIF1 CSIF11 IICIF11</b>	<b>STIF1 CSIF10 IICIF10</b>
0	x	x	x	x	x	x	x

Bit 7

<b>TMIF00</b>	<b>Interrupt request flag</b>
0	<b>No interrupt request signal is generated</b>
1	Interrupt request is generated, interrupt request status

Symbol: MK1L

7	6	5	4	3	2	1	0
<b>TMMK03</b>	<b>TMMK02</b>	<b>TMMK01</b>	<b>TMMK00</b>	<b>IICAMK0</b>	<b>SREMK1 TMMK03H</b>	<b>SRMK1 CSIMK11 IICMK11</b>	<b>STMK1 CSIMK10 IICMK10</b>
0	x	x	x	x	x	x	x

Bit 7

<b>TMMK00</b>	<b>Interrupt servicing control</b>
0	<b>Interrupt servicing enabled</b>
1	Interrupt servicing disabled

x: Bits not used in this setting item

Caution: For details on the register setup procedures, refer to RL78/G14 User's Manual: Hardware.

Enabling the timer output

- Timer output enable register 0 (TOE0)  
Enables the timer output for each channel.

Symbol: TOE0

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	TOE03	TOE02	TOE01	TOE00
0	0	0	0	0	0	0	0	0	0	0	0	1	x	x	x

Bit 3

TOE03	Timer output enable/disable of channel 3
0	Timer output is disabled. Timer operation is not applied to the TO03 bit and the output is fixed. Writing to the TO03 bit is enabled and the level set in the TO03 bit is output from the TO03 pin.
1	<b>Timer output is enabled.</b> <b>Timer operation is applied to the TO03 bit and an output waveform is generated.</b> <b>Writing to the TO03 bit is ignored.</b>

Configuring the timer startup

- Timer channel start register 0 (TS0)  
Enables count operation of channel 0 and channel 3.

Symbol: TS0

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	TSH03	0	TSH01	0	0	0	0	0	TS03	TS02	TS01	TS00
0	0	0	0	x	0	x	0	0	0	0	0	1	x	x	x

Bit 3

TS03	Operation enable (start) trigger of channel 3
0	No trigger operation
1	<b>The TE03 bit is set to 1 and the count operation becomes enabled.</b> <b>The TCR03 register count operation start in the count operation enabled state varies depending on each operation mode.</b>

x: Bits not used in this setting item

Caution: For details on the register setup procedures, refer to RL78/G14 User's Manual: Hardware.

### 5.4.5.9 INTTM03 Interrupt Processing

Figure 5.12 shows the flowchart for INTTM03 interrupt processing.

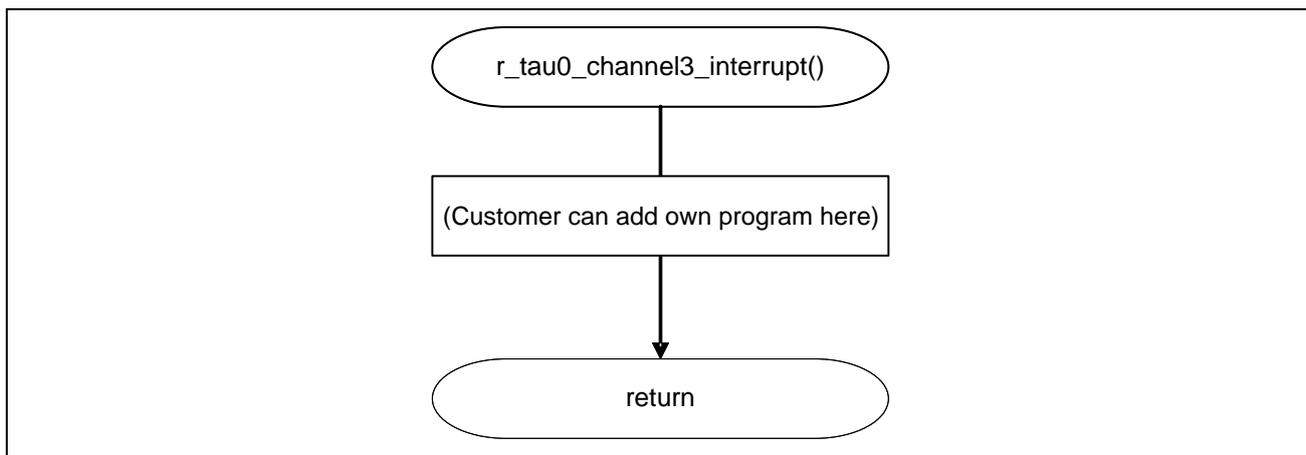


Figure 5.12 INTTM03 Interrupt Processing

## **6. Sample Code**

Sample code can be downloaded from the Renesas Electronics website.

## **7. Reference Application Note**

RL78/G14, R8C/36M Group Migration Guide from R8C to RL78: Timer RE to Real-time Clock (R01AN1502)  
The latest versions can be downloaded from the Renesas Electronics website.

## **8. Reference Documents**

User's Manual: Hardware

RL78/G14 User's Manual: Hardware (R01UH0186)

R8C/36M Group User's Manual: Hardware (R01UH0259)

The latest versions can be downloaded from the Renesas Electronics website.

Technical Update/Technical News

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# Revision History

Rev.	Date	Description	
		Page	Summary
1.00	Mar. 30, 2018	-	First edition issued

## General Precautions in the Handling of Microprocessing Unit and Microcontroller Unit Products

The following usage notes are applicable to all Microprocessing unit and Microcontroller unit products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

### 1. Handling of Unused Pins

Handle unused pins in accordance with the directions given under Handling of Unused Pins in the manual.

- The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible. Unused pins should be handled as described under Handling of Unused Pins in the manual.

### 2. Processing at Power-on

The state of the product is undefined at the moment when power is supplied.

- The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the moment when power is supplied.

In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the moment when power is supplied until the reset process is completed.

In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the moment when power is supplied until the power reaches the level at which resetting has been specified.

### 3. Prohibition of Access to Reserved Addresses

Access to reserved addresses is prohibited.

- The reserved addresses are provided for the possible future expansion of functions. Do not access these addresses; the correct operation of LSI is not guaranteed if they are accessed.

### 4. Clock Signals

After applying a reset, only release the reset line after the operating clock signal has become stable. When switching the clock signal during program execution, wait until the target clock signal has stabilized.

- When the clock signal is generated with an external resonator (or from an external oscillator) during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Moreover, when switching to a clock signal produced with an external resonator (or by an external oscillator) while program execution is in progress, wait until the target clock signal is stable.

### 5. Differences between Products

Before changing from one product to another, i.e. to a product with a different part number, confirm that the change will not lead to problems.

- The characteristics of Microprocessing unit or Microcontroller unit products in the same group but having a different part number may differ in terms of the internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

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